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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E70RA-I-MW1530-C

Overview:

- 7.0-inch TFT (182.07x117.6 ŸŸ)
- 1024È600 LJ̀ÈŜfă
- 4-lane MIPI DSI LyűŜ₦₹I·ŎŜ
- ² ìŘŜ ¢ŜŸLJerature
- All View
- IPS
- Transmissive
- Capacitive Touch Panel
- 1530 NITS
- TFT IC: EK73217A
- CTP Controller: GT9271
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT LCD Panel, driver circuit, capacitive touch panel, and a backlight unit. The resolution of the 7.0" TFT LCD contains 1024(RGB)x600 pixels and can display up to 16.7M colors.

TFT Features

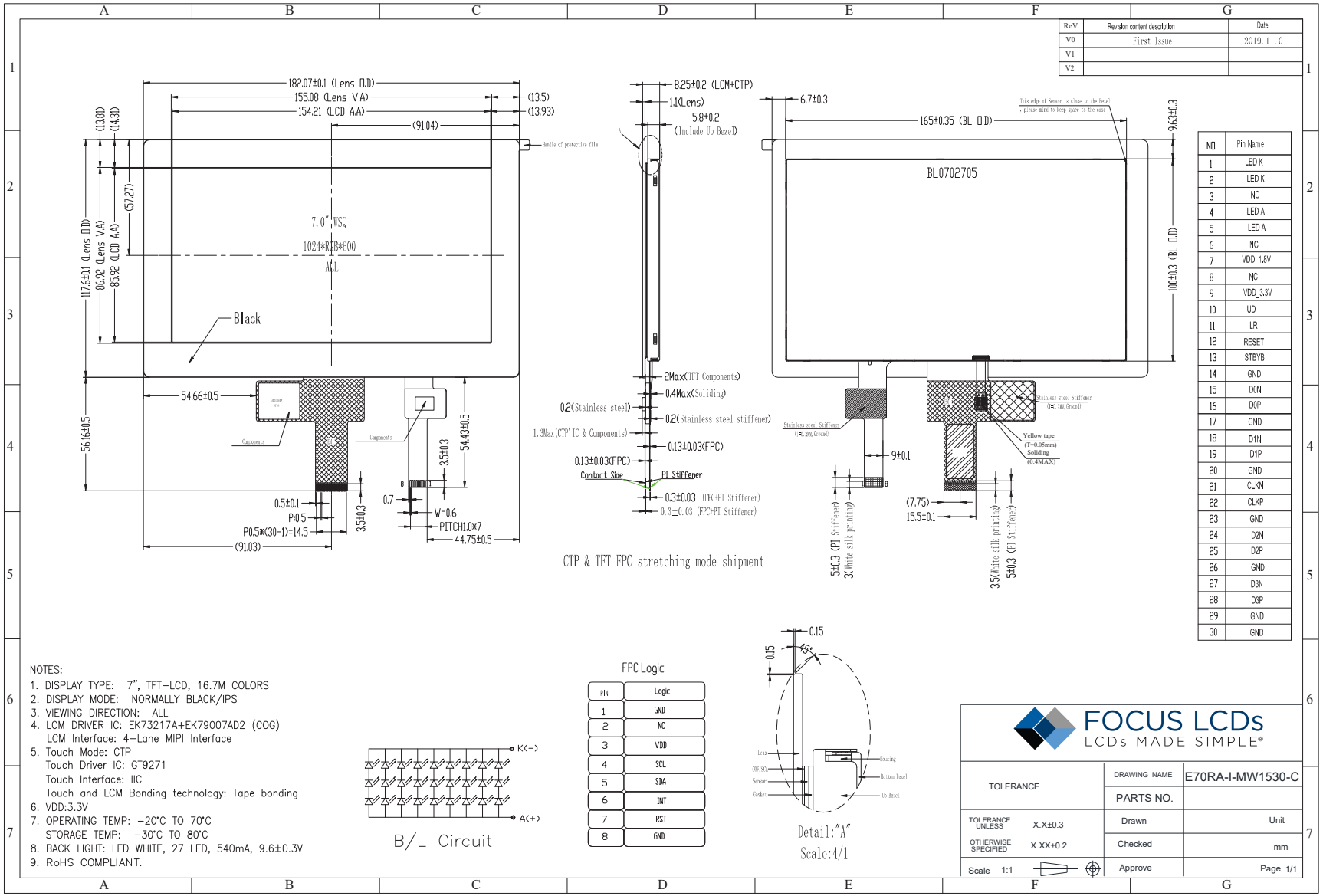
Display Colors: 16.7M
Interface: 4-lane MIPI

General Information Items	Specification Main Panel	Unit	Note
TFT Display area (AA)	154.21(H) x 85.92 (7.0 inch)	mm	-
Driver Element	TFT active matrix	-	-
Display Colors	16.7M	colors	-
Number of pixels	1024(RGB)x600	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel Pitch	0.1506 (H)x0.1432(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	EK73217A + EK79007AD2	-	-
TFT Interface	4-lane MIPI	-	-
Display mode	Transmissive/ Normally Black	-	-
CTP Structure	G+G	-	-
CTP Slave Address	0x5D(7bit) or 0x14(7bit)		
CTP Interface	I2C	-	-
CTP Controller IC	GT9271		
CTP Touch Mode	10-points and gestures	-	-
Operating temperature	-20-+70	℃	-
Storage temperature	-30-+80	℃	-

Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module Size	Horizontal (H)		182.07		mm	-
	Vertical (V)		117.60		mm	-
	Depth (D)		8.25		mm	-
	Weight		TBD		g	

1. Outline Dimensions



ReV.	Revision content description	Date
V0	First Issue	2019.11.01
V1		
V2		

NOTES:
1. DISPLAY TYPE: 7", TFT-LCD, 16.7M COLORS
2. DISPLAY MODE: NORMALLY BLACK/IPS
3. VIEWING DIRECTION: ALL
4. LCM DRIVER IC: EK73217A+EK79007AD2 (COG)
   LCM Interface: 4-Lane MIPI Interface
5. Touch Mode: CTP
   Touch Driver IC: GT9271
   Touch Interface: IIC
   Touch and LCM Bonding technology: Tape bonding
6. VDD:3.3V
7. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
8. BACK LIGHT: LED WHITE, 27 LED, 540mA, 9.6±0.3V
9. RoHS COMPLIANT.

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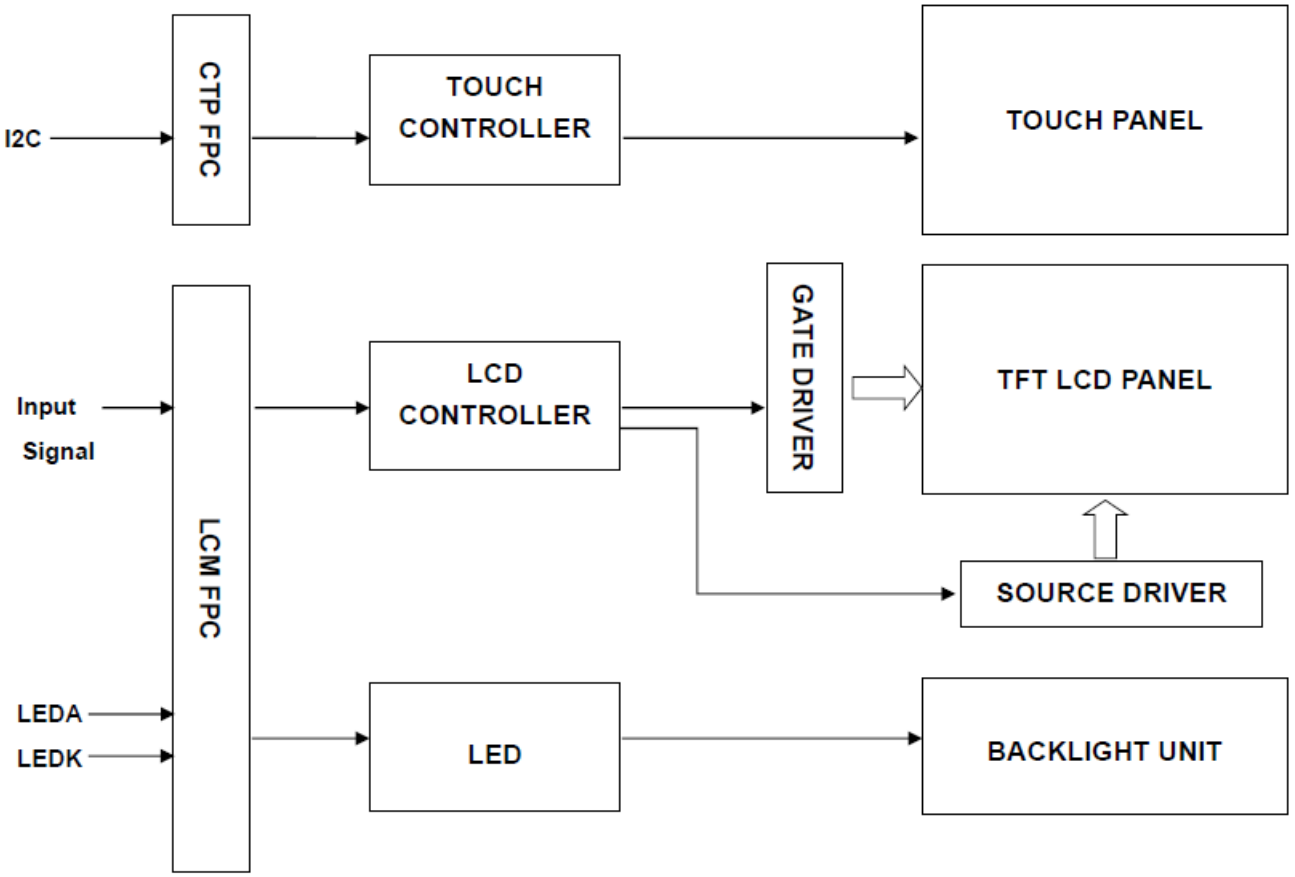
TOLERANCE	DRAWING NAME	E70RA-I-MW1530-C
	PARTS NO.	
TOLERANCE UNLESS OTHERWISE SPECIFIED X.X±0.3 X.XX±0.2	Drawn	Unit
	Checked	mm
Scale 1:1	Approve	Page 1/1

2. Block Diagram



3. Input Terminal Pin Assignment

3.1 TFT

NO.	Symbol	Description	I/O
1	LEDK	LED Cathode pin of the backlight	P
2	LEDK		
3	NC	Not connected	
4	LEDA	LED Anode pin of the backlight	P
5	LEDA		
6	NC	Not connected	
7	VDD	Voltage power supply (1.8V)	P
8	NC	Not connected	
9	VDD	Voltage power supply for DC/DC voltage converter circuit (3.3V)	P
10	UD	Vertical shift direction (gate output) selection	I
11	LR	Horizontal shift direction (source output) selection	I
12	RESET	Reset signal of the device. Active low.	I
13	STBYB	Standby mode. Normally pulled high. STBYB=1: normal operation, STBYB=0, timing controller and source driver will turn off. All outputs are High-Z.	I
14	GND	Ground	P
15	D0N	MIPI DSI differential data pair lane 0	I/O
16	D0P		
17	GND	Ground	P
18	D1N	MIPI DSI differential data pair lane 1	I/O
19	D1P		
20	GND	Ground	P
21	CLKN	MIPI DSI differential clock pair	I/O
22	CLKP		
23	GND	Ground	P
24	D2N	MIPI DSI differential data pair lane 2	I/O
25	D2P		
26	GND	Ground	P
27	D3N	MIPI DSI differential data pair lane 3	I/O
28	D3P		
29	GND	Ground	P
30	GND	Ground	P

I: Input, O: Output, P: Power

3.2 CTP

NO.	Symbol	Description	I/O
1	GND	Ground	P
2	NC	Not connected	
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt signal to the host	I
7	RST	External reset, active low	I
8	GND	Ground	O

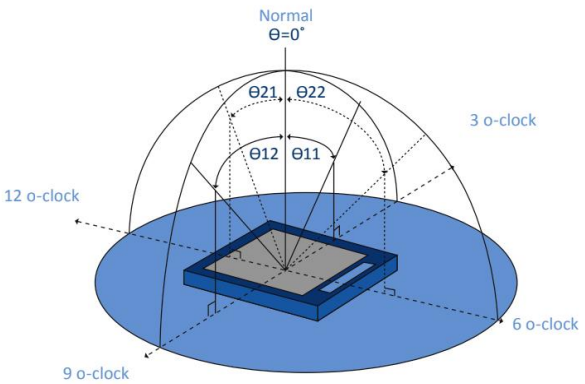
4. LCD Optical Characteristics

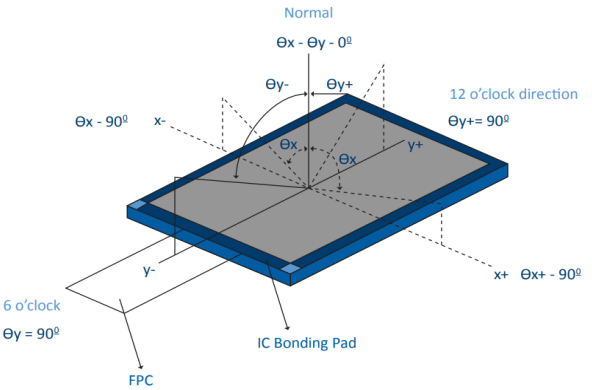
4.1 Optical Specifications

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Color Gamut		S%	θ=0 Normal viewing angle	--	50	--	%	(3)
Contrast Ratio		CR		600	800	--	%	(2)
Response Time	Rising	TR+TF		--	25	40	ms	(4)
	Falling							
Color Filter Chromaticity	White	W_X		0.2584	0.2984	0.3384		(5)(6)
		W_Y		0.3000	0.3400	0.3800		
	Red	R_X		0.5731	0.5931	0.6131		
		R_Y		0.3352	0.3552	0.3752		
	Green	G_X		0.2909	0.3109	0.2909		
		G_Y		0.5344	0.5544	0.5744		
	Blue	B_X		0.1334	0.1534	0.1734		
		B_Y		0.0872	0.1072	0.1272		
Viewing Angle	Hor.	ΘL	CR≥10	--	85	--	degrees	(1)(6)
		ΘR		--	85	--		
	Ver.	ΘT		--	85	--		
		ΘB		--	85	--		
Option View Direction		ALL						(1)

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.



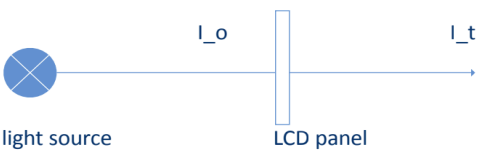


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

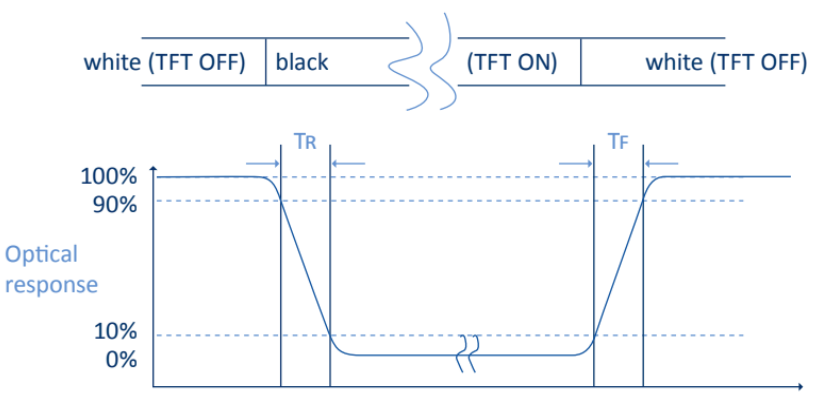
(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

$$Tr = \frac{It}{Io} x\ 100\%$$



Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90%to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut:
Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

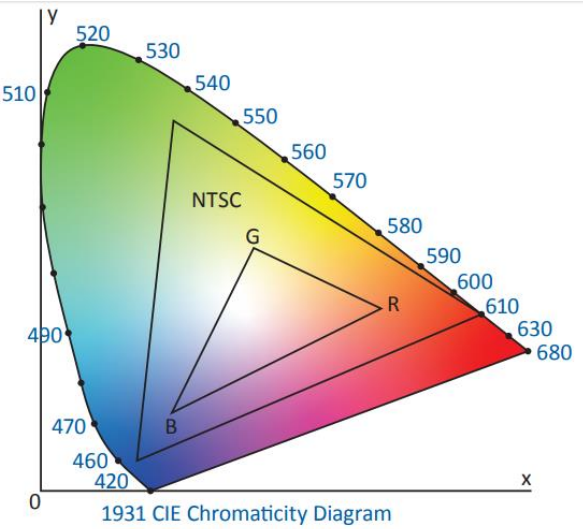
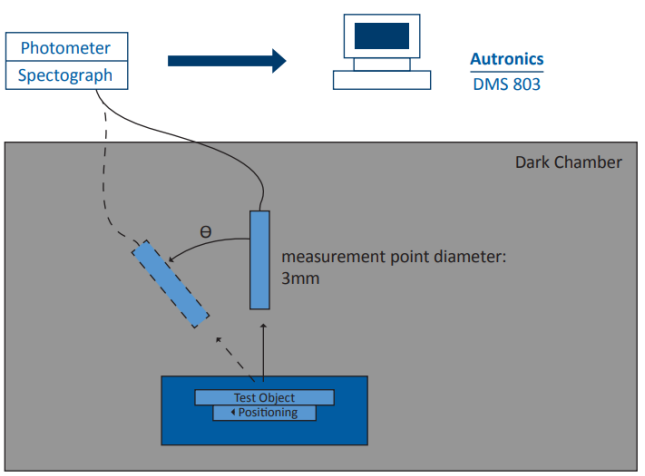


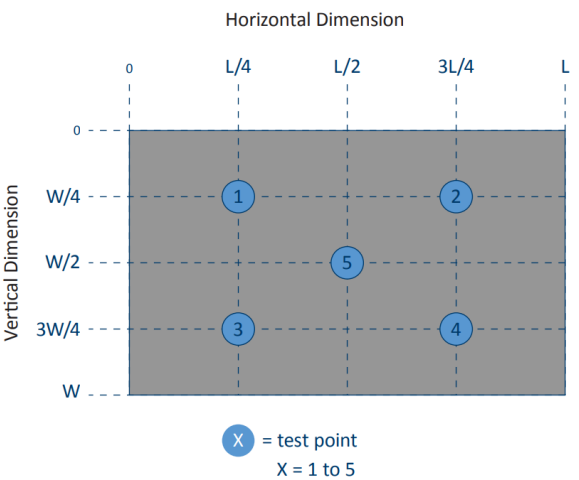
Fig. 1931 CIE chromacity diagram

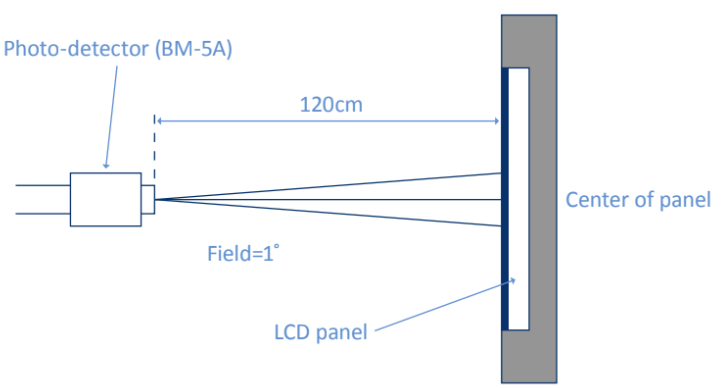
Color gamut: $S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.







5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VDD(1.8)	-0.3	2.0	V
DC/DC Supply Voltage	VDD(3.3)	-0.3	6.0	
Operating Temperature	TOP	-20	+70	℃
Storage Temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VDD(1.8)	1.71	1.8	1.89	V	
DC/DC Supply Voltage	VDD(3.3)	2.7	3.3	5.8	V	
Normal Mode Current	IDD(1.8)	--	0.05	--	mA	
	IDD(3.3)	--	140	--	mA	
Level Input Voltage	VIH	0.7IVDD(1.8)	--	VDD(1.8)	V	
	VIL	GND	--	0.3VDD(1.8)	V	
Level Output Voltage	VOH	VDD(1.8)-0.4	--	VDD(1.8)	V	
	VOL	GND	--	0.4	V	

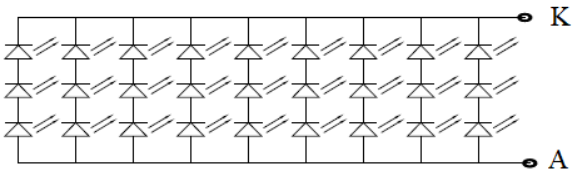
5.3 LED Backlight Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	180	540	--	mA	
Forward Voltage	VF	--	9.6	--	V	
LCM Luminance	LV	1480	1530	--	cd/m2	Note 3
LED lifetime	Hr	--	50000	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

The back-light system is edge-lighting type with 27 white LEDs.

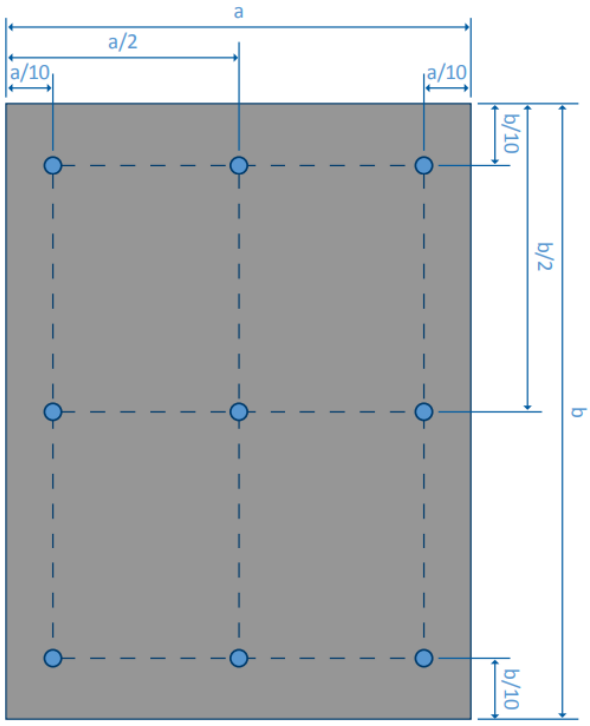
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=540mA. The LED lifetime could be decreased if operating IL is larger than 540mA. The constant current driving method is suggested.



Backlight LED Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:



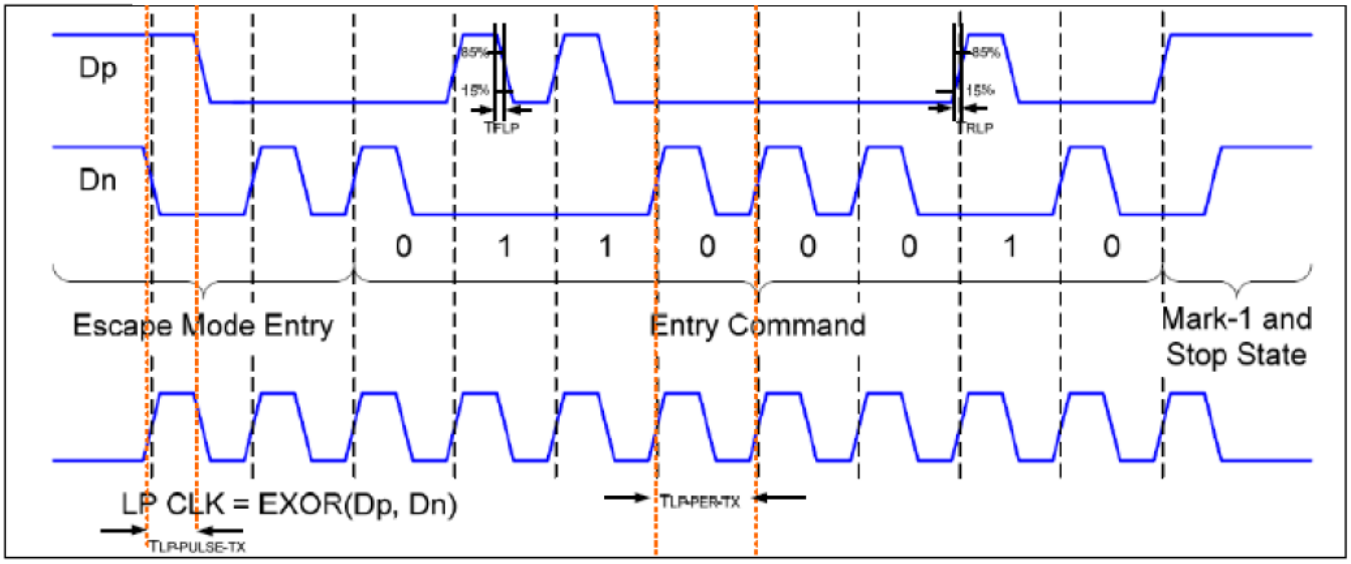
$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

6. MIPI AC Characteristics

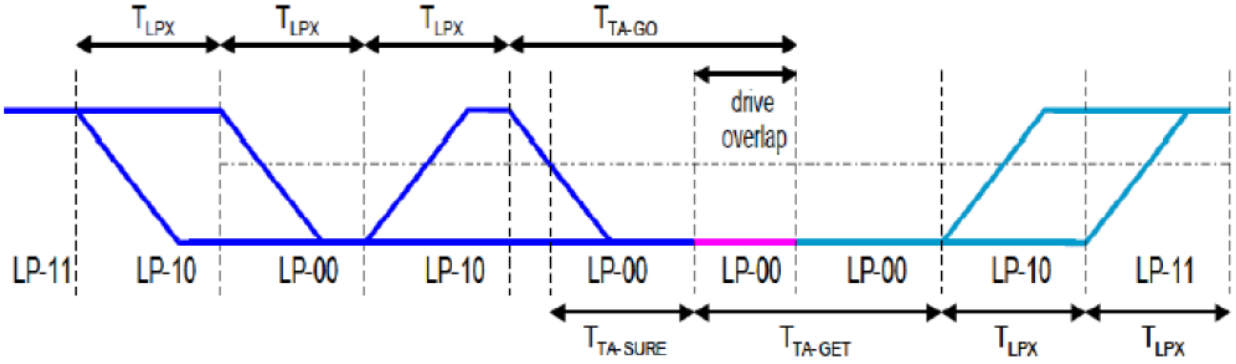
6.1 LP Transmitter AC Specification

Parameter		Symbol	Min	Typ.	Max	Unit	Note
15%-85% rising and falling time		T_{RLP}/T_{FLP}	--	--	25	ns	
30%-85% rising and falling time		T_{REOT}	--	--	35	ns	
Pulse width of LP exclusive OR clock	First LP XOR clock pulse after stop state or last pulse before stop state	$T_{LP-PULSE-TX}$	40	--	--	ns	
	All other pulses		20	--	--	ns	
Period of the LP XOR clock		$T_{LP-PER-TX}$	90	--	--	mV/ns	
Slew rate @CLOAD=0pF		dV/dtSR	30	--	500	mV/ns	
Slew rate @CLOAD=5pF			30	--	200	mV/ns	
Slew rate @CLOAD=20pF			30	--	150	mV/ns	
Slew rate @CLOAD=70pF			30	--	100	mV/ns	
Load capacitance		T_{RLP}	--	--	70	pF	



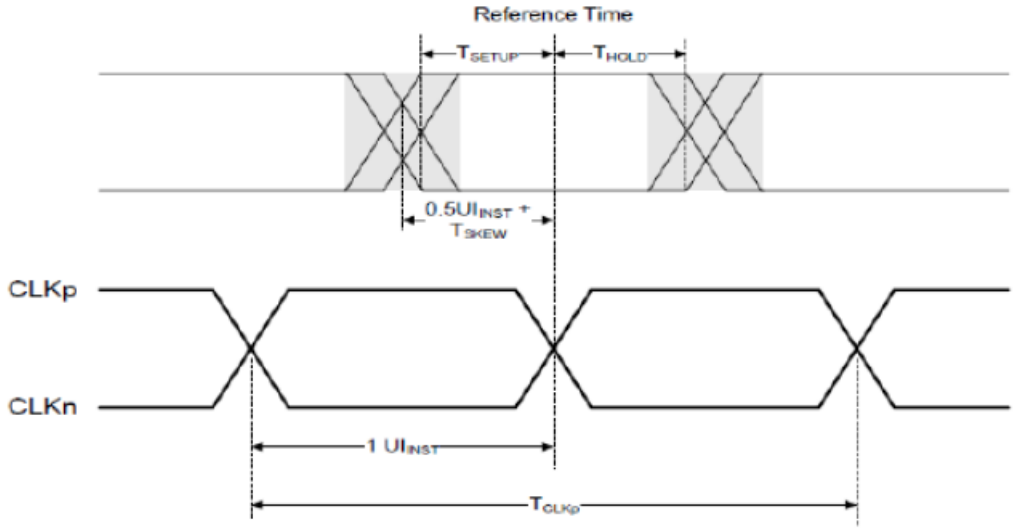
6.2 Turnaround Procedure

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Length of any low power state period: master side	T_{LPX}	50	--	75	ns	
Length of any low power state period: slave side	T_{LPX}	50	55.56	58.34	ns	
Ratio of TLPX(Master)/TLPX(Slave) between master and slave side	RatioT_{LPX}	2/3	--	3/2	ns	
Time-out before new TX side start driving	$T_{TA-Sure}$	T_{LPX}	--	2 T_{LPX}	ns	
Time to drive LP-00 by new TX	T_{TA-GET}	--	5 T_{LPX}	--	ns	
Time to drive LP-00 after turnaround request	T_{TA-GO}	--	4 T_{LPX}	--	ns	



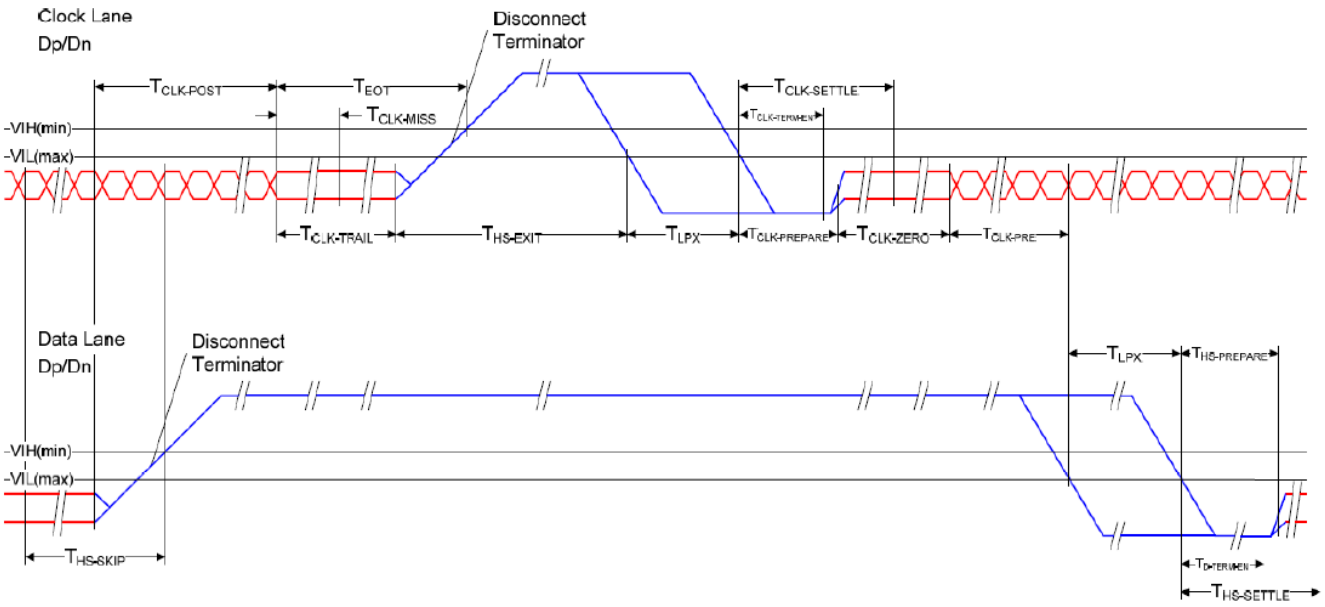
6.3 High Speed Transmission

Parameter	Symbol	Min	Typ.	Max	Unit	Note
UI Instantaneous	UIINST	2	--	12.5	ns	
Data to clock skew (measured at transmitter)	TSKEW(TX)	-0.15	--	0.15	UIINST	
Data to clock setup time (measured at receiver)	TSETUP(RX)	0.15	--	--	UIINST	
Data to clock hold time (measured at receiver)	THOLD(RX)	0.15	--	--	UIINST	
20%-80% rise and fall time	TR, TF	150	--	--	ps	
		--	--	--	UIINST	

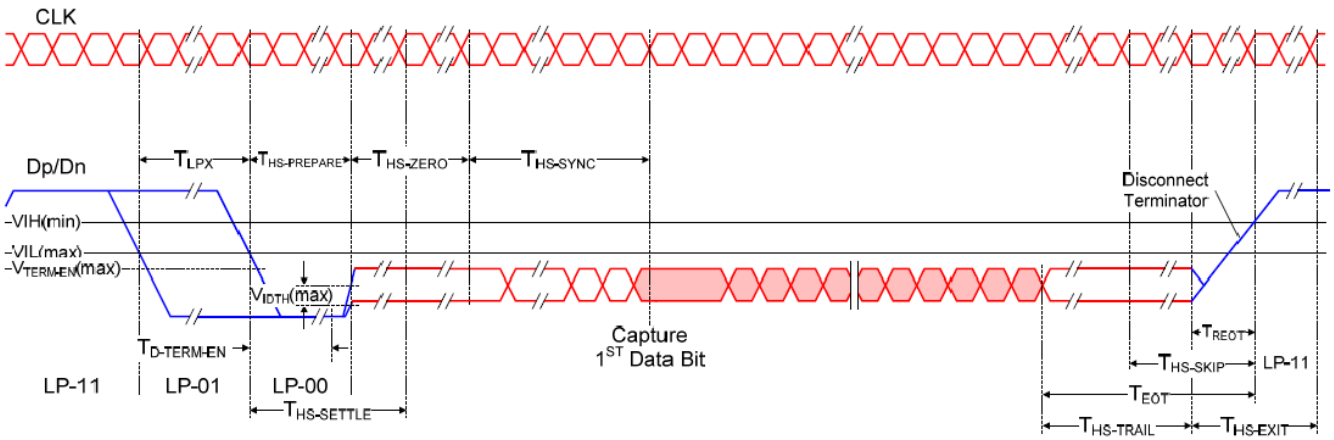


6.4 High Speed Clock Transmission

Parameter	Symbol	Min	Typ.	Max	Unit
Time that the transmitter shall continue sending HS clock after the last associated data lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI	--	--	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	--	--	60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38	--	95	ns
Minimum lead HS-0 drive period before starting clock	$T_{CLK-PREPARE}+T_{CLK-ZERO}$	300	--	--	ns
Time to enable clock lane receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$	--	--	38	ns
Minimum time that the HS clock must be prior to any associated data lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8	--	--	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	--	--	ns



6.5 High Speed Data Transmission in Bursts



7. CTP Specification

7.1 Absolute Maximum Rating

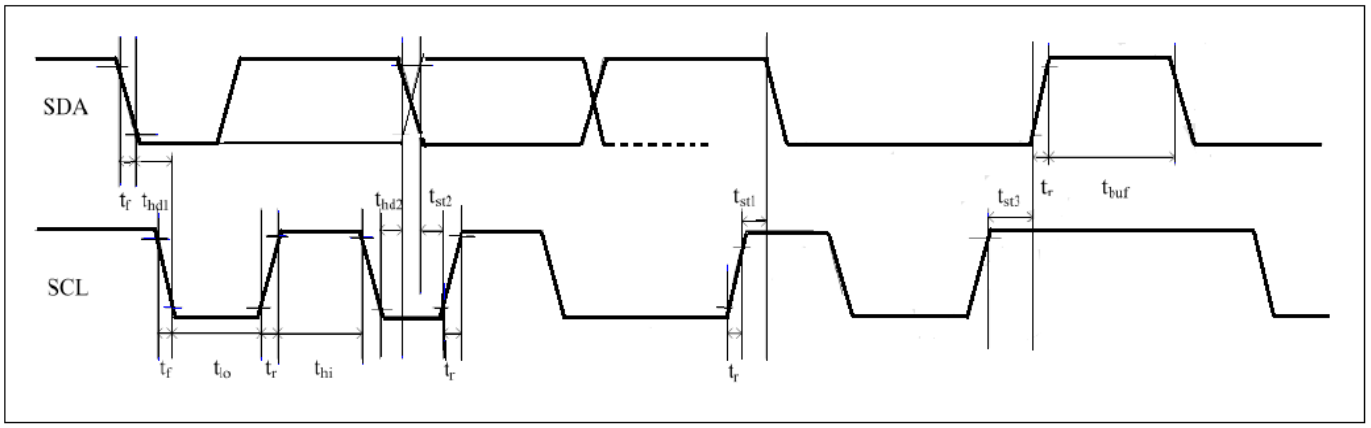
Item	Symbol	Min	Max	Unit	Note
Power Supply Voltage	VDD	2.66	3.47	V	--
Operating Temperature	TOP	-20	+70	˚C	--
Storage Temperature	TST	-30	+80	˚C	--

7.2 DC Electrical Characteristics (TA=25˚C)

Item	Min	Typ.	Max	Unit	Note
Normal Mode Operating Current	--	13	--	mA	--
Green Mode Current Consumption	--	4.5	--	mA	--
Sleep Mode Current Consumption	70	--	120	uA	--
Digital Supply Voltage (VDD)	2.8	--	3.3	mA	--
Digital Input Low Voltage (VIL)	-0.3	--	0.25VDD	V	--
Digital Input High Voltage (VIH)	0.75VDD	--	VDD+0.3	V	--
Digital Output Low Voltage (VOL)	--	--	0.15VDD	V	--
Digital Output High Voltage (VOH)	0.85VDD	--	--	V	--

7.3 I2C Interface Characteristics

GT9271 provides a standard I2C interface for SCL and SDA to communicate with the host. GT9271 always serves as slave device in the system with all communication being initialized by the host. It is recommended that transmission rate be kept at or below 400kbps. The figure shown below is the I2C timing:



Parameter	Symbols	Condition	Min	Max	Units
SCL low period	t_{lo}		1.3		us
SCL high period	t_{hi}		0.6		us
SCL setup time for start condition	t_{st1}		0.6		us
SCL setup time for stop condition	t_{st3}		0.6		us
SCL hold time for start condition	t_{hd1}		0.6		us
SDA setup time	t_{st2}		0.1		us
SDA hold time	t_{hd2}		0		us

Table 7.1: I2C AC Characteristics, 1.8V interface voltage, 400kbps transmission rate, 2k pull-up resistor

Parameter	Symbols	Condition	Min	Max	Units
SCL low period	t_{lo}		1.3		us
SCL high period	t_{hi}		0.6		us
SCL setup time for start condition	t_{st1}		0.6		us
SCL setup time for stop condition	t_{st3}		0.6		us
SCL hold time for start condition	t_{hd1}		0.6		us
SDA setup time	t_{st2}		0.1		us
SDA hold time	t_{hd2}		0		us

Table 7.2: I2C AC Characteristics, 3.3V interface voltage, 400kbps transmission rate, 2k pull-up resistor

GT9271 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. The configuration methods and timings are shown below:

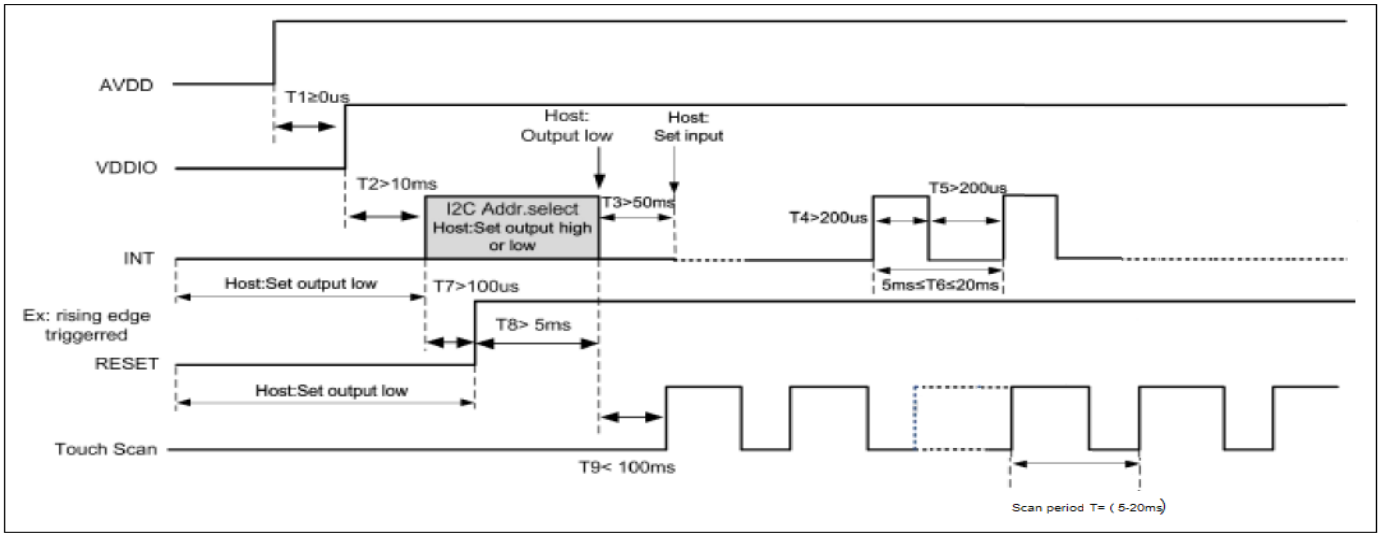


Figure 7.1: I2C Power on Timing

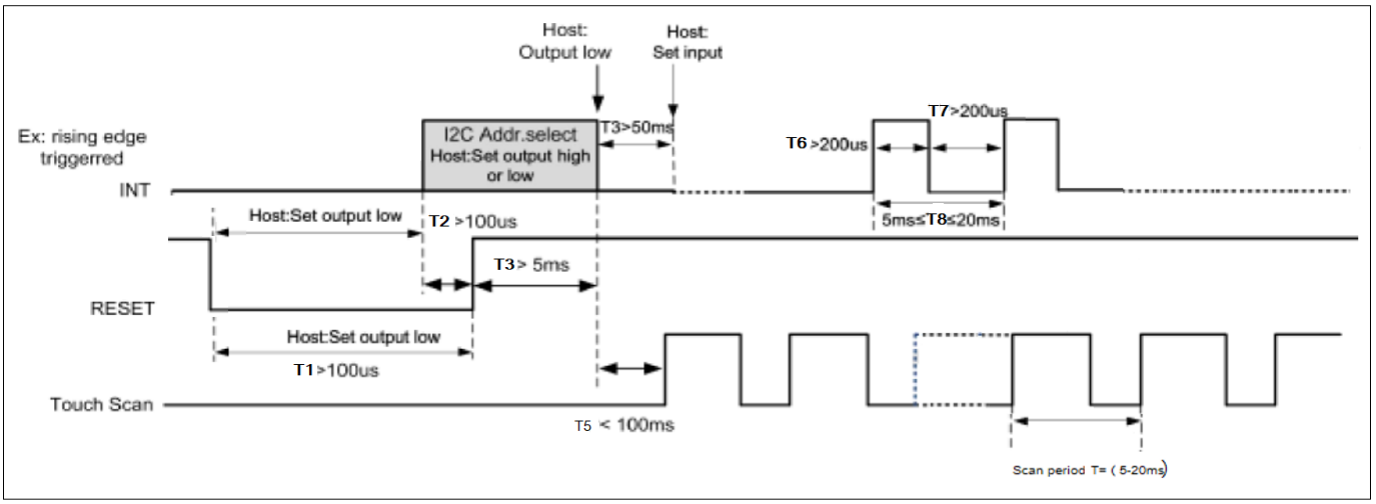


Figure 7.2: I2C Host Resetting Timing

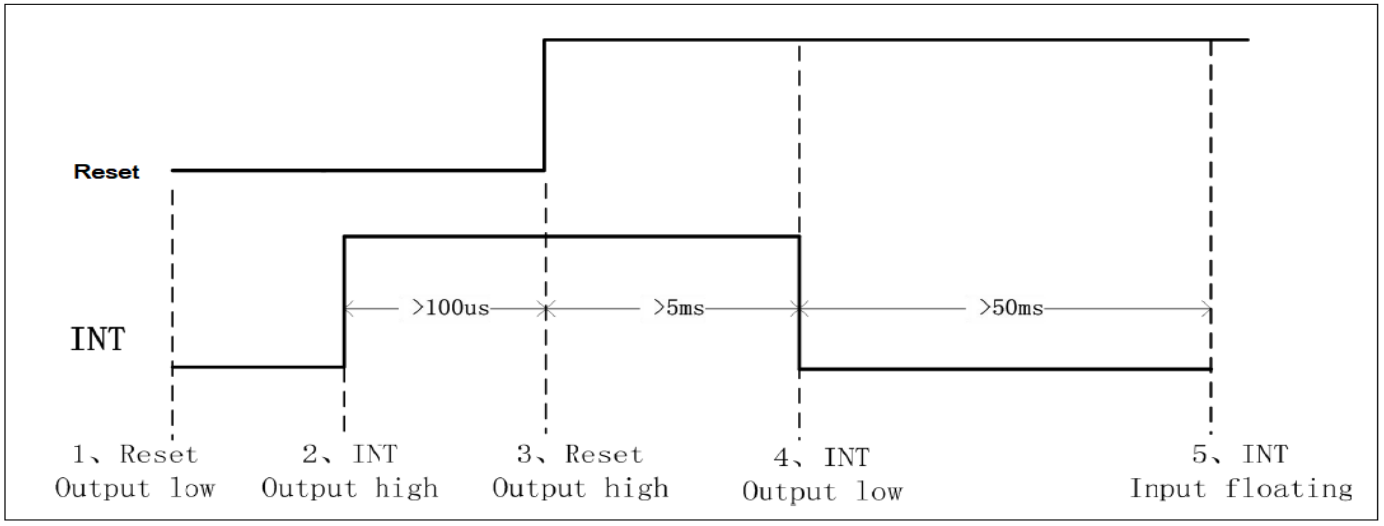


Figure 7.3: Setting Slave Address to 0x28/0x29 Timing

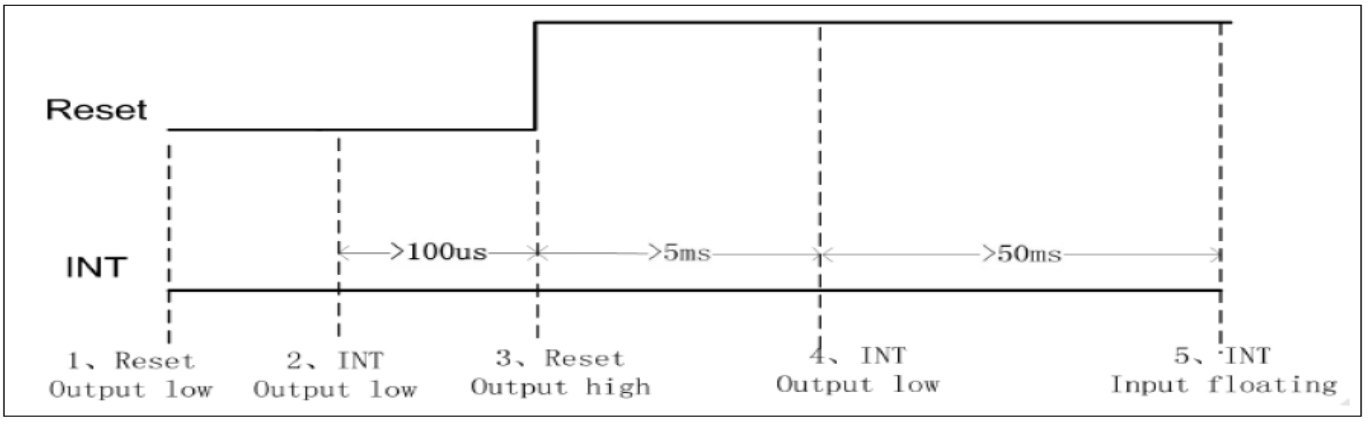


Figure 7.4: Setting Slave Address to 0xBA/0xBB Timing

Data Transmission *(ex. 0xBA/0xBB)*

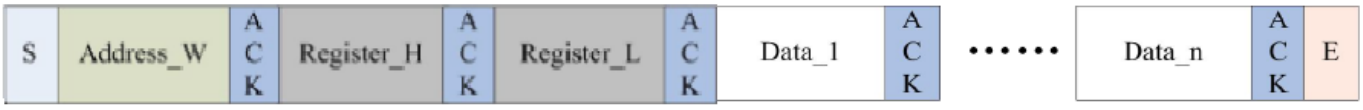
Communication is always initiated by the host. Valid start condition is signaled by pulling SDA line from high to low when SCL is high. Data flow or address is transmitted after the start condition.

All slave devices connected to I2C bus should detect the 8-bit address issued after start condition and send the correct ACK. After receiving matching address, GT9271 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely not 0xBA or 0xBB, GT9271 will stay in an idle state.

For data bytes on SDA, each of the 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is high. When communication is completed the host will issue the stop condition. Stop condition implies the transition of SDA line from low to high when SCL is high.

Writing Data to GT9271

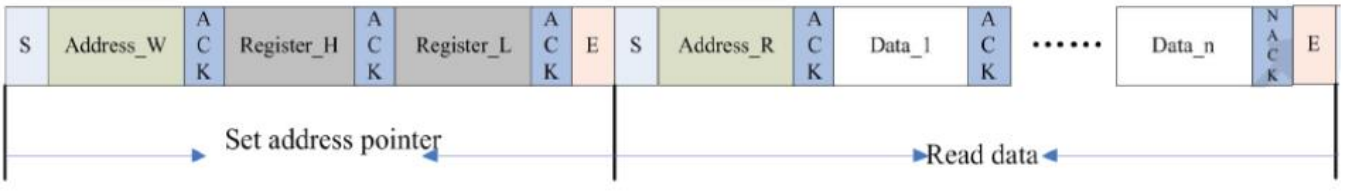
The diagram displays the timing sequence of the host writing data onto GT9271. First the host issues a start condition. The host sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates write operation) to the slave device. After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register)



The location of the register address pointer will automatically add 1 every write operation. When the host needs to perform write operations on a group of registers of continuous addresses it can write continuously. The write operation is terminated when the host issues the stop condition.

Reading Data from GT9271

The diagram below is the timing sequence of the host reading data from GT9271. The host issues the start condition and sends 0xBA (Address bits and R/W bit, R/W bit as 0 indicates write operation) to the slave device. After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.



The host issues the start condition once again and sends 0xBB (read operation). After receiving ACK, the host starts to read the data. GT9271 also supports continuous read operation. When receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

8. Cautions and Handling Precautions

8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

8.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.