September 30, 2019

Subject: PCN# 08A-19 Platform Manager 2 and L-ASC10 Datasheet Update

Dear Lattice Customer,

Lattice Semiconductor is providing this notification of changes to the Platform Manager™ 2 and L-ASC10 Data Sheets.

This PCN covers two distinct changes to the Platform Manager 2 family.

Change #1 Description

The Platform Manager 2 Data Sheet (FPGA-DS-02036 Version 2.3, released in September 2019) and L-ASC10 Data Sheet (FPGA-DS-02038 Version 2.1, released in September 2019) have updated R_{addr} values for the 6th and 7th device as noted below in Table 1. The R_{addr} resistor is connected from ground to the I2C_ADDR pin (pin 16 of the L-ASC10 and ball K6 of the LPTM21L 100-Ball caBGA). The function of the I2C_ADDR pin is to set the lower three bits of Analog Section's I^2C address at power up. This is to support multiple devices on the same I^2C chain.

Table 1. R_{addr} Value vs. Device Number.

R_{addr} Value[1]	Comment	3 LSB of I^2C Slave Address	Software ASC Device Number	Physical ASC Device Number
None (Tie to GND)	No change	000	0	1st
2.2 k Ω	No change	001	1	2nd
4.4 k Ω	No change	010	2	3rd
7 k Ω	No change	011	3	4th
10 k Ω	No change	100	4	5th
13.7 k Ω	Was 14 k Ω	101	5	6th
17.8 k Ω	Was 18 k Ω	110	6	7th
None (Tie to V_{CCA})	No change	111	7	8th

1: All resistor values should be +/- 1 % tolerance or better.

The R_{addr} datasheet change improves design performance margin for the I2C_ADDR scheme and more accurately matches silicon behavior. In conjunction with these datasheet changes, Lattice has adjusted the test screen to align with the new resistor values. These changes were identified as part of our continuous improvement process.

Affected Devices

The Platform Manager 2 Ordering Part Numbers (OPNs) affected by Change #1 in this PCN are as follows:

L-ASC10-1SG48I

LPTM21L-1ABG100I

Note 1: Change #1 in this PCN also affects any custom devices (i.e. factory programmed, special test, etc) which are derived from any of the devices listed above.

Note 2: Change #1 in this PCN does not affect the following Platform Manager 2 OPNs because the I2C_ADDR function is internally grounded and the 3 LSB of I^2C address bits are set to "000":

LPTM21-1AFTG237C

LPTM21-1AFTG237I

Device Identification

Devices that have been screened to the improved I2C_ADDR test can be identified by the assembly work week (date code) of the Inspection Lot Number, which is marked on the topside of the device. Inspection lot numbers are also marked on the label on the outside of the inventory box as well as on the anti-static moisture barrier bag within. The work week part of the Inspection Lot Number is shown in the example below.

Devices assembled beginning with 2019 work week **44** will be screened to the improved I2C_ADDR test.

Affected Software

Platform Designer (a tool in Lattice Diamond™ software) has also been modified to reflect the R_{addr} resistor value changes. This will be available in the D3.11 Service Pack 1, scheduled for release coincident with this notice. Note, the software service pack only updates the values displayed in the GUI; it is not necessary to recompile the Lattice Diamond design in response to this notification.

Data Sheet Specifications

The updated Platform Manager 2 Data Sheet (FPGA-DS-02036 Verion 2.3, released in September 2019) and L-ASC10 Data Sheet (FPGA-DS-02038 Version 2.1, released in September 2019) reflect the changes described above and are available on the Lattice website.

PCN Timing

The Data Sheet and software changes are effective immediately.

Recommended Customer Action

For customers utilizing the R_{addr} values for the 6th or 7th devices in the I^2C chain, Lattice recommends implementing the resistor change in conjunction with devices tested to the adjusted screen.

Customers using any other I^2C address configuration may contact Lattice for additional information by referencing this PCN in a technical support case at www.latticesemi.com/techsupport

Change #2 Description

The Platform Manager 2 Data Sheet (FPGA-DS-02036 Version 2.3, released in September 2019) removes the 12V to 3.3V DC-DC converter feature. This feature is no longer supported by Lattice.

Affected Devices

The Platform Manager 2 Ordering Part Numbers (OPNs) affected by Change #2 in this PCN are as follows:

LPTM21-1AFTG237C

LPTM21-1AFTG237I

Note 1: Change #2 in this PCN also affects any custom devices (i.e. factory programmed, special test, etc) which are derived from any of the devices listed above.

Note 2: Change #2 in this PCN does not affect the following Platform Manager 2 OPNs because they do not have the 12V to 3.3V DC-DC converter feature:

LPTM21L-1ABG100I

L-ASC10-1SG48I

Data Sheet Specifications

The updated Platform Manager 2 Data Sheet (FPGA-DS-02036 Verion 2.3, released in September 2019) contains Change #2 and is currently available on the Lattice website.

PCN Timing

The Data Sheet changes are effective immediately.

Recommended Customer Action

Those customers who may be planning on using the 12V DC-DC converter feature are advised against doing so.

Customers who have utilized the 12V DC-DC converter and have concerns may reference this PCN in a technical support case at www.latticesemi.com/techsupport.

Customers who have further questions regarding either Change #1 or Change #2 described in this notification are encouraged to contact local field support or email sales@latticesemi.com.

Lattice PCNs are available on the Lattice website. Please sign up to receive e-mail PCN alerts by registering here. If you already have a Lattice web account and wish to receive PCN alerts, you can do so by logging into your account and making edits to your subscription options.

Sincerely,

Lattice PCN Administration