Description

The AP3440 is a current mode, PWM synchronous buck (step-down) DC-DC converter, capable of driving a 4A load with high efficiency, excellent line and load regulation.

The device integrates two N-channel power MOSFETs with low on-resistance. Current mode control provides fast transient response and cycle-by-cycle current limit.

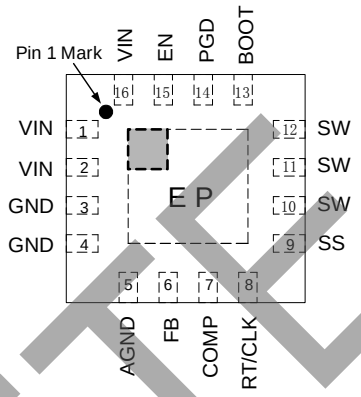
The switching frequency of AP3440 can be programmable from 200kHz to 2MHz, which allows small-sized components, such as capacitors and inductors. A standard series of inductors from several different manufacturers are available. This feature greatly simplifies the design of switch-mode power supplies.

Under voltage lockout is internally set at 2.6V, but can be increased by programming the threshold with a resistor network on the enable pin. The output voltage startup ramp is controlled by the soft-start pin. An open drain power good signal indicates the output is within 93% to 107% of its nominal voltage.

The AP3440 is available in U-QFN3030-16 package.

Pin Assignments

(Top View)



U-QFN3030-16

Applications

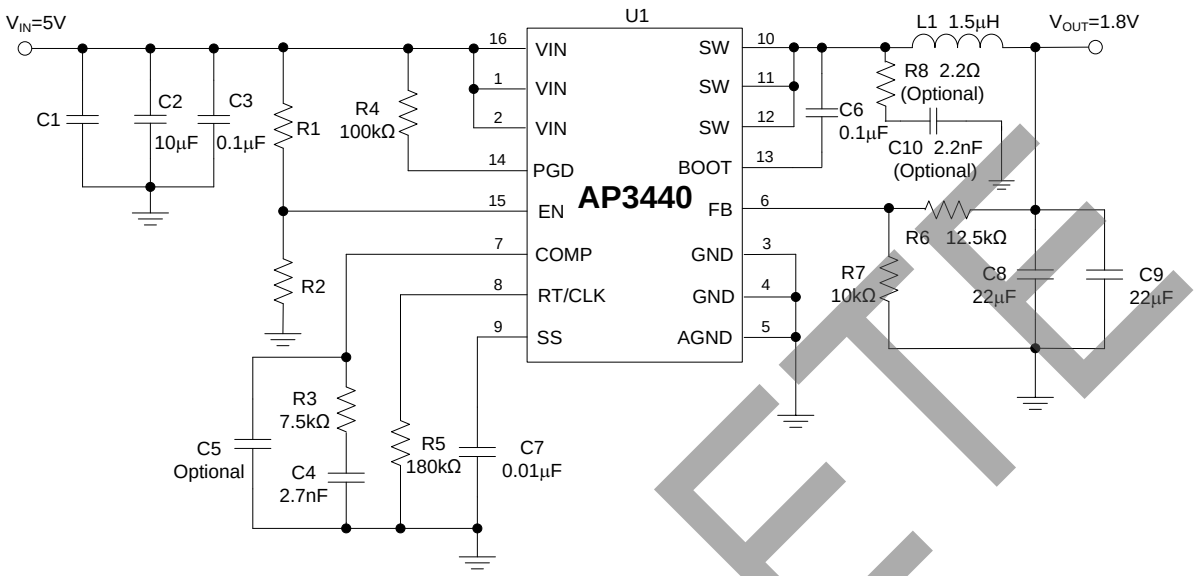
- Low-voltage, High-density Power Systems
- Point of Load Regulation for High Performance DSPs, FPGAs, ASICs and Microprocessors
- Broadband, Networking and Optical Communications Infrastructure

Features

- Input Voltage Range: 2.95V to 5.5V
- 0.8V Reference Voltage with ±3% Precision
- Two 30mΩ (Typical) MOSFETs for High Efficiency at 4A Load
- High Efficiency: Up to 94%
- Output Current: 4A
- Programmable Frequency:200kHz to 2MHz
- Current Mode Control
- Synchronizes to External Clock
- Adjustable Soft-start
- Soft Start-up into Pre-biased Output
- UV and OV Power Good Output
- Built-in Over Current Protection
- Built-in Thermal Shutdown Function
- Programmable UVLO Function
- Built-in Over Voltage Protection
- Thermally Enhanced 3mm×3mm 16-pin U-QFN3030-16
- **Totally Lead-free & Fully RoHS Compliant (Note1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

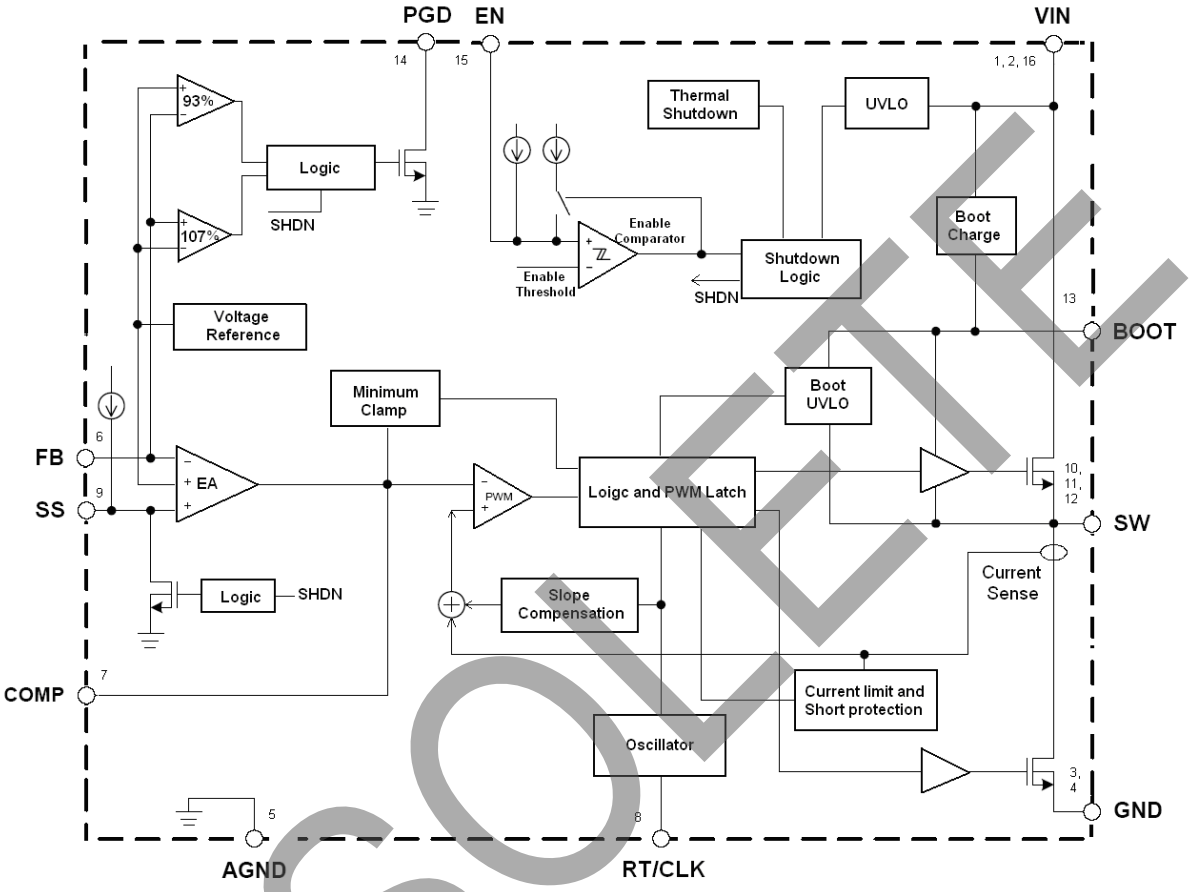
Typical Applications Circuit



Pin Description

Pin Number	Pin Name	Function
1,2,16	VIN	Supply input pin. A capacitor should be connected between the VIN and GND pin to keep the DC input voltage constant
3,4	GND	Power ground. This pin should be electrically connected to the power pad under the IC
5	AGND	Analog ground. This pin should be electrically connected to GND close to the device
6	FB	Feedback pin. Inverting node of the transconductance error amplifier
7	COMP	Compensation pin. This pin is the output of the transconductance error amplifier and the input to the current comparator. Connect external compensation elements to this pin to stabilize the control loop
8	RT/CLK	Resistor timing or external clock input pin
9	SS	Soft-start pin. An external capacitor connected to this pin sets the output voltage rise time. This pin can also be used for tracking
10,11,12	SW	Internal power switch output pin. This pin is connected to the inductor and bootstrap capacitor
13	BOOT	Bootstrap pin. A bootstrap capacitor is connected between the BOOT pin and SW pin. The voltage across the bootstrap capacitor drives the internal high-side power MOSFET
14	PGD	Power good indicator output. Asserts low if output voltage is low due to thermal shutdown, over-current, over/under-voltage or EN shut down
15	EN	Enable pin, internal pull-up current source. Pull below 1.2V to disable. Float to enable. Can be used to set the on/off threshold (adjust UVLO) with two additional resistors
EP	Exposed Thermal Pad	Exposed Pad can be connected to GND, for best thermal performance thermal vias are recommended under the package

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Pin Voltage	-0.3 to 6.5	V
V_{EN}	EN Pin Voltage	-0.3 to 6.5	V
V_{SW}	SW Pin Voltage	-0.3 to V_{IN}+0.3	V
V_{FB}	FB Pin Voltage	-0.3 to 6.5	V
V_{COMP}	COMP Pin Voltage	-0.3 to 6.5	V
V_{PGD}	PGD Pin Voltage	-0.3 to 6.5	V
$V_{RT/CLK}$	RT/CLK Pin Voltage	-0.3 to 6.5	V
V_{SS}	SS Pin Voltage	-0.3 to 6.5	V
θ_{JA}	Thermal Resistance	70	°C/W
T_J	Operating Junction Temperature	-40 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10sec)	+260	°C
—	ESD(Machine Model)	200	V
—	ESD(Human Body Model)	2000	V

Note 4: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	2.95	5.5	V
$I_{OUT(MAX)}$	Maximum Output Current	4	—	A
T_A	Operating Ambient Temperature	-40	+85	°C

Electrical Characteristics (@V_{IN}=2.95 to 5.5V, T_A=+25°C, unless otherwise specified. Specifications with **boldface type** apply over full operating temperature range from -40 to +85°C.)

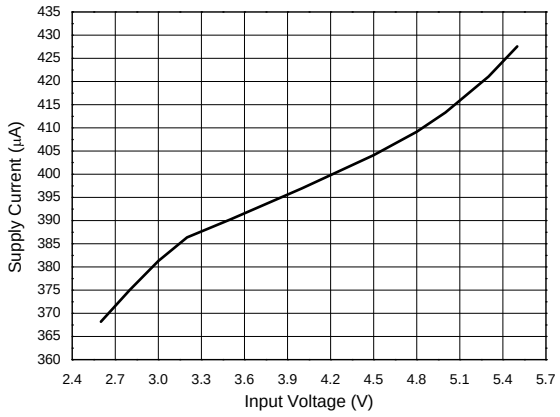
Symbol	Parameters	Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE (VIN PIN)						
V_{IN}	Input Voltage	—	2.95	—	5.5	V
I_Q	Quiescent Current	V_{FB}=0.9V, V_{IN}=5V, T_A=+25°C, R_T=400kΩ	—	360	575	μA
I_{SHDN}	Shutdown Supply Current	V_{EN}=0V,T_A=+25°C, 2.95V≤V_{IN}≤5.5V	—	2	5	μA
ENABLE AND UVLO (EN PIN)						
V_{EN_H}	Enable Threshold	Rising	1.16	1.25	1.37	V
V_{EN_L}		Falling	—	1.18	—	V
V_{UVLO}	Internal Under Voltage Lockout Threshold	—	—	2.6	2.8	V
V_{HYS}	Internal Under Voltage Hysteresis	—	—	150	—	mV

Electrical Characteristics (Cont.) (@V_{IN}=2.95 to 5.5V, T_A=+25ºC, unless otherwise specified. Specifications with **boldface type** apply over full operating temperature range from -40 to +85ºC.)

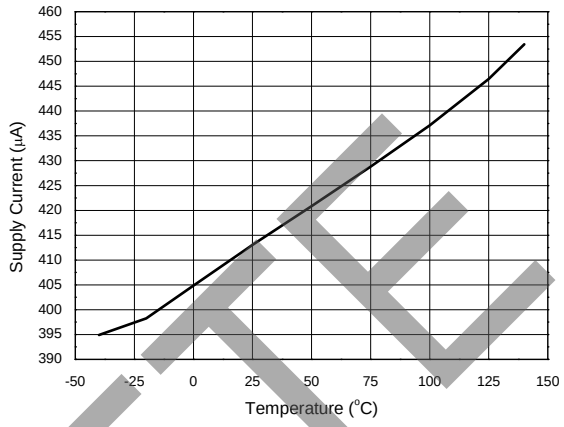
Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VOLTAGE REFERENCE (FB PIN)						
V_{REF}	Voltage Reference	2.95V≤V_{IN}≤5.5V	**0.779**	**0.803**	**0.827**	V
MOSFET						
R_{ON_H}	High Side Switch On-resistance	$V_{BOOT-SW}$=5V	—	30	60	mΩ
		$V_{BOOT-SW}$=2.95V	—	44	70	mΩ
R_{ON_L}	Low Side Switch On-resistance	V_{IN}=5V	—	30	60	mΩ
		V_{IN}=2.95V	—	44	70	mΩ
CURRENT LIMIT						
I_{LIMIT}	Current Limit Threshold	—	4.8	7.0	—	A
THERMAL SHUTDOWN						
T_{TSD}	Thermal Shutdown	—	—	+140	—	°C
—	Hysteresis	—	—	+20	—	°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
—	Switching Frequency Range (RT Mode)	—	200	—	2000	kHz
—	Switching Frequency Range (CLK Mode)	—	300	—	2000	kHz
f_S	Switching Frequency	R_T=400kΩ	400	500	600	kHz
—	Minimum CLK Pulse Width	—	75	—	—	ns
—	RT/CLK Voltage	R_T=400kΩ	—	0.5	—	V
—	RT/CLK High Threshold	—	—	1.6	2.2	V
—	RT/CLK Low Threshold	—	0.4	0.6	—	V
BOOT (BOOT PIN)						
R_{BOOT}	BOOT Charge Resistor	V_{IN}=5V	—	16	—	Ω
—	BOOT-SW UVLO	V_{IN}=2.95V	—	2.2	—	V
SOFT START (SS PIN)						
I_{SS}	Charge Current	V_{SS}=0.4V	—	2	—	μA
V_{SS}	SS to Reference Crossover	98% Nominal	—	1.1	—	V
POWER GOOD (PGD PIN)						
V_{FB_TH}	Feedback Threshold	V_{FB} Falling (Fault)	—	91	—	%V_{REF}
		V_{FB} Rising (Good)	—	93	—	
		V_{FB} Rising (Fault)	—	107	—	
		V_{FB} Falling (Good)	—	105	—	

Performance Characteristics

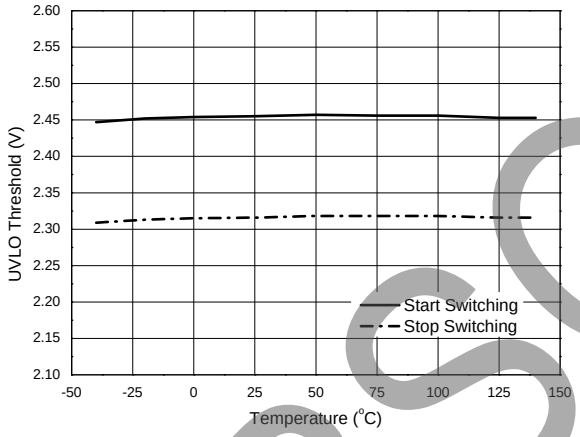
Supply Current vs. Input Voltage



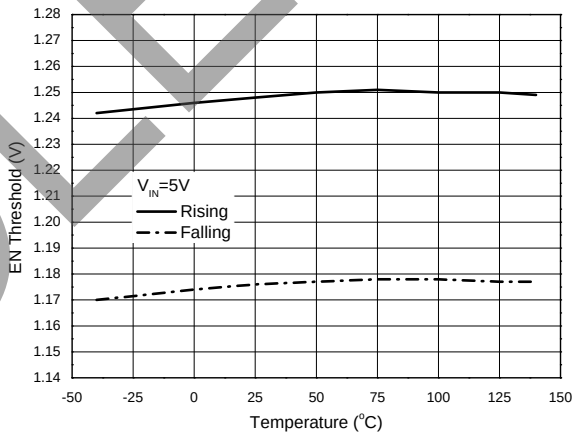
Supply Current vs. Temperature



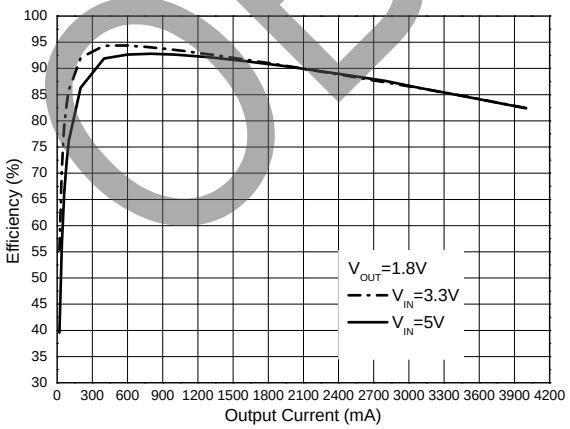
UVLO Threshold vs. Temperature



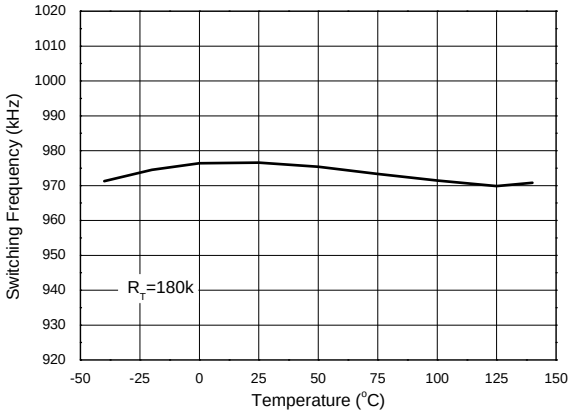
EN Threshold vs. Temperature



Efficiency vs. Output Current

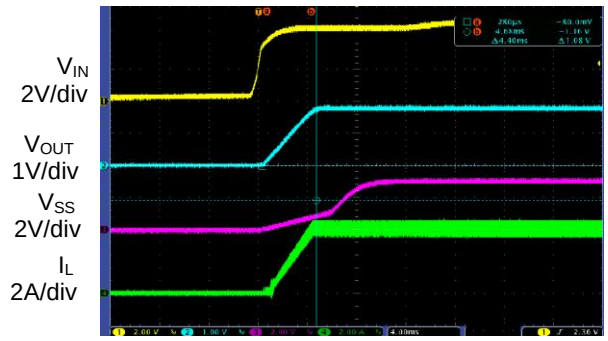


Switching Frequency vs. Temperature



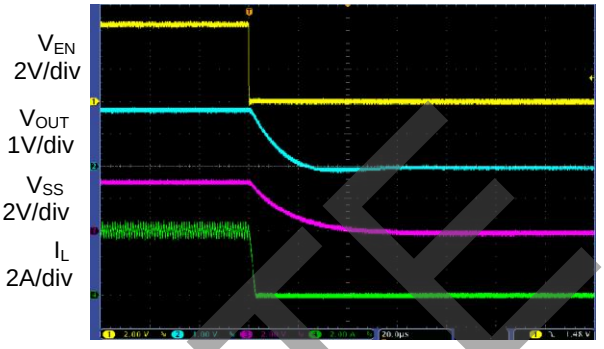
Performance Characteristics (Cont.)

Start Up from V_{IN} (V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



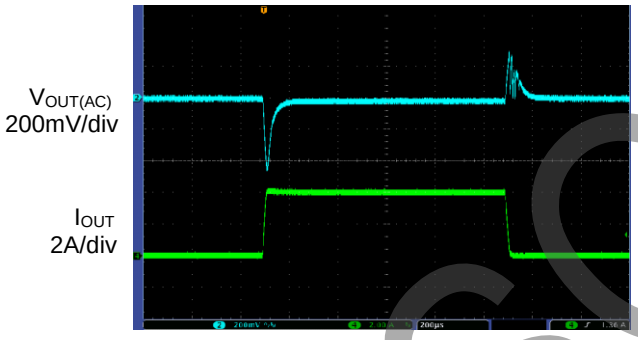
Time 4ms/div

Disable IC (V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



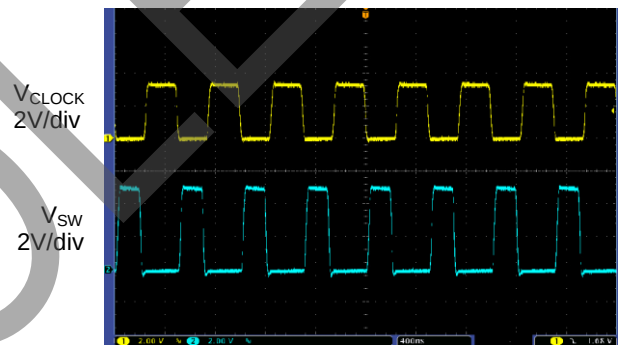
Time 20µs/div

Load Transient Response (V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0 to 4A)



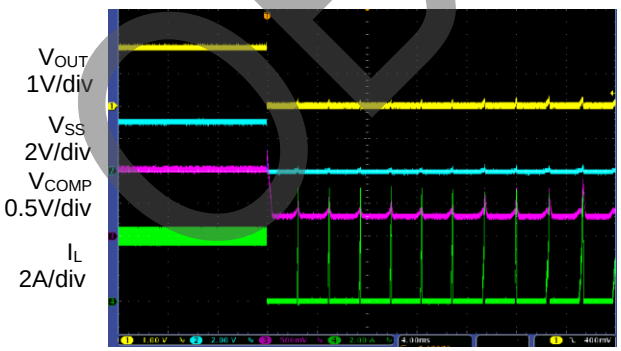
Time 200µs/div

Synchronizing to External Clock (f_{CLOCK}=2MHz)



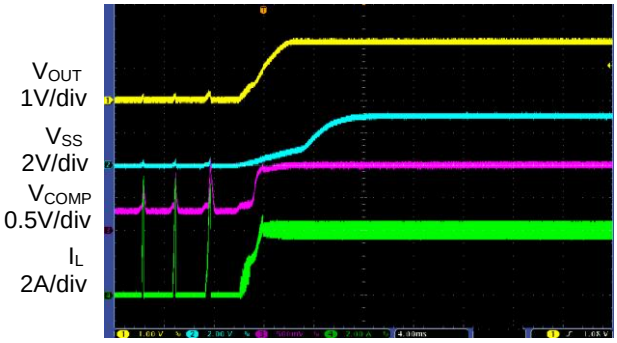
Time 400ns/div

Short Circuit Protection (V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



Time 4ms/div

Short Circuit Recovery (V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=4A)



Time 4ms/div

Application Note

Theory of Operation

The AP3440 consists of a reference voltage module, slope compensation circuit, error amplifier, PWM comparator, current limit circuit, two N-channel MOSFETs etc. (Refer to the Functional Block Diagram on page 3 for detailed information)

Soft-start

The AP3440 integrates an internal soft start circuit to minimize inrush currents or provide power supply sequencing during power up. A capacitor connected between SS pin and ground implements the soft-start time. The AP3440 has an internal pull-up current source of 2μA, which charges the external slow start capacitor. Equation 1 calculates the required slow start capacitor, I_{SS} is the internal slow start charging current of 2μA, and V_{REF} is the internal voltage reference of 0.803V.

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad \text{.....(1)}$$

During normal operation, if the V_{IN} goes below the UVLO, or the EN pin is pulled below 1.2V, or a thermal shutdown occurs, the AP3440 will stop switching and the SS pin will be discharged to 40mV before reinitiating a powering up sequence.

Enable and Adjusting UVLO

The AP3440 are disabled when the V_{IN} falls below 2.6V. If an application requires a higher under-voltage lockout (UVLO), use the EN pin as shown in Figure 1 to adjust the input voltage UVLO by using two external resistors. The EN pin has an internal pull-up current source that provides the default condition of the AP3440 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25V, an additional 2.55μA of hysteresis is added. When the EN pin is pulled below 1.18V, the 2.55μA hysteresis is removed. This additional current facilitates input voltage hysteresis.

For AP3440, the divider resistor R1 and R2 on the EN pin can be calculated according to equation 2 and 3.

$$R1 = \frac{0.944 \times V_{START} - V_{STOP}}{2.59 \times 10^{-6}} \quad \text{.....(2)}$$

$$R2 = \frac{1.18 \times R1}{V_{STOP} - 1.18 + R1 \times 3.2 \times 10^{-6}} \quad \text{.....(3)}$$

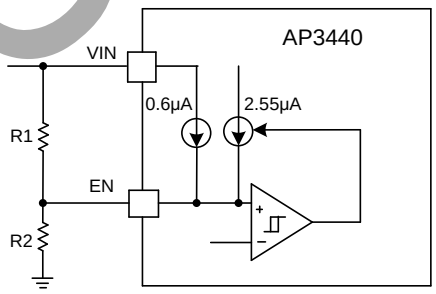


Figure 1. Adjustable Under Voltage Lock Out

Adjusting Output Voltage

The output voltage is set with a resistor divider from the FB pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 10kΩ R2 resistor and use the equation 4 to calculate R1. To improve efficiency at very light loads consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

Application Note (Cont.)

Resistor R1 can be calculated according to equation 4.

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.803} - 1 \right) \quad \text{..... (4)}$$

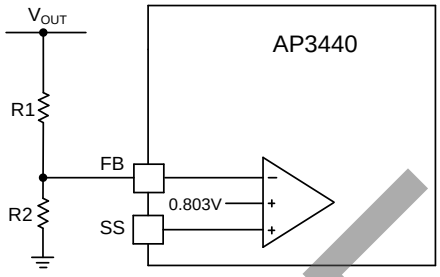


Figure 2. Voltage Divider Circuit

Synchronize Using the RT/CLK Pin

The RT/CLK pin of AP3440 is used to synchronize the converter with an external system clock referring to Figure 3. To implement the synchronization feature in a system, connect a square wave to the RT/CLK pin with an on-time of at least 75ns. When the clock is detected on the RT/CLK pin, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to the frequency set by the resistor. The low level of the square wave must be lower than 0.6V and the high level higher than 1.6V typically. The synchronization frequency range is from 300kHz to 2000kHz. The rising edge of the SW is synchronized to the falling edge of RT/CLK pin. Figure 4 shows a typical synchronizing waveform, the clock frequency is 2MHz.

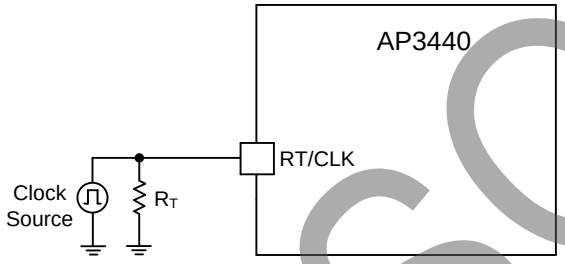


Figure 3. Synchronizing to a System Clock

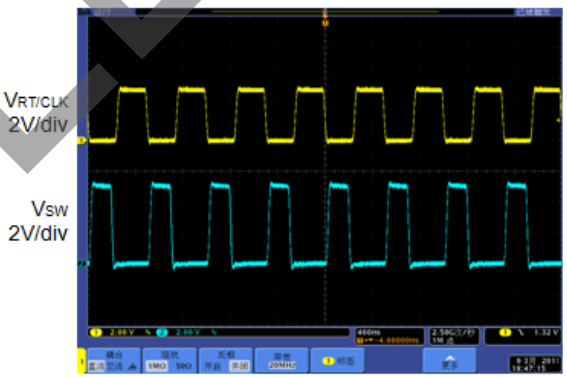


Figure 4. Synchronizing Waveform

Constant Switching Frequency and Timing Resistor

The switching frequency of the AP3440 is adjustable over a wide range from 200kHz to 2000kHz by placing a resistor with maximum value of 1000kΩ and minimum of 85kΩ, respectively, on the RT/CLK pin. An internal amplifier holds this pin at a fixed voltage when connecting an external resistor to ground to set the switching frequency. The $V_{RT/CLK}$ is typically 0.5V. To determine the timing resistance for a given switching frequency, use the equation 5.

$$R_T(k\Omega) = \frac{311890}{f_{SW}(kHz)^{1.0793}} \quad \text{.....(5)}$$

$$f_{SW}(kHz) = \frac{133870}{R_T(k\Omega)^{0.9393}} \quad \text{.....(6)}$$

To reduce the solution size one should typically set the switching frequency as high as possible, but tradeoffs of the efficiency, maximum input voltage and minimum controllable on time should be considered.

Application Note (Cont.)

Over Current Protection

The AP3440 implements a cycle-by-cycle current limit. The high side switch current is detected during each cycle. During SCP conditions, V_{OUT} is pulled down and V_{COMP} is drived to high, increasing the switch current. When the increased high side switch current is continuously detected to trigger the current limit of high side switch 6 times, the high side and low side switches are turned off for about 2.5ms. Then both switches start switching and they will not be turned off until the next 6 OCPs are triggered. The IC works with a hiccup mode during SCP conditions.

Power Good

The PGD pin output is an open drain MOSFET. The output is pulled low when the FB voltage enters the fault condition by falling below 91% or rising above 107% of the nominal internal reference voltage. There is a 2% hysteresis on the threshold voltage, so when the FB voltage rises to the good condition above 93% or falls below 105% of the internal voltage reference the PGD output MOSFET is turned off. It is recommended to use a pull-up resistor between the values of 1kΩ and 100kΩ to a voltage source that is 5V or less. The PGD is in a valid state once the VIN input voltage is greater than 1.2V.

Thermal Shutdown

The AP3440 implement an internal thermal shutdown to protect itself if the junction temperature exceeds +140°C. Switching is stopped when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below +120°C, the device reinitiates the soft start operation. The thermal shutdown hysteresis is +20°C.

Component Selection

Typical application circuit of AP3440 is shown in Figure 5. For the major component selection please refer to the following section.

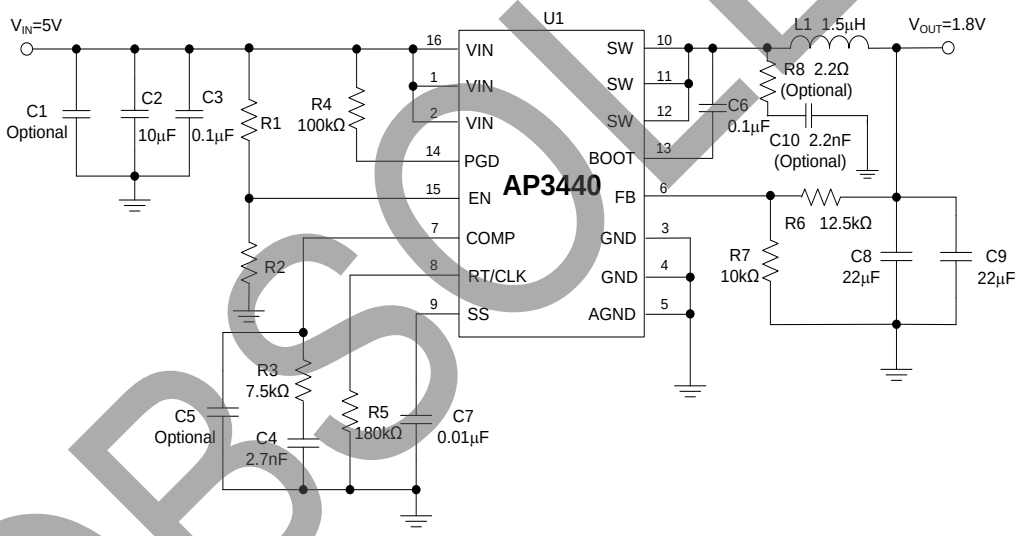


Figure 5. Typical Application of AP3440

Input Capacitor

The AP3440 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 4.7µF effective capacitance and in some applications a bulk capacitor. The effective capacitance includes any DC bias effects. To ensure a stable operation, the input capacitor should be placed as close to the VIN pin as possible, and its value varies according to different load and different characteristic of input impedance.

There are two important parameters of the input capacitor: the voltage rating and RMS current rating. The voltage rating of the input capacitor should be at least 1.25 times larger than the maximum input voltage. The capacitor must also have a RMS current rating greater than the maximum input current ripple of the AP3440. The RMS current of input capacitor can be expressed as:

$$I_{CIN\_RMS} = I_{OUT(MAX)} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad \text{.....(7)}$$

Application Note (Cont.)

Output Capacitor

The output capacitor is the most critical component of a switching regulator. It is used for filtering output and keeping the loop stable. The typical value is 44μF.

The primary parameters for output capacitor are the voltage rating and the equivalent series resistance (ESR). A low ESR capacitor is preferred to keep the output voltage ripple low. The output ripple is calculated as the following:

$$\Delta V_{OUT} \approx \Delta I_L \times (R_{ESR} + \frac{1}{8 \times f \times C_{OUT}}) \quad \text{.....(8)}$$

Where f is the switching frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor.

Inductor

The inductor is used to supply smooth current to output when it is driven by a switching voltage. The higher the inductance, the lower the peak-to-peak ripple current, as the higher inductance usually means the larger inductor size, so some trade-offs should be made when select an inductor. The AP3440 is a synchronous buck converter. It always works on continuous current mode (CCM), and the inductor value can be selected as the following:

$$L = V_{OUT} \times (\frac{V_{IN} - V_{OUT}}{f \times V_{IN} \times I_{OUT} \times k}) \quad \text{..... ....(9)}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, I_{OUT} is the output current, k is the coefficient of ripple current, and its typical value is 20% to 40%. Another important parameter for the inductor is the current rating. Exceeding an inductor's maximum current rating may cause the inductor to saturate and overheat. If inductor value has been selected, the peak inductor current can be calculated as the following:

$$I_{PEAK} = I_{OUT} + V_{OUT} \times (\frac{V_{IN} - V_{OUT}}{2 \times f \times V_{IN} \times L}) \quad \text{.....(10)}$$

It should be ensured that the current rating of the selected inductor is 1.5 times of the I_{PEAK}.

Slow Start Capacitor

The slow start capacitor determines the output voltage soft start time during power up.

The slow start capacitor value can be calculated using equation 11.

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad \text{..... (11)}$$

In AP3440, I_{SS} is 2μA and V_{REF} is 0.803V.

Bootstrap Capacitor

A 0.1μF ceramic capacitor must be connected between the BOOT pin and the SW pin for normal operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric.

Feedback Resistors

It is recommended to use divider resistors with 1% tolerance or better. Start with a 10kΩ for the R7 resistor and use the equation 12 to calculate R6.

$$R6 = R7 \times \left(\frac{V_{OUT}}{0.803} - 1 \right) \quad \text{.....(12)}$$

Application Note (Cont.)

Compensation

The output capacitor and the load resistance largely determine where the error amplifier poles and zeros need to be placed for optimum transient response and loop stability. The corner frequency of the pole and zero generated by output capacitor are:

$$f_{P1} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}} \quad \text{.....(13)}$$

$$f_{Z1} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad \text{..... .. (14)}$$

Where R_{LOAD} is the load resistance, C_{OUT} is the output capacitance and R_{ESR} is the capacitor ESR.

The error amplifier provides most of the loop gain. After selecting the output capacitor, the control loop is compensated by tailoring the frequency response of the error amplifier. The low frequency pole of the error amplifier is the dominant pole and is determined primarily by C_{COMP} and the output resistance of the error amplifier as shown by:

$$f_{P2} = \frac{1}{2\pi \times R_{OUT\_EA} \times C_{COMP}} \quad \text{.....(15)}$$

Resistor R_{COMP} adds a zero to the frequency response to control gain in the mid frequency range. This zero frequency is:

$$f_{Z2} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \quad \text{.....(16)}$$

Where R_{COMP} and C_{COMP} are compensation resistor and capacitor connected to COMP pin, R_{OUT_EA} is the output impedance of the error amplifier. A 7.5kΩ resistor and 2.7nF capacitor are used in typical application.

Layout Consideration

PCB layout is very important to the performance of AP3440. The loop which switching current flows through should be kept as short as possible. The external components (especially C_{IN}) should be placed as close to the IC as possible.

The feedback trace should be routed far away from the inductor and noisy power traces, and it needs to be routed as direct as possible. Locate the feedback divider resistor network near the feedback pin with short leads.

Since the SW connection is the switching node, the output inductor should be located very close to the SW pins, and the area of the PCB conductor is minimized to prevent excessive capacitive coupling.

The boot capacitor must also be located close to the device. The sensitive analog ground connections for the feedback voltage divider, compensation components, slow start capacitor and frequency set resistor should be connected to a separate analog ground trace.

The RT/CLK pin is sensitive to noise so the R_T resistor should be located as close as possible to the IC and routed with minimal lengths of trace.

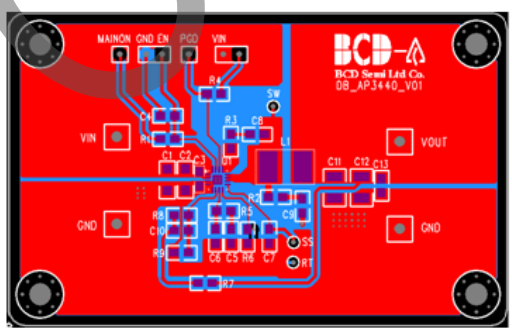


Figure 6. Top View of PCB Layout

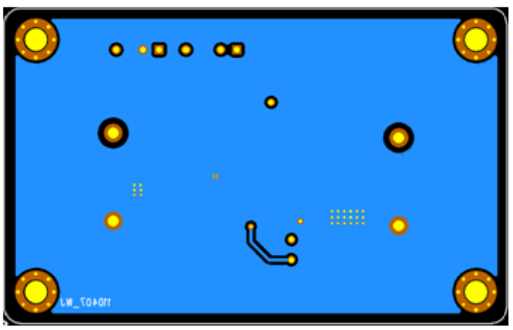
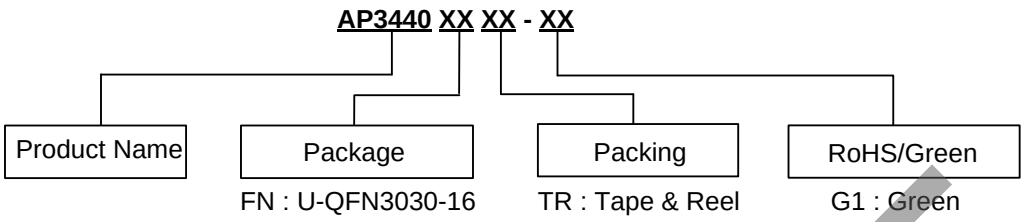


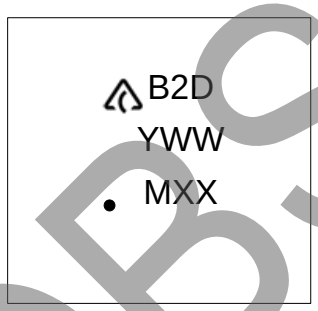
Figure 7. Bottom View of PCB Layout

Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing
U-QFN3030-16	-40 to +85ºC	AP3440FNTR-G1	B2D	5000/Tape & Reel

Marking Information

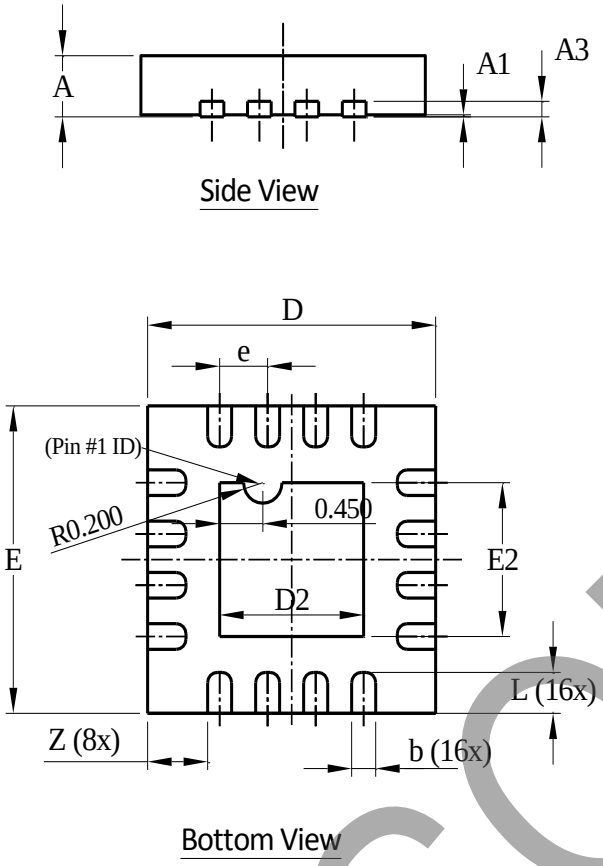


: AAC Logo
B2D: Marking ID (Per Datasheet)
YWW: Year and Work Week of Mold Operation
M: Assembly Site Code
XX: The 7th & 8th Digits of Batch No.
- Pin 1 Mark

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: U-QFN3030-16

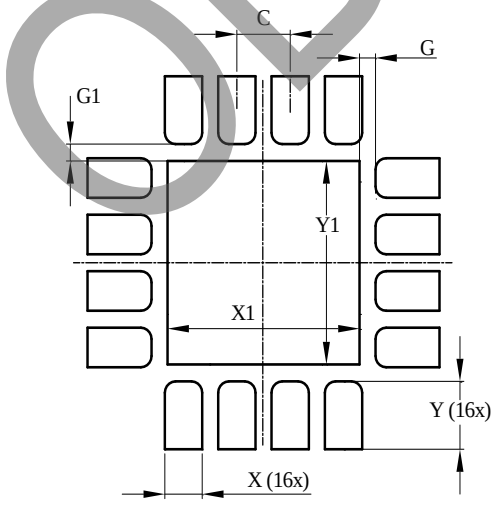


U-QFN3030-16 Type B			
Dim	**Min**	**Max**	**Typ**
A	0.55	0.65	0.60
A1	0	0.05	0.02
A3	–	–	0.15
b	0.18	0.28	0.23
D	2.95	3.05	3.00
D2	1.40	1.60	1.50
E	2.95	3.05	3.00
E2	1.40	1.60	1.50
e	–	–	0.50
L	0.35	0.45	0.40
Z	–	–	0.625
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: U-QFN3030-16



Dimensions	Value (in mm)
C	0.500
G	0.150
G1	0.150
X	0.350
X1	1.800
Y	0.600
Y1	1.800

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