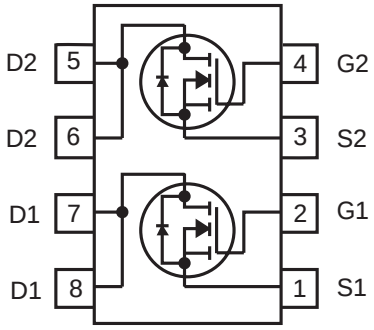
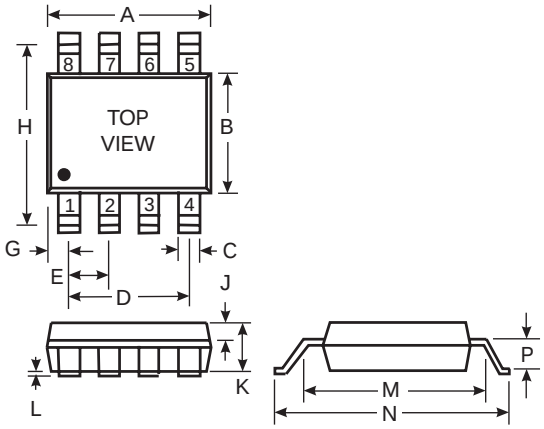
DI9956

DUAL N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

Features

- High Cell Density DMOS Technology
- Lower On-State Resistance
- High Power and Current Capability
- Fast Switching Speed
- High Transient Tolerance





SO-8		
Dim	**Min**	**Max**
A	3.94	4.19
B	3.20	3.40
C	0.381	0.495
D	2.67	3.05
E	0.89	1.02
G	0.527	0.679
J	0.41 Nominal	
K	0.94	1.09
L	0.025	0.152
M	4.37	4.62
N	4.39	4.70
P	0.939 Nominal	
All Dimensions in mm		

Mechanical Data

- SO-8 Plastic Case
- Terminal Connections: See Outline Drawing and Internal Circuit Diagram above

Maximum Ratings @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current — Note 1a Continuous Pulsed	I_D	±3.7 ±15	A
Power Dissipation for: Dual Operation (Note 1d) Single Operation (Note 1a) (Note 1b) (Note 1c)	P_d	 2.0 1.6 1.0 0.9	W
Operating and Storage Temperature Range	T_j, T_{STG}	-55 to +150	°C

Thermal Characteristics @ T_A = 25°C unless otherwise specified

Characteristic		Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	Note 1a	$R_{\Theta JA}$	78	°C/W
Thermal Resistance, Junction-to-Case	Note 1	$R_{\Theta JC}$	40	°C/W

Notes: 1. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance ($R_{\Theta JC}$ + $R_{\Theta CA}$) where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\Theta JC}$ in this instance is 40°C/W but is dependent on the specific circuit board thermal design.

1a. With 0.5 in^2 of 2 oz. copper mounting pad $R_{\Theta JA}$ = 78°C\W.

1b. With 0.02 in^2 of 2 oz. copper mounting pad $R_{\Theta JA}$ = 125°C\W.

1c. With 0.003 in^2 of 2 oz. copper mounting pad $R_{\Theta JA}$ = 135°C\W.

1d. With 1.0 in^2 of 2 oz. copper mounting pad, total power dissipation of up to 2W for dual operation can be achieved

Electrical Characteristics @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current T_j = 55°C	I_{DSS}	—	—	2.0 25	µA	V_{DS} = 24V, V_{GS} = 0V
Gate-Body Leakage, Forward	I_{GSSF}	—	—	100	nA	V_{GS} = 20V, V_{DS} = 0V
Gate-Body Leakage, Reverse	I_{GSSR}	—	—	-100	nA	V_{GS} = -20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage T_j = 125°C	$V_{GS(th)}$	1.0 0.7	1.7 1.2	2.8 2.2	V	VDS = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance T_j = 125°C T_j = 125°C	$R_{DS\ (ON)}$	—	0.06 0.08 0.08 0.11	0.08 0.13 0.11 0.18	Ω	V_{GS} = 10V, I_D = 2.2A V_{GS} = 10V, I_D = 2.2A V_{GS} = 4.5V, I_D = 1.0A V_{GS} = 4.5V, I_D = 1.0A
On-State Drain Current	$I_{D(ON)}$	15 3.5	—	—	A	V_{GS} = 10V, V_{DS} = 10V V_{GS} = 4.5V, V_{DS} = 10V
Forward Transconductance	g_{FS}	—	6.0	—	℧	V_{DS} = 15V, I_D = 3.7A
DYNAMIC CHACTERISTICS						
Input Capacitance	C_{ISS}	—	320	—	pF	V_{DS} = 10V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{OSS}	—	225	—	pF	
Reverse Transfer Capacitance	C_{RSS}	—	85	—	pF	
SWITCHING CHARACTERISTICS (Note 2)						
Turn-On Delay Time	$t_{D(ON)}$	—	10	20	ns	V_{DD} = 10V, I_D = 1.0A V_{GEN} = 10V, R_{GEN} = 6.0Ω
Turn-On Rise Time	t_r	—	13	20	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	21	50	ns	
Turn-Off Fall Time	t_f	—	5.0	50	ns	
Total Gate Charge	Q_g	—	9.5	27	nC	V_{DS} =10V, I_D = 3.7A. V_{GS} = 10V
Gate-Source Charge	Q_{gs}	—	1.5	—	nC	
Gate-Drain Charge	Q_{gd}	—	3.3	—	nC	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Max Continuous Drain-Source Diode Forward Current	I_S	—	—	1.2	A	
Drain-Source Diode Forward Voltage	V_{SD}	—	0.8	1.3	V	V_{GS} = 0V, I_S = 1.25A (Note 2)
Reverse Recovery Time	t_{rr}	—	—	100	ns	V_{GS} = 0V, I_F = 1.25A, dI_F/dt = 100A/µs

Note: 2. Pulse Test: Pulse width ≤ 300 µs duty cycle ≤ 2%.

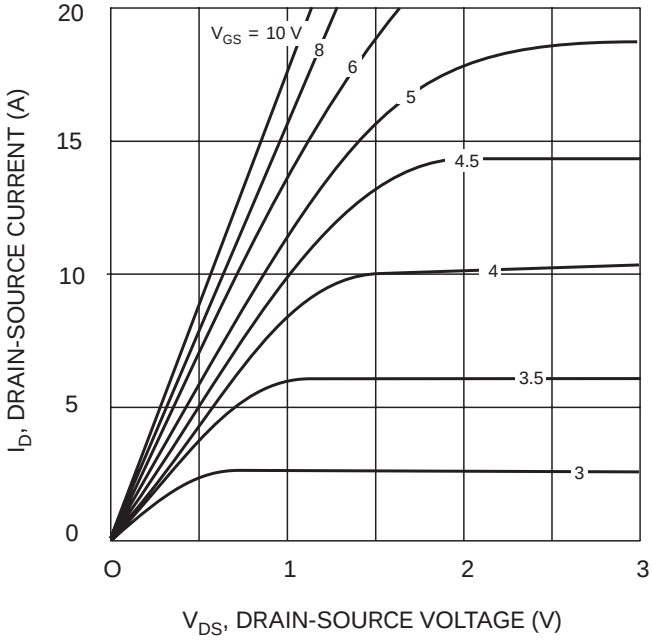


Fig. 1, On-Region Characteristics

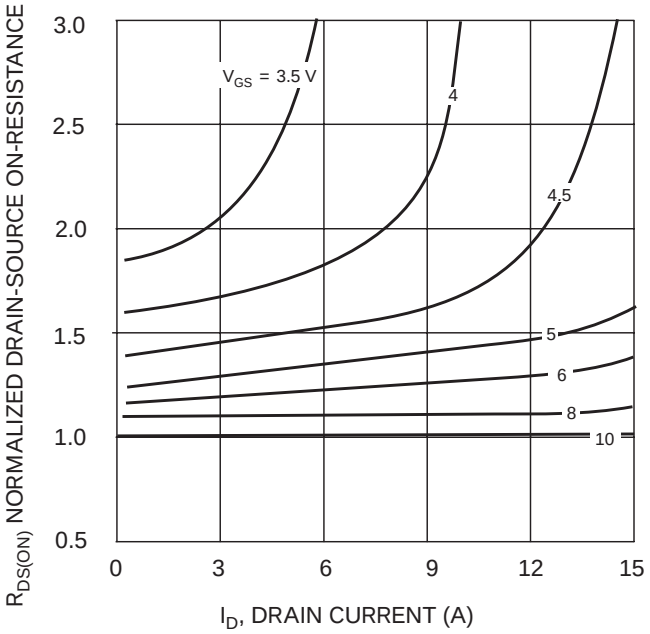


Fig. 2, On-Resistance vs Gate Voltage and Drain Current

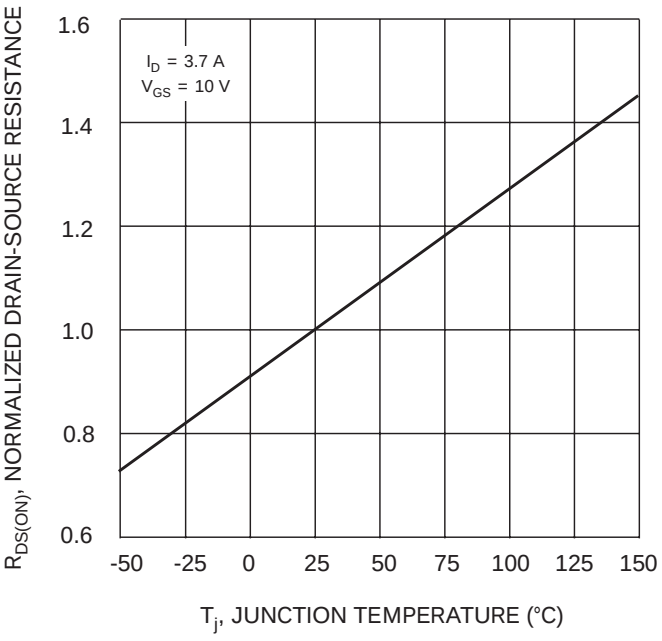


Fig. 3, On-Resistance vs Temperature

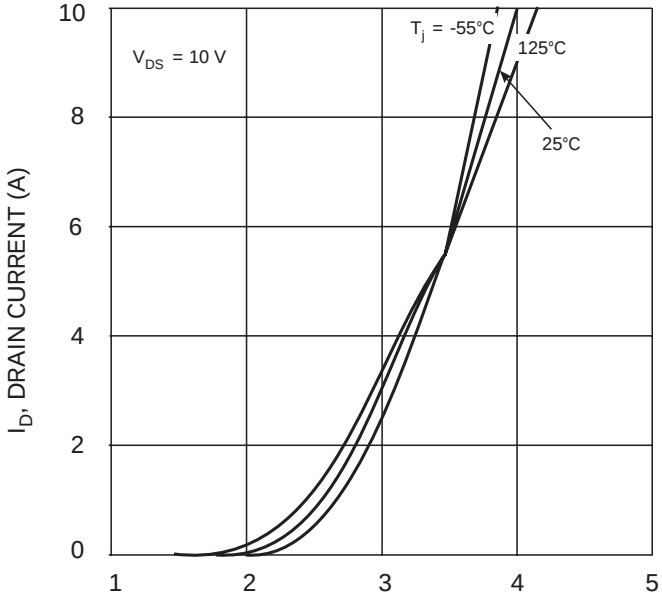


Fig. 4, Transfer Characteristics

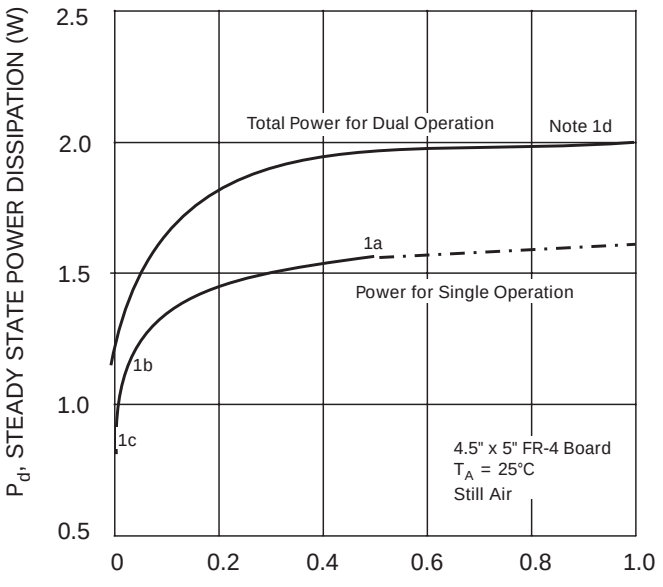


Fig. 5, Steady State Pwr Dissipation vs Copper Mtg Pad Area

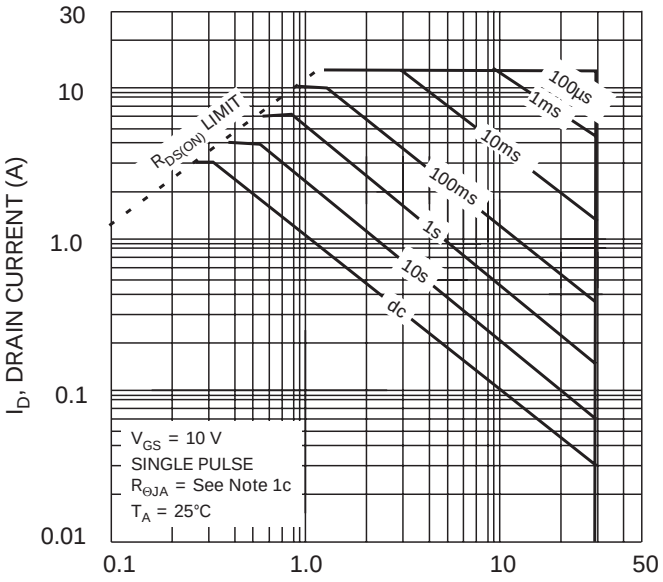


Fig. 6, Maximum Safe Operating Area

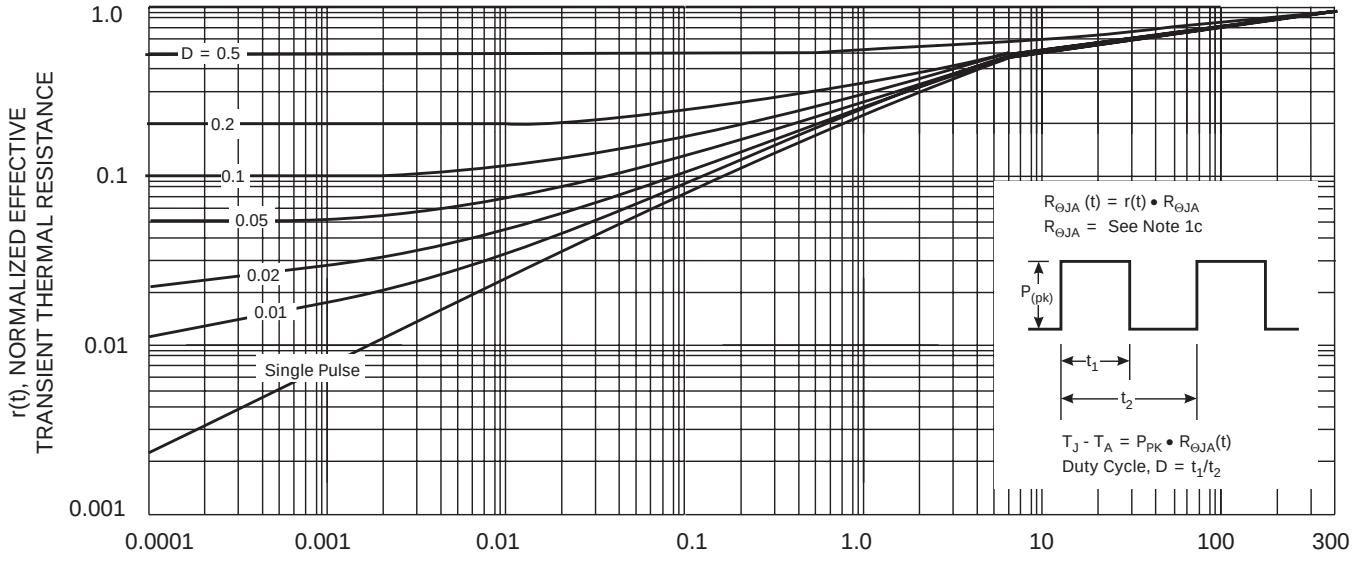


Fig. 7, Typical Normalized Transient Thermal Impedance Curves

Remark: Thermal characterization performed under conditions of Note 1c. Better thermal design such as shown in Notes 1a and 1b or 1d will offer lower $R_{\Theta JA}$ values and allow junction to reach thermal equilibrium sooner.