LMK60E2-100M, LMK60E2-125M, LMK60E2-156M, LMK60E0-156M
LMK60E0-212M, LMK60I2-100M, LMK60I2-322M
SNAS718C – DECEMBER 2016 – REVISED DECEMBER 2017

LMK60XX High Performance Low Jitter Oscillator

1 Features

- Low Noise, High Performance
  - Jitter: 150 fs RMS Typical Fout > 100 MHz
  - PSRR: –60 dBc, Robust Supply Noise Immunity
- Supported Output Format
  - LVPECL, LVDS and HCSL up to 400 MHz
- Total Frequency Tolerance of ±50 ppm (LMK60X2) and ±25 ppm (LMK60X0)
- 3.3-V Operating Voltage
- Industrial Temperature Range (–40ºC to +85ºC)
- 7-mm × 5-mm 6-pin Package That is Pin-Compatible With Industry Standard 7050 XO Package

2 Applications

- High-Performance Replacement for Crystal-, SAW-, or Silicon-Based Oscillators
- Switches, Routers, Network Line Cards, Base Band Units (BBU), Servers, Storage/SAN
- Test and Measurement
- Medical Imaging
- FPGA, Processor Attach

3 Description

The LMK60EX is a family of low jitter oscillators that generate a commonly used reference clock. The device is pre-programmed in factory to support any reference clock frequency; supported output formats are LVPECL, LVDS, and HCSL up to 400 MHz. Internal power conditioning provide excellent power supply ripple rejection (PSRR), reducing the cost and complexity of the power delivery network. The device operates from a single 3.3-V ±5% supply.

Device Information(1)

PART NUMBER	PACKAGE	SIZE
LMK60E2-100M	QFM (6)	7.00 mm × 5.00 mm
LMK60E2-125M	QFM (6)	7.00 mm × 5.00 mm
LMK60E2-156M	QFM (6)	7.00 mm × 5.00 mm
LMK60E0-156M	QFM (6)	7.00 mm × 5.00 mm
LMK60E0-212M	QFM (6)	7.00 mm × 5.00 mm
LMK60I2-100M	QFM (6)	7.00 mm × 5.00 mm
LMK60I2-322M	QFM (6)	7.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Output Frequency Options

PART NUMBER	OUTPUT FREQ (MHz) AND FORMAT	TOTAL FREQ STABILITY (ppm)
LMK60E2-100M	100 LVPECL	±50
LMK60E2-125M	125 LVPECL	±50
LMK60E2-156M	156.25 LVPECL	±50
LMK60E0-156M	156.25 LVPECL	±25
LMK60E0-212M	212.5 LVPECL	±25
LMK60I2-100M	100 HCSL	±50
LMK60I2-322M	322.265625 HCSL	±50

Pinout

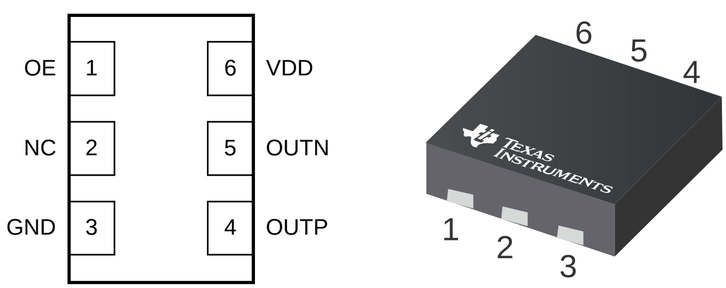


Table of Contents

4 Revision History

Changes from Revision B (November 2017) to Revision C — **Page**

- New release of LMK60E2-100M 1

Changes from Revision A (June 2017) to Revision B — **Page**

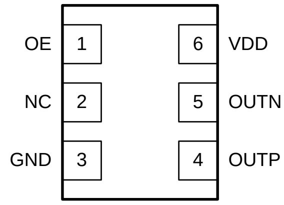
- New release of LMK60E2-125M 1
- New release of LMK60I2-100M 1
- New release of LMK60I2-322M 1

Changes from Original (December 2016) to Revision A — **Page**

- Added LMK60E0-156M and LMK60E0-212M 1

5 Pin Configuration and Functions

SIA Package
6-pin QFM
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
POWER			
GND	3	Ground	Device ground
VDD	6	Analog	3.3-V power supply
OUTPUT BLOCK			
OUTP, OUTN	4, 5	Universal	Differential output pair (LVPECL, LVDS or HCSL).
DIGITAL CONTROL / INTERFACES			
NC	2	N/A	No connect
OE	1	LVCMOS	Output enable (internal pullup). When set to low, output pair is disabled and set at high impedance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
VDD	Device supply voltage	–0.3	3.6	V
V_{IN}	Output voltage for logic inputs	–0.3	VDD + 0.3	V
V_{OUT}	Output voltage for clock outputs	–0.3	VDD + 0.3	V
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device supply voltage	3.135	3.3	3.465	V
T_A	Ambient temperature	–40	25	85	°C
T_J	Junction temperature			105	°C
t_{RAMP}	VDD power-up ramp time	0.1		100	ms

6.4 Thermal Information

THERMAL METRIC(1)		LMK60EX (2) (3) (4)	UNIT
		SIA (QFM)	
		6 PINS	
		Airflow (LFM) 0	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal resistance is calculated on a 4 layer JEDEC board.
(3) Connected to GND with 2 thermal vias (0.3-mm diameter).
(4) ψJB (junction to board) is used when the main heat flow is from the junction to the GND pad. Please refer to Thermal Considerations section for more information on ensuring good system reliability and quality.

6.5 Electrical Characteristics - Power Supply(1)

VDD = 3.3 V ± 5%, T_A = -40C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Device current consumption	LVPECL(2)		95	110	mA
		LVDS		85	100	
		HCSL(3)		90	105	
IDD-PD	Device current consumption when output is disabled	OE = GND		70		mA

(1) Refer to *Parameter Measurement Information* for relevant test conditions.
(2) On-chip power dissipation should exclude 40 mW, dissipated in the 150 Ω termination resistors, from total power dissipation.
(3) Excludes load current.

6.6 LVPECL Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency(2)				400	MHz
V_{OD}	Output voltage swing (V_{OH} – V_{OL})(2)		700	950	1200	mV
$V_{OUT, DIFF, PP}$	Differential output peak-to-peak swing			2 × $\|V_{OD}\|$		V
V_{OS}	Output common-mode voltage			VDD – 1.45		V
t_R / t_F	Output rise/fall time (20% to 80%)(3)			260	350	ps
ODC	Output duty cycle(3)		45%		55%	

(1) Refer to *Parameter Measurement Information* for relevant test conditions.
(2) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(3) Ensured by characterization.

6.7 LVDS Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency(1)				400	MHz
V_{OD}	Output voltage swing (V_{OH} – V_{OL})(1)		300	390	480	mV
$V_{OUT, DIFF, PP}$	Differential output peak-to-peak swing			2 x |V_{OD}|		V
V_{OS}	Output common-mode voltage			1.2		V
t_R / t_F	Output rise/fall time (20% to 80%)(2)			260	350	ps
ODC	Output duty cycle(2)		45%		55%	
R_{OUT}	Differential output impedance			107		Ω

(1) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.
(2) Ensured by characterization.

6.8 HCSL Output Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT}	Output frequency				400	MHz
V_{OH}	Output high voltage		660		900	mV
V_{OL}	Output low voltage		–100		100	mV
V_{CROSS}	Absolute crossing voltage(2)(3)		250		475	mV
$V_{CROSS\text{-}DELTA}$	Variation of V_{CROSS}(2)(3)		0		140	mV
dV/dt	Slew rate(4)		1		3	V/ns
ODC	Output duty cycle(4)		45%		55%	

(1) Refer to *Parameter Measurement Information* for relevant test conditions.
(2) Measured from –150 mV to +150 mV on the differential waveform with the 300 mVpp measurement window centered on the differential zero crossing.
(3) Ensured by design.
(4) Ensured by characterization.

6.9 OE Input Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		1.4			V
V_{IL}	Input low voltage				0.6	V
I_{IH}	Input high current	V_{IH} = VDD	–40		40	µA
I_{IL}	Input low current	V_{IL} = GND	–40		40	µA
C_{IN}	Input capacitance			2		pF

6.10 Frequency Tolerance Characteristics(1)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_T	Total frequency tolerance	LMK60X2: All output formats, frequency bands and device junction temperature up to 105°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and 5-year aging at 40°C	–50		50	ppm
		LMK60X0: All output formats, frequency bands and device junction temperature up to 105°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and 5-year aging at 40°C	–25		25	ppm

(1) Ensured by characterization.

6.11 Power-On/Reset Characteristics (VDD)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{THRESH}	Threshold voltage (1)		2.85		3	V
V_{DROOP}	Allowable voltage droop (2)				0.1	V
$t_{STARTUP}$	Start-up time (1)	Time elapsed from VDD at 3.135 V to output enabled			10	ms
t_{OE-EN}	Output enable time (2)	Time elapsed from OE at V_{IH} to output enabled			50	µs
t_{OE-DIS}	Output disable time (2)	Time elapsed from OE at V_{IL} to output disabled			50	µs

(1) Ensured by characterization.
(2) Ensured by design.

6.12 PSRR Characteristics (1)

VDD = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Spurs induced by 50-mV power supply ripple (2)(3) at 156.25-MHz output, all output types	Sine wave at 50 kHz		–60		dBc
		Sine wave at 100 kHz		–60		
		Sine wave at 500 kHz		–60		
		Sine wave at 1 MHz		–60		

(1) Refer to *Parameter Measurement Information* for relevant test conditions.
(2) Measured max spur level with 50 mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD pin
(3) DJ_{SPUR} (ps, pk-pk) = [2*10(SPUR/20) / (π*f_{OUT})]*1e6, where PSRR or SPUR in dBc and f_{OUT} in MHz.

6.13 PLL Clock Output Jitter Characteristics (1)(2)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ	RMS phase jitter (3) (12 kHz – 20 MHz)	f_{OUT} ≥ 100 MHz, all output types		150	250	fs RMS

(1) Refer to *Parameter Measurement Information* for relevant test conditions.
(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).
(3) Ensured by characterization.

6.14 Additional Reliability and Qualification

PARAMETER	CONDITION / TEST METHOD
Mechanical Shock	MIL-STD-202, Method 213
Mechanical Vibration	MIL-STD-202, Method 204
Moisture Sensitivity Level	J-STD-020, MSL3

7 Parameter Measurement Information

7.1 Device Output Configurations

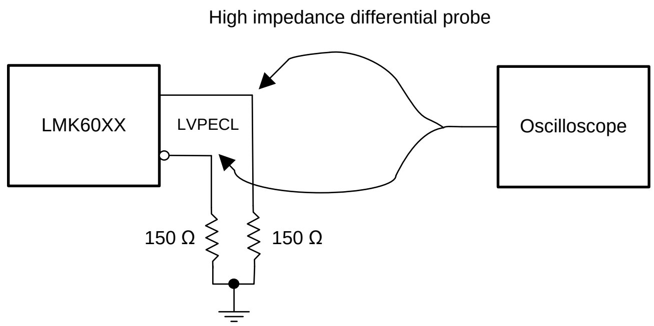


Figure 1. LVPECL Output DC Configuration During Device Test

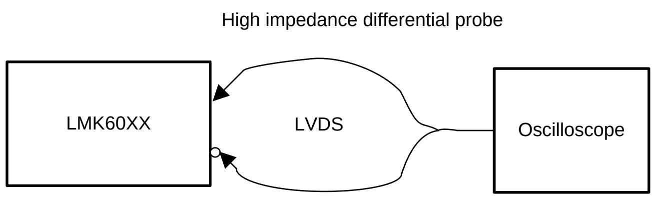


Figure 2. LVDS Output DC Configuration During Device Test

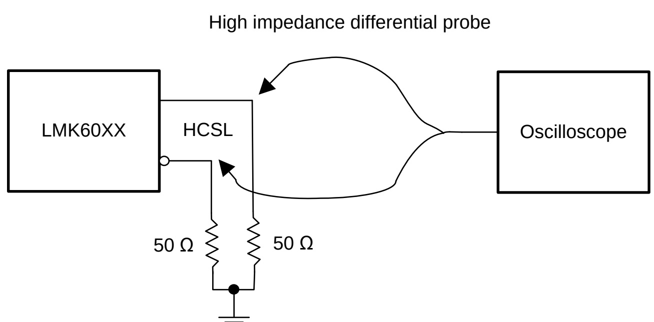


Figure 3. HCSL Output DC Configuration During Device Test (1)

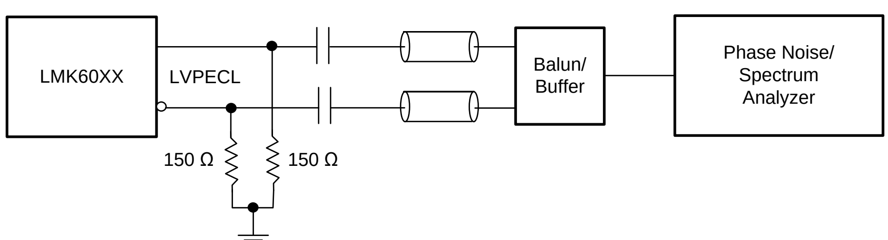


Figure 4. LVPECL Output AC Configuration During Device Test

(1) Also compatible with 85 Ω termination

Device Output Configurations (continued)

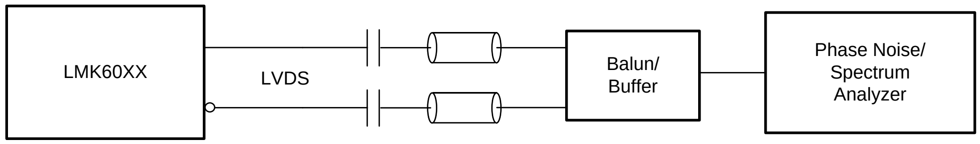


Figure 5. LVDS Output AC Configuration During Device Test

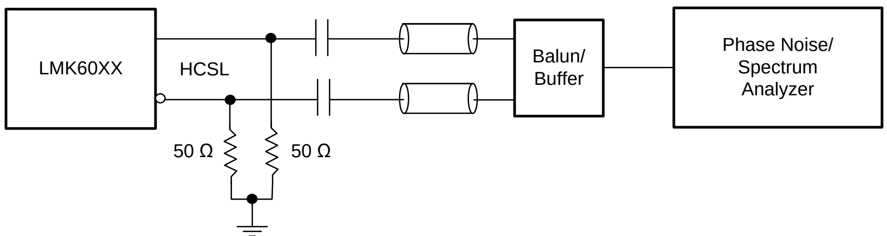


Figure 6. HCSL Output AC Configuration During Device Test

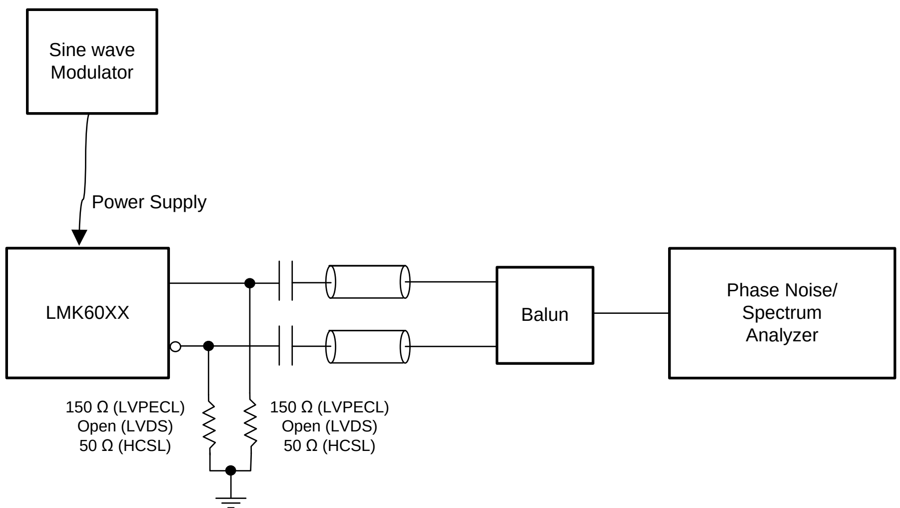


Figure 7. PSRR Test Setup

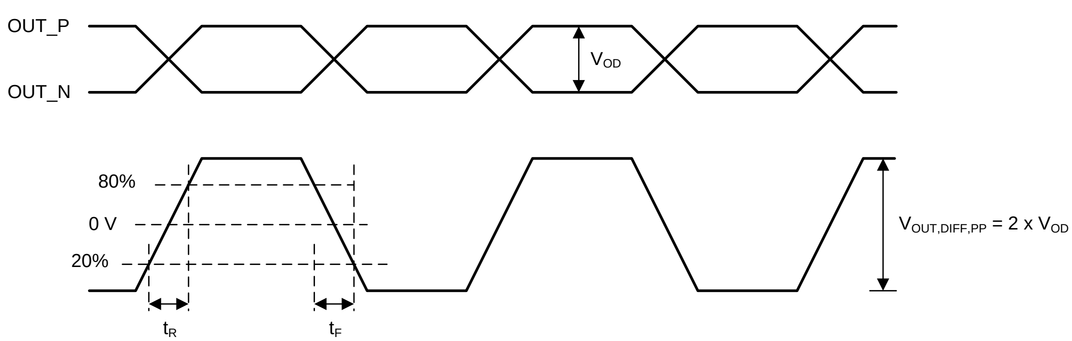


Figure 8. Differential Output Voltage and Rise/Fall Time

8 Power Supply Recommendations

For best electrical performance of LMK60EX, TI recommends using a combination of 10 µF, 1 µF, and 0.1 µF on its power-supply bypass network. TI also recommends using component side mounting of the power-supply bypass capacitors and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. Figure 9 shows the layout recommendation for power supply decoupling of LMK60EX.

9 Layout

9.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile, and power supply bypassing when using LMK60EX to ensure good thermal and electrical performance, along with overall signal integrity of entire system.

9.1.1 Ensuring Thermal Reliability

The LMK60EX is a high-performance device. Therefore, pay careful attention to device configuration and the printed-circuit board (PCB) layout with respect to power consumption. The ground pin must be connected to the ground plane of the PCB through three vias or more, as shown in Figure 9, to maximize thermal dissipation out of the package.

Equation 1 describes the relationship between the PCB temperature around the LMK60EX and its junction temperature.

$$T_B = T_J - \Psi_{JB} * P \quad (1)$$

where

- T_B: PCB temperature around the LMK60EX
- T_J: Junction temperature of LMK60EX
- Ψ_{JB}: Junction-to-board thermal resistance parameter of LMK60EX (48.7°C/W without airflow)
- P: On-chip power dissipation of LMK60EX

To ensure that the maximum junction temperature of LMK60EX is below 105°C, it can be calculated that the maximum PCB temperature without airflow should be at 87°C or below when the device is optimized for best performance resulting in maximum on-chip power dissipation of 0.36 W.

9.1.2 Best Practices for Signal Integrity

For best electrical performance and signal integrity of entire system with LMK60EX, TI recommends routing vias into decoupling capacitors and then into the LMK60EX. TI also recommends increasing the via count and width of the traces wherever possible. These steps ensure lowest impedance and shortest path for high frequency current flow. Figure 9 shows the layout recommendation for LMK60EX.

Layout Guidelines (continued)

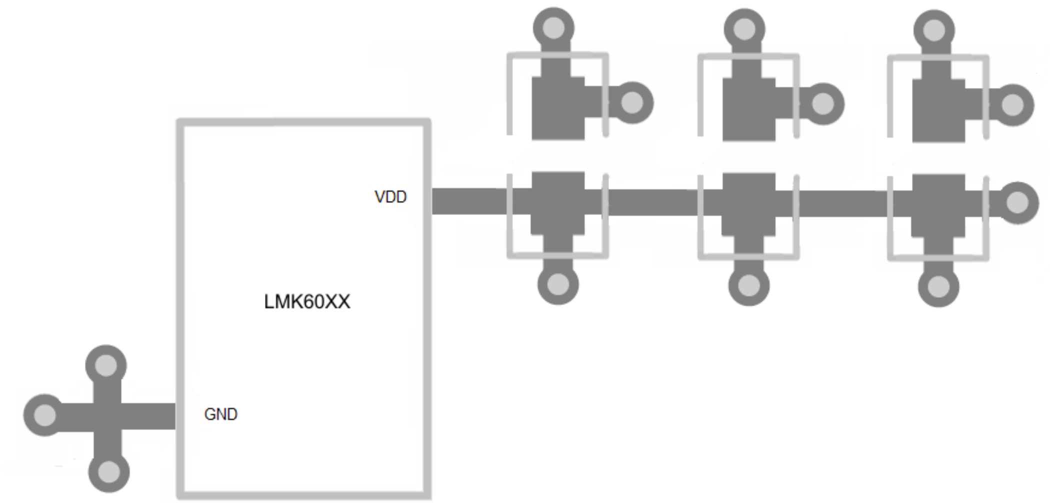


Figure 9. LMK60EX Layout Recommendation for Power Supply and Ground

9.1.3 Recommended Solder Reflow Profile

TI recommends following the recommendations of the solder paste supplier to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. Processing the LMK60EX to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label is preferred. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well as the recommended soldering profile from the manufacturer and capability of the reflow equipment to as confirmed by the SMT assembly operation.

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

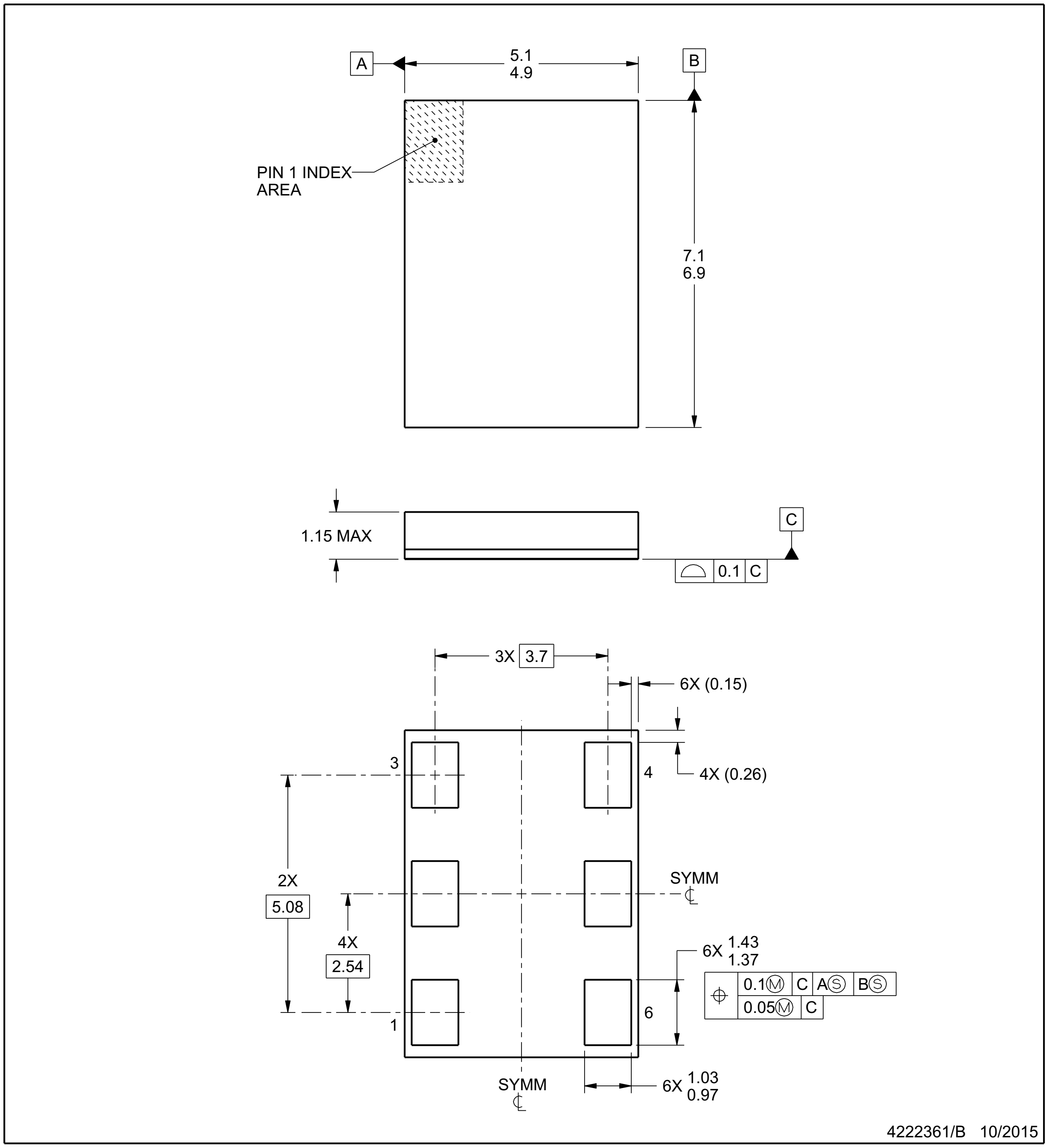
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

SIA0006A

QFM - 1.15 mm max height

QUAD FLAT MODULE



NOTES:

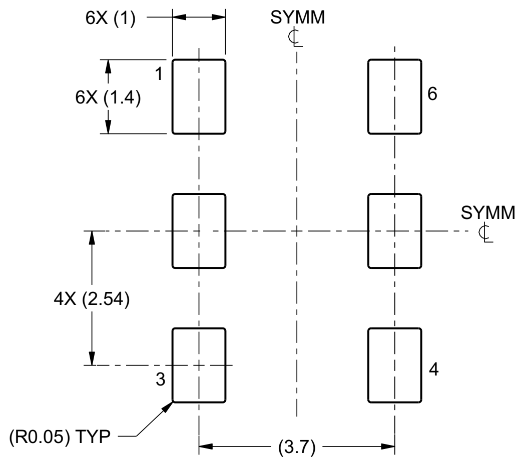
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

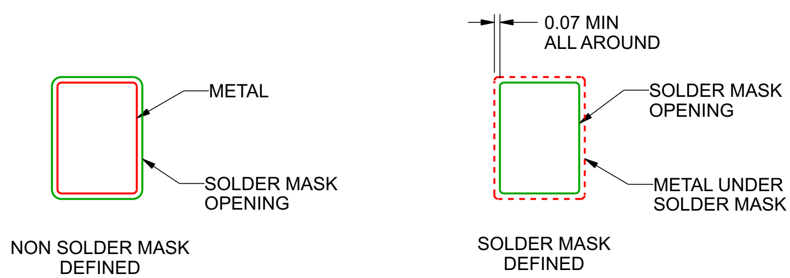
SIA0006A

QFM - 1.15 mm max height

QUAD FLAT MODULE



LAND PATTERN EXAMPLE
1:1 RATIO WITH PACKAGE SOLDER PADS
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

4222361/B 10/2015

NOTES: (continued)

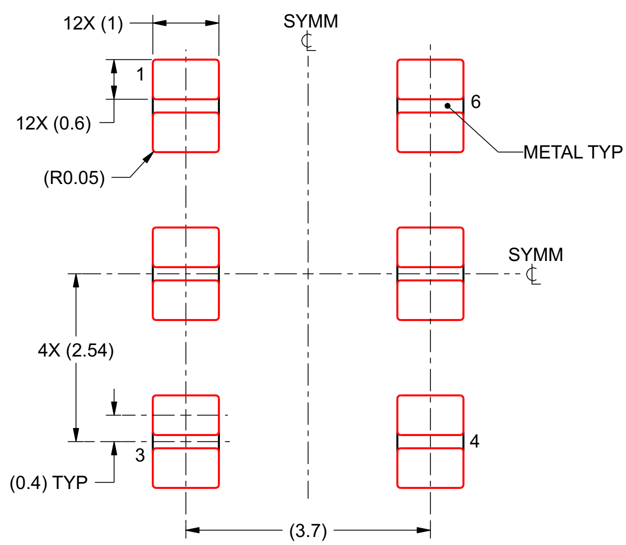
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIA0006A

QFM - 1.15 mm max height

QUAD FLAT MODULE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
ALL PADS: 86%
SCALE:10X

4222361/B 10/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK60E0-156M25SIAR	ACTIVE	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 156M25	Samples
LMK60E0-156M25SIAT	ACTIVE	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 156M25	Samples
LMK60E0-212M50SIAR	ACTIVE	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 212M50	Samples
LMK60E0-212M50SIAT	ACTIVE	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 212M50	Samples
LMK60E2-100M00SIAR	ACTIVE	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 100M00	Samples
LMK60E2-100M00SIAT	ACTIVE	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 100M00	Samples
LMK60E2-125M00SIAR	ACTIVE	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 125M00	Samples
LMK60E2-125M00SIAT	ACTIVE	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 125M00	Samples
LMK60E2-156M25SIAR	ACTIVE	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 156M25	Samples
LMK60E2-156M25SIAT	ACTIVE	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 156M25	Samples
LMK60I2-100M00SIAR	ACTIVE	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60I2 100M00	Samples
LMK60I2-100M00SIAT	ACTIVE	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60I2 100M00	Samples
LMK60I2-322M26SIAR	ACTIVE	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60I2 322M26	Samples
LMK60I2-322M26SIAT	ACTIVE	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60I2 322M26	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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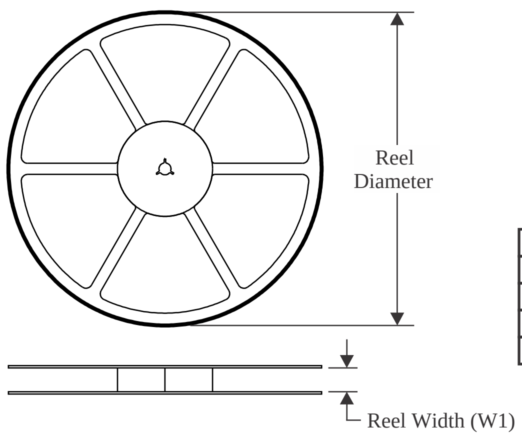
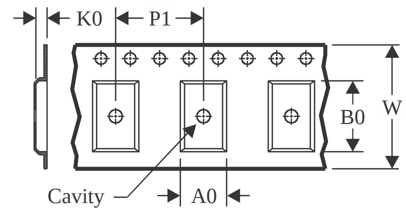
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

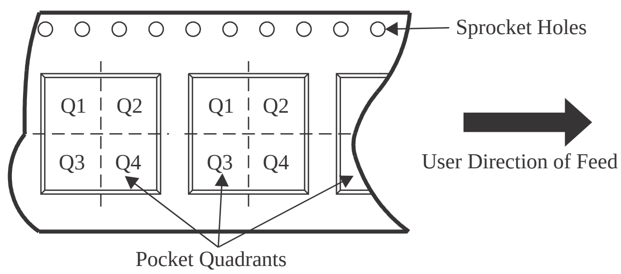


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

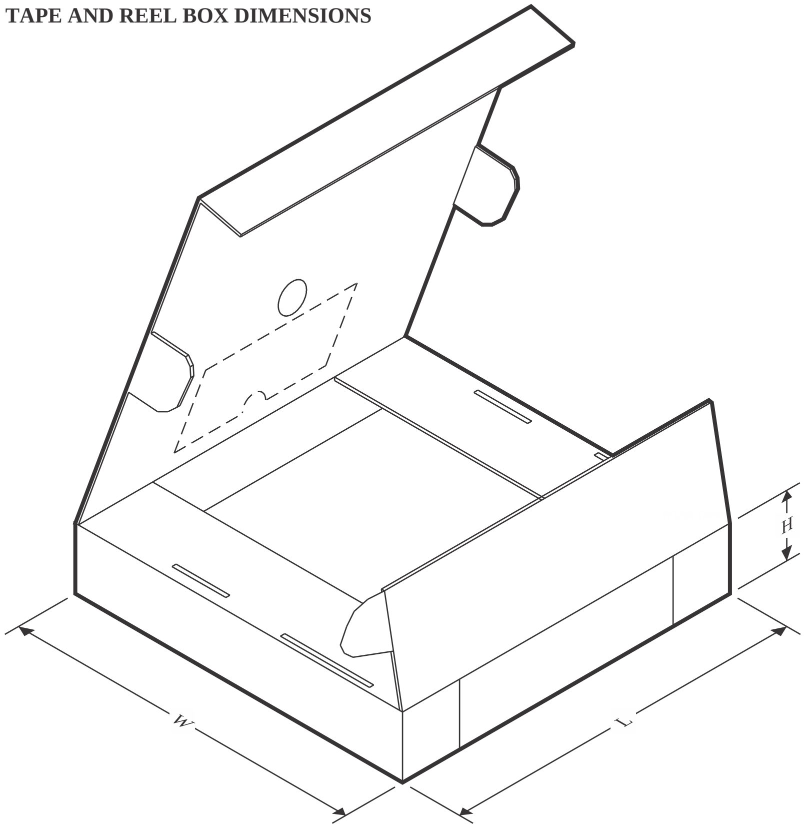
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK60E0-156M25SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E0-156M25SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E0-212M50SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E0-212M50SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-100M00SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-100M00SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-125M00SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-125M00SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-156M25SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-156M25SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60I2-100M00SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60I2-100M00SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60I2-322M26SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60I2-322M26SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK60E0-156M25SIAR	QFM	SIA	6	2500	356.0	356.0	35.0
LMK60E0-156M25SIAT	QFM	SIA	6	250	213.0	191.0	55.0
LMK60E0-212M50SIAR	QFM	SIA	6	2500	356.0	356.0	35.0
LMK60E0-212M50SIAT	QFM	SIA	6	250	208.0	191.0	35.0
LMK60E2-100M00SIAR	QFM	SIA	6	2500	356.0	356.0	35.0
LMK60E2-100M00SIAT	QFM	SIA	6	250	208.0	191.0	35.0
LMK60E2-125M00SIAR	QFM	SIA	6	2500	356.0	356.0	35.0
LMK60E2-125M00SIAT	QFM	SIA	6	250	208.0	191.0	35.0
LMK60E2-156M25SIAR	QFM	SIA	6	2500	356.0	356.0	35.0
LMK60E2-156M25SIAT	QFM	SIA	6	250	208.0	191.0	35.0
LMK60I2-100M00SIAR	QFM	SIA	6	2500	356.0	356.0	35.0
LMK60I2-100M00SIAT	QFM	SIA	6	250	208.0	191.0	35.0
LMK60I2-322M26SIAR	QFM	SIA	6	2500	356.0	356.0	35.0
LMK60I2-322M26SIAT	QFM	SIA	6	250	208.0	191.0	35.0