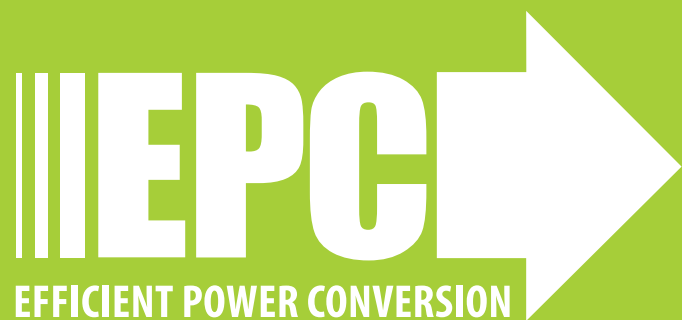


Development Board EPC9004C Quick Start Guide

200 V Half-Bridge with Gate Drive, Using EPC2012C

Rev 3.0



DESCRIPTION

The EPC9004C development board is a 200 V maximum device voltage, 2 A maximum output current, half bridge with onboard gate drives, featuring the EPC2012C enhancement mode (eGaN®) field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2012C eGaN FET by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9004C development board is 2" x 1.5" and has two EPC2012C eGaN FETs in a half bridge configuration using Texas Instruments UCC27611 gate driver with supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in figure 1.

For more information on the EPC2012C eGaN FET please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

QUICK START PROCEDURE

Development board EPC9004C is easy to set up to evaluate the performance of the EPC2012C eGaN FET. Refer to figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to +V_{IN} (J5, J6) and ground / return to -V_{IN} (J7, J8).
2. With power off, connect the switch node (SW) of the half bridge V_{OUT} (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to +V_{DD} (J1, Pin-1) and ground return to -V_{DD} (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the controller / PWM input source .
7. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 200 V on V_{OUT}).
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node, care must be taken to avoid long ground leads. Measure the switch node by using a probe jig with the oscilloscope probe tip. Refer to figure 3 and the section "Measurement Considerations".

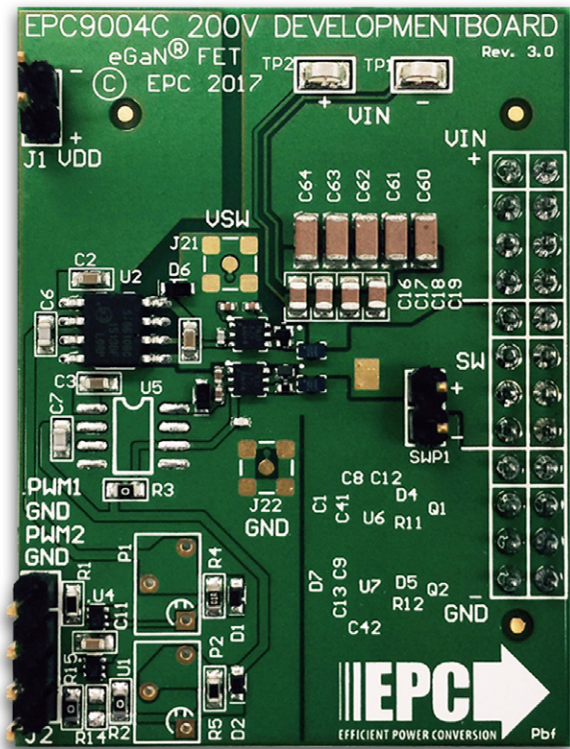
For more information about measurement techniques, please review the how to GaN series: HTG09- Measurement

<http://epc-co.com/epc/DesignSupport/TrainingVideos/HowtoGaN/>

Table 1: Performance Summary (T_A = 25°C) EPC9004C

Symbol	Parameter	Conditions	Min	Max	Units
V _{DD}	Gate Drive Input Supply Range		7	12	V
V _{IN}	Bus Input Voltage Range			160	V
V _{OUT}	Switch Node Output Voltage			200	V
I _{OUT}	Switch Node Output Current			2*	A
V _{PWM}	PWM Logic Input Voltage Threshold	Input 'High' Input 'Low'	3.5 0	6 1.5	V V
	Minimum 'High' State Input Pulse Width	V _{PWM} rise and fall time < 10ns	100		ns
	Minimum 'Low' State Input Pulse Width	V _{PWM} rise and fall time < 10ns	500#		ns

* Assumes inductive load, maximum current depends on die temperature – actual maximum current will be subject to switching frequency, bus voltage and thermals.
Dependent on time needed to 'refresh' high side bootstrap supply voltage.



EPC9004C development board

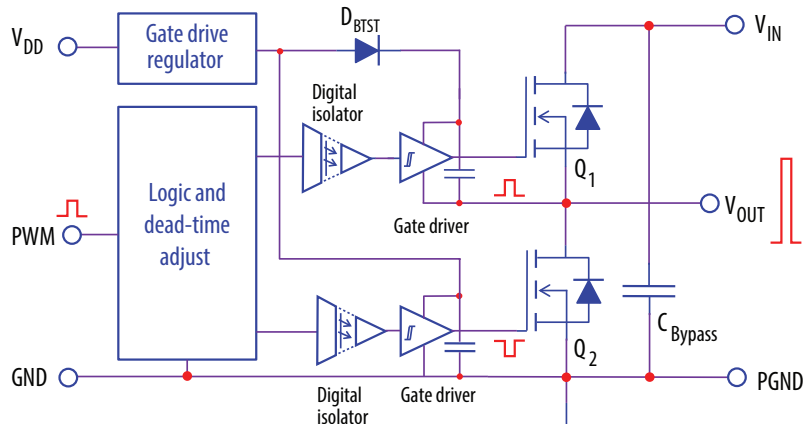


Figure 1: Block diagram of EPC9004C development board.

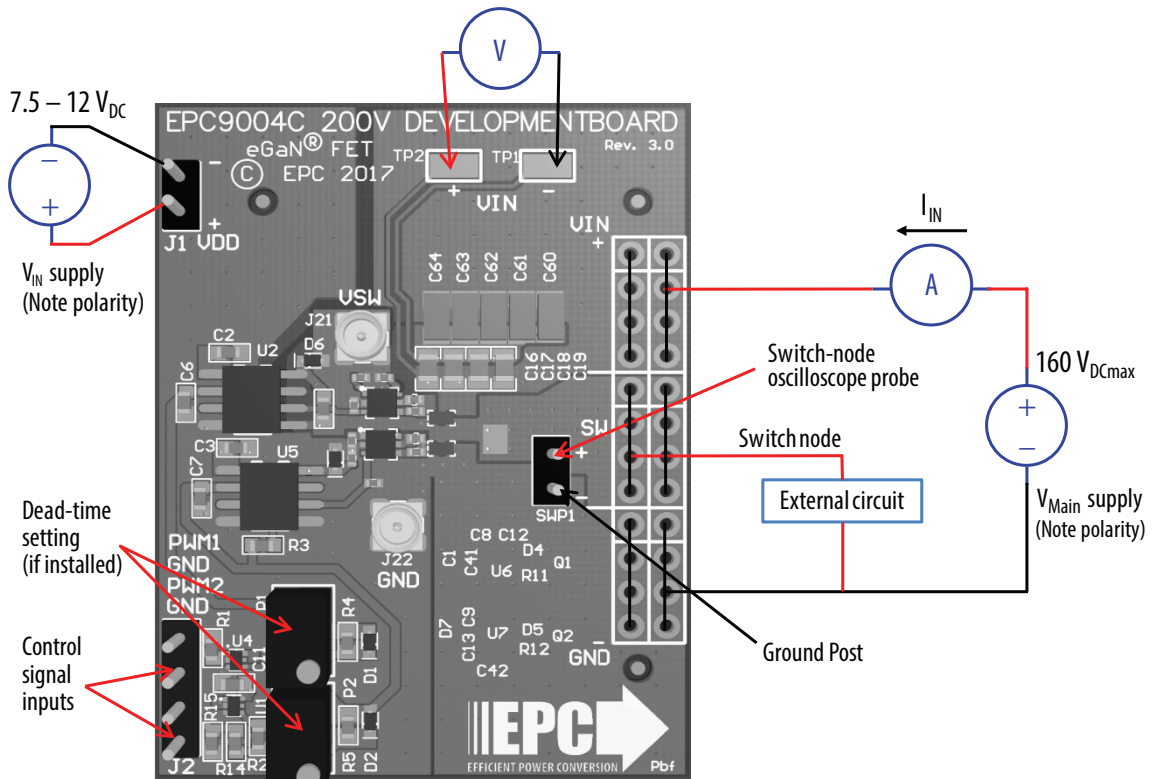


Figure 2: Proper connection and measurement setup.

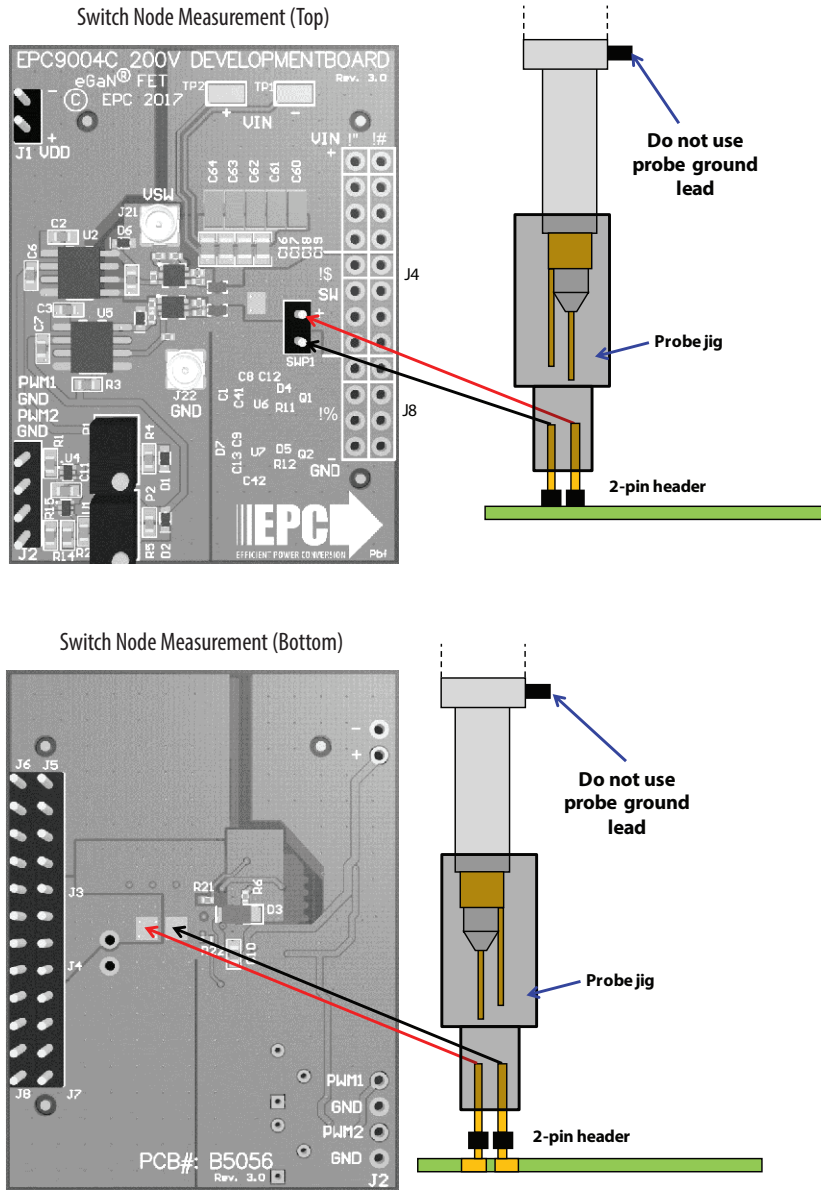


Figure 3: Switch Node Measurement.

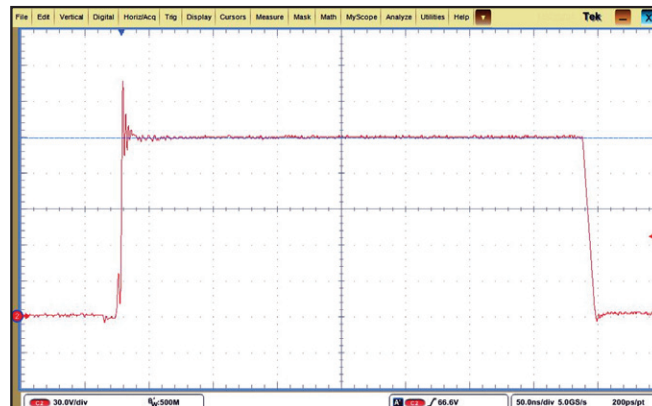


Figure 4: Typical waveform for $V_{IN} = 150V$ to $5V/2A$ (100 kHz) buck converter.

MEASUREMENT CONSIDERATIONS

The EPC9004C development board has been provided with specially designed high frequency (up to 1 GHz minimum) capable measurement connections using MMCX connectors located at J22 & J21 with direct access to the gate signals of both the upper and lower FETs. These nodes can be measured directly using the Tektronix IsoVu probe shown in figure 5. Figure 6 shows typical gate waveforms measured using the IsoVu probe.



Figure 5: Tektronix IsoVu measurement setup.

This native connection between the high and low side gate-source nodes to an IsoVu probe tip cable has less than 2 pF common mode loading and completely eliminates ground loops due to its galvanic isolation. These MMCX connectors offer a shielded coaxial environment to the test point which minimizes noise pickup.

Please contact EPC for special instructions on using these connections. To prevent an unterminated transmission line hanging on the gate it is recommended to remove resistors R21 & R22 when not using this feature. The maximum impedance loading of these nodes is 2.5 kΩ.

Tektronix is a leading manufacturer of power test solutions for design validation, characterization, and performance testing. EPC partnered with Tektronix to define the requirements for accurate measurements on GaN devices which led to the development of the Tektronix IsoVu measurement system. IsoVu is a galvanically isolated differential measurement system with 1 GHz bandwidth, 1 Million to 1 (120 dB) common mode rejection ratio, 50 V differential, and 2000 V common mode voltage range. Previously impossible differential measurements such as the high-side V_{GS} are now possible because of IsoVu's high common mode rejection across bandwidth.

IsoVu allows you to:

- Characterize the time alignment of high side and low side events
- Optimize and tune switching characteristics such as edge rates, overshoot, ringing and dead time
- See the interactions due to parasitic coupling between the high and low side transistors
- Make isolated high frequency current measurements using low impedance sense resistors
- Improve reliability through accurate characterization across all operating conditions

EPC would like to acknowledge Tektronix (<http://www.tek.com/isolated-measurement-systems>) for their support of this project.

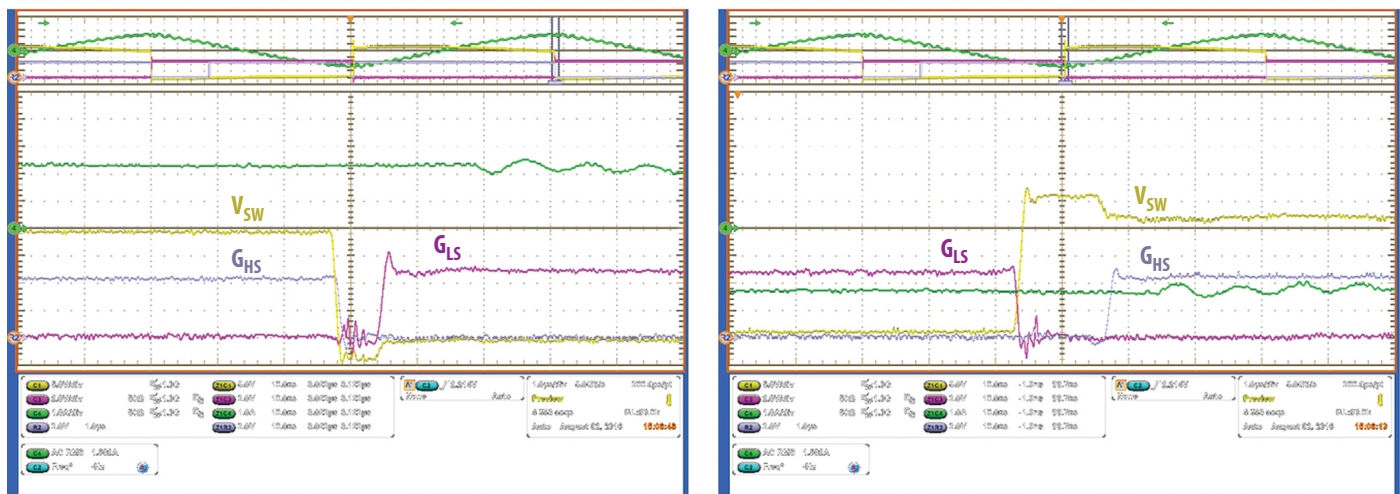


Figure 6: Upper gate and lower gate measurements using the Tektronix IsoVu and switch-node voltage measurement using the TPP1000 probe.

THERMAL CONSIDERATIONS

The EPC9004C development board showcases the EPC2012C eGaN FET. Although the electrical performance surpasses that for traditional Si devices, their relatively smaller size does magnify the thermal management requirements. The EPC9004C is intended for bench evaluation with low ambi-ent temperature and convection cooling.

The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 150°C.

NOTE. The EPC9004C development board does not have any current or thermal protection on board.

Table 2: Bill of Materials

Item	Qty	Reference	Part Description	Manufacturer	Component
1	5	C1, C2, C3, C10, C11	Capacitor, 1µF, 10%, 25 V, X5R	Murata	GRM188R61E105KA12D
2	2	C6, C7	Capacitor, 100 pF, 5%, 50 V, NP0	TDK	C1608C0G1H101J080AA
3	4	C8, C9, C12, C13	Capacitor, 0.22 µF, 10%, 16 V, X7R	TDK	C1005X7R1C224K050BC
4	4	C16, C17, C18, C19	Capacitor, 0.1 µF, 10%, 250 V, X7T	TDK	C2012X7T2E104K125AE
5	1	C41	Capacitor, 10 pF, 5%, 50 V, NP0	KEMET	C0402C100J5GACTU
6	1	C42	Capacitor, 100 pF, 5%, 50 V, NP0	TDK	C1005C0G1H101J050BA
7	5	C60, C61, C62, C63, C64	Capacitor, 0.22 µF, 10%, 250 V, X7T	TDK	C3216X7T2E224K160AA
8	2	D1, D2	Schottky Diode, 30 V	Diodes Inc.	SDM03U40-7
9	1	D3	Diode, 200 V, 1 A	Diodes Inc.	DFLS1200-7
10	2	D4, D5	Schottky Diode, 40 V, 200 mA	Diodes Inc.	BAS40LP-7
11	2	J1, SWP1	.1" Male Vert. 2 pos	Würth	61300211121
12	1	J2	.1" Male Vert. 4 pos	Tyco	4-103185-0-04
13	6	J3, J4, J5, J6, J7, J8	.1" Male Vert. 4 pos	FCI	68602-224HLF
14	2	Q1, Q2	200 V 100 mΩ eGaN FET	EPC	EPC2012C
15	1	R1	Resistor, 10.0 K, 5%, 1/8 W	Stackpole	RMCF0603FT10K0
16	3	R2, R3, R15	Resistor, 0 Ω, 1/8 W, 0603	Panasonic	ERJ-3GEY0R00V
17	1	R4	Resistor, 240 Ω, 0.1 W, 0603	Stackpole	RMCF0603JT240R
18	1	R5	Resistor, 200 Ω, 0.1 W, 0603	Stackpole	RMCF0603JT200R
19	1	R6	Resistor, 0 Ω, 1/10 W, 0402	Panasonic	ERJ-2GE0R00X
20	2	R11, R12	Resistor, 1 Ω, 1/16 W, 0402	Stackpole	RMCF0402FT1R00
21	2	TP1, TP2	Test Point, SMT	Keystone Electronics	Keystone Elect, 5015
22	1	U1	IC GATE NAND 1CH 2-INP 6MICROPAK	Fairchild	NC7SZ00L6X
23	1	U2	DGTL ISO 3.75KV GEN PURP 8SOIC	Silicon Labs	SI8610BC-B-IS
24	1	U4	IC GATE AND 1CH 2-INP 6-MICROPAK	Fairchild	NC7SZ08L6X
25	2	U6, U7	IC GATE DRVR 6SON UCC27611	Texas Instruments	UCC27611

Optional Components

Item	Qty	Reference	Part Description	Manufacturer	Component
1	1	R14	Resistor, 0 Ω, 1/8 W, 0603	Panasonic	ERJ-3GEY0R00V
2	2	D6, D7	5.1 V, Zener Diode, 0603	Comchip Technology	CZRU52C5V1
3	2	J21, J22	MMCX JACK, 50 Ω, SMD	Molex	0734152063
4	2	P1, P2	TRIMMER, 1 K Ω, 0.25 W	Bourns Inc.	PV37W102C01B00
5	2	R21, R22	Resistor, 0 Ω, 1/16 W, 0402	Stackpole	RMCF0402ZTOR00
6	1	U5	DGTL ISO 3.75 KV GEN PURP 8SOIC	Silicon Labs	SI8610BC-B-IS

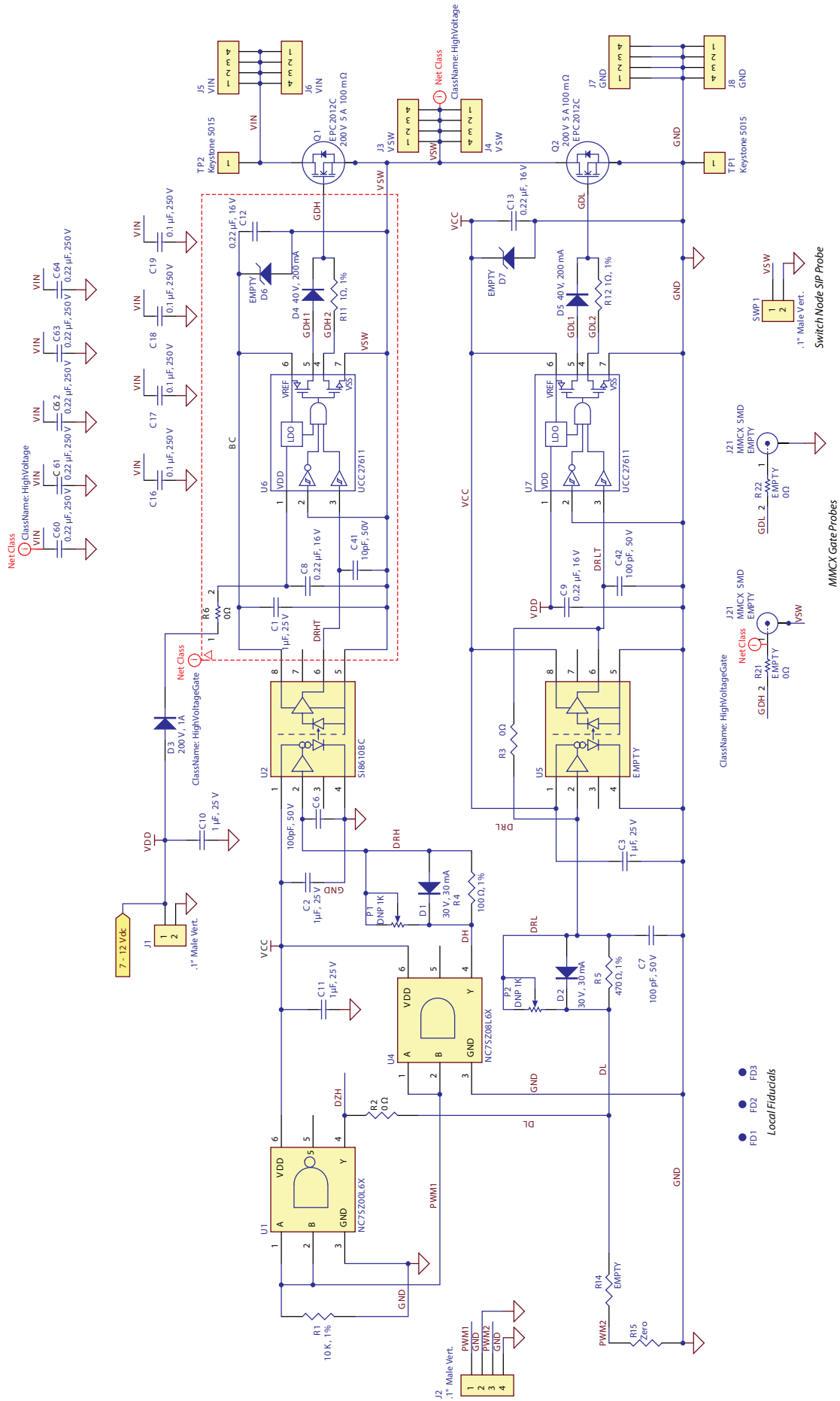


Figure 7: EPC9004C - Schematic
200V Half-Bridge with Gate Drive, using EPC2012C Rev 3.0

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The EPC9004C board is intended for product evaluation purposes only and is not intended for commercial use. Replace components on the Evaluation Board only with those parts shown on the parts list (or Bill of Materials) in the Quick Start Guide. Contact an authorized EPC representative with any questions.

This board is intended to be used by certified professionals, in a lab environment, following proper safety procedures. Use at your own risk.

As an evaluation tool, this board is not designed for compliance with the European Union directive on electromagnetic compatibility or any other such directives or regulations. As board builds are at times subject to product availability, it is possible that boards may contain components or assembly materials that are not RoHS compliant. Efficient Power Conversion Corporation (EPC) makes no guarantee that the purchased board is 100% RoHS compliant.

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