Electrical Performance Advantages of Ultra-Thin Dielectric Materials Used for Power-Ground Cores in High Speed, Multilayer Printed Circuit Boards

Joel Peiffer
3M Company
St. Paul, MN

Bob Greenlee
Merix Corporation
Forest Grove, OR

Istvan Novak
Sun Microsystems
Burlington, MA

Introduction

Thin layers (50 um) of FR-4 material have been used for power-ground cores for a number of years to improve electrical performance. These thin power-ground cores serve as distributed capacitor layers to assist in power supply decoupling. However, with the ever-increasing speeds of circuits and the trend to lower voltages and higher switching speeds, these thin layers no longer provide the required electrical properties (low impedance, high capacitance) necessary for next generation, high speed digital circuits. New ultra-thin (<25 um) dielectric materials loaded with high dielectric constant materials have been developed to meet the low target impedance values and high capacitance necessary for effective power supply decoupling for these next generation products.

Sun Microsystems designed a multilayer printed circuit board that was used to measure self and transfer-impedance values over a wide frequency range. Test boards were fabricated and electrically tested with a dielectric thickness in the range of 8 um to 50 um between power and ground planes. The results of this testing indicate that ultra-thin dielectric materials have a very low impedance over a wide frequency range, much lower than existing commercial materials. Additionally, these ultra-thin materials tend to be lossy at high frequencies, which effectively dampens noise on the power plane. When these ultra-thin materials are used for power-ground cores, they are capable of effective power supply decoupling, well beyond the frequency range of existing commercial materials.

In addition, the fabricator of the test vehicles will discuss the changes in processing, material handling and electrical test required to successfully manufacture these and other multiplayer boards utilizing ultra-thin dielectrics in a high volume production setting.

Ultra-Thin Materials

As the frequency increases in high speed, digital designs, thinner and thinner dielectrics in power-ground cores will be necessary to supply the needed low impedance to have the system run at optimal electrical performance. The thin dielectric materials currently used (50 um) will no longer be able to perform the power supply decoupling function to the degree needed. Many thinner laminate materials are being investigated for use in next-generation products. One such novel ultra-thin laminate material is 3M C-Ply. It's material and electrical properties are shown in table 1. It has a dielectric thickness well under 25 microns, even as thin as 8 microns. The dielectric material is epoxy-based and is loaded with barium titanate particles to increase the dielectric constant. The dielectric is sandwiched between two, one-ounce (35 um) copper layers. The laminate material was designed to be compatible with existing printed circuit board processing.

Table 1 - Material and Electrical Properties

Dielectric Material: Ceramic filled epoxy (bromine free)
Dielectric Thickness: 0.30 – 1.00 mils (8 – 25 microns)
Copper Thickness: 1.4 mils (35 microns)

Capacitance/Unit Area: 4 – 10 nF/in^2 at 1 kHz (10 nF/in^2 for 8 um)
Capacitance Uniformity: +/- 10%
Dissipation Factor: .005 (1 kHz)
Frequency: Tested to 18 GHz, no issues seen

Operating Temperature: -40 – 130°C ("X7R" behavior over this range)
UL Flammability Rating: 94V-0
UL Relative Thermal Index (RTI): 130°C

Fabrication of Ultra-Thin Dielectric Boards

A test vehicle board was designed so that different thickness power-ground dielectric materials could be compared to each other. Merix fabricated this test board with four different capacitor materials: 2 mil ZBC from MEM, and ~8 µm, ~12.5µm, and ~25 µm C-Ply from 3M. The process flow for building the C-Ply boards was greatly simplified from earlier test board builds, and was therefore quite successful. The first part of this paper describes the processes used to build the C-Ply test boards, and presents some lessons learned from working with this material.

Background:

The initial approach to building C-Ply test boards for the NIST Advanced Embedded Passives Technology (AEPT) consortium was not very elegant, and involved several non-standard processes. The registration of these first boards was not particularly good. A significant amount of particles were generated when the panels were etched in the develop-etch-strip (DES) line due to dielectric break out. We discovered that for the most part our standard subpart processes worked with this material and gave improved registration.

Due to the extremely thin and flexible nature of the C-Ply core material, it was not practical to etch copper from both sides of it at the same time. Therefore we used a subpart process, so that only one side of the material was etched at a time.

C-Ply Subpart Processing Steps:

Figure 1 shows one of the Sun test board C-Ply layers after etching the first side. The opposite side of the layer is solid copper. After the first side is laminated into a subpart, the opposite side can be etched without risk of damaging the thin dielectric. Since only one side is etched at a time, there is no risk of introducing debris into the DES line.

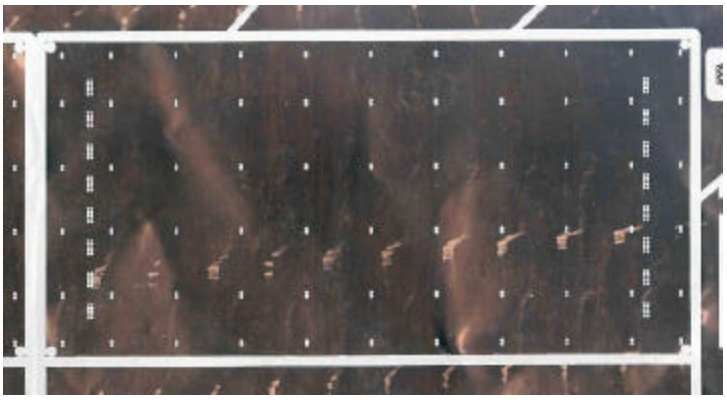

Figure 1. Etched C-Ply layer for Sun test board.

Most of the innerlayer processing steps are standard:

1. photo resist lamination;
2. printing and etching an image on one side;
3. high-pot test;
4. post-etch-punch;
5. oxide;
6. pressing subpart layers together;
7. tooling hole drill;
8. deburr;
9. photo resist lamination;
10. printing outside of subpart layers on autoprinter;
11. develop, etch, and strip;
12. lamination of the C-Ply subpart into the parent part.

Fabricating the C-Ply subparts in this standard fashion resulted in fewer and simpler processing steps. Some of our newer equipment with thin core capability also helped make the process more robust. For example, our horizontal conveyorized alternative oxide line processed the thin core C-Ply well without the need for any frames or leaders. Our new autolaminators with thin core capability eliminated the need for the adjustments we had previously made to prevent wrinkling in the photoresist.

Registration was challenging, since the unreinforced C-Ply material tended to move with the material adjacent to it. However, once the scaling values for each layer have been determined, they appeared to be stable for subsequent builds.

Sun Test Vehicle

The Sun test vehicle is a relatively simple design, with ground planes on the capacitance layers, parallel impedance traces on the signal layers, and laser microvias between layers 1 and 3. Figure 2 is a cross section showing two 8 µm C-Ply cores separated by an FR406 core.

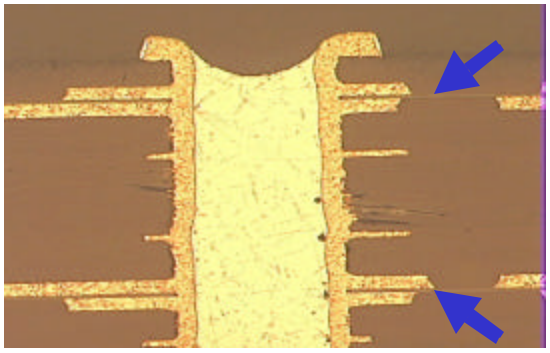

Figure 2. Two C-Ply cores separated by an FR406 core (arrows show location of the thin C-Ply dielectric).

The Sun test board consists of twenty layers with four cores of thin core capacitor material (ZBC or C-Ply) and one core of 2 mil ZBC in the center. For the C-Ply versions of the boards, layers 2/3, 6/7, 14/15, and 18/19 were all C-Ply, and the middle layer 10/11 was 2 mil ZBC. The other layers consisted of FR406 material. Figures 3-6 show the stack-ups for each of these boards, with thickness measurements in mils.

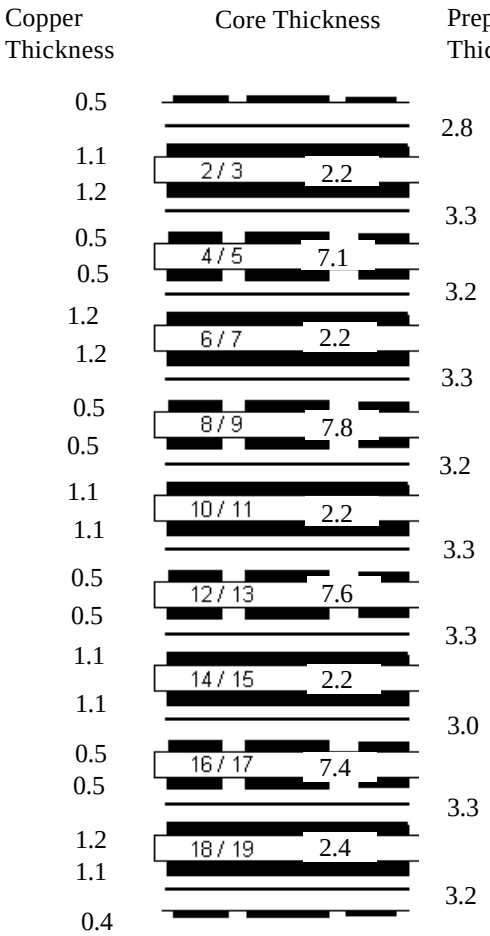

Figure 3. Stackup and measurements for 2 mil ZBC version of Sun test board (measurements in mils). ZBC comprises layers 2/3, 6/7, 10/11, 14/15, and 18/19. Other layers are FR406 material. (Part number 811-9098-00, lot 0212A.)

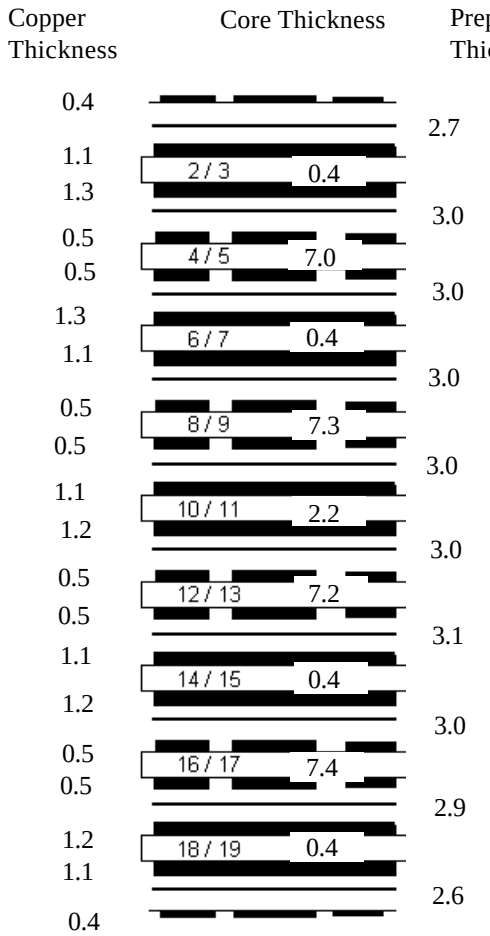

Figure 4. Stackup and measurements for ~8 um C-Ply version of Sun test board (measurements in mils). C-Ply comprises layers 2/3, 6/7, 14/15, and 18/19. ZBC comprises layers 10/11. Other layers are FR406 material. (Part number 811-9099-00, lot 0213A.)

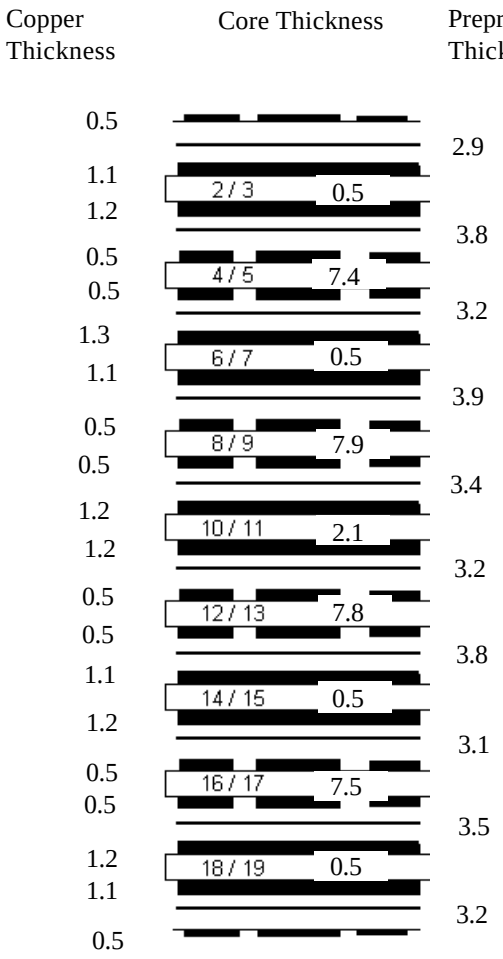

Figure 5. Stackup and measurements for ~12.5 um C-Ply version of Sun test board (measurements in mils). C-Ply comprises layers 2/3, 6/7, 14/15, and 18/19. ZBC comprises layers 10/11. Other layers are FR406 material. (Part number 811-9099-00, lot 0218A.)

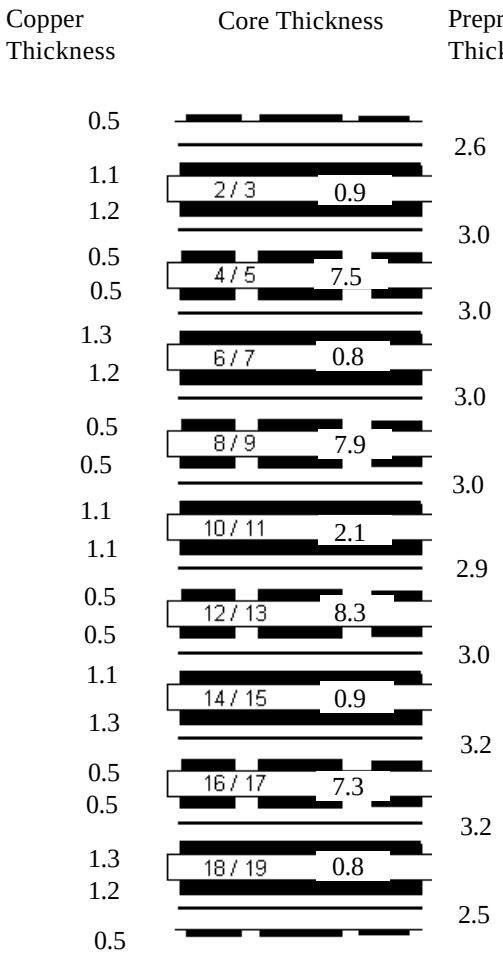

Figure 6. Stackup and measurements for ~25 um C-Ply version of Sun test board (measurements in mils). C-Ply comprises layers 2/3, 6/7, 14/15, and 18/19. ZBC comprises layers 10/11. Other layers are FR406 material. (Part number 811-9099-00, lot 0220A.)

Laser Microvias

The Sun test board had laser microvias between layers 1 and 3, and there was some initial concern that the laser would ablate the C-Ply material too rapidly. Therefore a microvia test board was designed with microvia coupons in the center and each corner, with laser drill sizes of 4, 6, 8, and 10 mils. Two test boards were built using the ~8 µm C-Ply material. Figure 7 shows cross-sections of two of the 10-mil microvias. All drill sizes showed adequate plating, even at the higher aspect ratios.

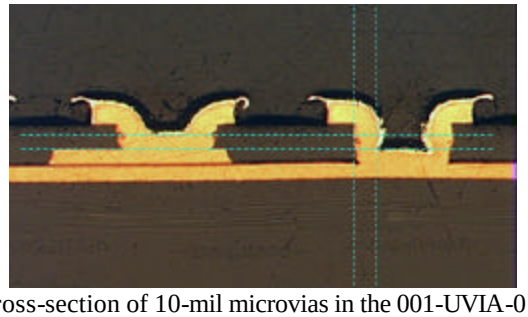

Figure 7. Cross-section of 10-mil microvias in the 001-UVIA-01 test board.

Electrical Test
Figure 8 shows the resistance measured across an ~8 µm C-Ply layer using a hand-held Fluke 89 IV logging multimeter. The resistance increases at about 1.6 Megohm/sec until the meter goes over its measurement limit of about 30 Megohm.

The same phenomenon can be seen when the boards are electrically tested, and may need to be compensated for, although the charging time is much shorter since the electrical test voltage is much higher.

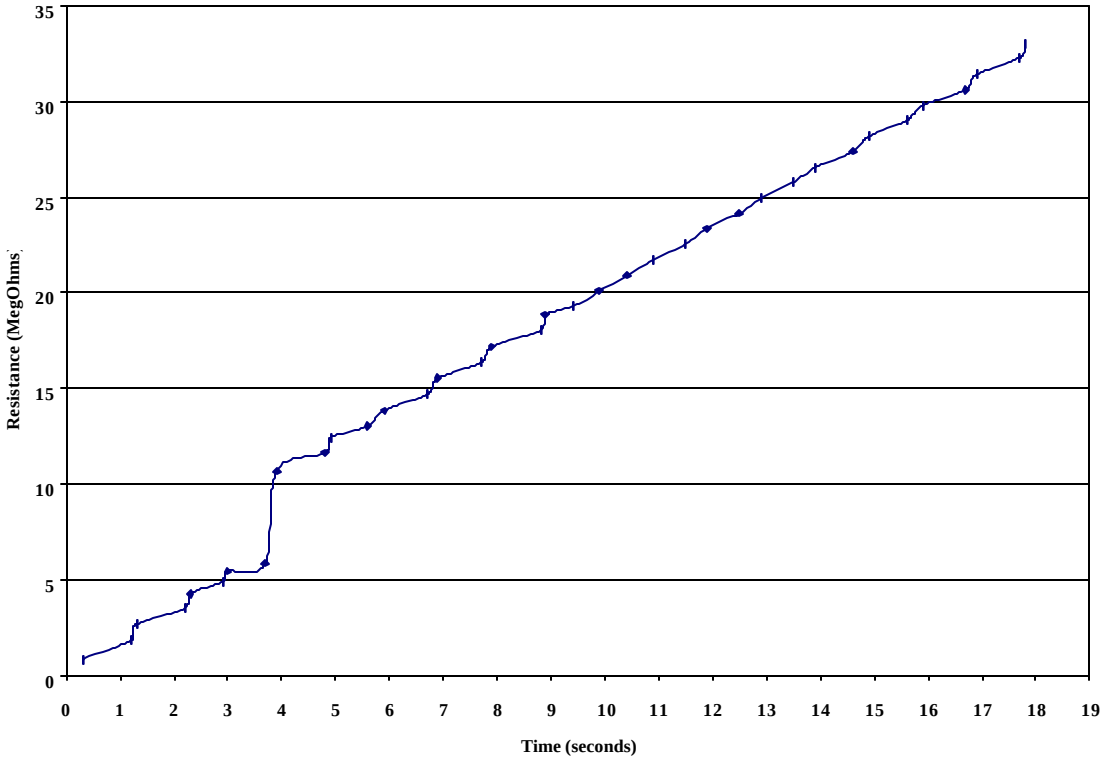

Figure 8. Resistance across a C-Ply layer measured as a function of time. (The step change in resistance at 4 seconds appears to be an anomaly associated with the multimeter).

The simplified subpart lamination process outlined here appears to make fabrication with C-Ply capacitor material viable for production parts. Having equipment that is capable of handling thin cores has made working with this material almost routine.

Test points and instrumentation for impedance measurements
There are two one-inch grids on the main area of the boards, one grid determines the locations of possible capacitors to mount to, the other grid identifies the test points. There are six rows and eleven columns of test points, giving a total of 66 test connection possibilities. The two grids are offset by half an inches. The planes are unsplit, with a 50-mil pullback at the edges: the total area was 9.9”x4.9”.

To connect the measurement probes , as shown below, a set of plated through holes are located on one set of the grid points. The bigger pads are surface pads only, no through hole was attached. The smaller-size pads are connected to 22-mil finished through holes with 50-mil center-to-center spacing, and are sized to take 0.082” semirigid probes (shown later).

The self and transfer impedances were measured with the two-port measurement method [1] with a Hewlett Packard HP4396A Vector Network Analyzer and the Hewlett-Packard 85046 S-Parameter Test Kit. The frequency range was 0.1MHz to 1.8GHz, the output power at the RF OUT connector was set to 0dBm. RF bandwidth was usually set to 100Hz, in cases when the impedance dropped to low values and the thermal noise began to show up on the measured trace, the bandwidth was further reduced to 10Hz. The test points were connected to the VNA inputs through two pieces of 24-inch long Tensolite 0.082” E-Z coax cables with semirigid coax probes. To suppress cable-shield resonances, each cable was covered with FerrShield 28B0250-1 absorbing ferrite sleeves. For self-impedance measurements, the two probes were connected to the same vias from opposite sides.

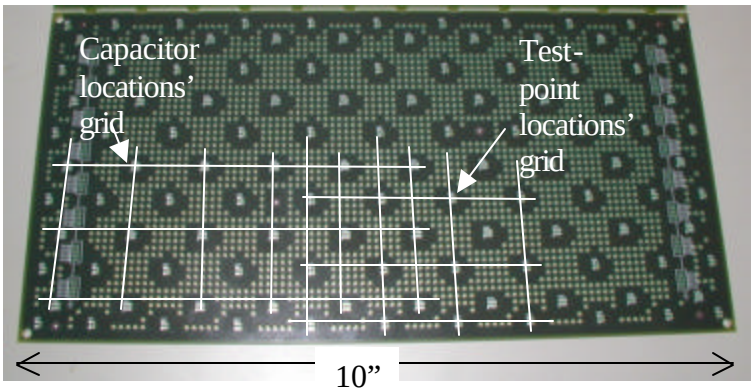

Figure 9. Main area of the test board. The outline dimensions were 10”x5”. There are two 1” grids on the board, with 0.5” offset. One grid has surface connections for capacitors, the other grid has pairs of through holes connecting to the thin laminate. The thin laminate is nominally 3 mils below the surface.

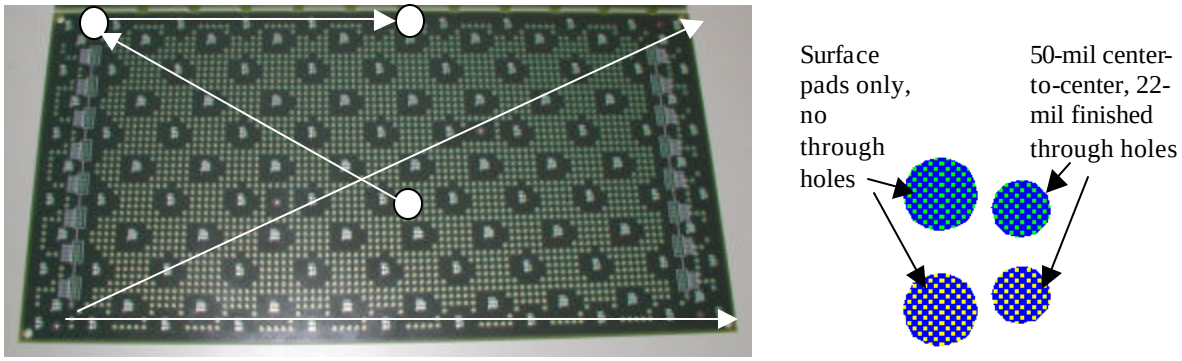

Figure 10. Identification of the measurement points is on the left: self impedances are identified by large dots and are shown later at the corner, in the center and at the mid-side. Transfer impedances are shown by arrows and are given from center to corner, from corner to mid side, along the longer side and along the diagonal. The test-via connection top view is shown on the right. The same test vias are located at every grid points of the one-inch grid.

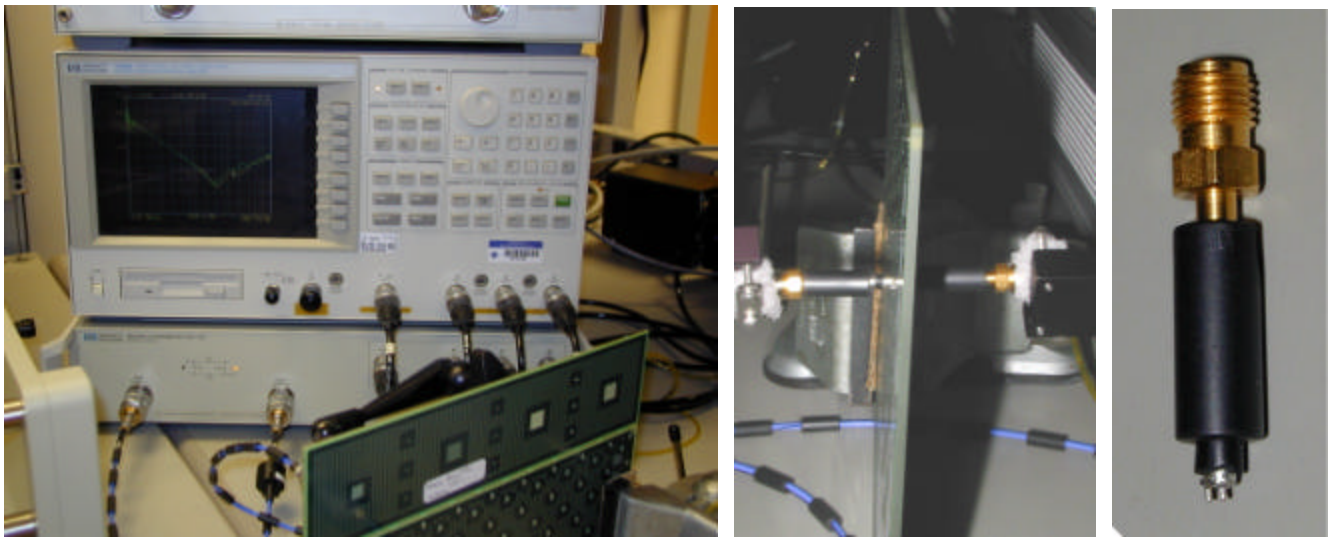

Figure 11. Instrumentation and cabling: full setup shown on the left, two-sided probe connection is shown in the middle, the close-up picture of a semirigid probe is on the right.

Self-impedance comparison at the center

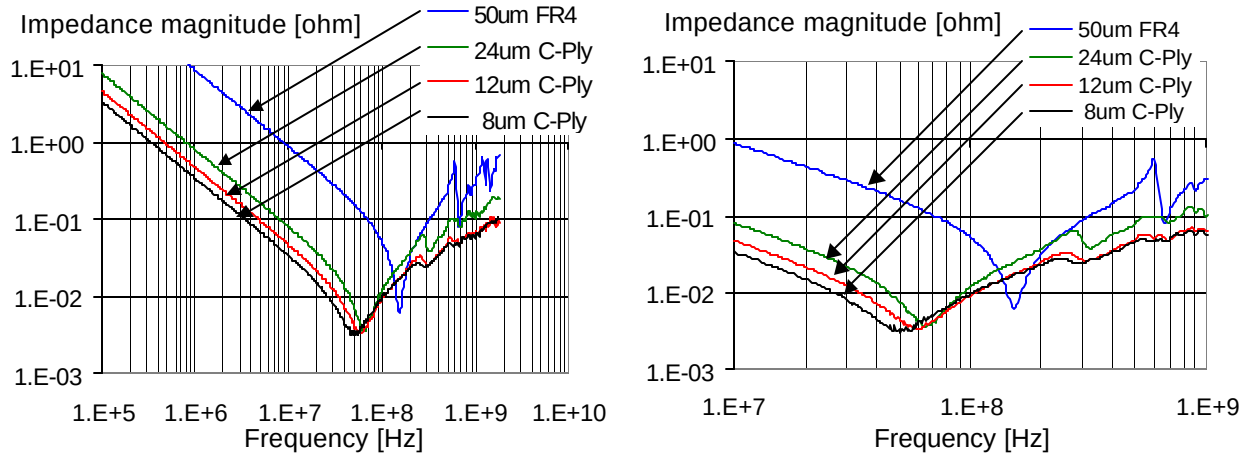

Figure 12. Full-range and zoomed self-impedance magnitude comparison of four laminates.

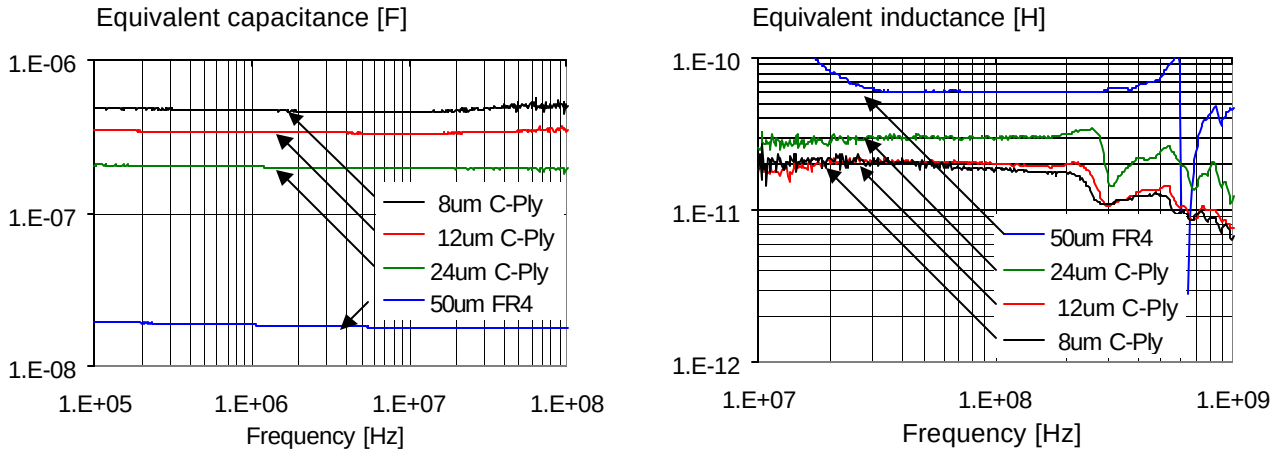

Figure 13. Comparison of extracted equivalent capacitances and inductances of the four laminates.

The extracted capacitance and inductance parameters, based on the procedure described in [2], are given in the table below.

	Capacitance [F]	Inductance [H]
8um C-Ply	4.55E-7	1.80E-11
12um C-Ply	3.30E-7	1.95E-11
24um C-Ply	1.94E-7	3.00E-11
50um FR4	1.78E-8	6.00E-11

Self-impedance comparison at mid-side

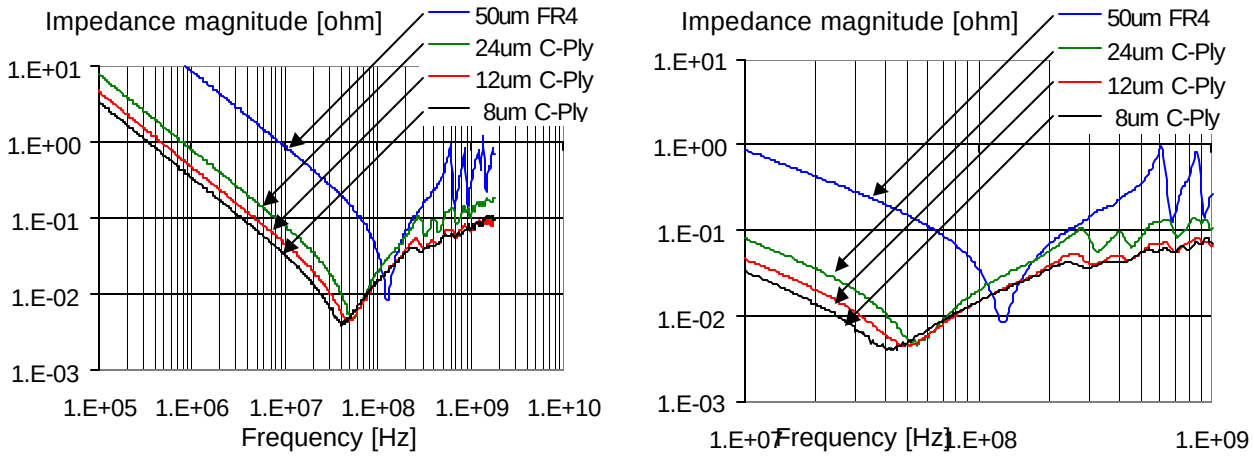

Figure 14. Full-range and zoomed self-impedance magnitude comparison of four laminates.

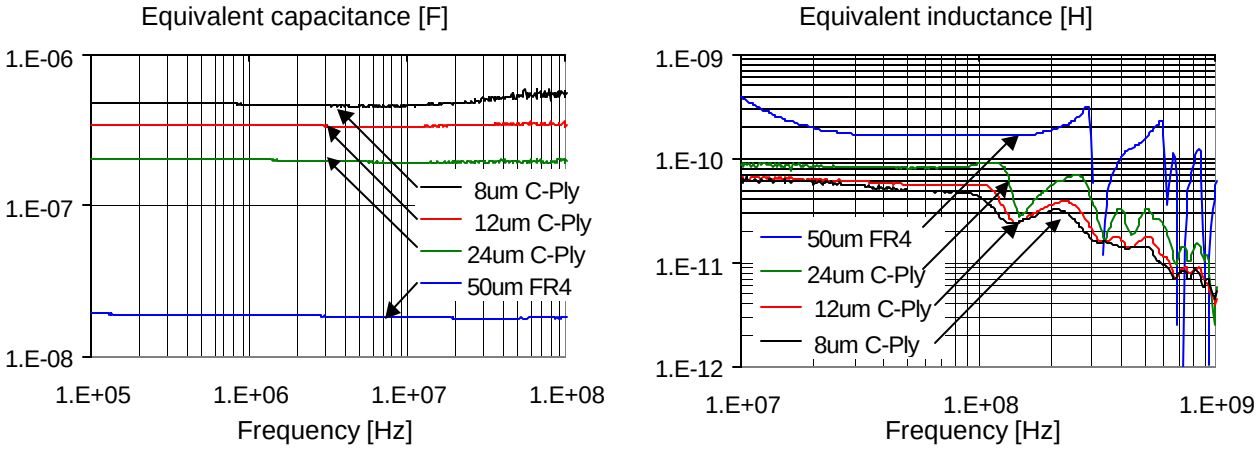

Figure 15. Comparison of extracted equivalent capacitances and inductances of the four laminates.

The extracted capacitance and inductance parameters are given in the table below.

	Capacitance [F]	Inductance [H]
8um C-Ply	4.55E-7	2.50E-11
12um C-Ply	3.30E-7	2.80E-11
24um C-Ply	1.94E-7	4.20E-11
50um FR4	1.78E-8	8.5E-11

Self-impedance comparison at corner

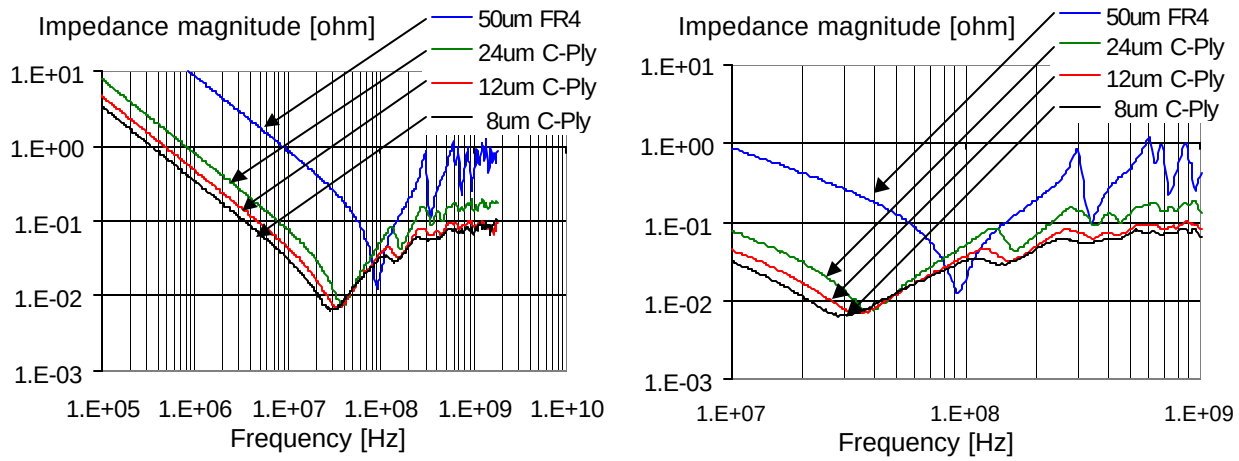

Figure 16. Full-range and zoomed self-impedance magnitude comparison of four laminates.

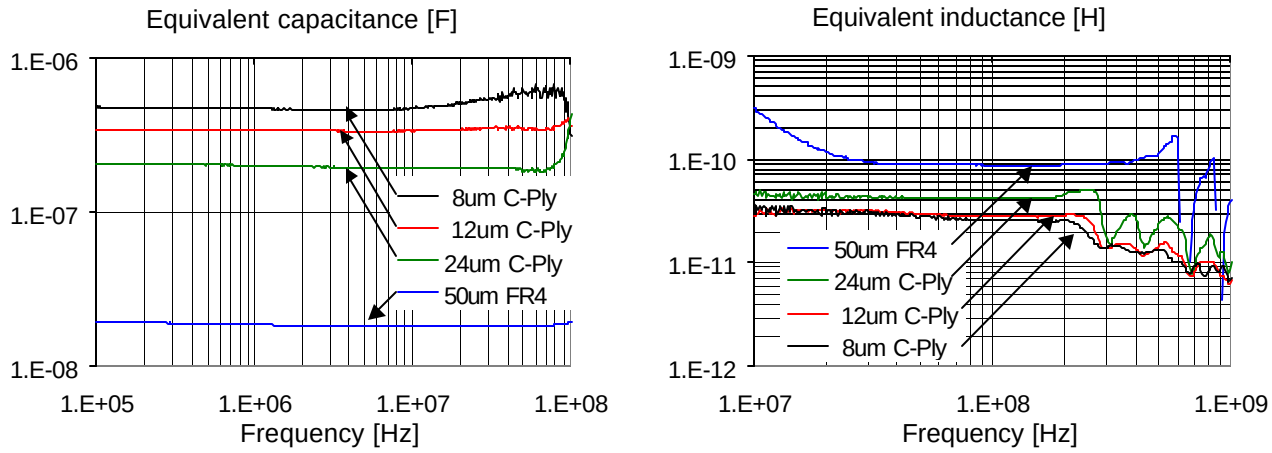

Figure 17. Comparison of extracted equivalent capacitances and inductances of the four laminates.

The extracted capacitance and inductance parameters are given in the table below.

	Capacitance [F]	Inductance [H]
8um C-Ply	4.55E-7	4.50E-11
12um C-Ply	3.30E-7	5.50E-11
24um C-Ply	1.94E-7	8.20E-11
50um FR4	1.78E-8	1.55E-10

Note that capacitance values do not change with location, but inductance does: it is the lowest in the middle, going up quadratically as we move outwards toward the sides and corners.

The capacitance values were extracted from the imaginary part of the measured self impedance, with the estimated plane inductance taken into account as a correction factor. This low-frequency approach yields the static capacitance of the planes, which by definition, is not dependent on location. The equivalent inductance is calculated from the imaginary part of the measured self impedance values, with the static capacitance taken into account as correction. With a location-independent static capacitance, the extracted inductance will be higher as we move out from the center, proportionally to the increase of impedance shown on the graphs. The same location dependency of inductance can be explained by concentrating on the series resonance frequency. For the C-Ply laminates, it is around 60MHz at the center, around 50MHz at mid-side, and around 35MHz at the corner. Assuming a simple series L-C equivalent circuit near the series resonance frequency, where C is the static plane capacitance, the changing resonance frequencies are an indication of varying inductance.

Self-impedance plots show a decreasing high-frequency impedance value, proportional to the laminate thickness. However, the difference between the 8um and 12um laminates is less than proportional. This is due to the connection geometry, which limits the self-impedance values such that it saturates around the inductance of the 12um laminate.

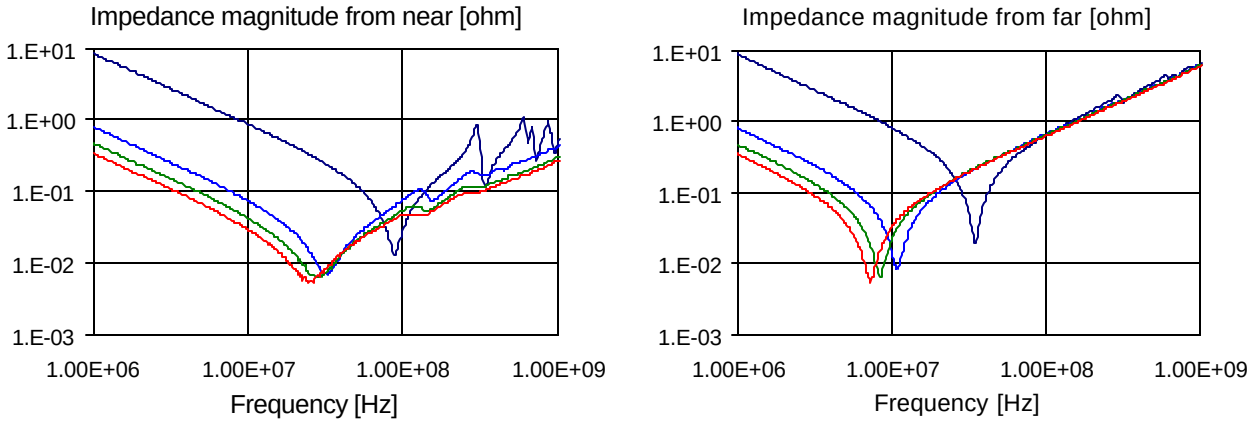

Figure 18. Self-impedance at the corner, measured from the top side (on the left) and bottom side (on the right) across the pads of the same via pair.

To show the significance of connection when measuring the self impedance of thin laminates, the same test boards were also measured with calibrated PicoProbes from the top side, where there is a nominally 3-mil via length connects to the planes, and from the bottom side, where there is a nominally 90-mil via length connecting to the planes. The two graphs below show the self impedance at the corner, measured from the top (labeled as near) and from the bottom (labeled as far). Even the 3-mil long via barrels alter the self-impedance values noticeably at high frequency: note the upslope of impedance plots of the C-Ply laminates between 300 and 1000MHz, as opposed to the almost flat response when measured from the opposite sides. With a 90-mil long via barrel in series, all four self-impedance plots blend together at high frequencies at significantly raised values.

In contrast to self-impedance values, as it is shown below, transfer impedances show a proportional high-frequency difference for all four laminates, including the 8um laminate thickness. This is because in transfer-impedance measurements the local via-connection geometry does not impact the measured values. In fact, measuring the transfer impedance from the opposite sides or from the same side, through the via barrels, will hardly change the measured data.

Transfer-impedance comparison from center to corner

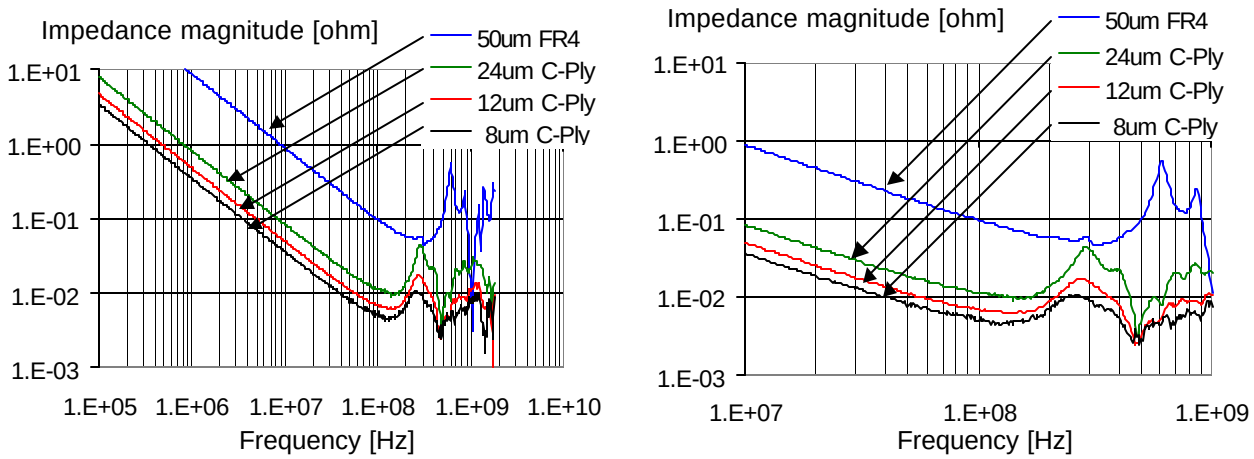

Figure 19. Full-range and zoomed self-impedance magnitude comparison of four laminates.

Transfer-impedance comparison from corner to mid-side

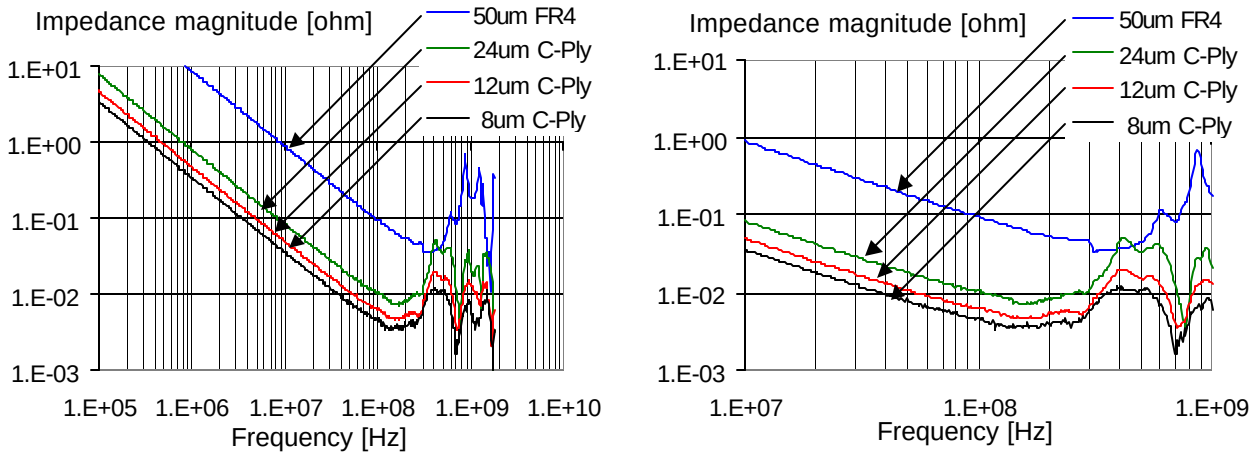

Figure 20. Full-range and zoomed self-impedance magnitude comparison of four laminates.

Transfer-impedance comparison along longer side

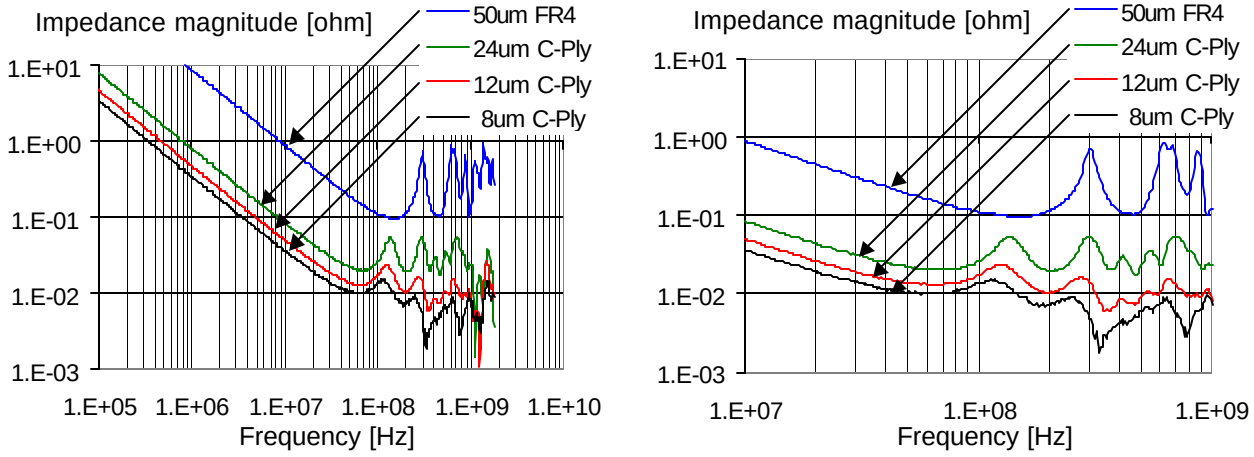

Figure 21. Full-range and zoomed self-impedance magnitude comparison of four laminates.

Transfer-impedance comparison along diagonal

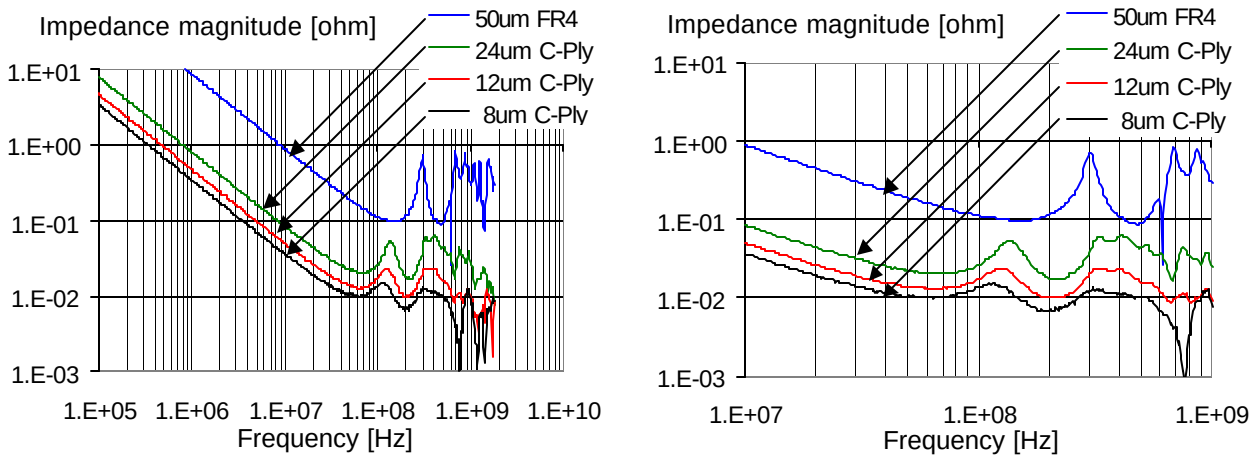

Figure 22. Full-range and zoomed self-impedance magnitude comparison of four laminates.

Impedance surfaces

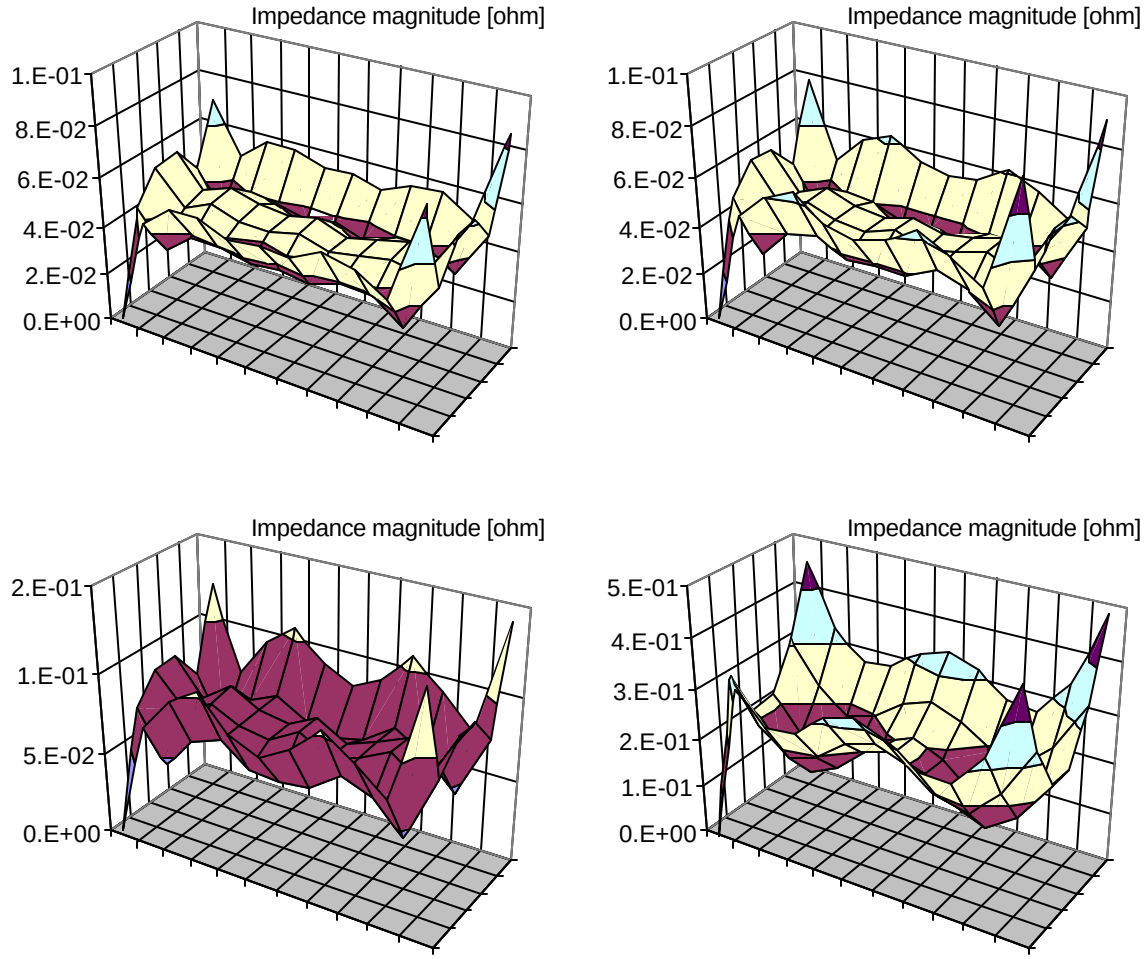

Figure 23. Measured self impedance surfaces at 500MHz. Clockwise from upper left: 8um C-Ply, 12um C-Ply, 24um C-Ply and 50um FR4 laminates.

The impedance plots in Figure 23 compare the self-impedance surfaces at 500MHz for the four different laminates. The bottom wall of each chart represent the top view of the board. Note that the lower left corner is a shorted reference point, hence the low impedance. The impedance surfaces become smoother as we move toward the thinner laminates: with 50um FR4 laminate the resonating standing-wave pattern is clearly visible. With 8um C-Ply laminate, the inside of the impedance plot is fairly flat, only there is an increase due to the increasing inductance along the sides and at the corners.

Acknowledgment
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Conclusion
Ultra-thin dielectrics for power-ground layers provide very low impedance across a very wide frequency range. This impedance can be as much as an order of magnitude or more lower than existing thin commercial laminates. These ultra-thin dielectric laminates also offer the advantage of dampening noise on the power and ground planes. The development and commercialization of these thinner dielectric materials will be imperative for acceptable electrical performance in future high speed digital designs.

References:
[1] Istvan Novak, "Measuring Milliohms and PicoHenrys in Power Distribution Networks," DesignCon2000, Santa Clara, CA, February 1-4, 2000.
[2] Istvan Novak, "Overview of Frequency-Domain Power Distribution Measurements," DesignCon2003, HP-TF2, Santa Clara, CA, January 27, 2000.