ADMV7310-EVALZ User Guide
UG-1590

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Evaluating the ADMV7310 E-Band Upconverter SIP, 71 GHz to 76 GHz

FEATURES

Simple power-up with on-board LDO regulators
Gain tuning and devices bias adjustment with potentiometers
Option to bypass LDO regulators with connector jumpers

EVALUATION KIT CONTENTS

ADMV7310-EVALZ
Connector jumpers

EQUIPMENT NEEDED

5 V and −5 V dc power supplies
Baseband signal generator
RF signal generator
E-band spectrum analyzer
WR-12 waveguide

ADMV7310-EVALZ PHOTOGRAPH

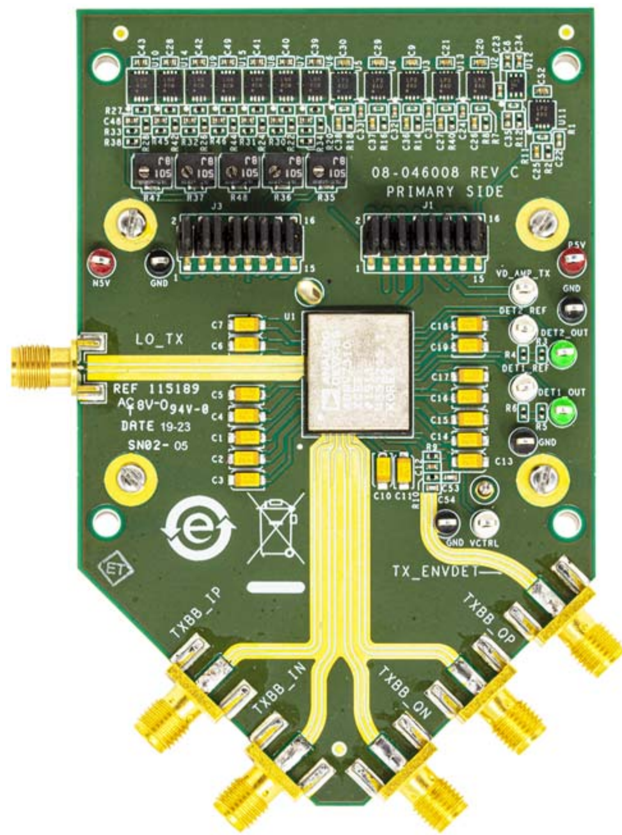

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Figure 1.

GENERAL DESCRIPTION

The ADMV7310-EVALZ evaluation board incorporates the ADMV7310 with low dropout (LDO) regulators, potentiometers, and a waveguide back plate to allow quick and easy evaluation of the ADMV7310. The LDO regulators allow the ADMV7310 to be powered on by ±5 V supplies. Potentiometers allow gate tuning for various gain ranges.

The ADMV7310 is a fully integrated system in package (SiP) in phase/quadrature (I/Q) upconverter that operates at an intermediate frequency (IF) input range of dc to 2 GHz and a radio frequency (RF) output range of 71 GHz to 76 GHz.

The ADMV7310 data sheet, available at www.analog.com, provides full specifications for the ADMV7310. Consult the ADMV7310 data sheet in conjunction with this user guide when using the evaluation board.

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REVISION HISTORY

11/2019—Revision A: Initial Version

EVALUATION BOARD SETUP

QUICK START PROCEDURE

The ADMV7310-EVALZ evaluation board is equipped with LDO regulators to provide biases for all drains and gates. Only +5 V dc and −5 V dc power supplies are needed to power up the chip. Note that the ADMV7310-EVALZ board is tuned in factory to achieve a typical current level. To ensure that damage does not occur, use the following sequence to power up:

1. Place jumpers on all pins of J3.
2. Place jumpers on all pins for J1 except Pin 1 and Pin 2.
3. Connect a −5 V dc power supply to the N5V test point and ground to the nearest GND test point.
4. Connect the 5 V dc power supply to the P5V test point.
5. Turn on the −5 V dc supply, then the 5 V dc supply.
6. Place jumpers on Pin 1 and Pin 2 of J1.
7. Connect VCTRL to −5 V dc for maximum gain.
8. Adjust the dc voltages between −0.2 V and +0.2 V to the TXBB_IN, TXBB_IP, TXBB_QN, and TXBB_QP ports for LO nulling.

To power down the chip, use the following sequence:

1. Disconnect the −5 V dc supply on VCTRL.
2. Turn off the 5 V dc supply.
3. Turn off −5 V dc supply.

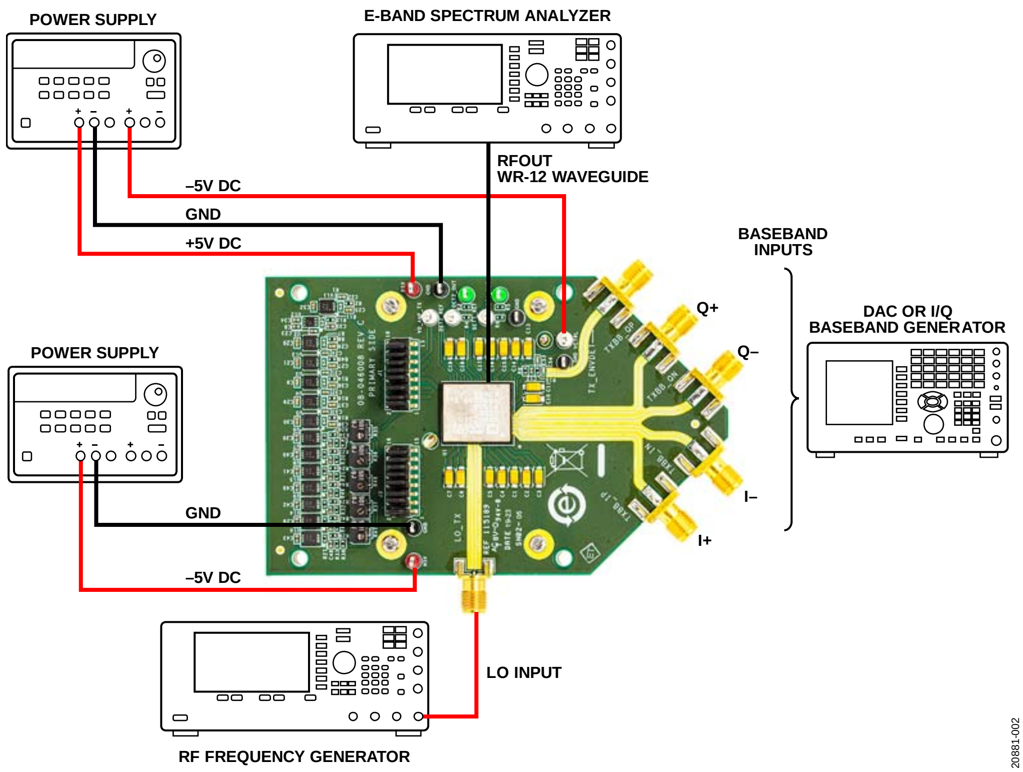

Figure 2. ADMV7310-EVALZ Lab Bench Setup

GAIN TUNING PROCEDURE

Table 1. Gain Tuning Summary

Gain Tuning Order	Gain Reduction Range (dB)	Gain Tuning	Recommended Gain Tuning Voltage Range (V)
1	0 to 10	VGA_VCTL12	−5 to −1
2	10 to 25	VGA_VG345 and VGA_VG6	−2 to 0
3	25 to 40	PA_VG1	−2 to 0

There are three steps to control the total gain of the transmitter (follow the gain tuning order in Table 1 to achieve the correct gain level for optimal performance).

Step 1: VGA_VCTL12 Tuning

The VGA_VCTL12 pin is tied to the VCTRL test point. To achieve maximum gain, set the VCTRL test point to −5 V dc. To achieve a gain reduction between 0 dB and 10 dB, adjust the VCTRL test point voltage between −5 V and −1 V (typical minimum gain for the variable gain amplifier).

Step 2: VGA_VG345 and VGA_VG6 Tuning

If further gain reduction is needed after conducting Step 1, lower the third to sixth variable gain amplifier drain current levels, I_{VGA_VD345} and I_{VGA_VD6}, by adjusting VGA_VG345 and VGA_VG6 together, between −2 V and 0 V, to achieve the correct gain level. The total current consumption of I_{VGA_VD345} and I_{VGA_VD6} can drop to 25 mA.

To tune VGA_VG345 and VGA_VG6 on the ADMV7310-EVALZ, use the following sequence:

1. Power down the chip by turning off the 5 V dc supply and then turning off the −5 V dc supply.
2. The R36 potentiometer tunes VGA_VG345 and VGA_VG6. Place an ampere meter between Pin 9 and Pin 10 on J1 to monitor the I I_{VGA_VD345} and I_{VGA_VD6} current.
3. Power up the chip by turning on the −5 V dc supply and then turning on the 5 V dc supply.
4. Adjust the R36 resistor to tune VGA_VG345 and VGA_VG6. The total current of I_{VGA_VD345} and I_{VGA_VD6} must not drop below 25 mA.

Step 3: PA_VG1 Tuning

If further gain reduction is needed after conducting Step 1 and Step 2, lower the drain current level of the first power amplifier, I_{PA_VD1}, by adjusting PA_VG1 between −2 V and 0 V to achieve the correct gain level. The current consumption of I_{PA_VD1} can drop to 80 mA.

To tune PA_VG1 on the ADMV7310-EVALZ, use the following sequence:

1. Power down the chip by turning off the 5 V dc supply and then turning off the −5 V dc supply.
2. The R47 potentiometer tunes the PA_VG1 pin. Place an ampere meter between Pin 3 and Pin 4 on J1 to monitor the current of PA_VD1.
3. Power up the chip by turning on the −5 V dc supply and then turning on the 5 V dc supply.
4. Adjust the R47 to tune PA_VG1. The PA_VD1 current must not drop below 80 mA for Power Amplifier 1 (PA1) tuning.

EVALUATION BOARD SCHEMATICS

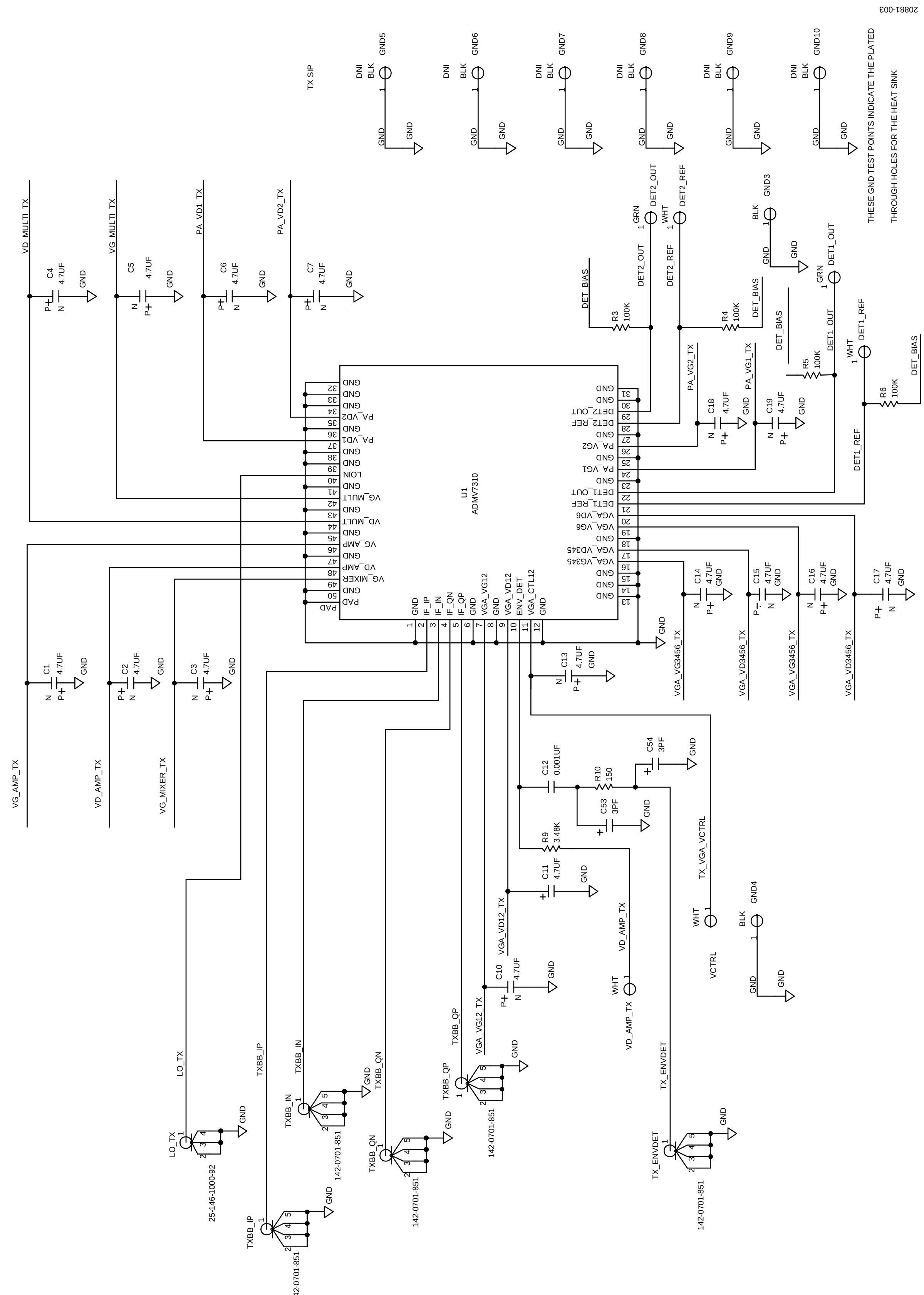

Figure 3. ADMV7310-EVALZ Schematic

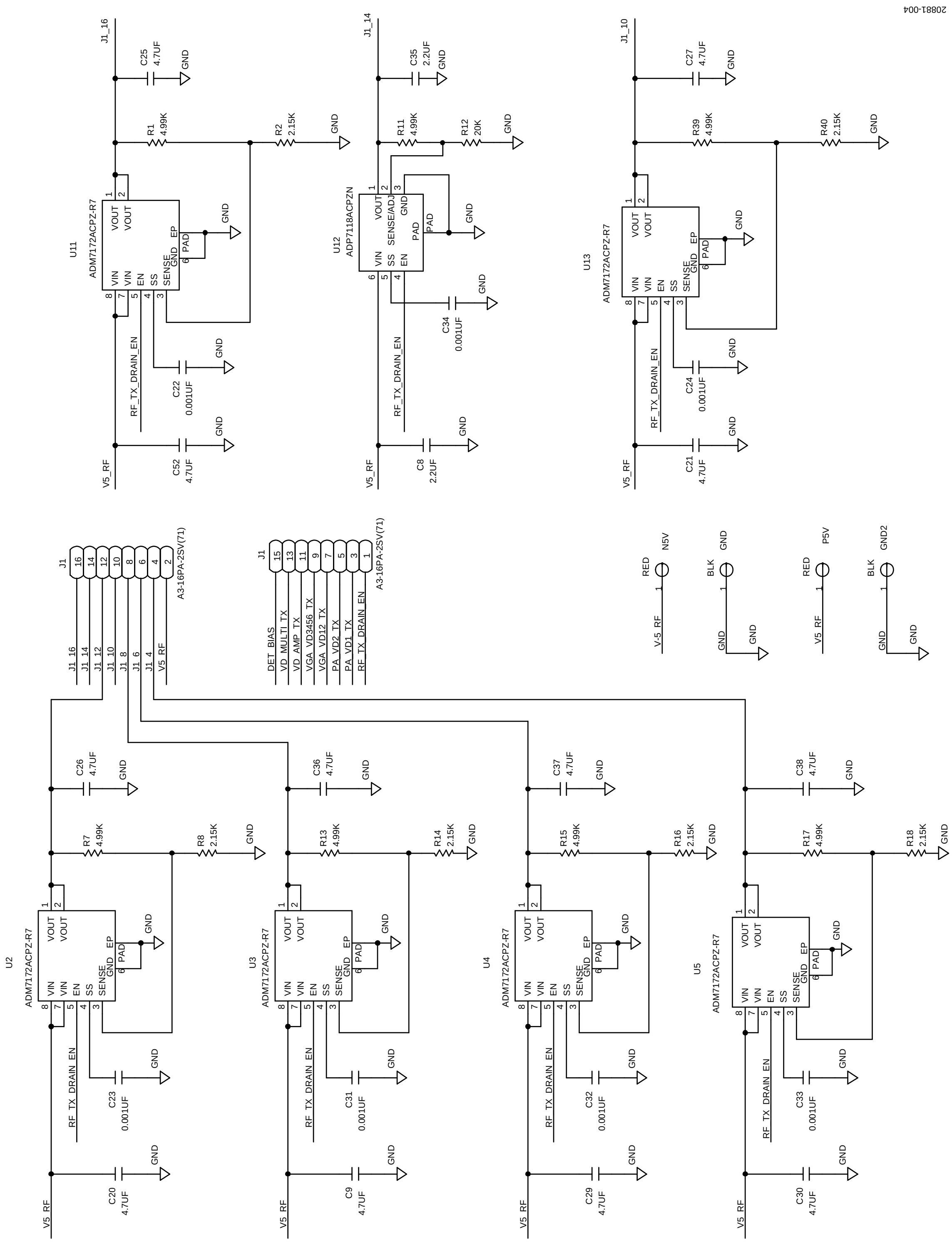

Figure 4. ADMV7310-EVALZ Drain Supplies

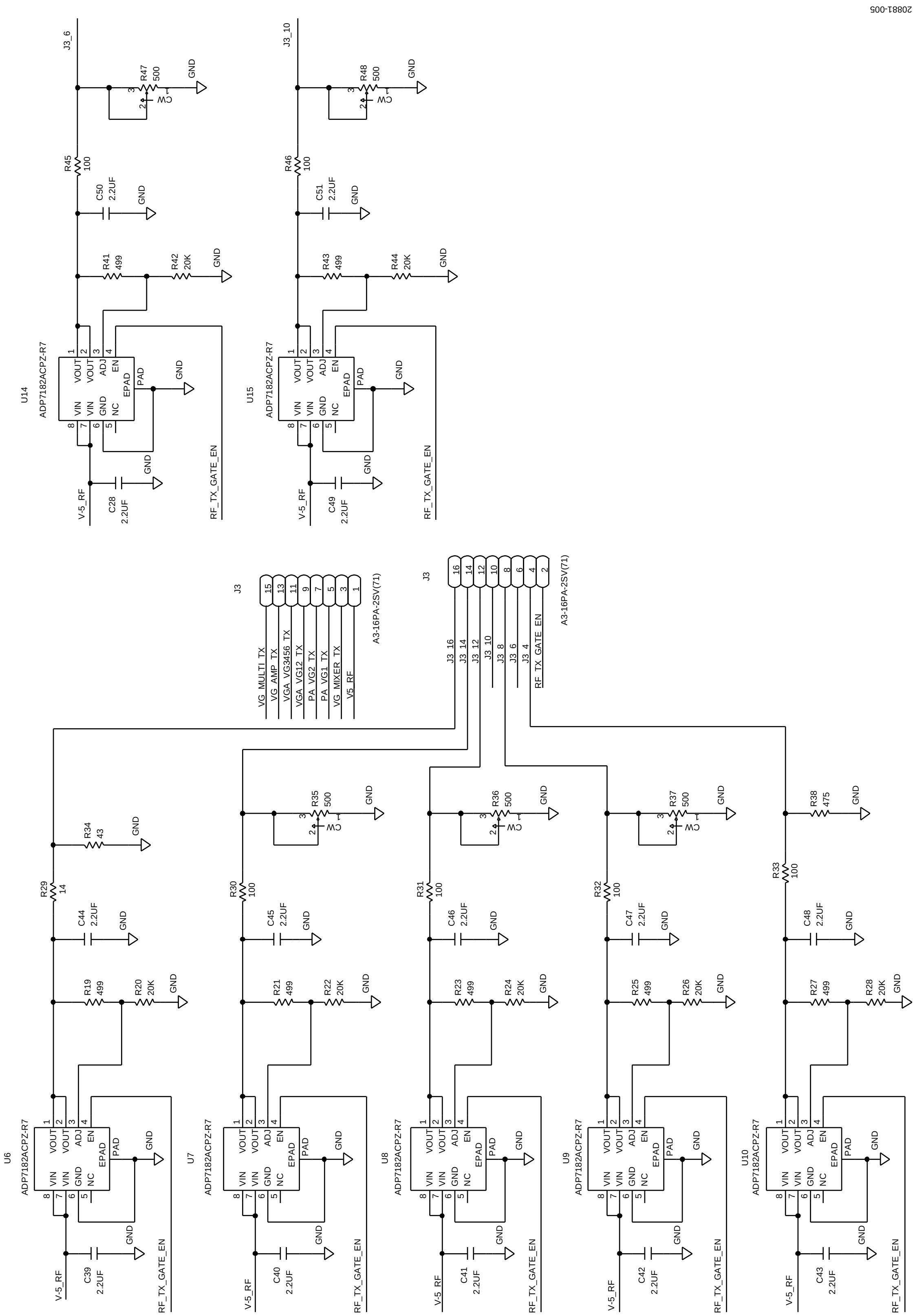

Figure 5. ADMV7310-EVALZ Gate Supplies

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. Bill of Materials

Qty	Designators	Description	Part Number
16	C1, C2, C3, C4, C5, C6, C7, C10, C11, C13, C14, C15, C16, C17, C18, C19	Tantalum capacitor, 4.7 µF	TAJA475K020RNJ
8	C12, C22, C23, C24, C31, C32, C33, C34	Capacitors, ceramic, X7R, automotive grade, 1 nF	CGA2B2X7R1H102K050BA
12	C9, C20, C21, C25, C26, C27, C29, C30, C36, C37, C38, C52	Capacitors, ceramic, X5R, general-purpose, 4.7 µF	GRM155R60J475ME87D
16	C8, C28, C35, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51	Capacitors, ceramic, 2.2 µF	C1005X5R0J225K050BC
2	C53, C54	Capacitors, ceramic, NP0, high frequency, high Q, 3 pF	GJM1555C1H3R0BB01B
2	DET1_OUT, DET2_OUT	Test point	TP104-01-05
4	DET1_REF, DET2_REF, VCTRL, VD_AMP_TX	Test point	TP-104-01-09
4	GND, GND2, GND3, GND4	Test point	TP-104-01-00
2	J1, J3	Connector header	A3-16PA-2SV(71)
1	LO_TX	End launch connector	25-146-1000-92
2	N5V, P5V	Test point	TP-104-01-02
7	R1, R7, R11, R13, R15, R17, R39	Resistor, high stability, flat chip, 4.99 kΩ	TNPW04024K99BEED
1	R10	Resistor, precision, thick film chip, 150 Ω	ERJ-2RKF1500X
8	R12, R20, R22, R24, R26, R28, R42, R44	Resistor, precision, thick film chip, 20 kΩ	ERJ-2RKF2002X
6	R2, R8, R14, R16, R18, R40	Resistor, precision, thick film, 2.15 kΩ	ERJ-2RKF2151X
7	R19, R21, R23, R25, R27, R41, R43	Resistor, precision, thick film chip, 499 Ω	ERJ-2RKF4990X
1	R29	Resistor, 14 Ω	TFCR0402-16W-E-14R0DT
4	R3, R4, R5, R6	Resistor, precision, thick film chip, 100 kΩ	ERJ-2RKF1003X
6	R30, R31, R32, R33, R45, R46	Resistor, precision, thick film chip, 100 Ω	ERJ-2RKF1000X
1	R34	Resistor, precision, thick film chip, 43 Ω	ERJ-2RKF43R0X
5	R35, R36, R37, R47, R48	Resistor, Potentiometer, 500 Ω	SM-42TW501CT-ND
1	R38	Resistor, precision, thick film chip, 475 Ω	ERJ-2RKF4750X
1	R9	Resistor, precision, thick film chip, 3.48 kΩ	ERJ-2RKF3481X
5	TXBB_IN, TXBB_IP, TXBB_QN, TXBB_QP, TX_ENVDET	SMA end launch connector	142-0701-851
1	U1	IC Analog Devices, Inc., E-band upconverter system in package (SiP), 71 GHz to 76 GHz	ADMV7310
7	U6, U7, U8, U9, U10, U14, U15	IC Analog Devices, Inc., low noise regulator	ADP7182ACPZ-R7
6	U2, U3, U4, U5, U11, U13	IC Analog Devices low noise regulator	ADM7172ACPZ-R7
1	U12	IC Analog Devices low noise regulator	ADP7118ACPZN

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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