Sup*IR*Buck™

USER GUIDE FOR IR3843A EVALUATION BOARD

Double Sided PCB

DESCRIPTION

The IR3843A is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 5mmx6mm Power QFN package.

Key features offered by the IR3843A include programmable soft-start ramp, precision 0.7V reference voltage, Power Good, thermal protection, programmable switching frequency, Sequence input, Enable input, input under-voltage lockout for proper start-up, and pre-bias start-up.

An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the IR3843A evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3843A is available in the IR3843A data sheet.

BOARD FEATURES

- V_{in} = +12V (13.2V Max)
- V_{cc}=+5V (5.5V Max)
- V_{out} = +1.8V @ 0- 3A
- F_s=600kHz
- L= 2.2uH
- C_{in}= 1x10uF (ceramic 1206)
- C_{out}= 3x22uF (ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum 3A load should be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IR3843A has two input supplies, one for biasing (Vcc) and the other as input voltage (Vin). Separate supplies should be applied to these inputs. Vcc input should be a well regulated 4.5V-5.5V supply and it would be connected to Vcc+ and Vcc-.

Table I. Connections

Connection	Signal Name
VIN+	V_{in} (+12V)
VIN-	Ground of V_{in}
Vcc+	Vcc input
Vcc-	Ground for Vcc input
VOUT-	Ground of V_{out}
VOUT+	V_{out} (+1.8V)
Enable	Enable
Seq.	Sequence Input
PGood	Power Good Signal

LAYOUT

The PCB is a 4-layer board. All of layers are 2 Oz. copper. It is a double sided board with components mounted on both sides.

Power supply decoupling capacitors, the Bootstrap capacitor and feedback components are located close to IR3843A. The feedback resistors are connected to the output voltage at the point of regulation and are located close to the SupIRBuck. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

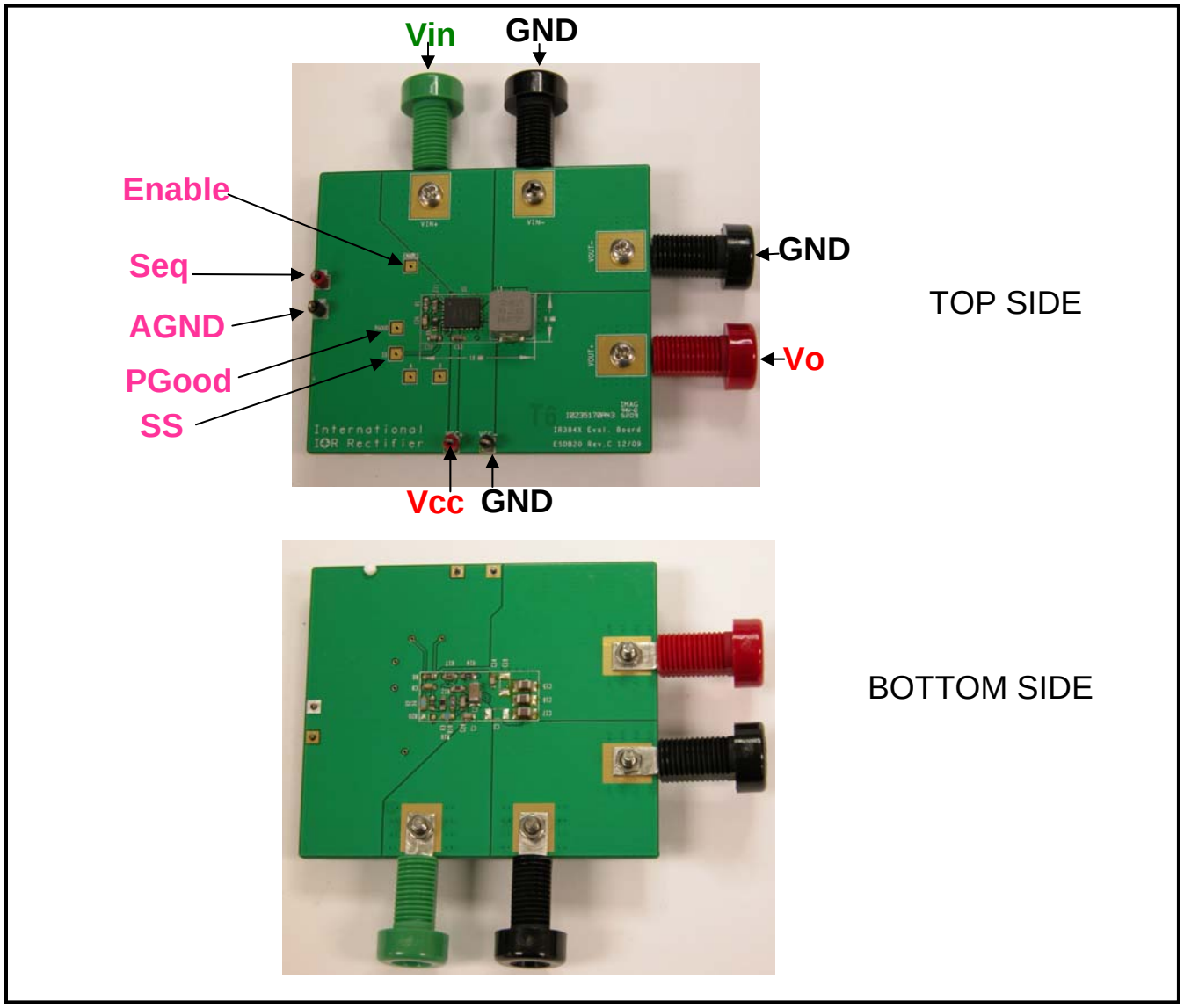


Fig. 1: Connection diagram of IR384xA evaluation boards

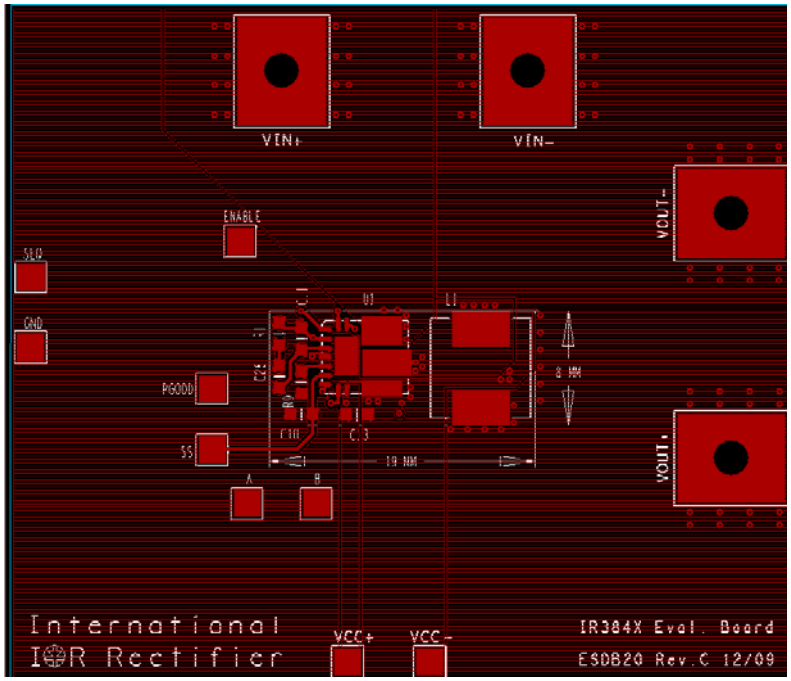


Fig. 2: Board layout, top overlay

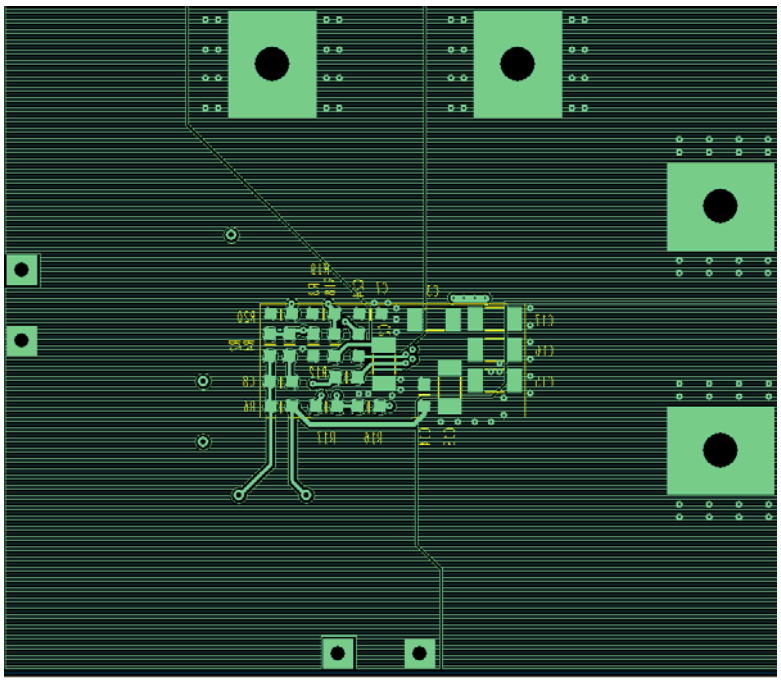


Fig. 3: Board layout, bottom overlay (rear view)

Fig. 4: Board layout, mid-layer I.

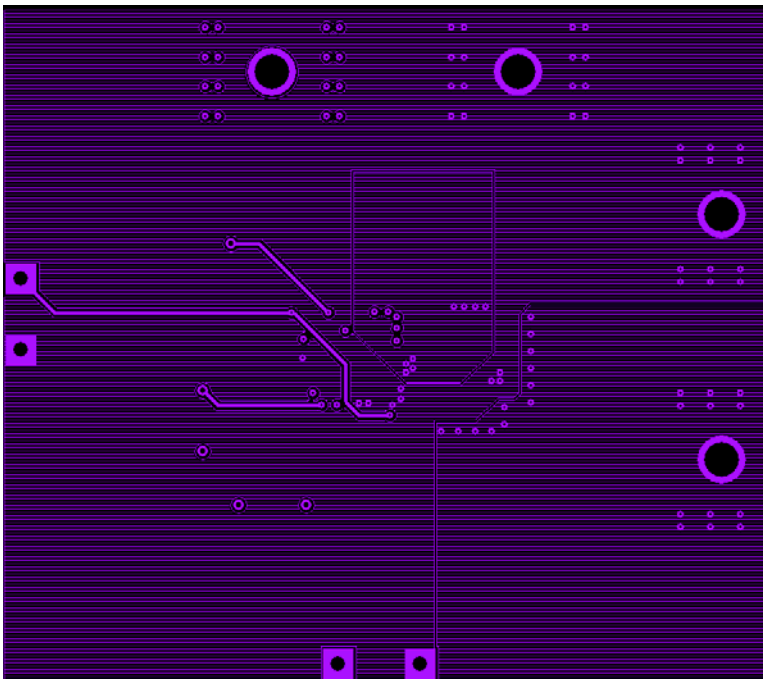


Fig. 5: Board layout, mid-layer II.

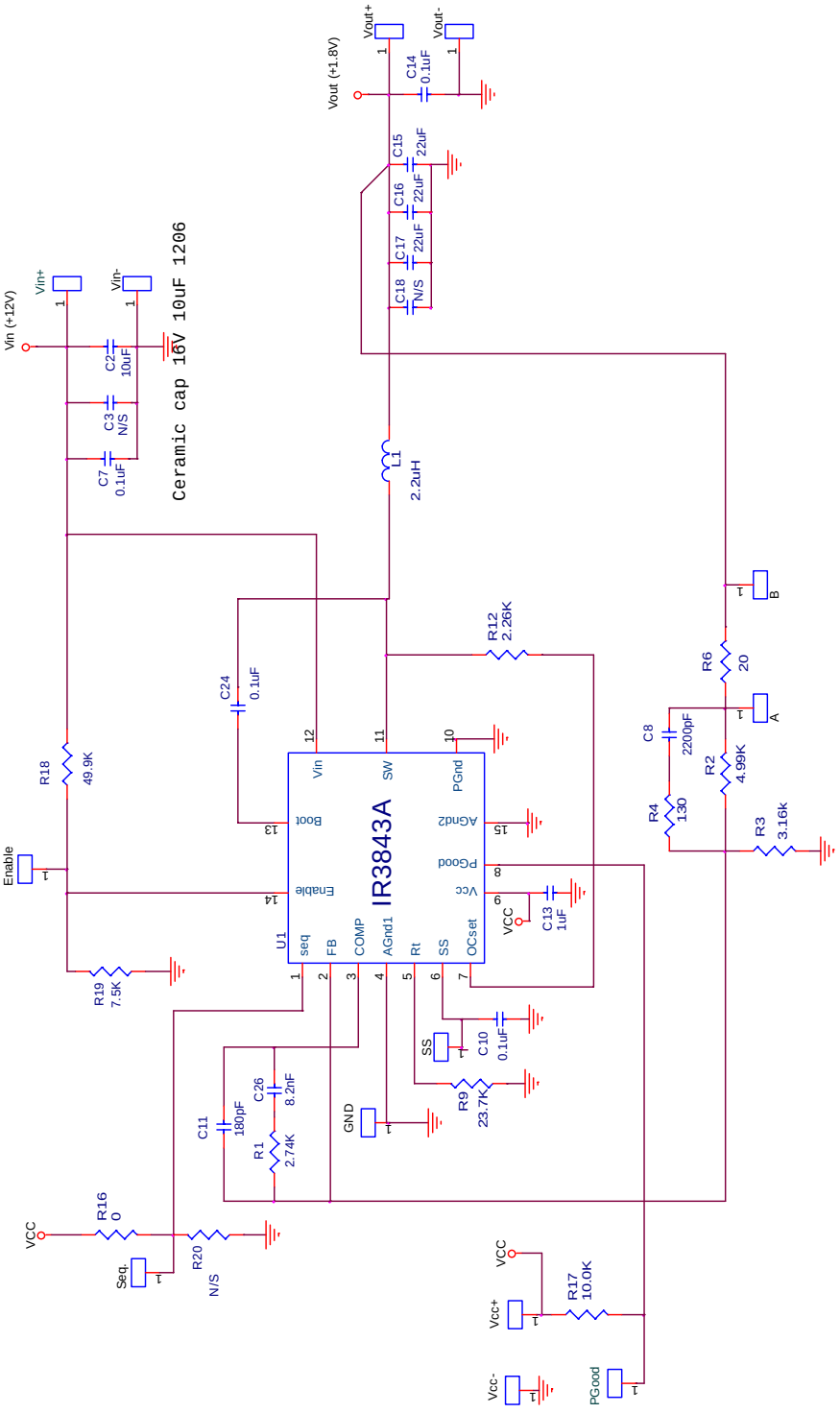


Fig. 6: Schematic of the IR3843A evaluation board

Bill of Materials

Item	Quantity	Part Reference	Value	Description	Manufacturer	Part Number
1	1	C2	10uF	10uF,1206,16V, X7R, 20%	Panasonic - ECG	ECJ-3YX1C106K
2	4	C7 C14 C24 C10	0.1uF	0603, 25V, X7R, 10%	Panasonic	ECJ-1VB1E104K
3	1	C8	2200pF	0603,50V,X7R, 10%	Panasonic	ECJ-1VB1H222K
4	1	C11	180pF	50V, 0603, NP0, 5%	Murata	GRM1885C1H181JA01D
5	1	C13	1uF	16V, 0603, X5R, 10%	Murata	GRM188R61C105KA93B
6	3	C15 C16 C17	22uF	0805, 6.3V, X5R, 20%	Panasonic	ECJ-2FB0J226M
7		C3,C18	Not used			
8	1	C26	8200pF	0603, 50V, X7R, 10%	Panasonic	ECJ-1VB1H822K
9	1	L1	2.2uH	7.05*6.6*4.8mm,12.5mΩ max	Cyntec	PCMB065T-2R2MS
10	1	R1	2.74k	0603,1/10W,1%	Rohm	MCR03EZPFX2741
11	1	R2	4.99k	0603,1/10W,1%	Rohm	MCR03EZPFX4991
12	1	R3	3.16k	0603,1/10W,1%	Rohm	MCR03EZPFX3161
13	1	R4	130	0603,1/10W,1%	Panasonic	ERJ-3EKF1300V
14	1	R6	20	0603,1/10 W,1%	Vishay/Dale	CRCW060320R0FKEA
15	1	R9	23.7K	0603,1/10W,1%	Rohm	MCR03EZPFX2372
16	1	R16	0	0603,1/10 W,5%	Vishay/Dale	CRCW06030000Z0EA
17	1	R12	2.26K	0603,1/10 W,1%	Rohm	MCR03EZPFX2261
18	1	R17	10K	0603,1/10 W,1%	Rohm	MCR03EZPFX1002
19	1	R18	49.9k	0603,1/10 W,1%	Rohm	MCR03EZPFX4992
20	1	R19	7.5k	0603,1/10W,1%	Rohm	MCR03EZPFX7501
21		R20	Not used			
22	1	U1	IR3843A	3A SupIRBuck, PQFN 5x6mm	International Rectifier	IR3843AMPbF

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vcc=5V, Vo=1.8V, Io=0-3A, Room Temperature, No Air Flow

Fig. 7. Start up at 3A Load
Ch_1:V_{in}, Ch_2:V_o, Ch_3:V_{ss}, Ch_4:Enable

Fig. 8. Start up at 3A Load,
Ch_1:V_{in}, Ch_2:V_o, Ch_3:V_{ss}, Ch_4:V_{PGood}

Fig. 9. Start up with 1.62V Pre Bias, 0A Load, Ch_2:V_o, Ch_3:V_{SS}

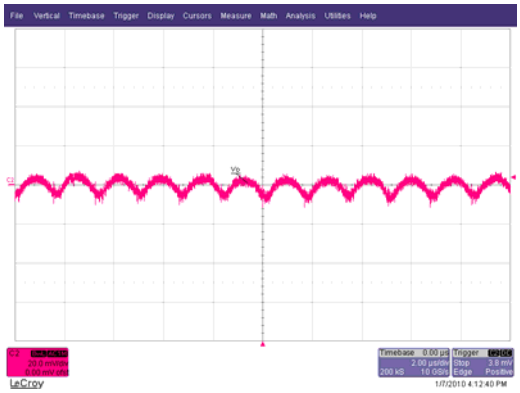


Fig. 10. Output Voltage Ripple, 3A load
Ch_2: V_o

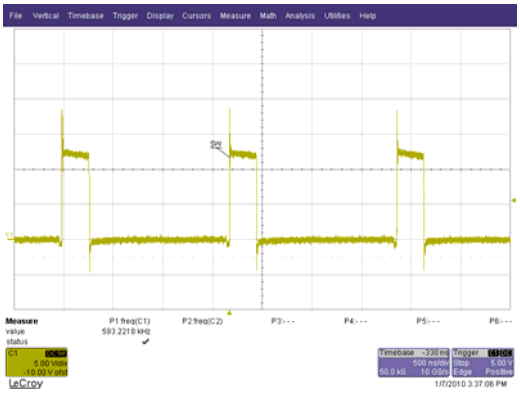


Fig. 11. Inductor node at 3A load
Ch_1:LX

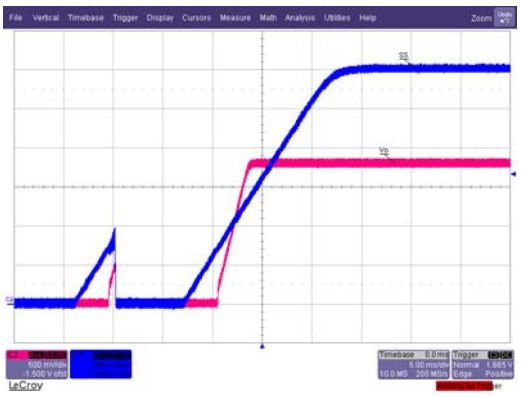


Fig. 12. Short (Hiccup) Recovery
Ch_2:V_o , Ch_3:V_{SS}

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Io=0-3A, Room Temperature, No Air Flow

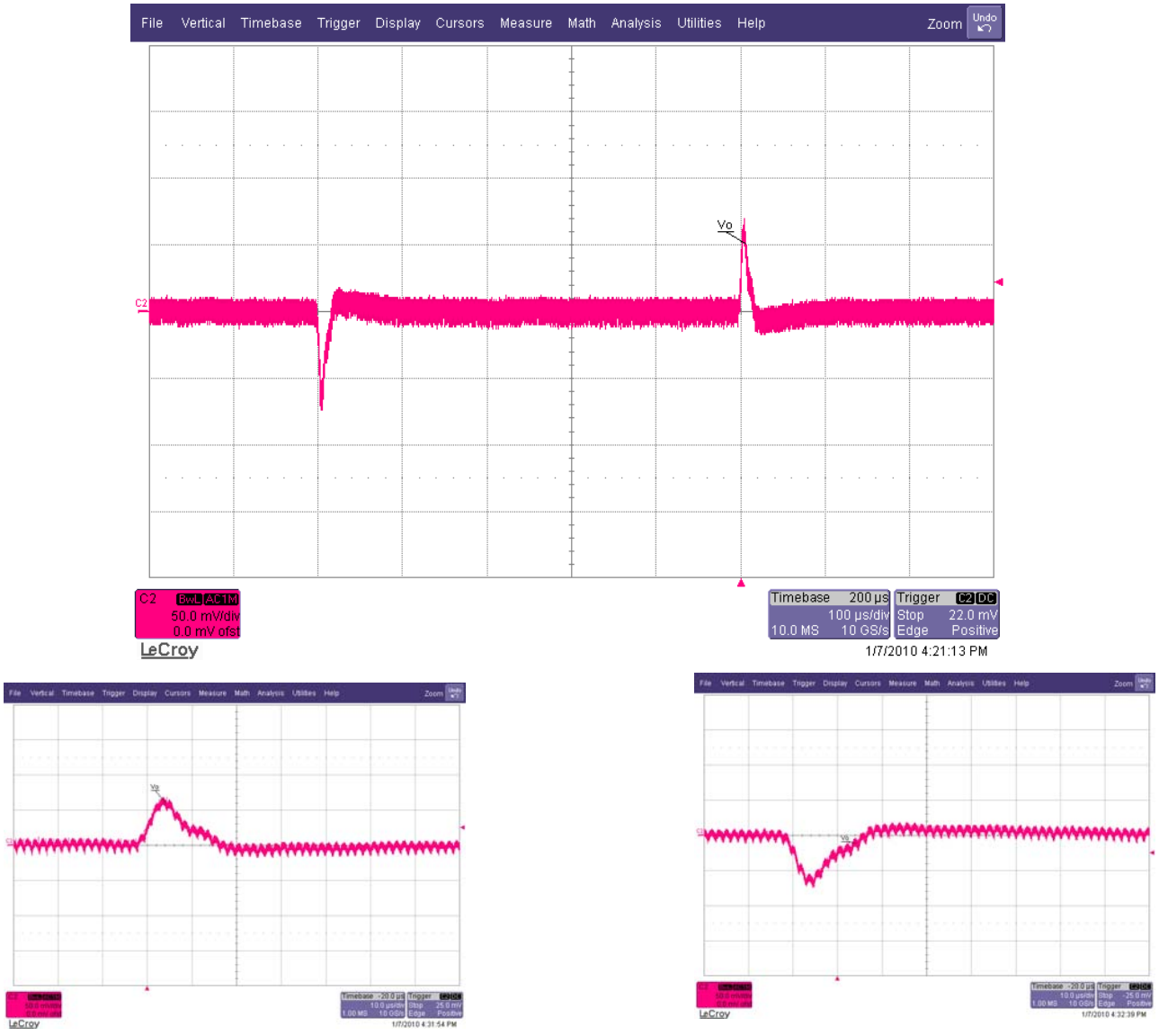


Fig. 13. Transient Response, 1.5A to 3A step 2.5A/µs
Ch_2:V_o

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Io=3A, Room Temperature, No Air Flow

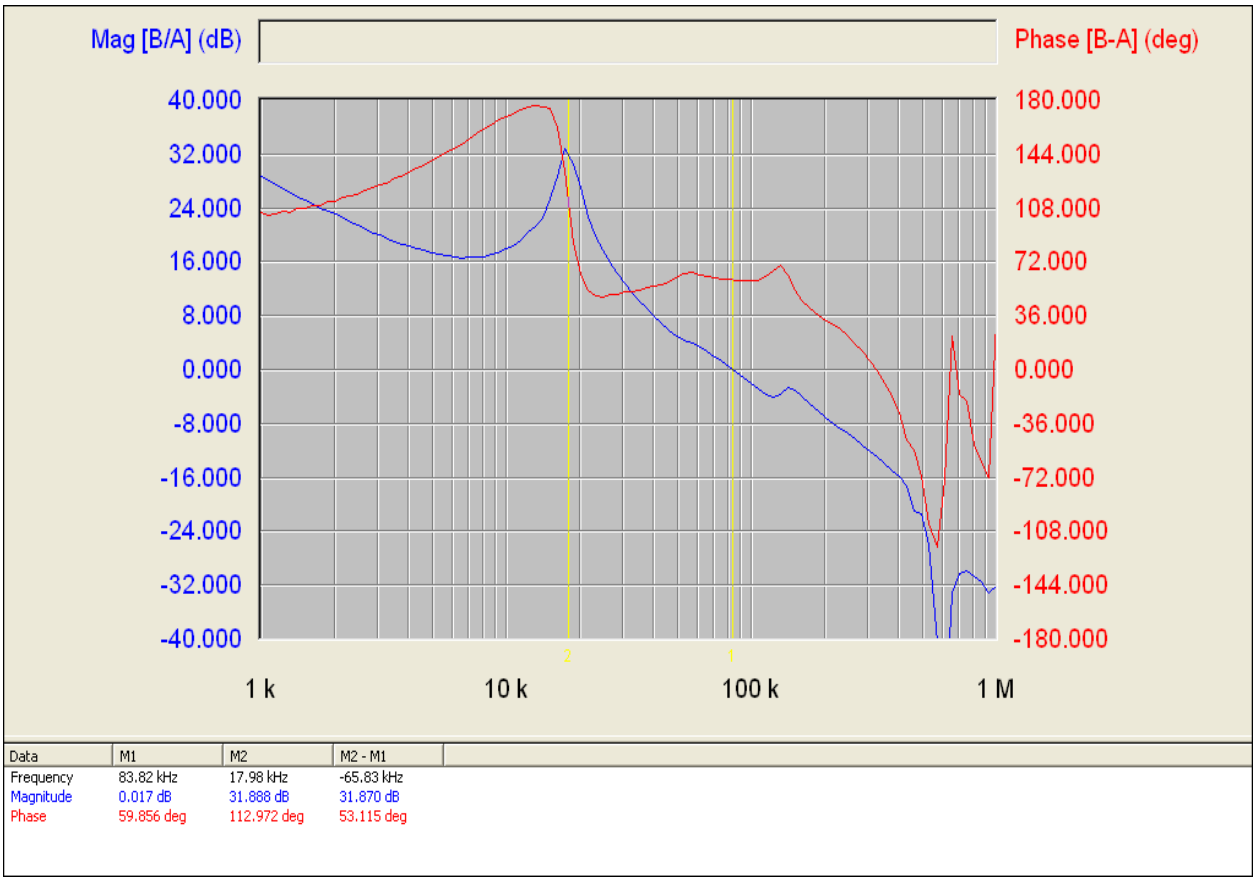


Fig. 14. Bode Plot at 3A load shows a bandwidth of 83.8KHz and phase margin of 59.8°

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Io=0- 3A, Room Temperature, No Air Flow

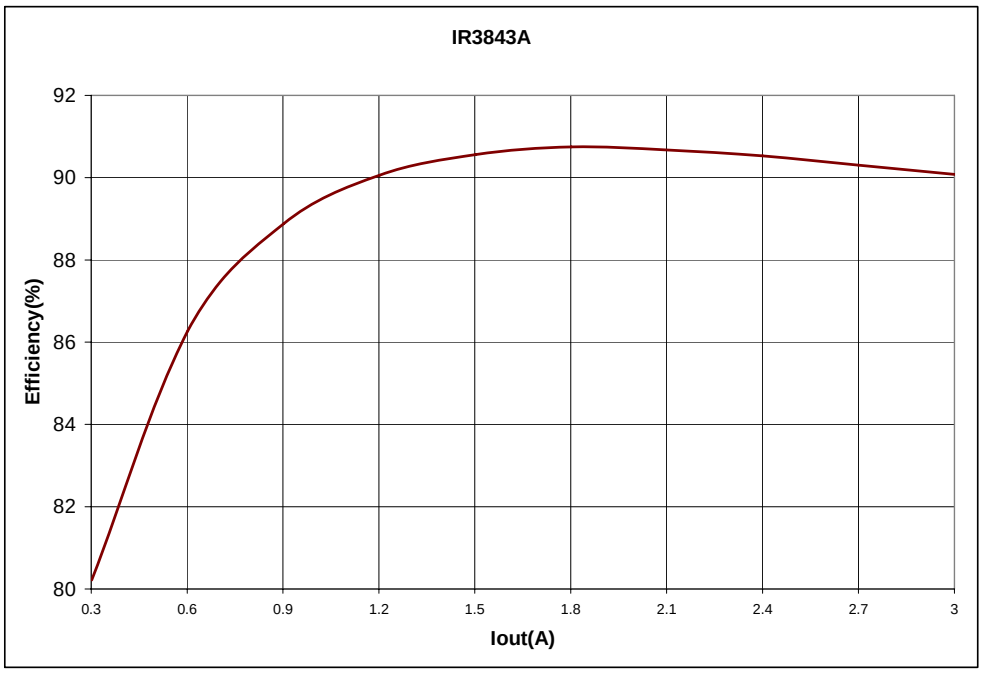


Fig.15: Efficiency versus load current

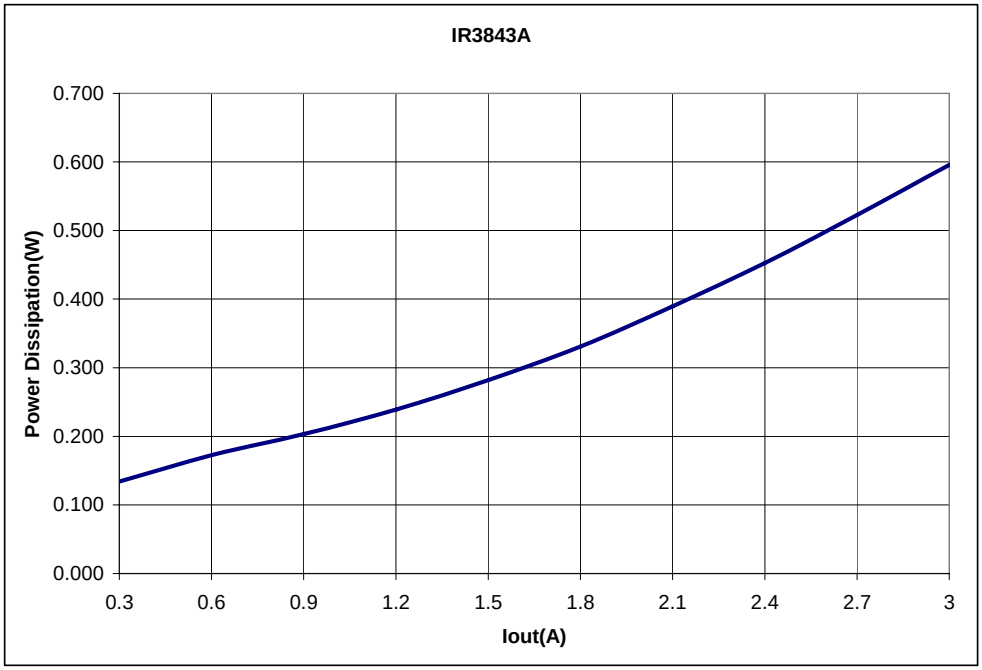


Fig.16: Power loss versus load current

THERMAL IMAGE
Vin=12V, Vcc=5V, Vo=1.8V, Io=3A, Room Temperature, No Air Flow

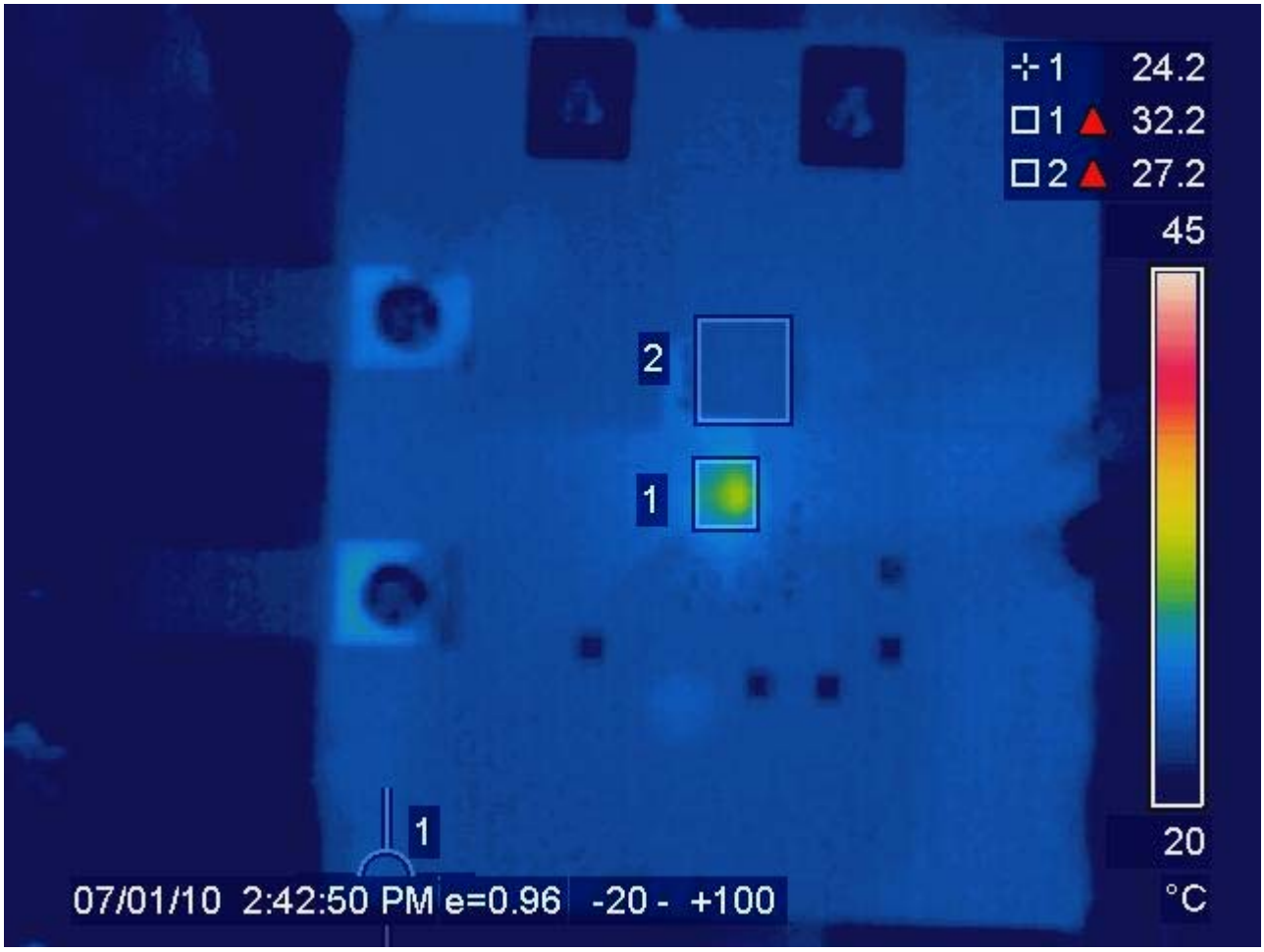


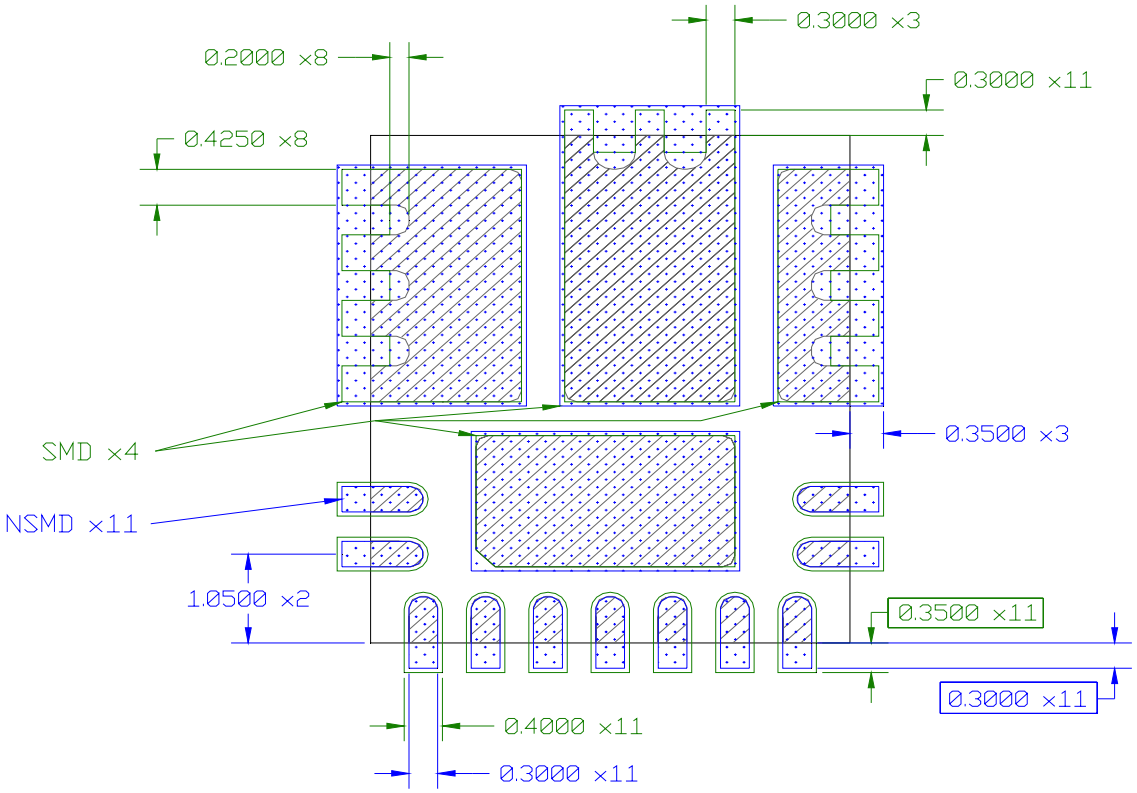
Fig. 17: Thermal Image at 3A load
Test points 1 and 2 are IR3843A and inductor, respectively.

PCB Metal and Components Placement

Lead lands (the 11 IC pins) width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.

Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large and inspectable toe fillet.

Pad lands (the 4 big pads other than the 11 IC pins) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than 0.17mm for 2 oz. Copper; no less than 0.1mm for 1 oz. Copper and no less than 0.23mm for 3 oz.



All Dimensions in mm

PCB Copper

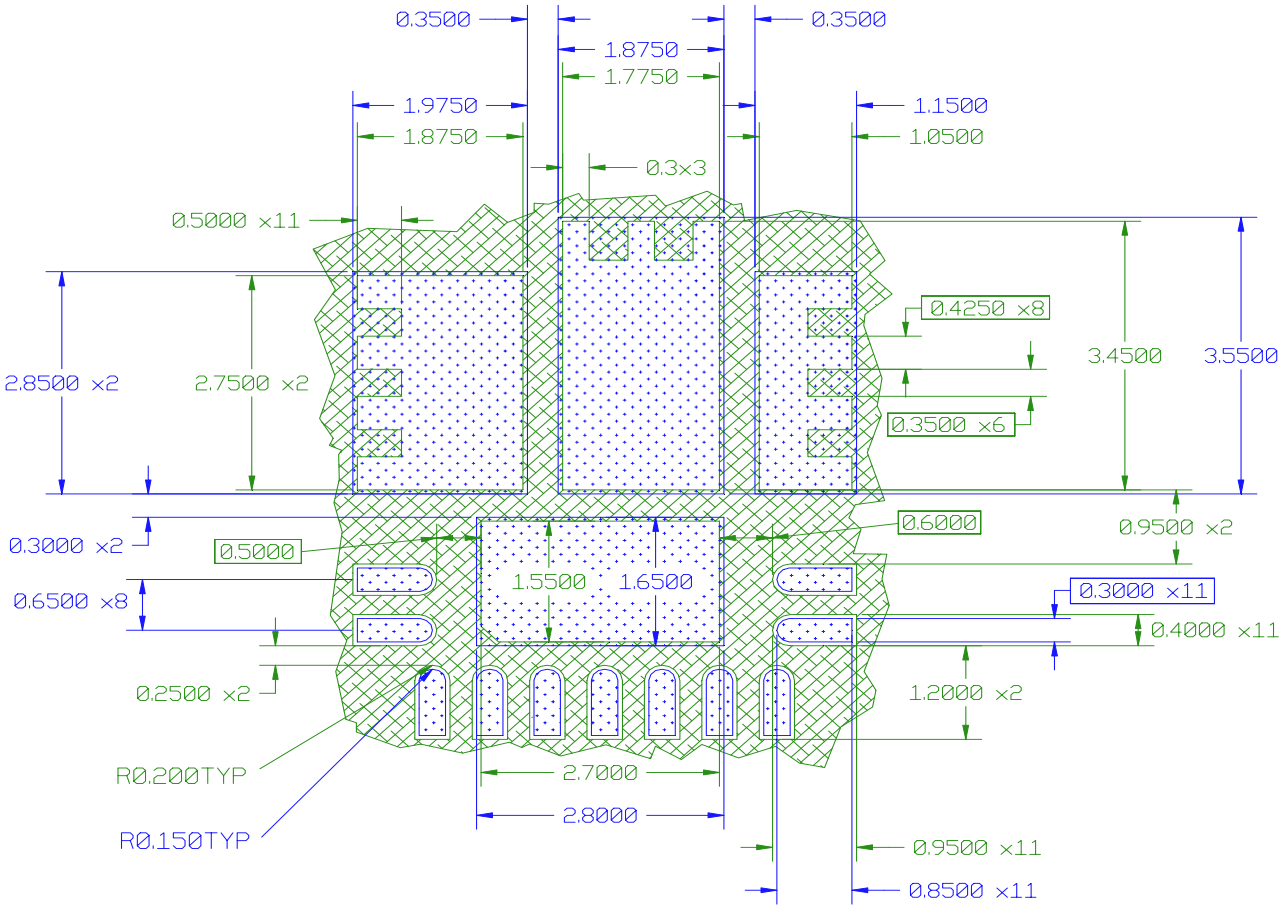
Component

Solder Resist

It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist misalignment.

Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.



All Dimensions in mm

PCB Copper

PCB Solder Resist

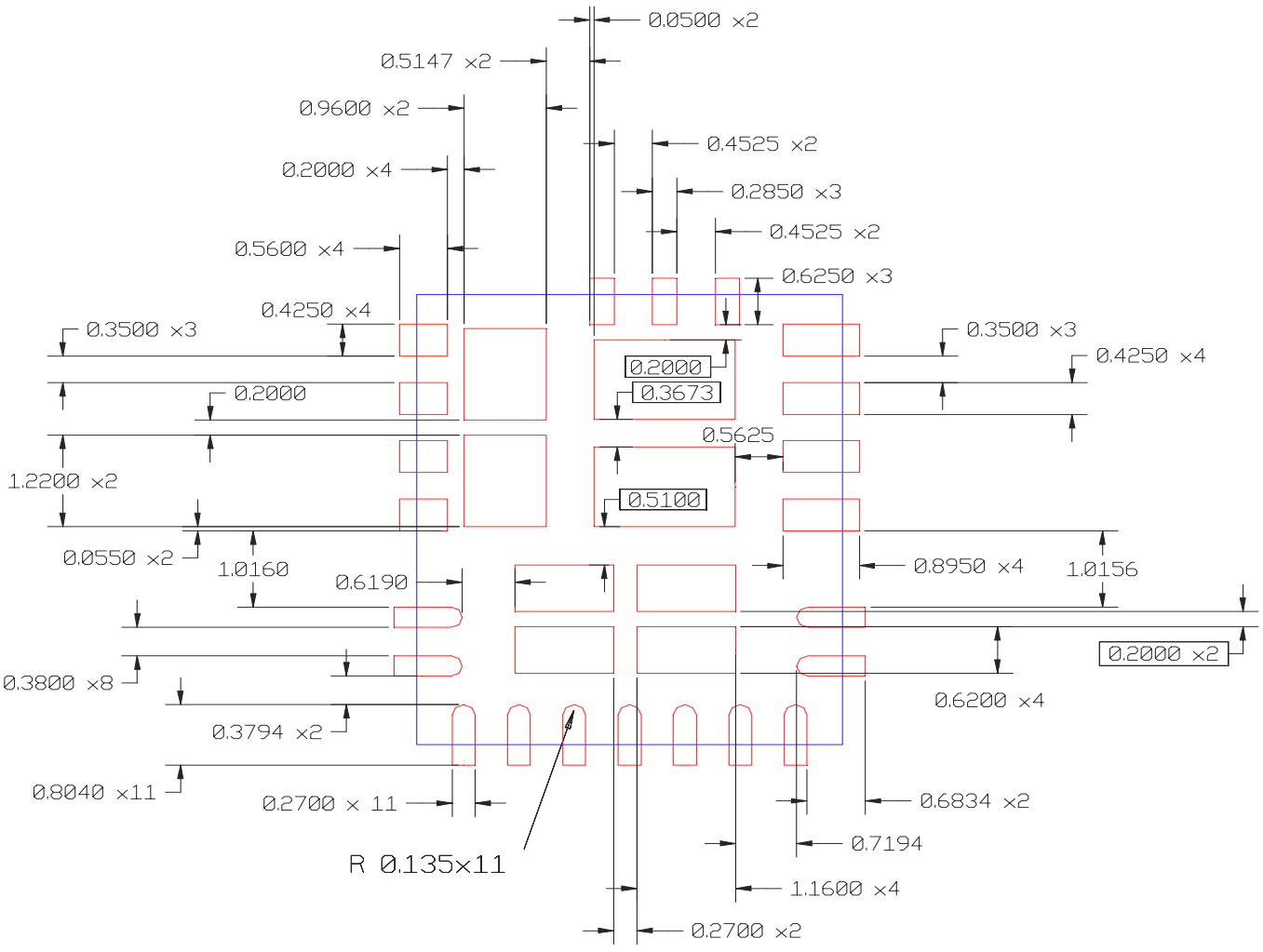
NOTE:

11x Signal Pins are NSMD

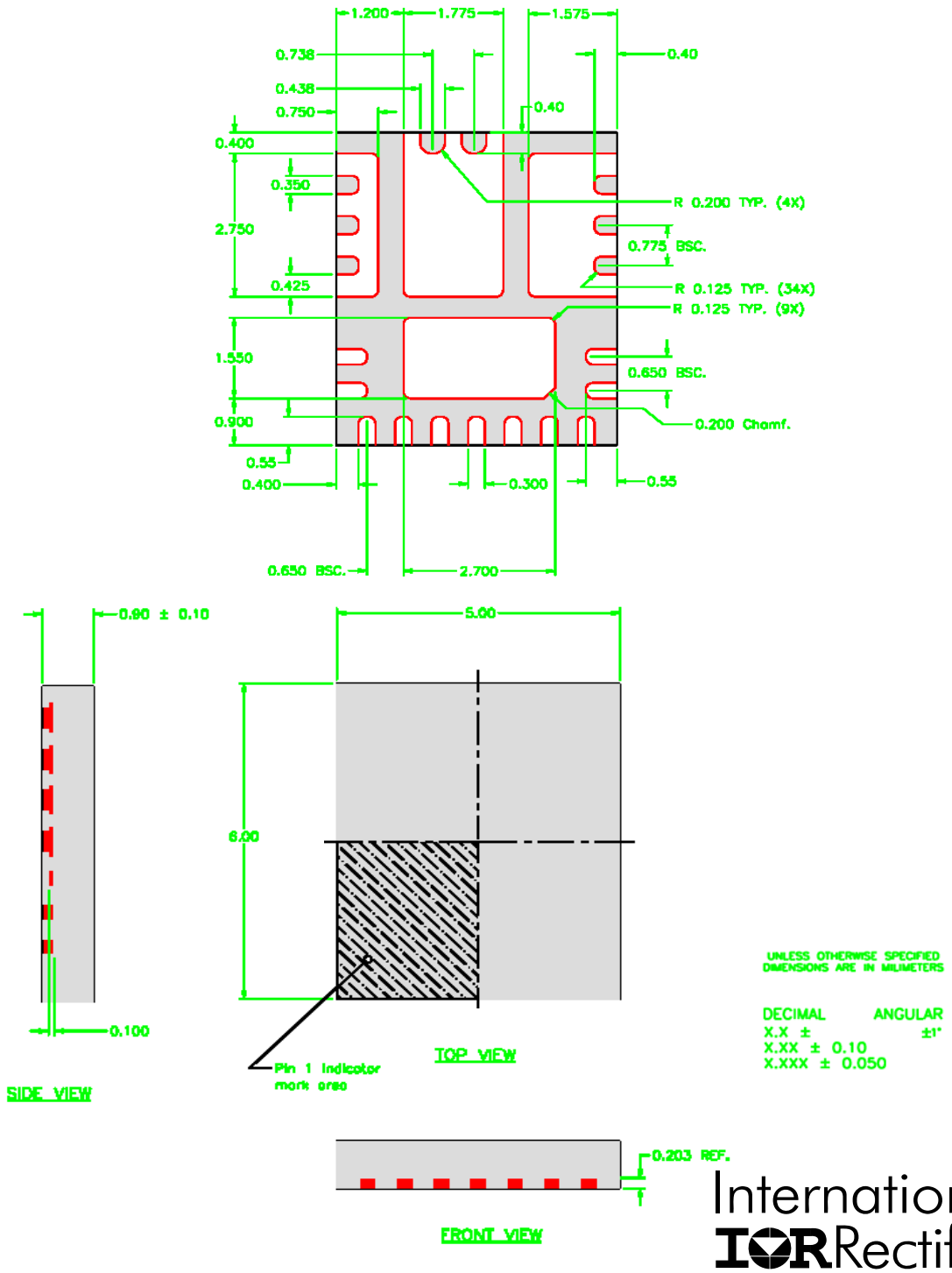
4x Power Pins are SMD

Stencil Design

- The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm



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