



Process Change Notification

PCN Number: PCN-2016-67

PCN Notification Date: 09/27/2016

Final PCN
WM0011 Assembly Relocation within SPIL

Dear Customer,

This notification is to advise you of the following change(s).

In order to ensure continuity of supply, the bumping and back-end assembly process for WM0011ECS/R is being relocated to a new SPIL factory within the same city.

There is no change to wafer probe.

If you have any questions, please contact your Sales Representative.

Sincerely,

Quality Systems Administrator
Cirrus Logic Corporate Quality
Phone: +1(512) 851-4000



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Products Affected:

The devices listed on this page are the complete list of affected devices. According to our records, these are the devices that you have purchased within the past twenty-four (24) months. The corresponding customer part number is also listed, if available.

Technical details of this Process / Product Change follow on the next page(s).

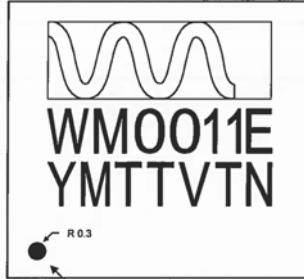
Title:		WM0011 Assembly Relocation within SPIL			
Customer Contact:		Local Field Sales Representative	Phone:	(512) 851-4000	Dept: Corporate Quality
Proposed 1st Ship Date:		Q4 2016	Estimated Sample Availability Date:		Now
Change Type:					
x	Assembly Site		Assembly Process		Assembly Materials
	Wafer Fab Site		Wafer Fab Process		Wafer Fab Materials
x	Wafer Bump Site	x	Wafer Bump Process	x	Wafer Bump Material
	Test Site		Test Process		Design
	Electrical Specification		Mechanical Specification		Part Number
	Packing/Shipping/Labeling	x	Other		
Comments:		Marking will change			

PCN Details		
Description of Change:		
Assembly location will change from CS to ZK SPIL factories, located in Taichung, Taiwan RDL thickness increasing from 5.25um to 8.25um, in line with SPIL and Cirrus Logic standard process Product marking will change, refer to details below		
Reason for Change:		
Assembly consolidation within SPIL		
Anticipated Impact on Form, Fit, Function, Quality or Reliability:		
There will be no impact to form, fit, function or reliability of the device		
Product Affected:		
Device	Cirrus Logic Part Number	Customer Part Number
1	WM0011ECS/R	

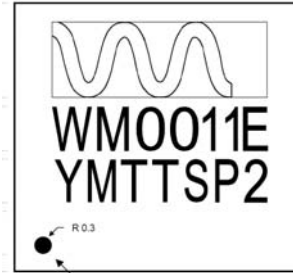
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Changes To Product Identification Resulting From This PCN:



Original Marking



New Marking

Qualification Data:

This qualification has been specifically developed for the validation of this change. The qualification data validates that the proposed change meets the applicable released technical specifications.

Qualification	Completed	June 2016	Status	PASSED
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Reliability Report

Report: Project ID 2064-0
Date: 20-April-2016
Approved by: Russell McMillan

Purpose	Status
Qualification of WM0011ECS	Qualification successful

WM0011ECS							
Fab:	TSMC, Fab 12	Assembly:	SPIIL-CS	Rev:	A	Package:	49 Ball W-CSP

Stress Name	Method	Conditions	Lot	Read Point	Results (Fail/Sample)
HTOL (High Temperature Op Life)	JESD22-A108	125°C / Dynamic Bias / VDDmax	1	1000 Hours	0 / 77
ESD HBM (Human Body Model)	JESD22-A114	25°C	1	2000 Volts	0 / 3
ESD CDM (Charged Device Model)	JESD22-C101	25°C	1	500 Volts	0 / 3
Latch-Up Over Voltage (VDD)	JESD78	85°C	1	1.5xVDDmax	0 / 3
Latch-Up Current Injection (I/O)	JESD78	85°C	1	+/- 100 mA	0 / 3

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Reliability Report: Project ID 2064-0

Date: 20-April-2016

WM0011ECS							
Fab:	TSMC, Fab 12	Assembly:	SPIL-ZK	Rev:	A	Package:	49 Ball W-CSP
Stress Name	Method	Conditions	Lot	Read Point	Results (Fail/Sample)		
Precondition	JESD22-A113	24HR 125°C Bake	1	Precon MSL1	0 / 50		
		168HR 85°C/85%RH Soak	2	Precon MSL1	0 / 50		
		3 pass 260°C peak reflow	3	Precon MSL1	0 / 50		
BHA (Highly Accelerated Temperature and Humidity Stress Test)	JESD22-A110	110°C / 85%RH / VDDmax	1	264 Hours	0 / 25		
		Post Precondition	2	264 Hours	0 / 25		
			3	264 Hours	0 / 25		
Temperature Cycle	JESD22-A104	-65 °C / +150 °C / air to air	1	500 Cycles	0 / 25		
		Post Precondition	2	500 Cycles	0 / 25		
			3	500 Cycles	0 / 25		
HTSL (High Temperature Storage Life)	JESD22-A103	150°C	1	1000 Hours	0 / 25		
			2	1000 Hours	0 / 25		
			3	1000 Hours	0 / 25		