UCD90320 32-Rail PMBus™ Power Sequencer and System Manager

1 Features

- Sequence, monitor, and margin 24 voltage rails plus 8 digital rails
- Monitor and respond to OV, UV, OC, UC, temperature, time-out, and GPI-triggered faults
- Flexible sequence-on and off dependencies, delay time, Boolean logic, and GPIO configuration to support complex sequencing aplications
- Four rail profiles for adaptive voltage identification (AVID) voltage regulator
- High-accuracy closed-loop margining
- Active trim function improves rail output voltage accuracy
- Advanced nonvolatile event logging to assist system debugging
  - Single-event fault log (100 entries)
  - Peak value log
  - Black box fault log to save status of all rails and I/O pins at the first fault
- Easily cascade up to 4 power sequencers and take coordinated fault responses
- Programmable watchdog timer and system reset
- Pin-selected rail state
- PMBus™ 1.2 compliant
- Dual-bank configurations to provide a fail-safe state when programming

2 Applications

- Wired networking
- Wireless infrastructure
- Datacom module
- Data center and enterprise computing
- Factory automation and control
- Test and measurement
- Medical

3 Description

The UCD90320 device is a 32-rail PMBus™ addressable power sequencer and system manager in a compact 0.8-mm pitch BGA package.

The 24 integrated ADC channels (AMONx) monitor the power supply voltage, current, and temperature. Of the 84 GPIO pins, 8 can be used as digital monitors (DMONx), 32 to enable the power supply (ENx), 24 for margining (MARx), 16 for logical GPO, and 32 GPIs for cascading, and system function.

The 32 ENx pins and the 16 LGPOx pins can be configured to be active driven or open drain outputs.

Nonvolatile event logging preserves fault events after power dropout. Black box fault log feature preserves the status for all rails and I/O pins when the first fault occurs. The cascading feature offers convenient ways to manage up to 128 voltage rails through one SYNC_CLK pin connection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCD90320	BGA (169)	12.0 mm × 12.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application

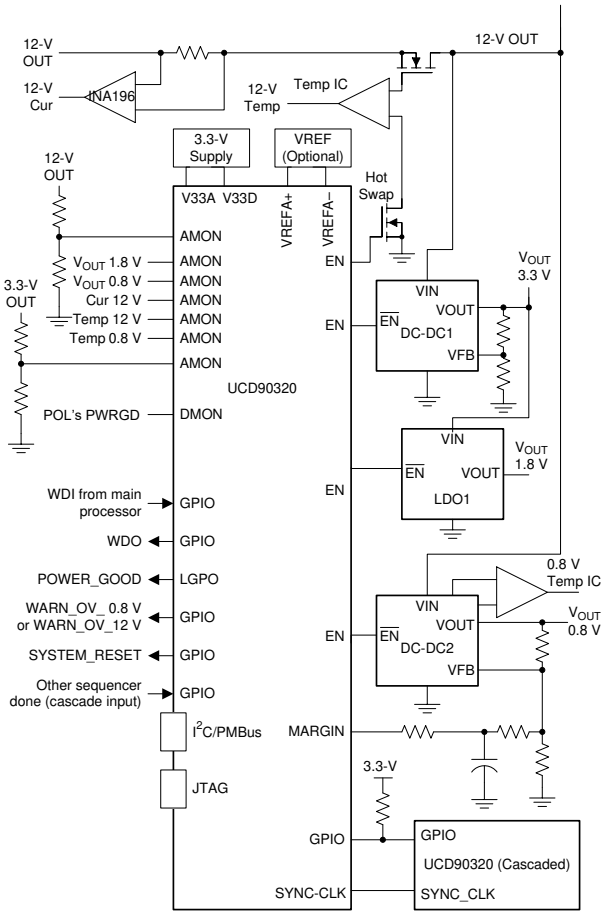


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Description (continued) ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 8
7.1 Absolute Maximum Ratings ... 8
7.2 ESD Ratings ... 8
7.3 Recommended Operating Conditions ... 8
7.4 Thermal Information ... 9
7.5 Electrical Characteristics ... 9
7.6 Non-Volatile Memory Characteristics ... 10
7.7 I^2C/PMBus Interface Timing Requirements ... 11
7.8 Typical Characteristics ... 12
8 Detailed Description ... 13
8.1 Overview ... 13
8.2 Functional Block Diagram ... 13
8.3 Feature Description ... 14
8.4 Device Functional Modes ... 15
8.5 Device Configuration and Programming ... 41
9 Application and Implementation ... 45
9.1 Application Information ... 45
9.2 Typical Application ... 45
10 Power Supply Recommendations ... 48
11 Layout ... 48
11.1 Layout Guidelines ... 48
11.2 Layout Example ... 49
12 Device and Documentation Support ... 50
12.1 Support Resources ... 50
12.2 Receiving Notification of Documentation Updates 50
12.3 Trademarks ... 50
12.4 Electrostatic Discharge Caution ... 50
12.5 Glossary ... 50
13 Mechanical, Packaging, and Orderable Information ... 50

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2019) to Revision C **Page**

- Added 'Dual-bank configurations' item to the *Features* ... 1
- Added explanation for dual-bank mechanism in *Device Configuration and Programming* section ... 41

Changes from Revision A (Septemebr 2016) to Revision B **Page**

- Changed pin D8 From: MRGN3 To: MAR3 in the pinout image ... 3
- Added I_{REF} specification to *ANALOG-TO-DIGITAL CONVERTER (ADC)* section of Electrical Characteristics ... 9
- Changed the values of V_{RESET} From: MIN = 2.85 , TYP = 3, MAX = 3.15 To: MIN = 2, TYP = 2.3, MAX = 2.6 in the *Electrical Characteristics* ... 10
- Changed 200 kΩ to 200 Ω in Figure 40 ... 47

Changes from Original (August 2016) to Revision A **Page**

- Changed data sheet status from *Product Preview* to *Production Data* ... 1

5 Description (continued)

The FAULT pin coordinates the cascaded devices to take synchronized fault responses. The pin-selected rail states feature uses up to 3 GPIs to control up to eight user-defined power states. These states can implement system low-power modes as outlined in the *Advanced Configuration and Power Interface* (ACPI) specification.

The TI Fusion Digital Power™ designer software is an intuitive PC-based graphic user interface (GUI) that can configure, store, and monitor all system operating parameters.

6 Pin Configuration and Functions

ZWS Package
169-Pin BGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	DVSS	Unused-NC	AMON6	AMON8	AMON10	AMON12	AMON22	AMON24	LGPO3	JTAG_TMS	JTAG_TDO	GPIO4	MAR15	A
B	AMON15	AMON16	AMON5	AMON7	AMON9	AMON11	AMON21	AMON23	LGPO2	JTAG_TDI	GPIO1	GPIO2	MAR16	B
C	AMON13	AMON14	AVSS	LGPO8	LGPO6	LGPO7	DVSS	LGPO4	LGPO1	JTAG_TCK	GPIO3	MAR14	MAR18	C
D	VREFA-	VREFA+	V33A	MAR5	LGPO5	BPCap	V33D	MAR3	DVSS	DMON4	MAR13	MAR17	PMBUS_DATA	D
E	AMON2	AMON1	AVSS	MAR6	DVSS	V33D	DVSS	V33D	V33D	PMBUS_CLK	PMBUS_CNTRL	MAR19	MAR20	E
F	AMON4	AMON3	DMON2	DMON1	MAR7	DVSS	DVSS	DVSS	DVSS	V33D	PMB ALERT#	EN26	EN25	F
G	AMON18	AMON17	DMON3	EN24	DVSS	DVSS	DVSS	DVSS	DVSS	____ RESET	EN27	Unused-DVSS	Unused-NC	G
H	AMON19	AMON20	EN23	EN22	DVSS	DVSS	DVSS	DVSS	DVSS	EN28	EN31	EN30	EN29	H
J	BPCap	EN20	EN21	EN19	DVSS	BPCap	V33D	DVSS	V33D	V33D	DVSS	MAR24	MAR1	J
K	PMBUS_ADDR2	SYNC_CLK	EN17	EN18	MAR10	MAR4	EN13	EN10	EN6	EN4	Unused-DVSS	Unused-V33D	BPCap	K
L	PMBUS_ADDR1	PMBUS_ADDR0	LGPO9	LGPO13	MAR2	MAR12	EN14	EN9	EN5	EN3	DMON5	MAR22	EN32	L
M	LGPO10	LGPO11	LGPO12	LGPO15	MAR23	MAR11	EN12	EN8	EN1	Unused-DVSS	DMON8	Unused-NC	MAR21	M
N	LGPO14	LGPO16	EN16	EN15	MAR8	MAR9	EN11	EN7	EN2	Unused-NC	DMON7	DMON6	Unused-DVSS	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ANALOG MONITOR PINS(1)			
AMON1	E2	I	Analog input monitor pin
AMON2	E1	I	Analog input monitor pin
AMON3	F2	I	Analog input monitor pin
AMON4	F1	I	Analog input monitor pin
AMON5	B3	I	Analog input monitor pin
AMON6	A3	I	Analog input monitor pin
AMON7	B4	I	Analog input monitor pin
AMON8	A4	I	Analog input monitor pin
AMON9	B5	I	Analog input monitor pin
AMON10	A5	I	Analog input monitor pin
AMON11	B6	I	Analog input monitor pin
AMON12	A6	I	Analog input monitor pin
AMON13	C1	I	Analog input monitor pin
AMON14	C2	I	Analog input monitor pin
AMON15	B1	I	Analog input monitor pin
AMON16	B2	I	Analog input monitor pin
AMON17	G2	I	Analog input monitor pin
AMON18	G1	I	Analog input monitor pin
AMON19	H1	I	Analog input monitor pin
AMON20	H2	I	Analog input monitor pin
AMON21	B7	I	Analog input monitor pin
AMON22	A7	I	Analog input monitor pin
AMON23	B8	I	Analog input monitor pin
AMON24	A8	I	Analog input monitor pin
ENABLE PINS			
EN1(GPIO)	M9	I/O	Digital output, rail enable signal or GPIO(2)
EN2(GPIO)	N9	I/O	Digital output, rail enable signal or GPIO
EN3(GPIO)	L10	I/O	Digital output, rail enable signal or GPIO
EN4(GPIO)	K10	I/O	Digital output, rail enable signal or GPIO
EN5(GPIO)	L9	I/O	Digital output, rail enable signal or GPIO
EN6(GPIO)	K9	I/O	Digital output, rail enable signal or GPIO
EN7(GPIO)	N8	I/O	Digital output, rail enable signal or GPIO
EN8(GPIO)	M8	I/O	Digital output, rail enable signal or GPIO
EN9(GPIO)	L8	I/O	Digital output, rail enable signal or GPIO
EN10(GPIO)	K8	I/O	Digital output, rail enable signal or GPIO
EN11(GPIO)	N7	I/O	Digital output, rail enable signal or GPIO
EN12(GPIO)	M7	I/O	Digital output, rail enable signal or GPIO
EN13(GPIO)	K7	I/O	Digital output, rail enable signal or GPIO
EN14(GPIO)	L7	I/O	Digital output, rail enable signal or GPIO
EN15(GPIO)	N4	I/O	Digital output, rail enable signal or GPIO
EN16(GPIO)	N3	I/O	Digital output, rail enable signal or GPIO
EN17(GPIO)	K3	I/O	Digital output, rail enable signal or GPIO
EN18(GPIO)	K4	I/O	Digital output, rail enable signal or GPIO
EN19(GPIO)	J4	I/O	Digital output, rail enable signal or GPIO

(1) TI recommends placing a 200-Ω resistor between analog input and monitor pins.
(2) GPIO: GPI, Command GPO, WDI, WDO, system reset ($\overline{\text{RESET}}$), FAULT pin for multiple chip cascading

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
EN20(GPIO)	J2	I/O	Digital output, rail enable signal or GPIO
EN21(GPIO)	J3	I/O	Digital output, rail enable signal or GPIO
EN22(GPIO)	H4	I/O	Digital output, rail enable signal or GPIO
EN23(GPIO)	H3	I/O	Digital output, rail enable signal or GPIO
EN24(GPIO)	G4	I/O	Digital output, rail enable signal or GPIO
EN25(GPIO)	F13	I/O	Digital output, rail enable signal or GPIO
EN26(GPIO)	F12	I/O	Digital output, rail enable signal or GPIO
EN27(GPIO)	G11	I/O	Digital output, rail enable signal or GPIO
EN28(GPIO)	H10	I/O	Digital output, rail enable signal or GPIO
EN29(GPIO)	H13	I/O	Digital output, rail enable signal or GPIO
EN30(GPIO)	H12	I/O	Digital output, rail enable signal or GPIO
EN31(GPIO)	H11	I/O	Digital output, rail enable signal or GPIO
EN32(GPIO)	L13	I/O	Digital output, rail enable signal or GPIO
CLOSED-LOOP MARGIN PINS			
MAR1(GPIO)	J13	I/O	Closed-loop margin PWM output or General GPIO
MAR2(GPIO)	L5	I/O	Closed-loop margin PWM output or General GPIO
MAR3(GPIO)	D8	I/O	Closed-loop margin PWM output or General GPIO
MAR4(GPIO)	K6	I/O	Closed-loop margin PWM output or General GPIO
MAR5(GPIO)	D4	I/O	Closed-loop margin PWM output or General GPIO
MAR6(GPIO)	E4	I/O	Closed-loop margin PWM output or General GPIO
MAR7(GPIO)	F5	I/O	Closed-loop margin PWM output or General GPIO
MAR8(GPIO)	N5	I/O	Closed-loop margin PWM output or General GPIO
MAR9(GPIO)	N6	I/O	Closed-loop margin PWM output or General GPIO
MAR10(GPIO)	K5	I/O	Closed-loop margin PWM output or General GPIO
MAR11(GPIO)	M6	I/O	Closed-loop margin PWM output or General GPIO
MAR12(GPIO)	L6	I/O	Closed-loop margin PWM output or General GPIO
MAR13(GPIO)	D11	I/O	Closed-loop margin PWM output or General GPIO
MAR14(GPIO)	C12	I/O	Closed-loop margin PWM output or General GPIO
MAR15(GPIO)	A13	I/O	Closed-loop margin PWM output or General GPIO
MAR16(GPIO)	B13	I/O	Closed-loop margin PWM output or General GPIO
MAR17(GPIO)	D12	I/O	Closed-loop margin PWM output or General GPIO
MAR18(GPIO)	C13	I/O	Closed-loop margin PWM output or General GPIO
MAR19(GPIO)	E12	I/O	Closed-loop margin PWM output or General GPIO
MAR20(GPIO)	E13	I/O	Closed-loop margin PWM output or General GPIO
MAR21(GPIO)	M13	I/O	Closed-loop margin PWM output or General GPIO
MAR22(GPIO)	L12	I/O	Closed-loop margin PWM output or General GPIO
MAR23(GPIO)	M5	I/O	Closed-loop margin PWM output or General GPIO
MAR24(GPIO)	J12	I/O	Closed-loop margin PWM output or General GPIO
GPIO AND CASCADING PINS			
DMON1(GPIO)	F4	I/O	Digital input monitor pin or GPIO
DMON2(GPIO)	F3	I/O	Digital input monitor pin or GPIO
DMON3(GPIO)	G3	I/O	Digital input monitor pin or GPIO
DMON4(GPIO)	D10	I/O	Digital input monitor pin or GPIO
DMON5(GPIO)	L11	I/O	Digital input monitor pin or GPIO
DMON6(GPIO)	N12	I/O	Digital input monitor pin or GPIO
DMON7(GPIO)	N11	I/O	Digital input monitor pin or GPIO

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DMON8(GPIO)	M11	I/O	Digital input monitor pin or GPIO
GPIO			
GPIO1	B11	I/O	GPIO
GPIO2	B12	I/O	GPIO
GPIO3	C11	I/O	GPIO
GPIO4	A12	I/O	GPIO
SYNC_CLK	K2	I/O	Synchronization clock I/O for multiple chip cascading
LOGIC GPO PINS			
LGPO1(GPIO)	C9	I/O	Logic GPO or GPIO
LGPO2(GPIO)	B9	I/O	Logic GPO or GPIO
LGPO3(GPIO)	A9	I/O	Logic GPO or GPIO
LGPO4(GPIO)	C8	I/O	Logic GPO or GPIO
LGPO5(GPIO)	D5	I/O	Logic GPO or GPIO
LGPO6(GPIO)	C5	I/O	Logic GPO or GPIO
LGPO7(GPIO)	C6	I/O	Logic GPO or GPIO
LGPO8(GPIO)	C4	I/O	Logic GPO or GPIO
LGPO9(GPIO)	L3	I/O	Logic GPO or GPIO
LGPO10(GPIO)	M1	I/O	Logic GPO or GPIO
LGPO11(GPIO)	M2	I/O	Logic GPO or GPIO
LGPO12(GPIO)	M3	I/O	Logic GPO or GPIO
LGPO13(GPIO)	L4	I/O	Logic GPO or GPIO
LGPO14(GPIO)	N1	I/O	Logic GPO or GPIO
LGPO15(GPIO)	M4	I/O	Logic GPO or GPIO
LGPO16(GPIO)	N2	I/O	Logic GPO or GPIO
PMBus COMM INTERFACE			
PMBUS_CLK	E10	I	PMBus clock (must pull up to V33D)
PMBUS_DATA	D13	I/O	PMBus data (must pull up to V33D)
$\overline{\text{PMBALERT}}$	F11	O	PMBus alert, active-low, open-drain output (must pull up to V33D)
PMBUS_CNTRL	E11	I	PMBus control pin
PMBUS_ADDR0	L2	I	PMBus digital address input. Bit 0
PMBUS_ADDR1	L1	I	PMBus digital address input. Bit 1
PMBUS_ADDR2	K1	I	PMBus digital address input. Bit 2
JTAG			
JTAG_TMS	A10	I	Test mode select with internal pull-up
JTAG_TCK	C10	I	Test clock with internal pull-up
JTAG_TDO	A11	O	Test data out with internal pull-up
JTAG_TDI	B10	I	Test data in with internal pull-up
INPUT POWER, GROUND, AND EXTERNAL REFERENCE PINS			
$\overline{\text{RESET}}$	G10	I	Active-low device reset input. Pull up to V33D.
V33A	D3	I	Analog 3.3-V supply. Decouple from V33D to minimize the electrical noise contained on V33D from affecting the analog functions.
V33D	D7, E6, E8, E9, F10, J7, J9, J10	I	Digital 3.3-V supply for I/O and some logic.
BPCap	D6, J1, J6, K13	I	Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The BPCap pins should only be connected to each other and an external capacitor as specified in *On-Chip Low Drop-Out (LDO) Regulator* section of the Electrical Characteristics table.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
AVSS	C3, E3	I	Analog ground. These are separated from DVSS to minimize the electrical noise contained on V33D from affecting the analog functions.
DVSS	A1, C7, D9, E5, F9, H5, H9, J5, J8, J11, H6, H7, H8, G5, G6, G7, G8, G9, F6, F7, F8, E7	I	Ground reference for logic and I/O pins.
VREFA+	D2	I	(Optional) positive node of external reference voltage
VREFA-	D1	I	(Optional) negative node of external reference voltage
UNUSED PINS			
UNUSED-NC	A2, G13, M12, N10	–	Do not connect. Leave floating or isolated.
UNUSED-DVSS	G12, K11, M10, N13	–	Tie to DVSS.
UNUSED-V33D	K12	–	Tie to V33D.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V33D to DVSS	0	4	V
	V33A to AVSS	0	4	V
Input voltage	on all I/O pins except PMBUS_CNTRL, $\overline{\text{PMBALERT}}$, MARGIN19, and MARGIN20, regardless of whether the device is powered(2)	–0.3	5.5	V
	PMBUS_CNTRL, $\overline{\text{PMBALERT}}$, MARGIN19, and MARGIN20	–0.3	V_{V33D} + 0.3	V
Output current	Maximum current per output pin		25	mA
Operating junction temperature, T_J		TBD	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those listed in the *Recommended Operating Conditions* table. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Applies to static and dynamic signals including overshoot.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{V33D}	Supply input voltage	3.15	3.3	3.63	V
V_{V33A}(1)		2.97	3.3	3.63	V
T_A	Operating ambient temperature	–40		85	°C
T_C	Operating case temperature	–40		90	°C
T_J	Operating junction temperature	–40		93	°C

(1) It is recommended to connect the V33A pin and the V33D pin to the same supply. V33A must be powered before V33D if sourced from different supplies. There is no restriction on the ordering sequence for powering off.

7.4 Thermal Information

THERMAL METRIC[1]		UCD90320 ZWS (BGA) 169 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2][3]	41.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[2]	15.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance[2][4][5]	18.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter[6]	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter[4]	20.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Junction to ambient thermal resistance (θ_{JA}), junction to board thermal resistance (θ_{JB}), and junction to case thermal resistance (θ_{JC}) numbers are determined by a package simulator.
(3) $T_J = T_A + (P \times \theta_{JA})$
(4) $T_J = T_{PCB} + (P \times \Psi_{JB})$
(5) $T_J = T_B + (P \times \theta_{JB})$()
(6) $T_J = T_C + (P \times \Psi_{JT})$

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{V33}	Supply Current	$V_{V33D} = V_{V33A} = 3.3$ V		31.4	54.9	mA
ON-CHIP LOW DROP-OUT (LDO) REGULATOR						
C_{LDO}	External filter capacitor size for internal power supply[1]		2.5		4	µF
V_{LDO}	LDO output voltage		1.08	1.2	1.32	V
I_{INRUSH}	Inrush current		50		250	mA
ANALOG-TO-DIGITAL CONVERTER (ADC)[2][3]						
V33A	ADC supply voltage		2.97	3.3	3.63	V
AVSS	ADC ground voltage			0		V
C_{V33A}	Voltage reference decoupling capacitance between V33A and AVSS (if using internal reference) [4]			1.01		µF
V_{REFA+}	Positive external voltage reference on VREFA+ pin		2.4		3	V
V_{REF-}	Negative external voltage reference on VREF– pin		V_{AVSS}	AVSS	0.3	V
I_{REF}	Current on VREF+ pin input	External $V_{REF+} = 3.3$ V		330.5	440	µA
C_{REF}	Voltage reference decoupling capacitance between VREFA+ and VREFA– (if using external reference)[4]			1.01		µF
V_{ADCIN}	Analog input range, internal reference[5]		0		V33A	V
	Analog input range, external reference[6]		V_{VREFA-}		V_{VREFA+}	
I_L	ADC input leakage current				2	µA
R_{ADC}	ADC equivalent input resistance				2.5	kΩ
C_{ADC}	ADC equivalent input capacitance				10	pF

(1) Connect the capacitor as close as possible to pin D6.
(2) Total of two ADC channels run independently during normal operation.
(3) Total unadjusted error is the maximum error at any one code versus the ideal ADC curve. It includes offset error, gain error, and INL at any given ADC code.
(4) Two capacitors (1.0 µF and 0.01 µF) connected in parallel.
(5) Internal reference is connected directly between V33A and AVSS.
(6) External reference noise level must be under 12 bit (–74 dB) of full scale input, over input bandwidth, measured at VREFA+ - VREFA–.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{CONV}	ADC conversion rate (on each ADC channel)(1)			1		MSPS
N	ADC resolution			12		bits
E_T	Total unadjusted error, over full input rangea when using internal reference			±10	±30	LSB
	Total unadjusted error, over full input range when using external reference			±2.5	±4	
DIGITAL INPUTS AND OUTPUTS (GPIO, Logic GPO, EN, AND MARGIN PINS)						
V_{IH}	I/O high-level input voltage(7)		0.65 × V_{V33D}		5.5	V
V_{IL}	I/O low-level input voltage		0		0.35 × V_{V33D}	V
V_{HYS}	I/O input hysteresis		0.2			V
V_{OH}	I/O high-level output voltage		2.4			V
V_{OL}	I/O low-level output voltage				0.4	V
I_{OH}	High-level source current	V_{OH} = 2.4 V(8)	4			mA
I_{OL}	Low-level sink current	V_{OL} = 0.4 V(8)	4			mA
RESET AND BROWNOUT						
V33DSlew	Minimum V33D slew rate between 2.8 V and 3.2 V		0.1			V/ms
V_{RESET}	Supply voltage at which device comes out of reset		2	2.3	2.6	V
V_{BOR}	Supply voltage at which device enters brownout		2.93	3.02	3.11	V
V_{SHDN}	Supply voltage at which device shuts down		2.7	2.78	2.87	V
t_{RESET}	Minimum low-pulse width needed at $\overline{\text{RESET}}$ pin			250		ns
t_{IRT}	Internal reset time(9)			9	11.5	ms

(7) PMBUS_CNTRL, $\overline{\text{PMBALERT}}$, MARGIN19 and MARGIN20 pins have V_{V33D} + 0.3 V as maximum input voltage rating.
(8) I_O specifications reflect the maximum current where the corresponding output voltage meets the V_{OH}/V_{OL} thresholds.
(9) If power-loss or brown-out event occurs during an EEPROM program or erase operation, and EEPROM needs to be repaired (which is a rare case), the internal reset time may be longer.

7.6 Non-Volatile Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONFIGURATION FLASH MEMORY						
PE_{CYC}	Number of program and erase cycles before failure		100,000			Cycles
T_{RET}	Data retention	–40°C ≤ T_J ≤ 85°C	20			Years
FAULT AND EVENT LOGGING EEPROM						
EPE_{CYC}	Number of mass program and erase cycles of a single word before failure		500,000			Cycles
ET_{RET}	Data retention	–40°C ≤ T_J ≤ 85°C	20			Years

7.7 I²C/PMBus Interface Timing Requirements

			MIN	NOM	MAX	UNIT
I1	$t_{(HD:STA)}$	Start condition hold time	450			ns
I2	$t_{(LOW)}$	Clock low period (1)	450			ns
I3	t_r	Clock rise time and data rise time (2)			See (2)	ns
I4	$t_{(HD:DAT)}$	Data hold time		25		ns
I5	t_f	Clock fall time and data fall time (3)		112.5	125	ns
I6	$t_{(HIGH)}$	Clock high time	300			ns
I7	$t_{(SU:DAT)}$	Data setup time	225			ns
I8	$t_{(SU:STA)}$	Start condition setup time (repeated start only)	450			ns
I9	$t_{(SU:STO)}$	Stop condition setup time	300			ns
I10	$t_{(DV)}$	Data valid		25		ns

(1) PMBus host must support clock stretching per *PMBus Power System Management Protocol Specification Part I General Requirements, Transport and Electrical Interface,* Revision 1.2, Section 5.2.6.
(2) Because the I2CSCL signal and the I2CSDA signal operate as open-drain-type signals, which the controller can actively drive only "Low", the time that either signal takes to reach a high level depends on external signal capacitance and pull-up resistor values.
(3) Specified at a nominal 50-pF load.

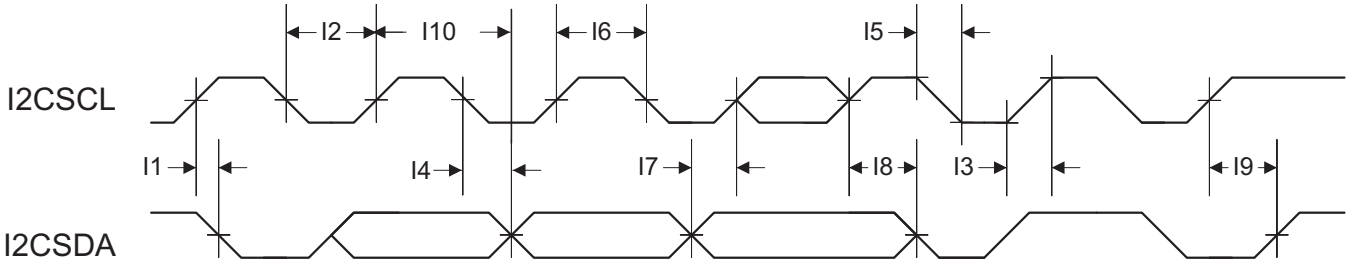


Figure 1. I²C/PMBus Timing Diagram

7.8 Typical Characteristics

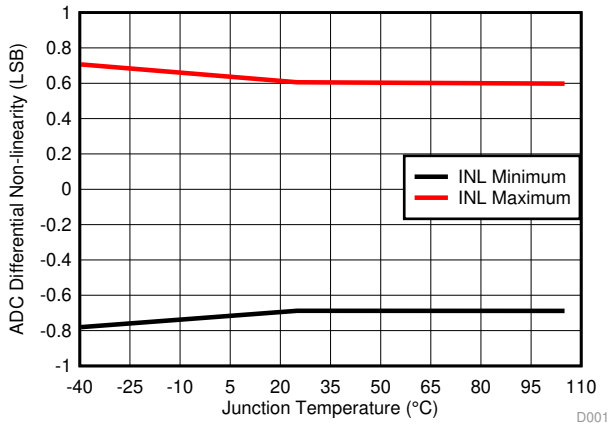


Figure 2.

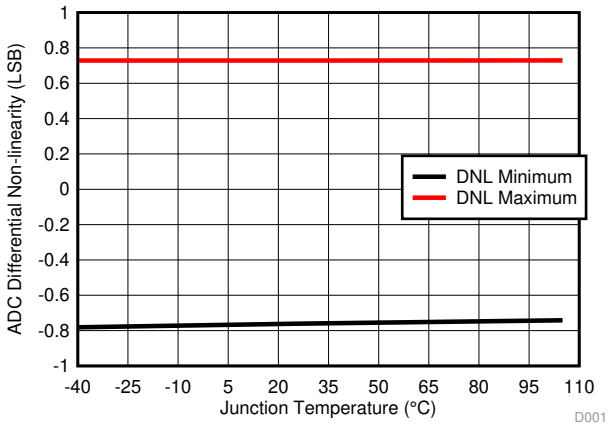


Figure 3.

8 Detailed Description

8.1 Overview

Electronic systems such as CPU, DSP, microcontroller, FPGA, and ASIC can have multiple voltage rails and require certain power-ON and power-OFF sequences in order to function correctly. The UCD90320 device can control up to 32 voltage rails and ensure correct power sequences during normal condition and fault conditions.

In addition to sequencing, the device can continuously monitor rail voltages, currents, temperatures, fault conditions, and report the system health information to upper computers through a PMBus interface, improving long term reliability.

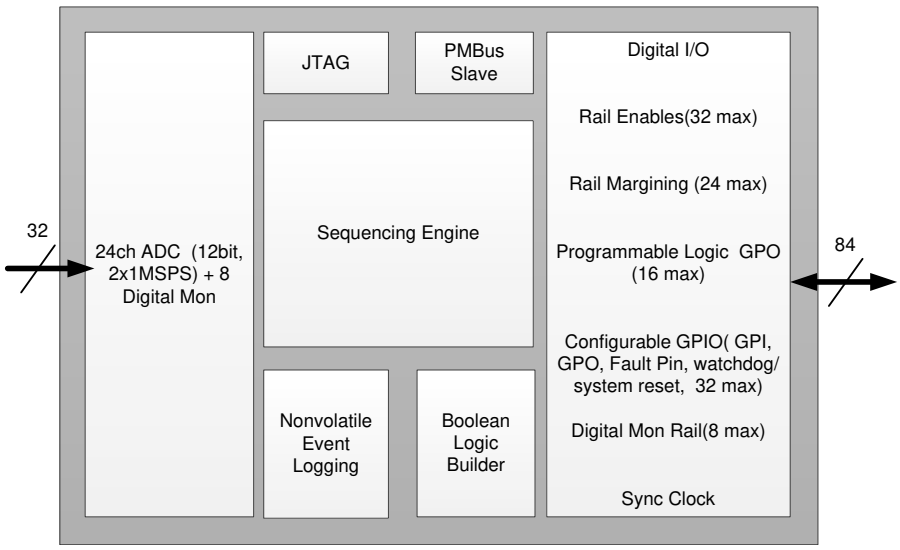
The device can protect electronic systems by responding to power system faults. The fault responses are conveniently configured by users through *Fusion Digital Power Designer* software. Fault events are stored in on-chip nonvolatile flash memory in order to assist failure analysis. A Black Box Fault Log feature stores comprehensive system statuses at the moment when the first fault occurs. With this feature, failure analysis can be more effective.

System reliability can be improved through four-corner testing during system verification. During four-corner testing, each voltage rail is required to operate at the minimum and maximum output voltages, commonly known as margining. The device can perform accurate closed-loop margining for up to 24 voltage rails. During normal operation, UCD90320 can also actively trim DC output voltages using the same margining circuitry. This feature allows tuning rail voltages to an optimal level.

The UCD90320 device supports control environments through both PMBus interface and pin-based interface. The device functions as a PMBus slave. It can communicate with upper computers with PMBus commands, and control voltage rails accordingly. In addition to rail enable (EN) pins, up to 32 GPIO pins can be configured as GPOs and directly controlled by PMBus commands. The device can be controlled by up to 32 GPIO configured GPI pins. The GPIs can be used as fault inputs which can shut down rails. The GPIs can be also used as Boolean logic input to control the 16 Logic GPO outputs. Each of the 16 Logic GPO pins has a flexible Boolean logic builder. Input signals of the Boolean logic builder can include GPIs, other GPOs, and selectable system flags such as POWER_GOOD, faults, warnings, and so forth. A simple state machine is also available for each Logic GPO pin.

The device provides additional features such as cascading, pin-selected states, system watchdog, system reset, run time clock, peak value log, reset counter, and so forth. Cascading feature offers convenient ways to cascade up to four UCD90320 devices and manage up to 128 voltage rails through one SYNC_CLK pin connection. Pin-selected states feature allows users to define up to 8 rail states. These states can implement system low-power modes as set out in the *Advanced Configuration and Power Interface (ACPI)* specification. The *Feature Description* of this datasheet describes other device features.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 TI *Fusion Digital Power Designer* Software

The Texas Instruments Fusion Digital Power Designer software allows the user to configure the device. This PC-based graphic user interface (GUI) offers an intuitive I^2C and PMBus interface to the device. The *Fusion Digital Power Designer* software allows the design engineer to configure the system operating parameters for the application without directly using PMBus commands, store the configuration to on-chip nonvolatile memory, and observe system status (voltage, current, temperature, faults, and so forth). This data sheet references the Fusion Digital Power Designer software is as *Fusion Digital Power Designer* software and many sections include screenshots. Download the *Fusion Digital Power Designer* software from TI here. After configuration, the device can perform all designed functions independently without further need for the Fusion GUI.

8.3.2 PMBUS Interface

PMBus refers to a serial interface specifically designed to support power management. The PMBus interface is based on the SMBus interface that is built on the I^2C physical specification. The UCD90320 device supports revision 1.2 of the PMBus standard. Wherever possible, standard PMBus interface commands support the function of the device. Unique features of the device are defined to configure or activate via the MFR_SPECIFIC commands. These commands are defined in the *UCD90320 Sequencer and System Health Controller PMBUS Command Reference*. The most current UCD90320 PMBus Command Reference can be found within the TI Fusion Digital Power Designer software through the Help Menu *(Help, Documentation & Help Center, Sequencers tab, Documentation* section).

This data sheet makes frequent mention of the PMBus specification. Specifically, this document is *PMBus Power System Management Protocol Specification Part II – Command Language*, Revision 1.2, dated 6 September 2010. The specification is published by the Power Management Bus Implementers Forum and is available from www.pmbus.org.

The UCD90320 device meets all of the requirements of the *Compliance* section of the PMBus specification. The firmware complies with the SMBus 1.2 specification, including support for the SMBus ALERT function. The hardware supports either 100-kHz or 400-kHz PMBus operation.

8.3.3 Rail Setup

Power rails are defined under the **Pin Assignment** tab, as shown in Figure 4. Click corresponding buttons to add or delete a rail. After a rail is added, AMON, DMON, EN, and MARGIN pins can be assigned to the rail. UCD90320 has 24 AMON pins, 8 DMON pins, 32 EN pins, and 24 MARGIN pins, thus can support up to 32 rails.

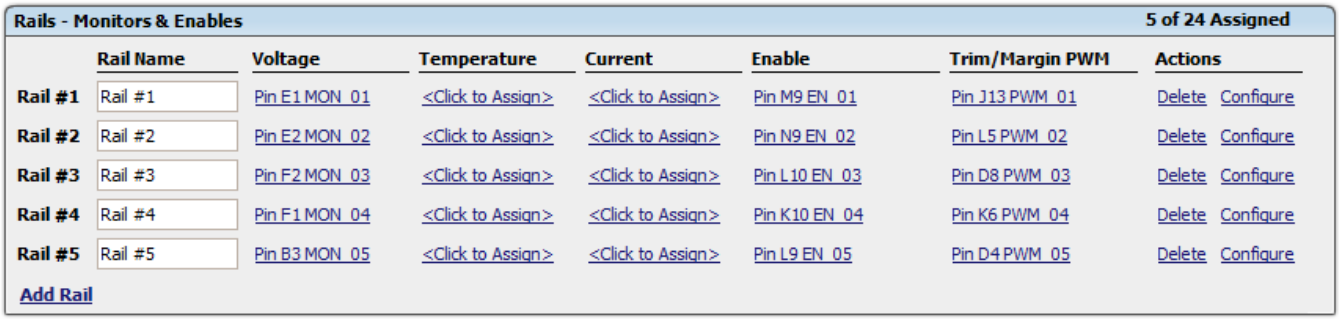


Figure 4. *Fusion Digital Power Designer* Software Rail Setup Window (Configure ►Pin Assignment Tab)

8.4 Device Functional Modes

8.4.1 Rail Monitoring Configuration

After rails are set up in the **Pin Assignment** tab, they are visible under the **Vout Config** tab, as shown in Figure 5. The initial voltage values are 0.

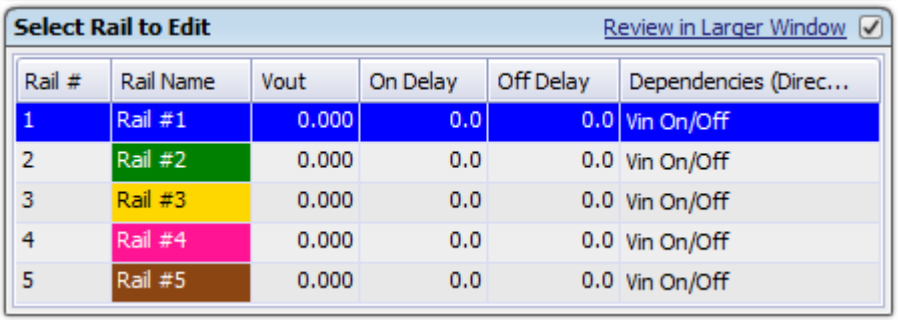


Figure 5. Rail Selection Window (Rail Configuration)

Configure the voltage monitoring parameters of the selected rail under the **Vout Config** tab. Figure 6 shows the configuration window.

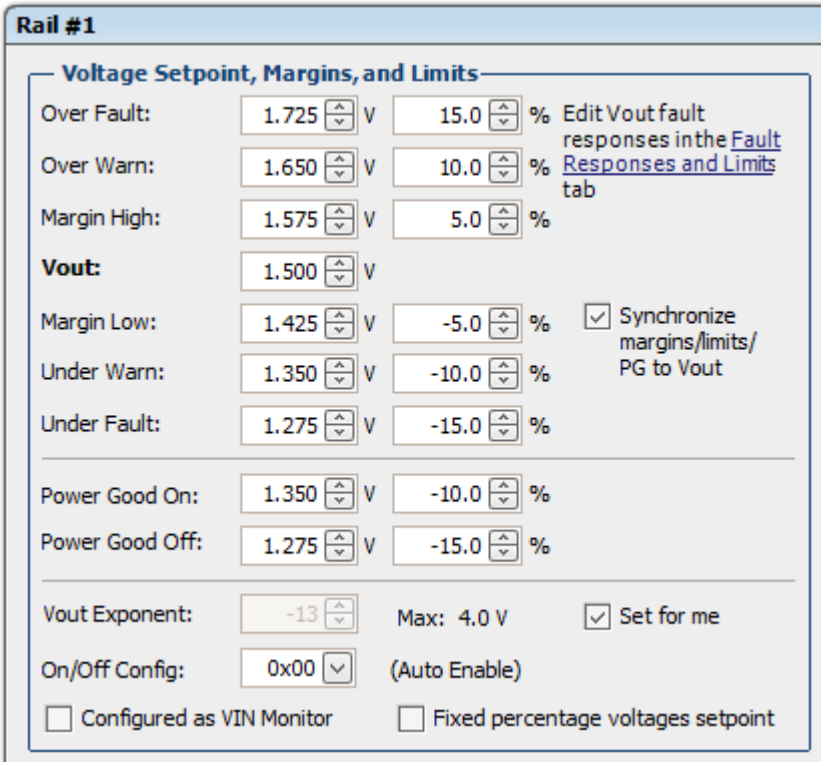


Figure 6. Rail Voltage Configuration Window (Rail Configure, Vout Config Tab)

When a AMON pin is assigned in Figure 4 to monitor the voltage of a particular a rail, a fault or warn event occurs when the monitored rail voltage exceeds the voltage window defined by the *Over and Under Warn/Fault* thresholds. When a fault is detected, the device responds with user-defined actions. See the *Fault Responses Configuration* section for more details.

Rail Profile is composed of a group of nine thresholds set by the following:

- VOUT_COMMAND

Device Functional Modes (continued)

- VOUT_OV_FAULT_LIMIT
- VOUT_OV_WARNING_LIMIT
- VOUT_OV_MARGIN_HIGH
- POWER_GOOD_ON
- VOUT_MARGIN_LOW
- POWER_GOOD_OFF
- VOUT_UV_WARNING_LIMIT
- VOUT_UV_FAULT_LIMIT

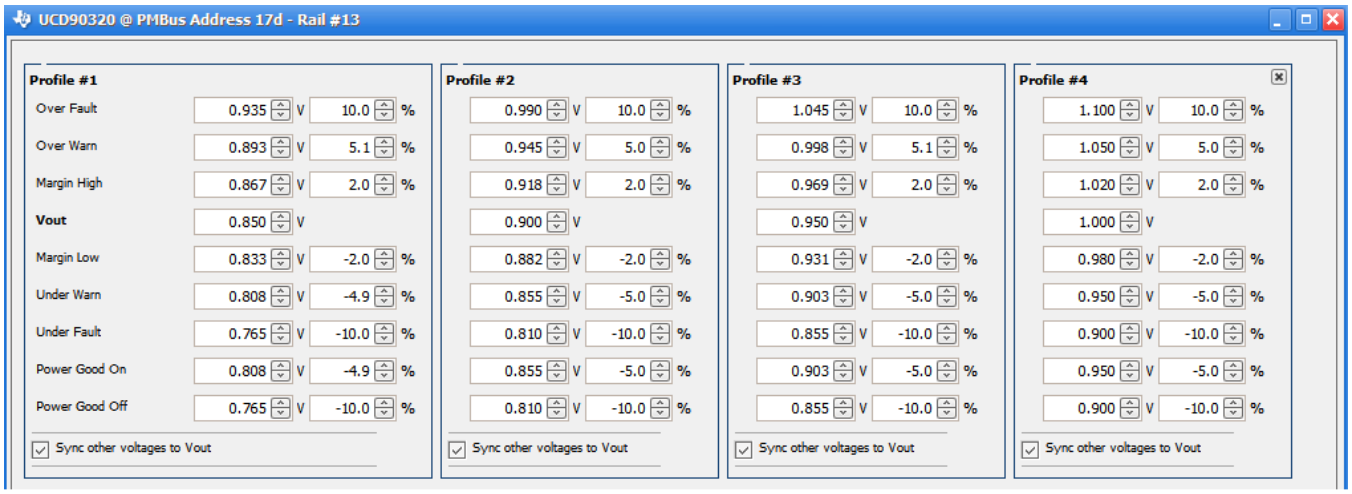
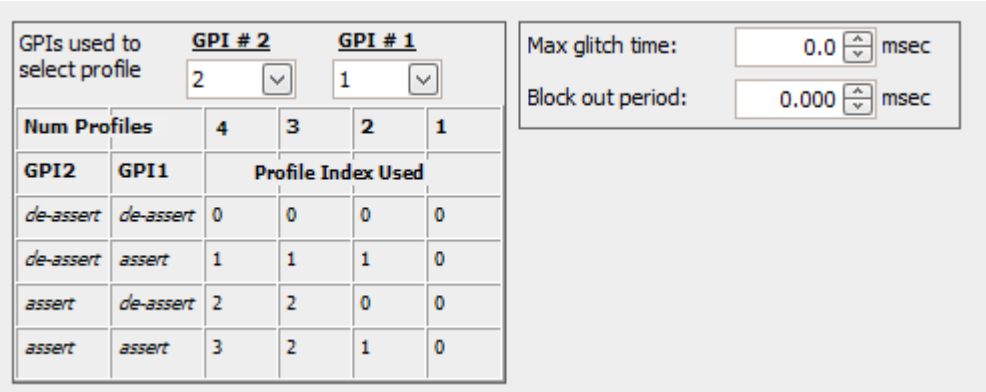


Figure 7. Rail Profile Configurations (Rail Config ► Edit Rail Profiles)

The device offers 50 individual profiles shared among all 24 AMON voltage rails. Each AMON voltage rail can have at least one but no more than four profiles. The profiles are controlled by 2 GPIs as shown in Figure 8. A programmable block-out period is used to block all voltage related faults on the given rail when profile is changed.



Num Profiles		4	3	2	1
GPI2	GPI1	Profile Index Used			
de-assert	*de-assert*	0	0	0	0
de-assert	*assert*	1	1	1	0
assert	*de-assert*	2	2	0	0
assert	*assert*	3	2	1	0

Figure 8. Rails Profile Selection Through GPIs (Rail Config ► Edit Rail Profiles)

The device supports digital monitor. If a DMON pin is assigned in Figure 7 to monitor POWER_GOOD of POL, the DMON rail has no rail profile. If the DMON input is logic HIGH, the rail is POWER_GOOD, otherwise the rails has UV fault or warns and is at POWER_NOT_GOOD.

Device Functional Modes (continued)

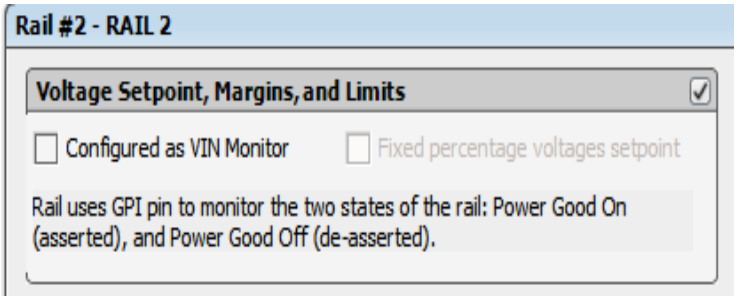


Figure 9. Digital Rail Configuration Window

Vout Exponent defines the voltage value resolution according to PMBus linear data format. *Fusion Digital Power Designer* software can automatically select optimal *Vout Exponent* value to cover the required voltage range with the finest possible resolution. For more information regarding PMBus linear data format, refer to PMBus specification mentioned at the beginning of this section.

On/Off Config defines a rail turn-ON and turn-OFF command:

- None (Auto enable). Rail always seeks to turn-ON as long as UCD90320 is powered.
- CONTROL Pin Only. Rail seeks to turn-ON and turn-OFF according to PMBus CONTROL line (asserted/de-asserted).
- OPERATION Only. Rail seeks to turn-ON and turn-OFF according to PMBus OPERATION command (On/Off).
- Both CONTROL pin and OPERATION. Rail seeks to turn-ON when CONTROL pin is asserted, AND PMBus OPERATION command sets the rail to On. Rail seeks to turn-OFF when OPERATION command sets the rail to OFF, OR when CONTROL line is de-asserted.

After receiving a turn ON or turn OFF command, a rail examines a series of conditions before asserting or de-asserting its EN pin. Conditions include *Rail Sequence On/Off Dependency*, *GPI Sequence On/Off Dependency*, *Turn-On/Off Delay*, as shown in *Rail Sequence Configuration* section.

Fixed percentage voltages setpoint, when checked, configures a rail into adaptive voltage scaling technology (AVS) mode. The *Vout Setpoint* can be dynamically set by PMBus during operation in order to achieve energy saving. The rail warn and fault voltage thresholds maintain fixed ratios with respect to the *Vout Setpoint*. Due to the fact that the power supply and UCD90320 device may not change *Vout Setpoint* simultaneously or with the same slew rate, the device takes the following steps to avoid false-triggering warn and fault. If the new *Vout Setpoint* is higher than the current *Vout Setpoint*, the OV warn and fault thresholds are immediately set to their respective new levels. Other thresholds are initially maintained, and then increase by 20-mV step size in every 400 µs until the new levels are reached. If the new *Vout Setpoint* is lower than the current *Vout Setpoint*, the UV warn and fault and Power Good On and Power Good Off thresholds are immediately set to their respective new levels. Other thresholds are initially maintained, and then decrease by 20-mV step size every 400 µs until the new levels are reached. Table 1 summarizes the thresholds adjustment scheme in AVS mode. This feature is not available for DMON pin.

Table 1. Thresholds Adjustment Scheme in AVS Mode

TRANSITION	IMMEDIATE UPDATE	ADJUSTMENT(1)
New *Vout Setpoint* to Current *Vout Setpoint*	OV fault and warn notification	UV fault and warn notification, Margin High and Margin Low, Power Good On and Power Good Off
	UV fault and warn notification, Power Good On and Power Good Off	OV fault and warn notification, Margin High and Margin Low

(1) Gradual adjustment towards new levels with 2-0mV step size and 400-µs step interval

Current and temperature monitoring parameters of the selected rail can be configured under the **Fault Responses and Limits** tab. First, select a rail in the top-right corner of the *Fusion Digital Power Designer* software, then edit the current and temperature monitoring parameters as shown in Figure 10.

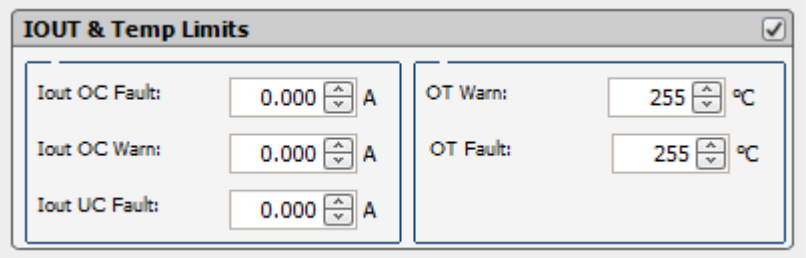


Figure 10. Current and Temperature Limits Configuration Window (Rail Config ► IOUT and Temperature Limits)

Each rail has a Power Good status determined by the following rules.

- If rail voltage is monitored by an AMON pin, the *Power Good* status is solely determined by *Power Good On and Power Good Off* thresholds as shown in Figure 6. A rail is given *Power Good* status if its rail voltage is above the *Power Good On* threshold. Otherwise, the rail is given *Not Power Good* status if the rail voltage is below the *Power Good Off* threshold. The rail remains in the current status if its voltage is neither above *Power Good On* nor below *Power Good Off* thresholds.
- If rail voltage is not monitored by a AMON or DMON pin, the *Power Good* status is determined by the turn-ON and turn-OFF eligibility of the rail. A rail is immediately given *Power Good* status when the rail meets all the turn-on conditions set by the user, such as *On and Off Config*, dependencies and delays. Similarly, a rail is immediately given *Not Power Good* status when the rail meets all the turnoff conditions set by the user. The behavior is the same regardless whether a physical EN pin is assigned to the rail.

The *Power Good* status is not affected by any warnings and faults unless the fault response is to turn OFF the rail.

UV fault and warn notification is ignored when a rail is off. UV fault and warn notification is also ignored during start up until the rail enters *Power Good* status for the first time. This mechanism avoids false-triggering UV fault and warn notification when the rail voltage is expected to be below UV thresholds.

A *Graceful Shutdown* feature is enabled by checking the *Configured as VIN Monitor* checkbox. When enabled, the rail is configured to monitor VIN. When VIN drops below *Power Good Off* threshold, the device ignores any UV fault and warn notifications on any other rail.

8.4.2 GPI Configuration

Up to 32 of the 84 GPIO pins of the UCD90320 device can be configured as GPI. The GPI configuration window is under the **Pin Assignment** tab. Figure 11 shows an example.

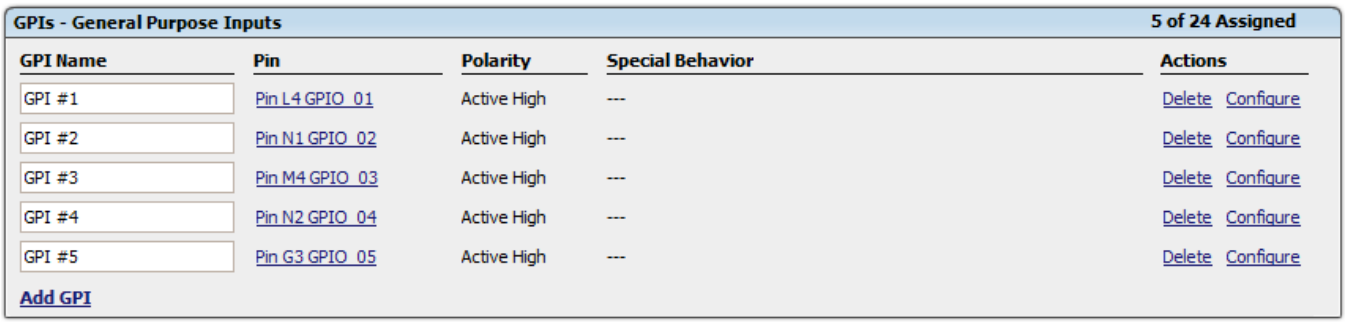


Figure 11. GPI Configuration Window (Hard Configuration ► Monitors and GPIO Pins Assignment)

The polarity of GPI pins can be configured to be either active high or active low. Each GPI can be used as a source of sequence dependency (see the *Rail Sequence Configuration* section). The GPI pins can be also used for cascading function (see the *Cascading Multiple Devices* section). The first defined three GPIs regardless of their main purpose are assigned to the pin selected states function (see the *Pin Selected Rail States Configuration* section).

In addition to hard configuration functions, four special behaviors can be assigned to each GPI pin using the dropdown window shown in Figure 12:

- **GPI Fault**: The de-assertion of this pin is treated as a fault, which can trigger shutdown actions for any voltage rails (see the *Fault Responses Configuration* section).
- **Latched Statuses Clear Source**: This pin can be used to clear latched-type statuses (_LATCH) (see the *GPO Configuration* section).
- **Input Source for Margin Enable**: When this pin is asserted, all rails with margining enabled enter into a margined state (low or high). This special behavior can be assigned to only one GPI.
- **Input Source for Margin Low and Not-High**: When this pin is asserted, all margined rails are set to Margin Low as long as the Margin Enable is asserted. When this pin is de-asserted the rails are set to Margin High as long as the Margin Enable is asserted. This special behavior can be assigned to only one GPI.
- **Configured as Debug Pin**: When the pin is asserted, the device does not alert the $\overline{\text{PMBALERT}}$ pin, and neither responds to, nor logs, any faults as defined in Table 2. The device ignores the rail sequence ON and OFF dependency conditions. As soon as the sequence ON and OFF timeout expires, the rails are sequenced ON or OFF accordingly regardless of the timeout action. If the sequence ON or OFF timeout value is set to 0, the rails are sequenced ON or OFF immediately. The fault pins do not pull the fault bus low. LGPOs affected by these events return to the original states.
- **Configured as Fault Pin**: GPI fault enable functionality must be set to enable this feature. When set, if there is no fault on a fault bus. The FAULT pin is digital input pin and it monitors the fault bus. When one or more UCD90329 devices detect a rail fault, the corresponding FAULT pin is turned into active driven low state, pulling down the fault bus voltage and informing all other UCD90320 devices of the corresponding fault. This behavior allows a coordinated action to be taken across multiple devices. After the fault is cleared, the state of the FAULT pin reverts to that of an input pin (see the *Cascading Multiple Devices* section).

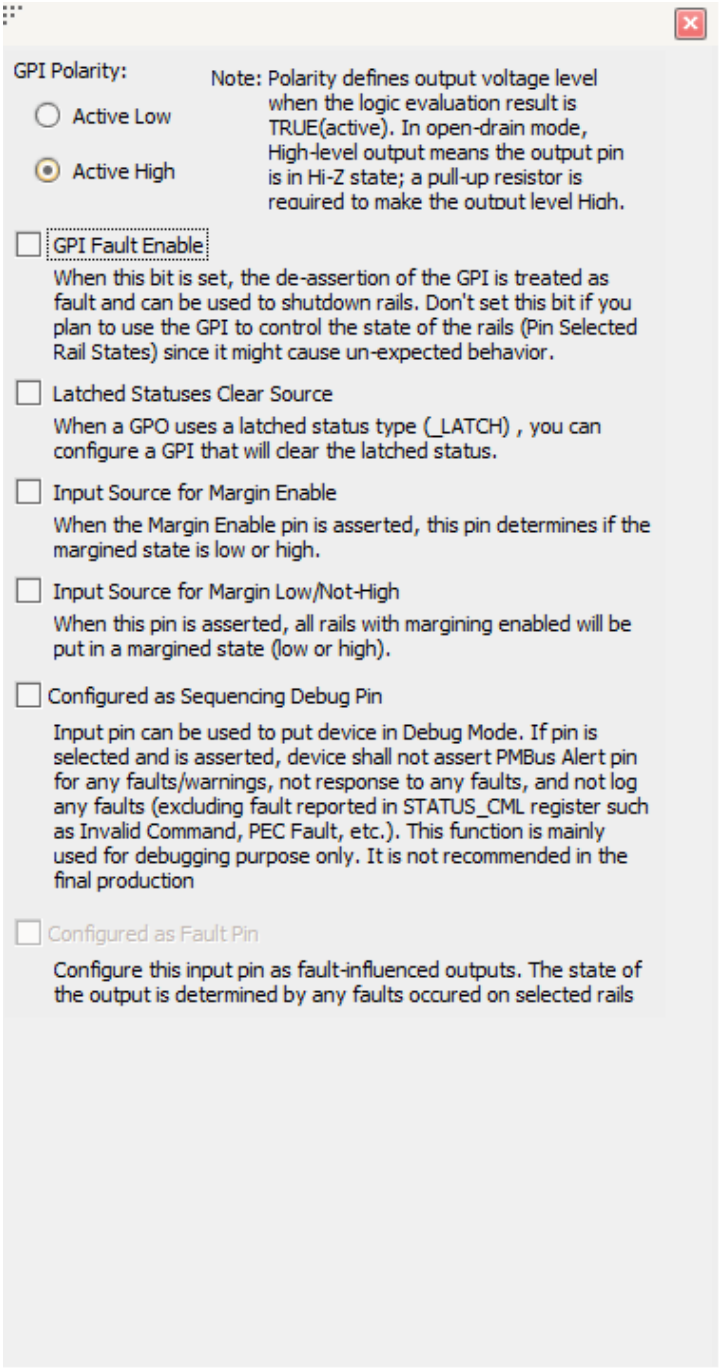


Figure 12. GPI Configuration Dropdown Window (Hardware Configuration ► Monitor and GPIO Pins Assignment)

Table 2. List of Events Affected by Debug Mode

EVENTS	DESCRIPTION
VOUT_OV_FAULT	Voltage rail is over OV fault threshold
VOUT_OV_WARNING	Voltage rail is over OV warning threshold
VOUT_UV_FAULT	Voltage rail is under UV fault threshold
VOUT_UV_WARNING	Voltage rail is under UV warning threshold
TON_MAX	Voltage rail fails to reach power good threshold in predefined period.
TOFF_MAX Warning	Voltage rail fails to reach power not good threshold in predefined period
IOUT_OC_FAULT	Current rail is over OC fault threshold
IOUT_OC_WARNING	Current rail is under OC warning threshold
IOUT_UC	Current rail is under UC fault threshold
OT_FAULT	Temperature rail is over OT fault threshold
OT_WARNING	Temperature rail is over OT warning threshold
All GPI de-asserted	No logging and fault response, but the function of the GPI is not ignored.
SYSTEM_WATCHDOG_TIMEOUT	System watch timeout
RESEQUENCE_ERROR	Rail fails to resequence
SEQ_ON_TIMEOUT	Rail fails to meeting sequence on dependency in predefined period
SEQ_OFF_TIMEOUT	Rail fails to meeting sequence on dependency in predefined period
SLAVE_FAULT	Rail is shut down due to that its master has fault

8.4.3 Rail Sequence Configuration

Rail sequences can be configured through the **Vout Config** tab. First, select a rail in the top-right corner of the *Fusion Digital Power Designer* software, and then edit the rail sequence as shown in Figure 13.

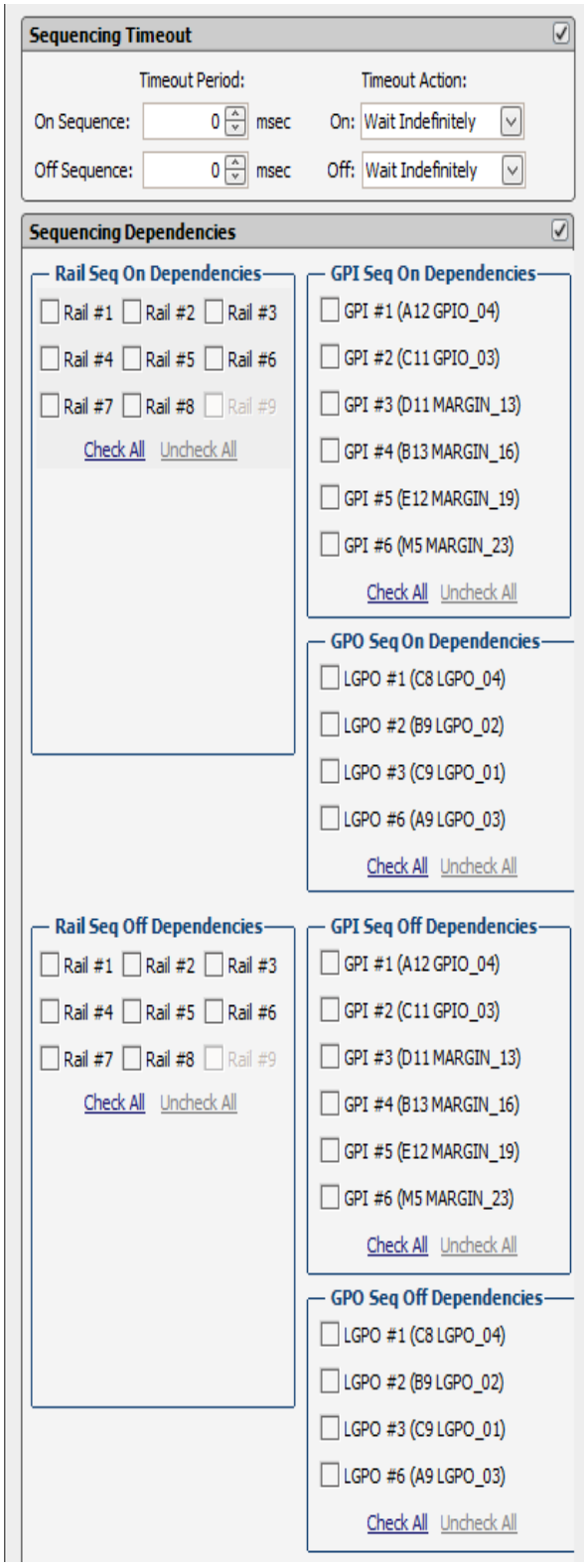


Figure 13. Rail Sequence Configuration Window (Rail Config)

When a rail receives a turn-ON or turn-OFF command as defined in *On/Off Config*, it checks its dependency conditions. When all dependencies are fulfilled, the rail then waits for a *Turn ON Delay* time or a *Turn OFF Delay* time, and then asserts or de-asserts the EN pin.

The device fulfills a *Rail Sequence On Dependency* status when the rail is in *Power Good* status. The device fulfills a *Rail Sequence Off Dependency* status when the rail is in *Not Power Good* status. The device fulfills a *GPI Sequence On Dependency* status when the GPI pin is asserted. The device fulfills a *GPI Sequence Off Dependency* status when the GPI pin is de-asserted. The device fulfills a *GPO Sequence On Dependency* status when the logical sate of the GPO is TRUE. The device fulfills a *GPO Sequence Off Dependency* status when the logic state of the GPO is FALSE.

After the EN pin of a rail is asserted, if the rail voltage does not rise above *Power Good On* threshold within the *Maximum Turn-ON* time, a *Time On Max* fault occurs. Similarly, after the EN pin of a rail is de-asserted, if the rail voltage does not fall below 12.5% nominal output voltage within *Maximum Turn-OFF* time, a *Time Off Max* warning occurs.

Each rail can include a *Fault Shutdown Slaves* function. When a rail shuts down as a result of a fault, the associated slave rails also shut down. The device continues to monitor delays and dependencies of the slave rails during the shutdown process. Fault Shutdown Slaves cannot cascade. In other words, if a rail that is acting as a slave shuts down, the associated slave rails does not shut down.

Each rail can set *Sequencing On/Off Timeout* periods. The timeout periods begin to increment when a rail receives a turn-ON or a turn-OFF command as defined in *On/Off Config*. When the *Sequencing On/Off Timeout* period elapsed, the rail executes one of 3 actions including:

- Wait Indefinitely
- Enable or Disable Rail
- Re-sequence (Sequencing On only)

Re-sequence is a series of actions that shuts down a rail and the Fault Shutdown Slaves, and then re-enables the rails according to sequence-on delay times and dependencies. The re-sequencing parameters can be configured in the **Other Config** tab, as shown in Figure 14.

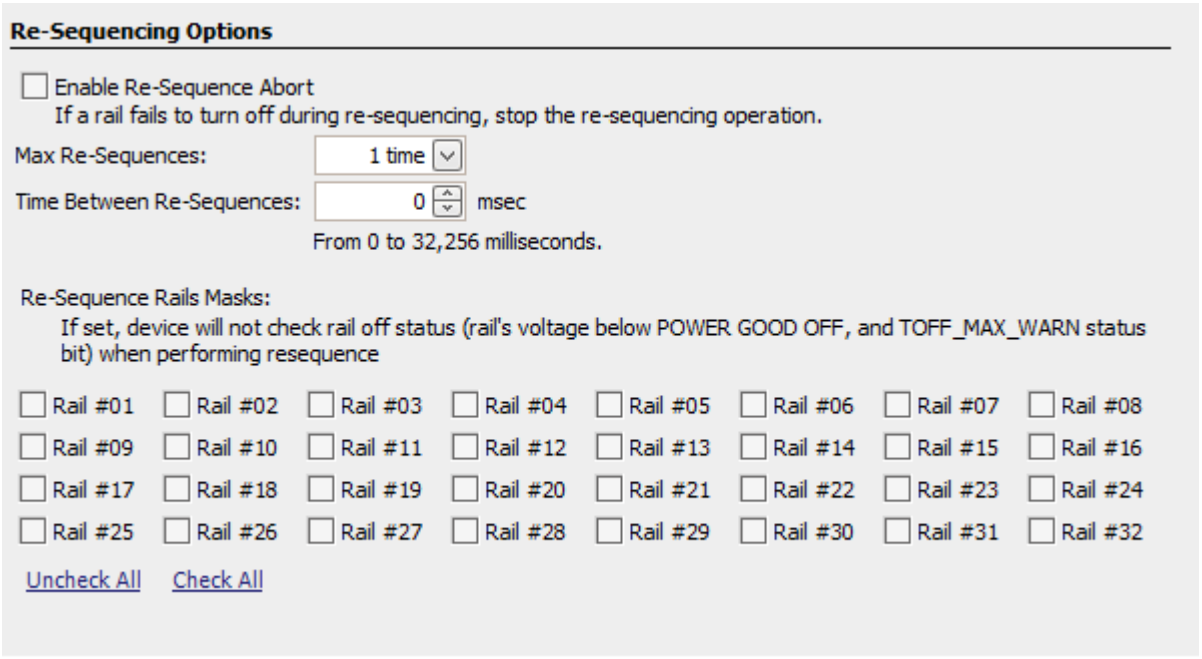
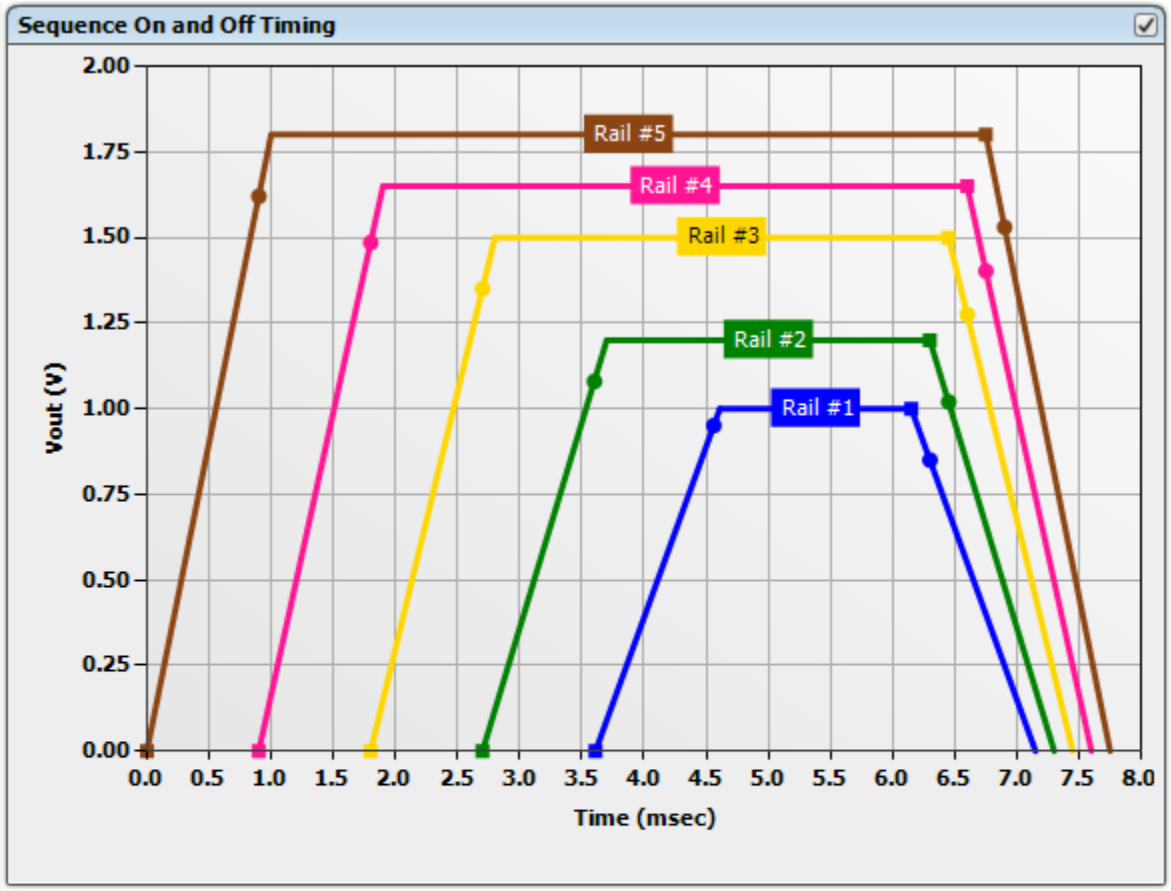


Figure 14. Re-Sequencing Options (Global Configuration ► Misc Config)

A re-sequencing event can be repeated for one to approximately four times or unlimited times. The *Time Between Re-Sequences* period begins to increment when all the relevant rails are given *Not Power Good* statuses. When the time period elapses, a re-sequence event begins. When the *Enable Re-Sequence Abort* is checked, the re-sequence event aborts if any relevant rail triggers a *Max Turn Off* warning. However, the *Max Turn Off* warning does not stop an ongoing re-sequence event. If any rails at the re-sequence state are caused by a GPI fault response, the device suspends the entire re-sequence event until the GPI fault is physically clear.

It is also configurable to ignore the POWER_GOOD_OFF and TOFF_MAX_WARN status of a rail when performing re-sequencing if the corresponding bits are set.

After the Rail Sequence is configured, the GUI displays simulated sequence timing in the **Vout Config** tab. It demonstrates the dependencies among the rails. An example is shown in Figure 15. The rails power-on and power-off slew rates in Figure 15 are for demonstration purpose only.



Rail #	Rail Name	Vout	On Delay	PG On	PG Off	Off Delay	Dependencies (Direct Only)
1	Rail #1	1.000	0.0	0.951	0.850	0.0	CONTROL; Vin On/Off; Turn On
2	Rail #2	1.200	0.0	1.080	1.020	0.0	CONTROL; Vin On/Off; Turn On
3	Rail #3	1.500	0.0	1.350	1.275	0.0	CONTROL; Vin On/Off; Turn On
4	Rail #4	1.650	0.0	1.485	1.402	0.0	CONTROL; Vin On/Off; Turn On
5	Rail #5	1.800	0.0	1.620	1.530	0.0	CONTROL; Vin On/Off; Turn Off

Figure 15. Simulated Sequence Timing Window (Rail Config)

8.4.4 Fault Responses Configuration

In the previous sections, various fault and warn notification thresholds have been configured to monitor voltage, current, temperature, and turn-ON time and turn-OFF time. When a fault threshold is reached, a fault event occurs. The device performs the following three actions in response of a fault event.

- Asserts the PMBus $\overline{\text{ALERT}}$ line
- Logs the fault event into nonvolatile memory (data flash), set status register bit
- Executes fault responses defined by users

The Fault Responses can be configured under the Fault Responses and Limits tab. Figure 16 shows an example configuration window.

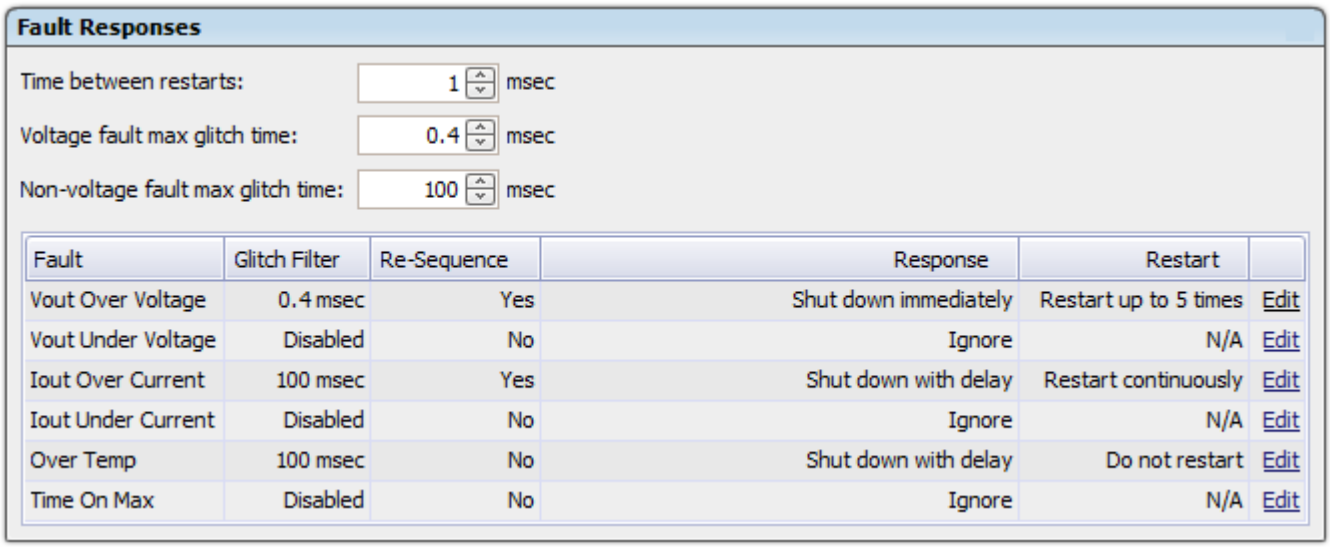


Figure 16. Fault Responses Configuration Window (Rail Configure ► Fault Responses)

A programmable glitch filter can be enabled or disabled for each type of fault. When a fault remains present after the glitch filter time expires, the device performs of the three selectable actions:

- Log the fault and take no further action.
- Log the fault and shut down the rail immediately.
- Log the fault and shut down the rail with *Turn Off* Delay.

After shutting down the rail, the device performs one of the three selectable actions:

- Do not restart the rail until a new turn-on command is received.
- Restart the rail. If the restart is unsuccessful, retry up to a user-defined number of times (up to a maximum of 14) and then remain off until the fault is cleared.
- Restart the rail. If the restart is unsuccessful, retry for an unlimited number of times unless the rail is commanded off by a signal defined in *On/Off Config*.

After the rail exhausts the restart attempts, Re-sequence can be initiated (see the *Rail Sequence Configuration* section).

Voltage, current, and temperature monitoring are based on results from the 12-bit ADC(AMON) and 8 DMON. All the voltage monitoring AMON and DMON channels are monitored every 400 µs for up to 32 channels. Current monitoring ADC channels are monitored at 200 µs per channel. Temperature monitoring ADC channels are monitored at approximately 4.17 ms per channel. The ADC results are compared with the programmed thresholds. The time to respond to an individual event is determined by when the event occurs within the ADC conversion cycle and the configured fault responses (glitch filters, time delays, and so forth).

GPI pins can also trigger faults if the GPI Fault Enable checkbox in Figure 12 is checked. The GPI Fault Responses options are the same as the Fault Responses discussed earlier in this section, with one exception: the GPI Fault Responses option does not support the retry action. An example configuration window is shown in Figure 17.

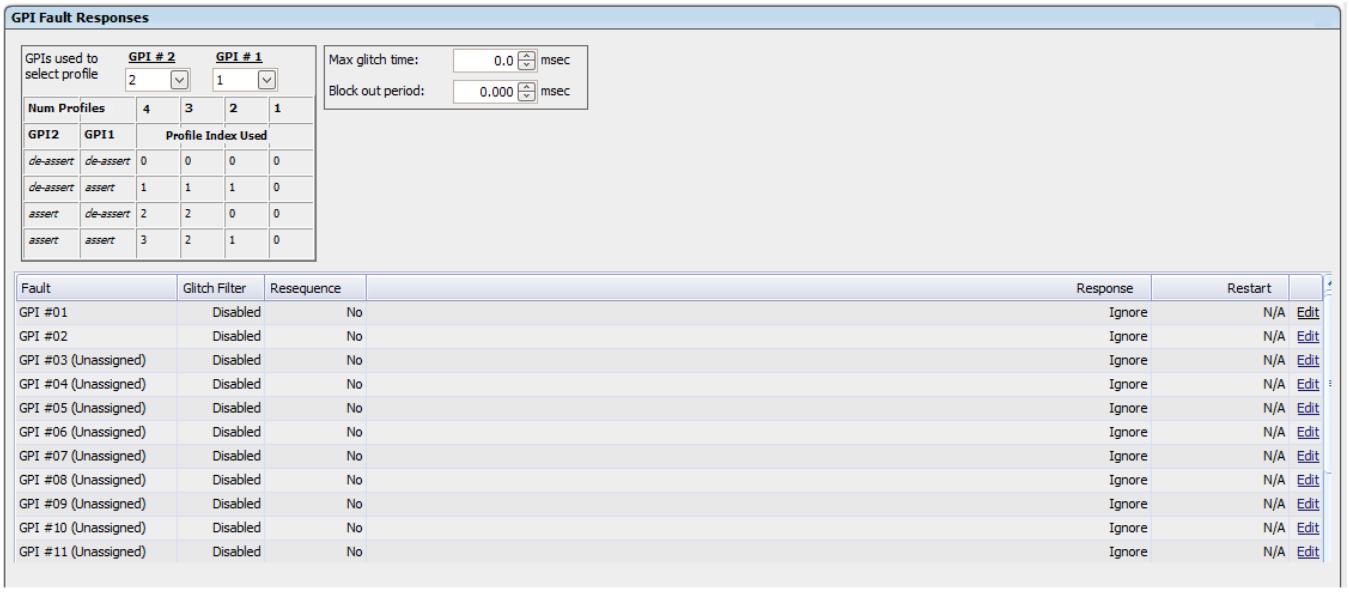


Figure 17. GPI Fault Responses Configuration Window (Rail Configure ► Fault Responses)

8.4.5 GPO Configuration

8.4.5.1 Command Controlled GPO

The UCD90320 device has 84 GPIO pins, all of which can be configured as Command Controlled GPOs. These GPOs are controlled by PMBus commands (GPIO_SELECT and GPIO_CONFIG) and can be used to control LEDs, enable switches, and so forth. Details on controlling a GPO using PMBus commands can be found in the *UCD90320 Sequencer and System Health Controller PMBus Command Reference*. The configuration window of Command Controlled GPO is under Pin Assignment tab. An example configuration window is shown in Figure 18.

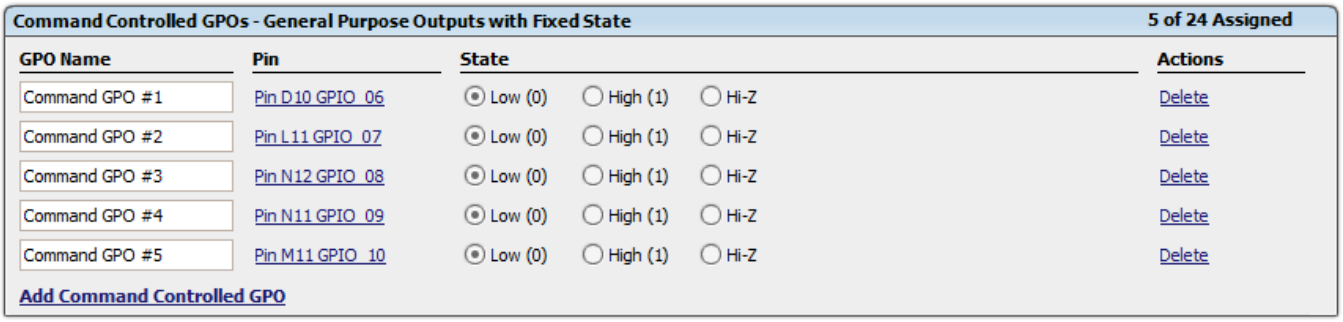


Figure 18. Command Controlled GPO Configuration Window (Hardware Configure ► Monitor and GPIO Pins Assignment)

8.4.5.2 Logic GPO

UCD90320 also has 16 dedicated Logic GPO (LGPO) pins. The configuration window is under Pin Assignment tab, as shown in Figure 19.

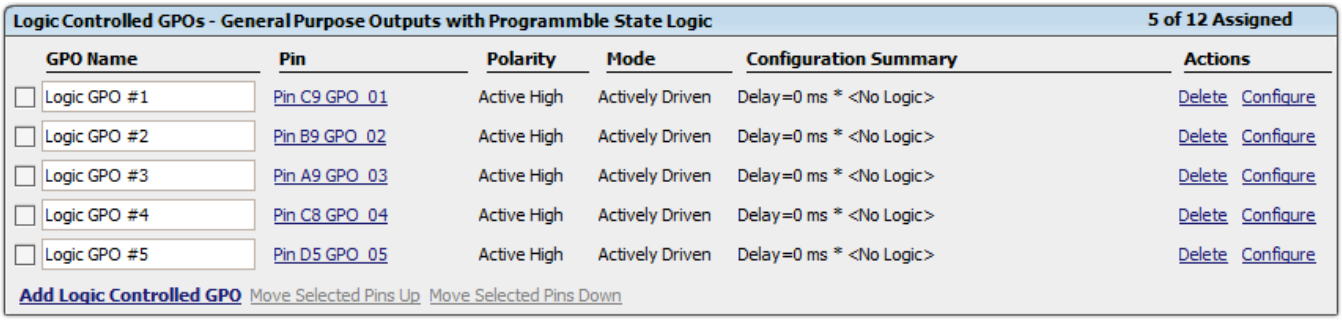


Figure 19. Logic GPO Configuration Window (Hardware Configure ► Monitor and GPIO Pins Assignment)

Each LGPO is controlled by an internal Boolean logic builder. Figure 20 shows the configuration interface of the Boolean logic builder. As shown, each Boolean logic builder has a top-level logic gate, which can be configured as AND, OR, or NOR gate with optional time delay. The inputs of the top-level logic gate are two AND paths. Each AND path can select a variety of inputs including GPI states, LGPO states, and rail statuses, as shown in Figure 21. The selectable rail statuses are summarized in Table 3. In Table 3, _LATCH type statuses stay asserted until cleared by a MFR PMBus command or by a specially configured GPI pin shown in Figure 12. See the *UCD90320 Sequencer and System Health Controller PMBus Command Reference* for complete definitions of rail-status types.

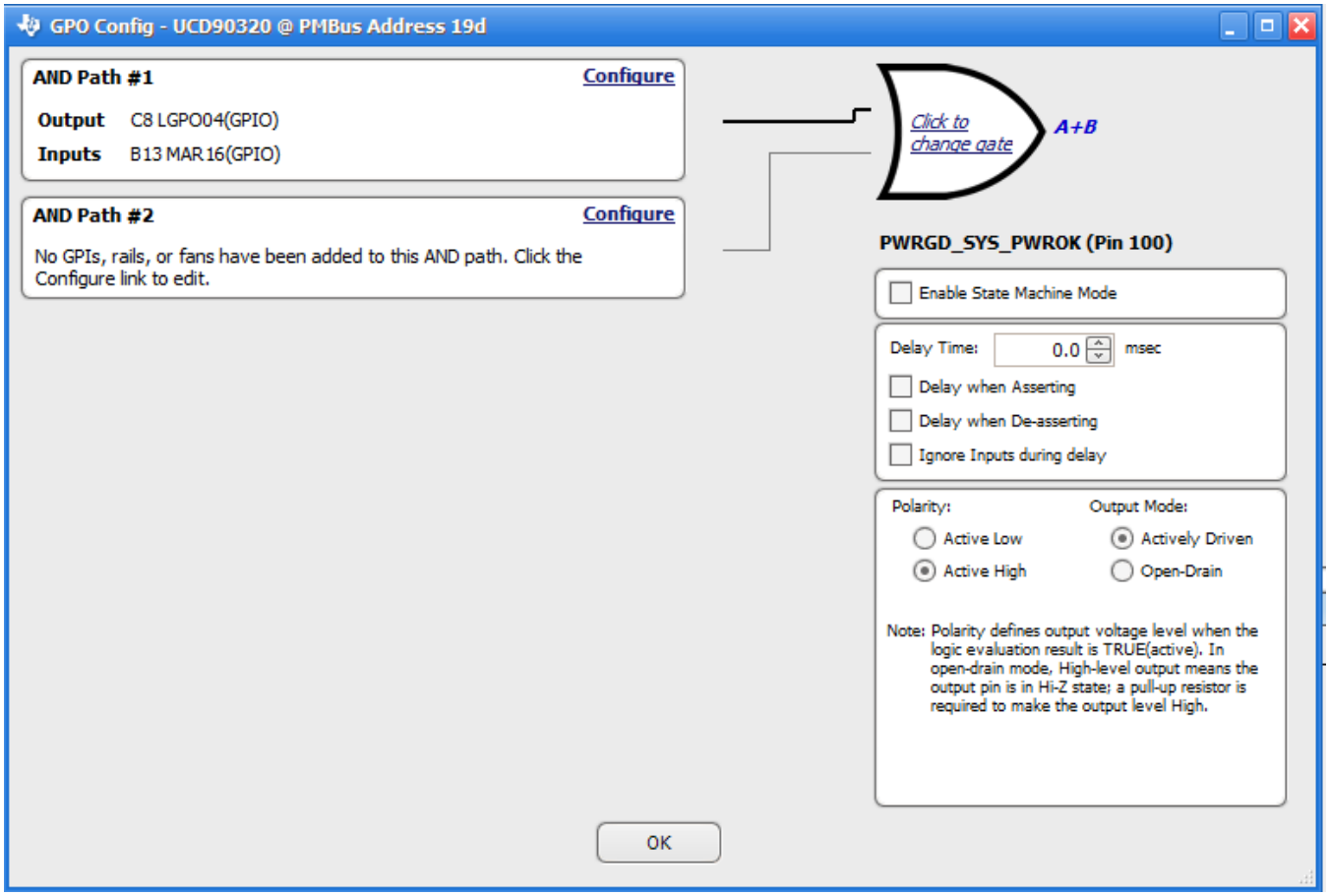


Figure 20. Boolean Logic Builder Interface

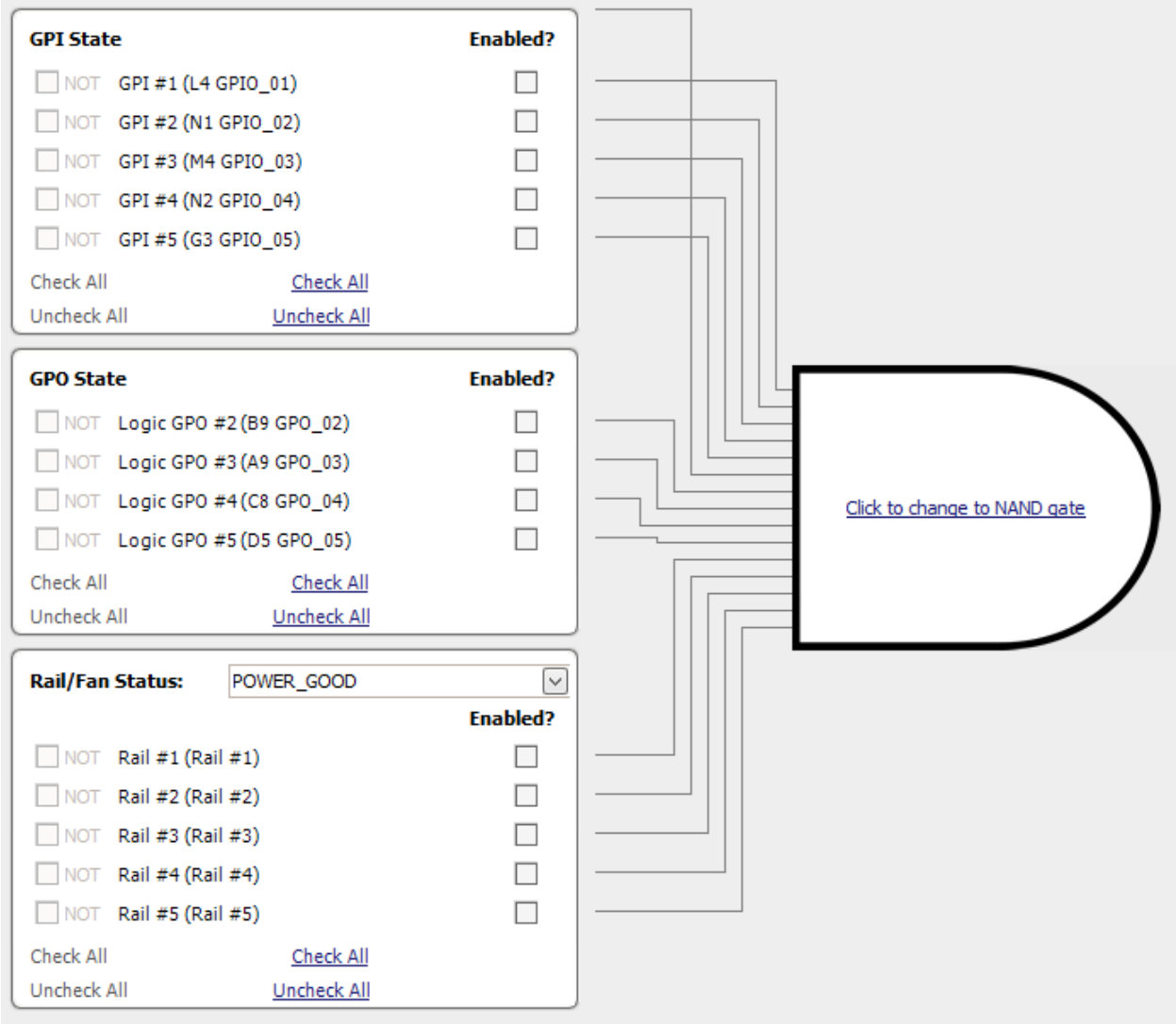


Figure 21. AND Path Configuration

Table 3. Selectable Rail Statuses in Boolean Logic Builder

Rail-Status Types		
POWER_GOOD	IOUT_OC_FAULT	TON_MAX_FAULT
MARGIN_EN	IOUT_OC_WARN	TOFF_MAX_WARN
MRG_LOW_nHIGH	IOUT_UC_FAULT	TON_MAX_FAULT_LATCH
VOUT_OV_FAULT	IOUT_OC_FAULT_LATCH	TOFF_MAX_WARN_LATCH
VOUT_OV_WARN	IOUT_OC_WARN_LATCH	SEQ_ON_TIMEOUT
VOUT_UV_WARN	IOUT_UC_FAULT_LATCH	SEQ_OFF_TIMEOUT
VOUT_UV_FAULT	TEMP_OT_FAULT	SEQ_ON_TIMEOUT_LATCH
VOUT_OV_FAULT_LATCH	TEMP_OT_WARN	SEQ_OFF_TIMEOUT_LATCH
VOUT_OV_WARN_LATCH	TEMP_OT_FAULT_LATCH	SYSTEM_WATCHDOG_TIMEOUT
VOUT_UV_WARN_LATCH	TEMP_OT_WARN_LATCH	SYSTEM_WATCHDOG_TIMEOUT_LATCH
VOUT_UV_FAULT_LATCH	SINGLE_EVENT_UPSET	

The POWER_GOOD status used by GPO evaluation is based on actual monitoring result from AMON or DMON pins. For a rail that does not have a voltage monitor pin, the POWER_GOOD status is used by sequencing purpose only, and is not used by GPO evaluation. Therefore during GPO evaluation, a rail without an AMON or DMON pin never reports POWER_GOOD status.

Each LGPO can be also configured as a simple state machine, as shown in Figure 16. In state machine mode, the top-level logic gate is omitted and only one of the two AND paths is evaluated. The output of the state machine is the result of the active AND path. The evaluation initially starts with AND Path #1. If the evaluation result is TRUE, AND Path #1 remains active until its evaluation result becomes FALSE. When the output associates with AND Path#1 becomes FALSE, AND Path #2 becomes active in the next evaluation cycle. AND Path #2 remains active until its evaluation result becomes TRUE, then AND Path #1 becomes active in the next evaluation cycle. An evaluation cycle is triggered when any input signal to the state machine changes state.

GPO1 to GPO8 outputs are internally synchronized to the same clock edge to enable them to change states together. GPO9 to GPO16 outputs are internally synchronized to enable them to change states together. GPO1 through GPIO8 and GPO9 through GPIO16 outputs status are updated within an time window between approximately 1 µs and 3 µs.

8.4.6 Margining Configuration

The UCD90320 device provides accurate closed-loop margining for up to 24 voltage rails. System reliability is improved through four-corner testing during system verification. During four-corner testing, the system operates at the minimum and maximum expected ambient temperature and with each power supply set to the minimum and maximum output voltage, commonly referred to as margining. Margining can be controlled via the PMBus interface using the OPERATION command or by configuring two GPI pins as margin-EN and margin-UP/DOWN inputs. The MARGIN_CONFIG command in the *UCD90320 Sequencer and System Health Controller PMBus Command Reference* user guide describes several margining options, including ignoring faults while margining and using closed-loop margining to trim the rail output voltage.

The device provides 24 PWM output pins for closed-loop margining. Figure 22 shows the block diagram of margining circuit. An external R-C network converts the PWM pulses into a DC margining voltage. The margining voltage is connected to the power supply feedback node through a resistor. The feedback node voltage is thus slightly pulled up or down by the margining voltage, causing the rail output voltage to change. The UCD90320 device monitors the rail output voltage. The device adjusts the margining PWM duty cycle accordingly such that the rail output voltage is regulated at the margin-high or margin-low voltages defined by the user. Effectively, margin control loop of the UCD90320 device overwrites the DC set point of the margined power supply. The margin control loop is extremely slow in order in order to not interfere with the power supply control loop.

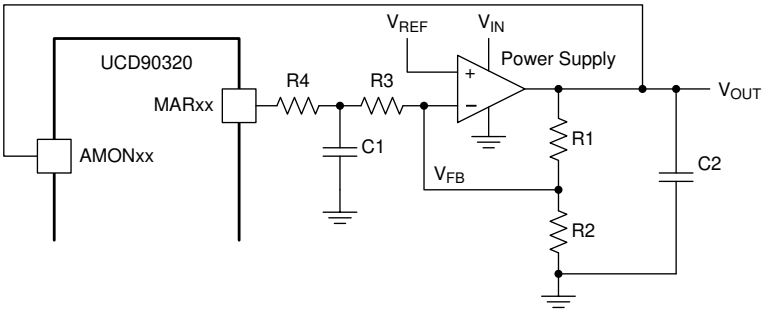


Figure 22. Block Diagram of Margining Circuit

Margining pins can be configured under the **Pin Assignment** tab, as shown in Figure 23. When not margining, the margin pin can operate in one of three modes:

- Tri-state
- Active trim
- Active duty cycle

Tri-state mode sets the margin pin to high-impedance. Active Trim mode performs a continuously trim the DC output voltage. Active Duty Cycle mode provides a user-defined fixed PWM duty cycle as shown in Figure 23.

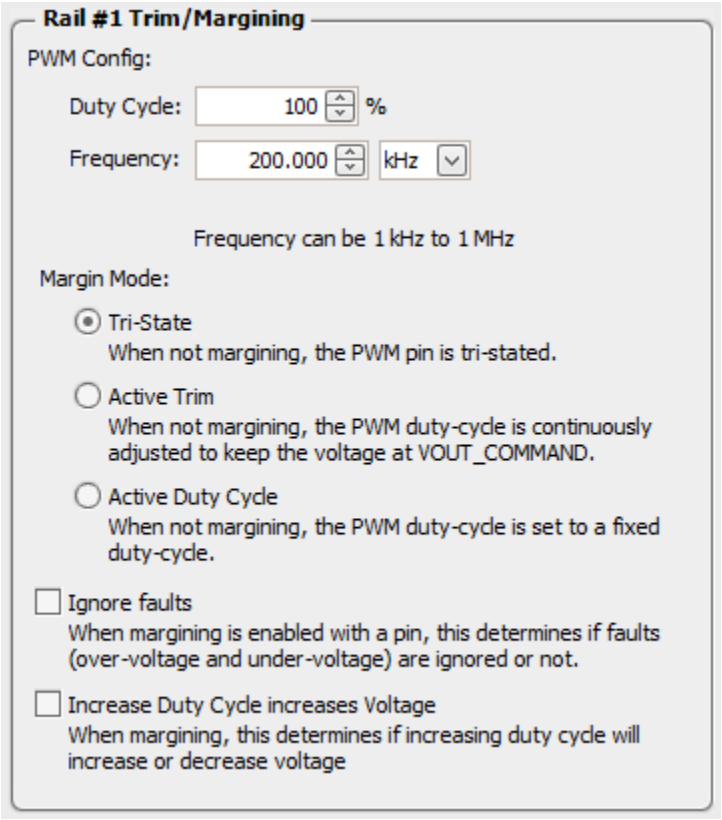


Figure 23. Margining Configuration Dropdown Window (Hardware Configuration ► Monitor and GPIO Pin Assignment)

8.4.7 Pin Selected Rail States Configuration

UCD90320 allows users to use up to three GPI pins to control up to eight rail states. Each rail state enables and disables certain rails. This feature is useful to implement system low-power modes, such as those compliant with the Advanced Configuration and Power Interface (ACPI) specification. The Pin Selected States function can be configured under the Pin Selected States tab, as shown in Figure 24.

When a new state is presented on the GPI pins, and a rail is commanded to turn ON, it does so according to its sequence-on dependencies and delays. If a rail is commanded to turn OFF by a new state, it can be configured either immediately turn-OFF (Immediate OFF), or turn-OFF with its sequence-off dependencies and delays (Soft Off). If a rail is commanded to remain in the same ON state or OFF state, no action occurs.

The Pin Selected Rail States function is implemented by modifying OPERATION command. Therefore, in order to use this function to control rail states, the related rails must be configured to use OPERATION command in *On/Off Config* (shown in Figure 6).

The Pin Selected States feature always uses the first three configured GPI pins to select system states. When selecting a new system state, state changes on GPI pins must be completed within 1 µs, otherwise an unintended system state may be selected. See the *UCD90320 Sequencer and System Health Controller PMBus Command Reference* for complete configuration settings of Pin Selected States.

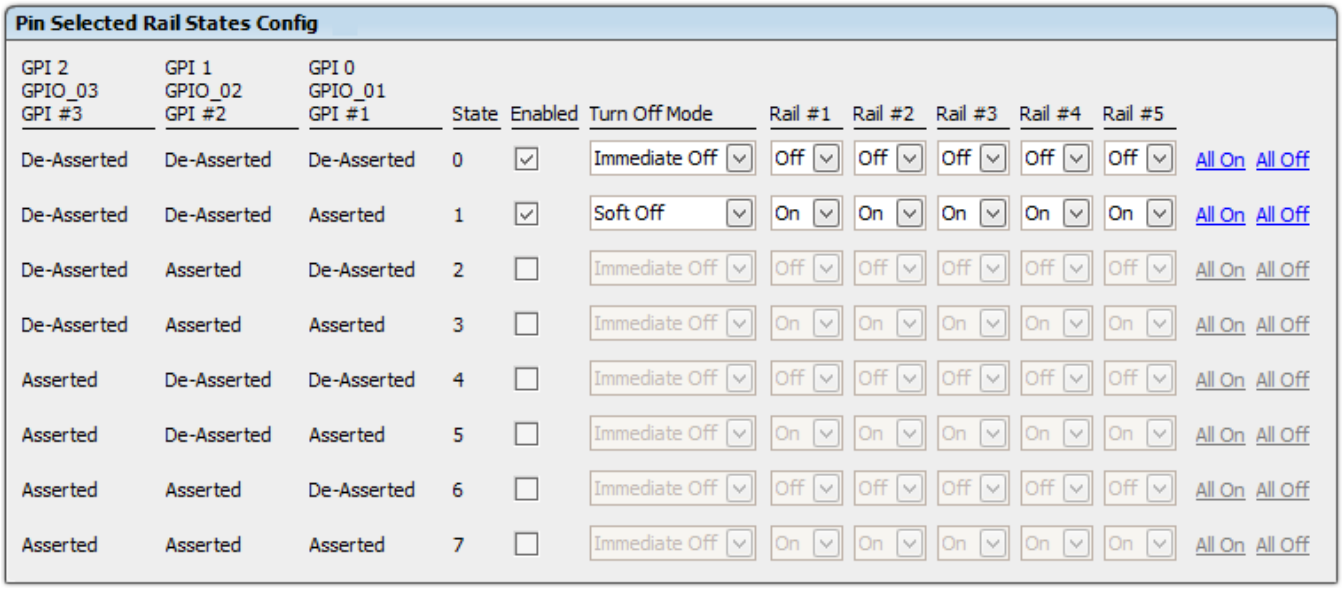


Figure 24. Pin Selected States Configuration Window (Global Configuration ►Pin Selected Rail States)

8.4.8 Watchdog Timer

The UCD90320 device provides a watchdog timer (WDT). The WDT can be reset by toggling a watchdog input (WDI) pin. If WDI is not toggled within a programmed period, the WDT times out. As a result, a watchdog output (WDO) pin is asserted (generates a pulse) to provide a system-reset signal.

The WDI and WDO pins are GPIO pins and are only optional. The WDI can be replaced by SYSTEM_WATCHDOG_RESET command sent over PMBus. The WDO can be manifested through the Boolean Logic defined GPOs, or its function can be integrated into the system reset pin ($\overline{\text{RESET}}$) configured in the system reset function. See the *System Reset Function* section.

The WDT timer is programmable from 0.001 s to 258.048 s. See also the UCD90320 Sequencer and System Health Controller PMBus Command Reference user guide for details on configuring the watchdog timer.

After a timeout, the WDT can be restarted by toggling the WDI pin or by writing a SYSTEM_WATCHDOG_RESET command over PMBus. Figure 25 shows the watchdog timing waveforms.

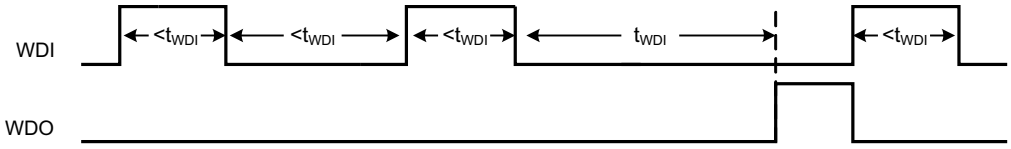


Figure 25. Watchdog Timer Operation Timing Diagram

The WDT can be active immediately at power up or after an initial wait time. These are the programmable wait times options that determine when the WDT operation begins.

- 100 ms
- 200 ms
- 400 ms
- 800 ms
- 1.6 s
- 3.2 s
- 6.4 s
- 12.8 s
- 25.6 s

- 51.2 s
- 102.4 s
- 204.8 s
- 409.6 s
- 819.2 s
- 1638.4 s

8.4.9 System Reset Function

The system reset function can generate a programmable system reset signal through a GPIO pin. The system reset signal is de-asserted when the selected rail voltages reach their respective Power Good On thresholds and the selected GPIs are asserted, plus a programmable delay time. These are the available options for the system-reset delay times.

- 0 ms
- 1 ms
- 2 ms
- 4 ms
- 8 ms
- 16 ms
- 32 ms
- 64 ms
- 128 ms
- 256 ms
- 512 ms
- 1.02 s
- 2.05 s
- 4.10s
- 8.19 s
- 16.38 s
- 32.8 s

The System Reset signal can be asserted immediately when any of the selected rail voltage falls below Power Good Off threshold, or any selected GPI is de-asserted. Alternatively, the System Reset signal can be configured as a pulse once Power Good On is achieved. An example in Figure 26 illustrates the difference of the two configurations. The pulse width can be configured between 0.001 s to 32.256 s. See the UCD90320 Sequencer and System Health Controller PMBus Command Reference for pulse width configuration details.

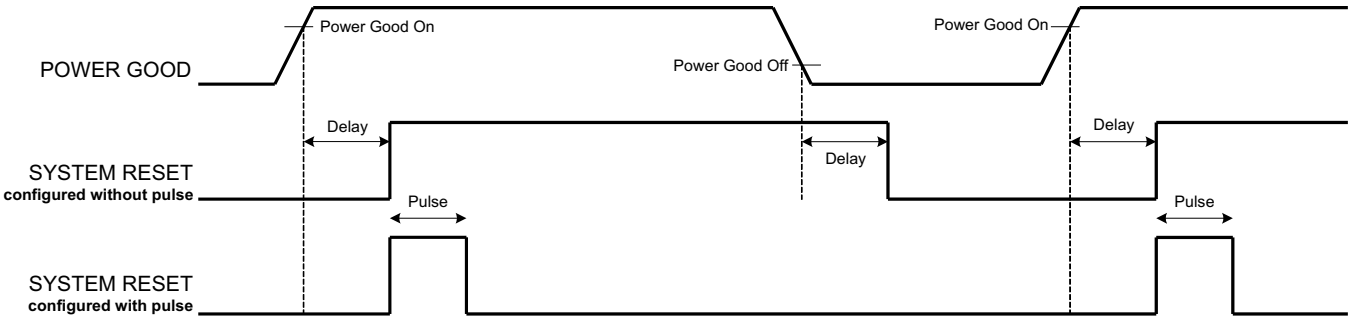


Figure 26. System Reset With and Without Pulse Setting (Active Low)

The *System Reset* signal can also integrate watchdog timer. An example is shown in Figure 27. In Figure 27, the first delay on *System Reset* is for the initial reset release that would enable the CPU once all necessary voltage rails are Power Good. The watchdog is configured with a Start Time and a Reset Time. If these times expire and timeout occurs, it means that the CPU providing the WDI signal is not operating. The *System Reset* signal is then toggled either using a Delay or GPI Tracking Release Delay to determine if the CPU recovers.

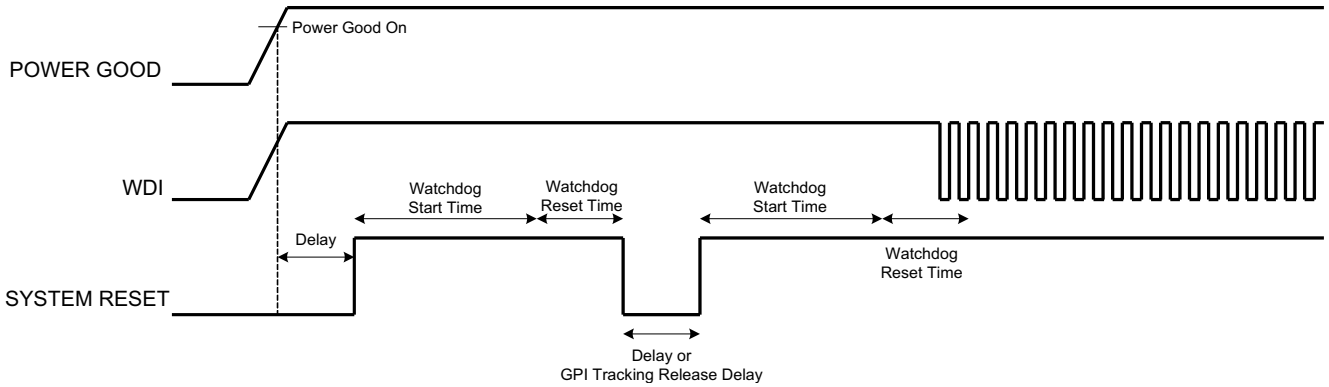


Figure 27. System Reset With Watchdog

The default state of the system reset pin ($\overline{\text{RESET}}$) is assert. When the system reset function is configured in-circuit through PMBus commands during normal operation, the ($\overline{\text{RESET}}$) pin is briefly asserted by default, even if conditions for de-assert are present. This is because the firmware requires a finite time to examine the de-assert conditions.

8.4.10 Cascading Multiple Devices

Multiple UCD90320 devices can work together and coordinate to determine fault notification.

Up to four GPI pins can be configured as *Fault Pins*. Each *Fault Pin* is connected to a *Fault Bus*. Each *Fault Bus* is pulled up to 3.3 V by a 10-kΩ resistor. All the UCD90320 devices on the same *Fault Bus* are informed of the same fault condition. An example of Fault Pin connections is shown in Figure 28.

When there is no fault on a *Fault Bus*, the *Fault Pins* are digital input pins and listen to the *Fault Bus*. When one or multiple UCD90320 devices detect a rail fault, the corresponding *Fault Pin* is turned into active driven low state, pulling down the *Fault Bus* and informing all other UCD90320 devices of the corresponding fault. This way, a coordinated action can be taken across multiple devices. After the fault is cleared, the state of the *Fault Pin* is turned back to an input pin.

Any of the 24 rails can be assigned to one or multiple *Fault Pins*. The configuration window is shown in Figure 29.

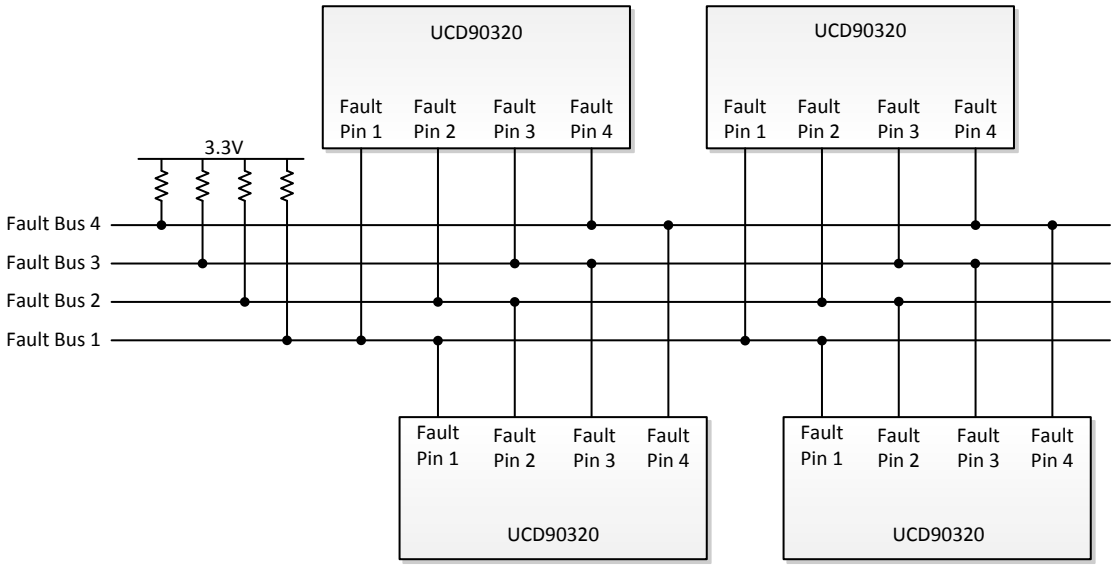


Figure 28. Example of Fault Pin Connections

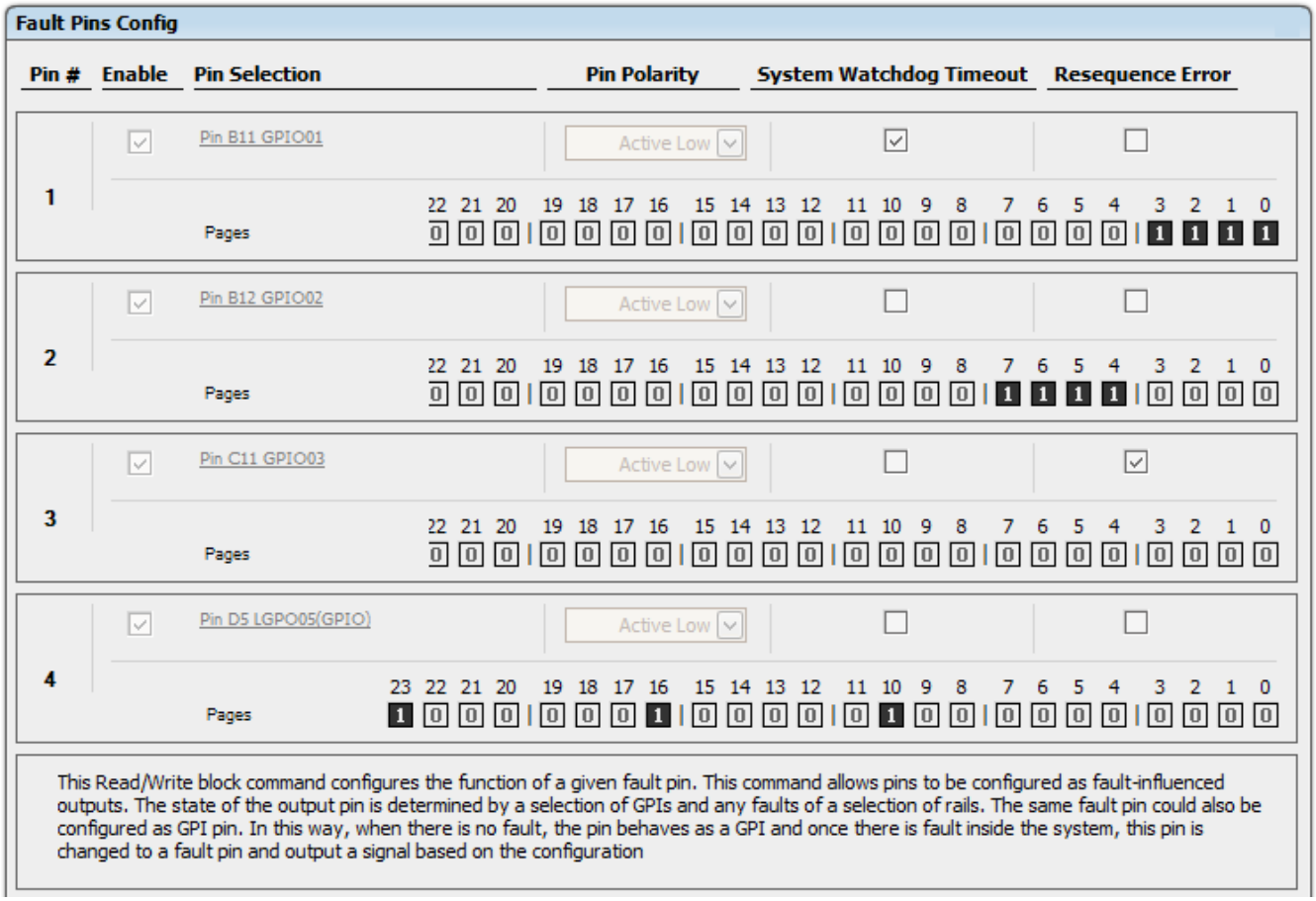


Figure 29. Example Fault Pins Configuration Window (Global Configuration ►Fault Pins Config)

These listed page-related faults have impact on the fault pin output. SYSTEM_WATCHDOG_TIMEOUT and RESEQUENCE_ERROR are optional to have impact on the fault pins.

- IOUT_OC_FAULT
- IOUT_UC_FAULT
- OT_FAULT
- SEQ_OFF_TIMEOUT
- SEQ_ON_TIMEOUT
- TON_MAX_FAULT
- VOUT_OV_FAULT
- VOUT_UV_FAULT

A SYNC_CLK pin is used as a single-wire time synchronization method. A master chip constantly drives a 5-kHz clock to the slave devices. This function offers a precise time base for multiple UCD90320 devices to respond to the same fault event at the same time. The configuration window is shown in Figure 30. If the system uses only one UCD90320 device, it is recommended to configure this pin as master clock output. The SYNC_CLK output can be used as a time base for other purposes if needed.

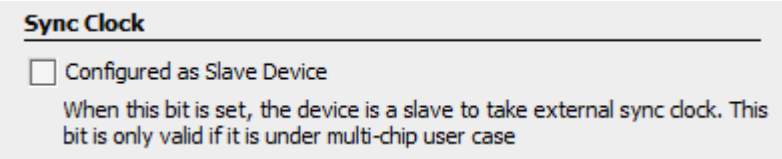


Figure 30. SYNC_CLK Pin Configuration (Global Configuration ► Misc Config)

8.4.11 Rail Monitoring

UCD90320 monitors up to 24 analog inputs including voltages, current, temperature, and eight digital inputs for POWER_GOOD. Use either the Fusion GUI or a PMBus interface host to poll data from the UCD90320. The Fusion GUI displays monitored rail voltage, current, and temperature information on the **Monitor** page, as shown in Figure 31. Use polling to debug system-level issues.

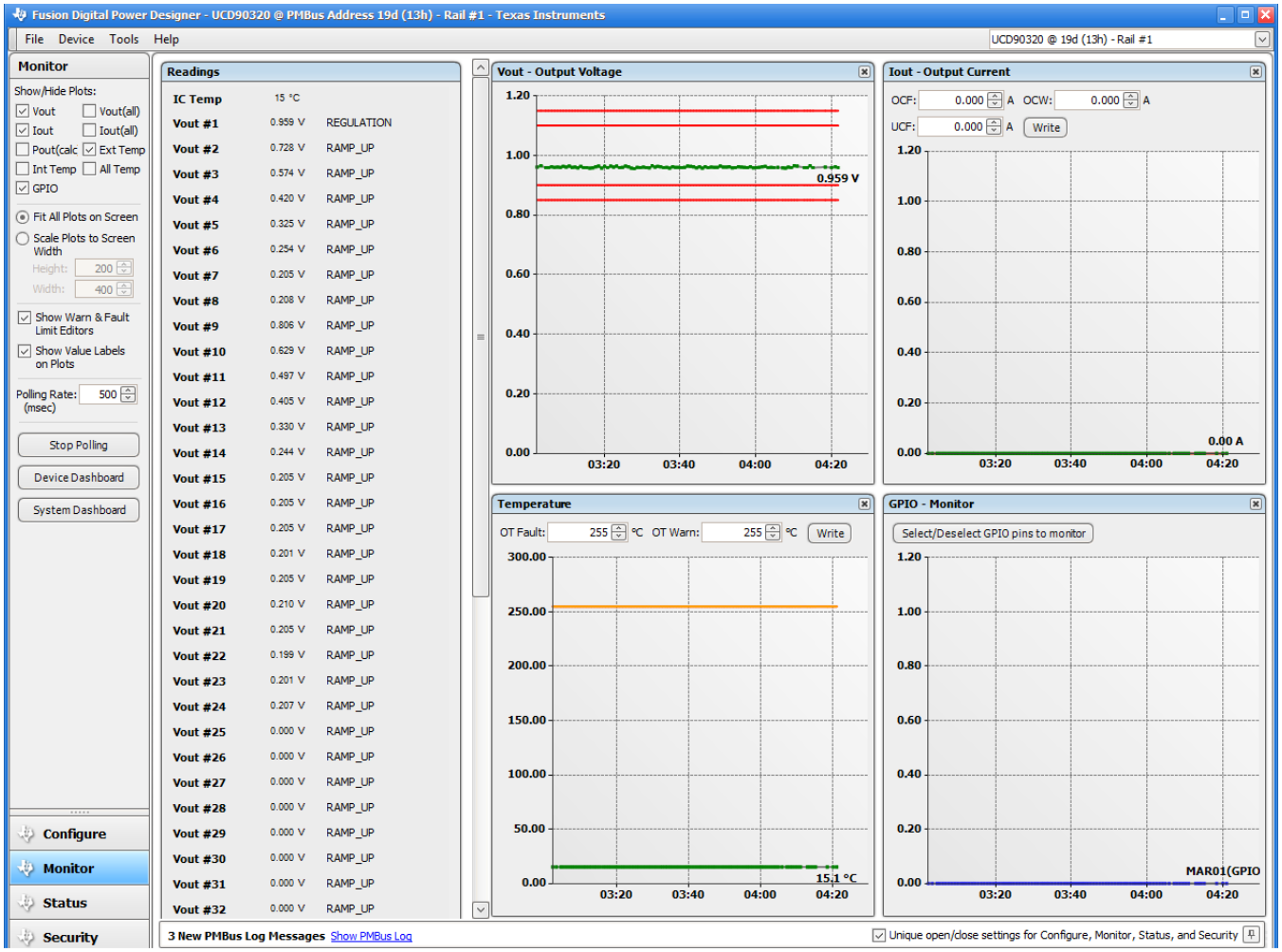


Figure 31. *Fusion Digital Power Designer* Software Monitor Page

Table 4. Rail State Value Descriptions

RAIL STATE	VALUE	CONDITION FOR ENTERING RAIL STATE
IDLE	1	When a turn-ON condition is not met, or when rail is shut down due to a fault, or when the rail is waiting for the turn-ON period to resequence
SEQ_ON	2	Waits for the dependency to be met to assert the enable signal
START_DELAY	3	TON_DELAY to assert the enable signal
RAMP_UP	4	Enable signal is asserted and rail is approaching the power good threshold. If the power good threshold is set to 0 V, the rail stays at this state even if the monitored voltage is higher than 0 V.
REGULATION	5	When the monitoring voltage is higher than the power good threshold when the enable signal is asserted, rails stay at this state even if the voltage is below the power good threshold and continues as long as there is no fault action taken.
SEQ_OFF	6	Wait for the dependency to be met to de-assert the enable signal
STOP_DELAY	7	TOFF_DELAY to de-assert the enable signal
RAMP_DOWN	8	The enable signal is de-asserted and rail is ramping down. This state is available only if TOFF_MAX_WARN_LIMIT is not set to unlimited, or if the turnoff sequence is triggered by a fault action. The rail must not be under fault retry sequence to show this RAMP_DOWN state. Otherwise, the IDLE state is present.

8.4.12 Status Monitoring

The UCD90320 has status registers for each rail. Faults and warnings are logged into EEPROM memory to assist system troubleshooting. The status registers (Figure 32) and the fault log (Figure 33) can be accessed from the *Fusion Digital Power Designer* software as well as the PMBus interface. See the *UCD90320 Sequencer and System Health Controller PMBus Command Reference*, and the PMBus Specification for detailed descriptions of each status register and supported PMBus commands.

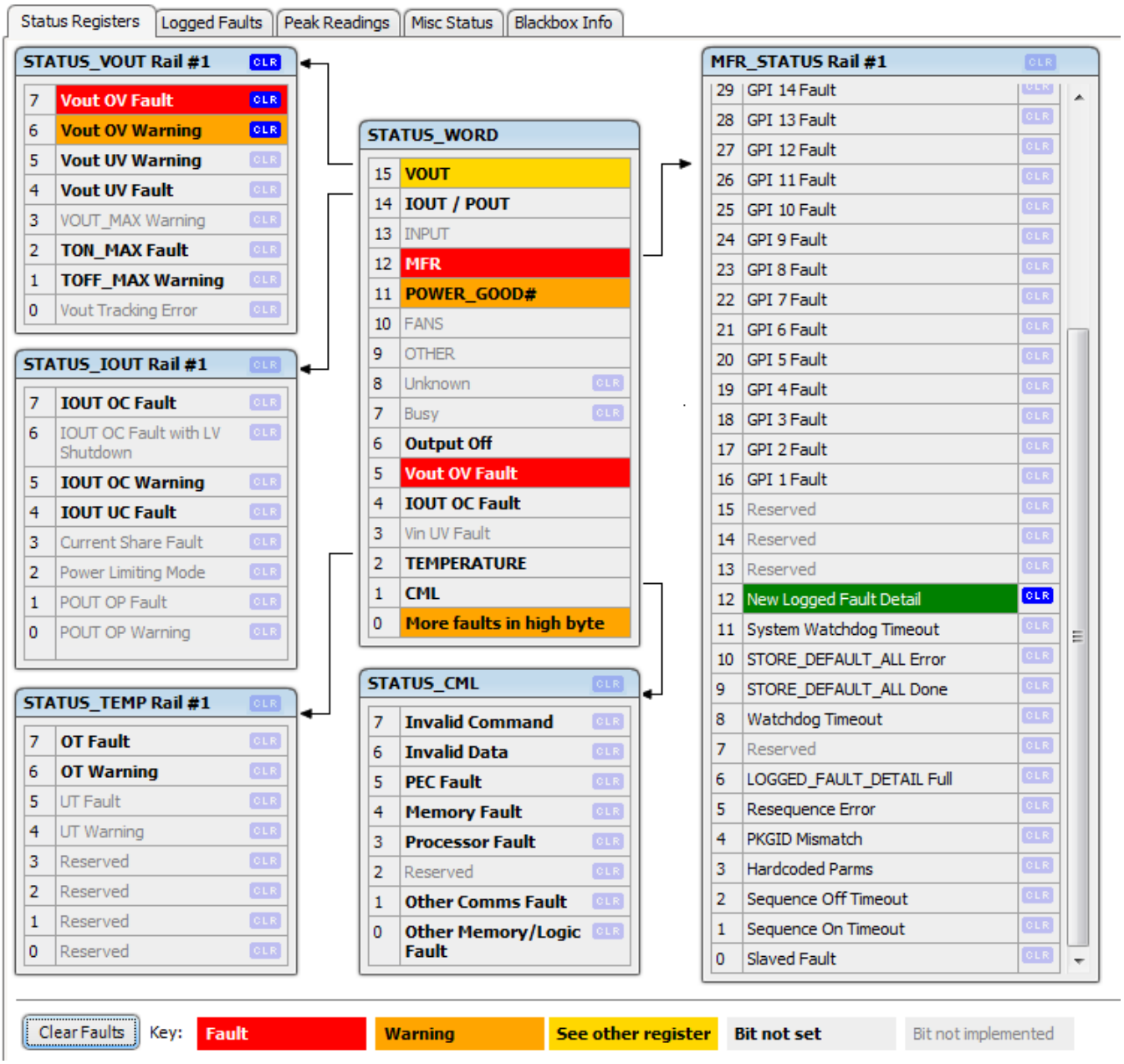


Figure 32. *Fusion Digital Power Designer* Software Rail Status Registers (Status ►Status Registers Tab)

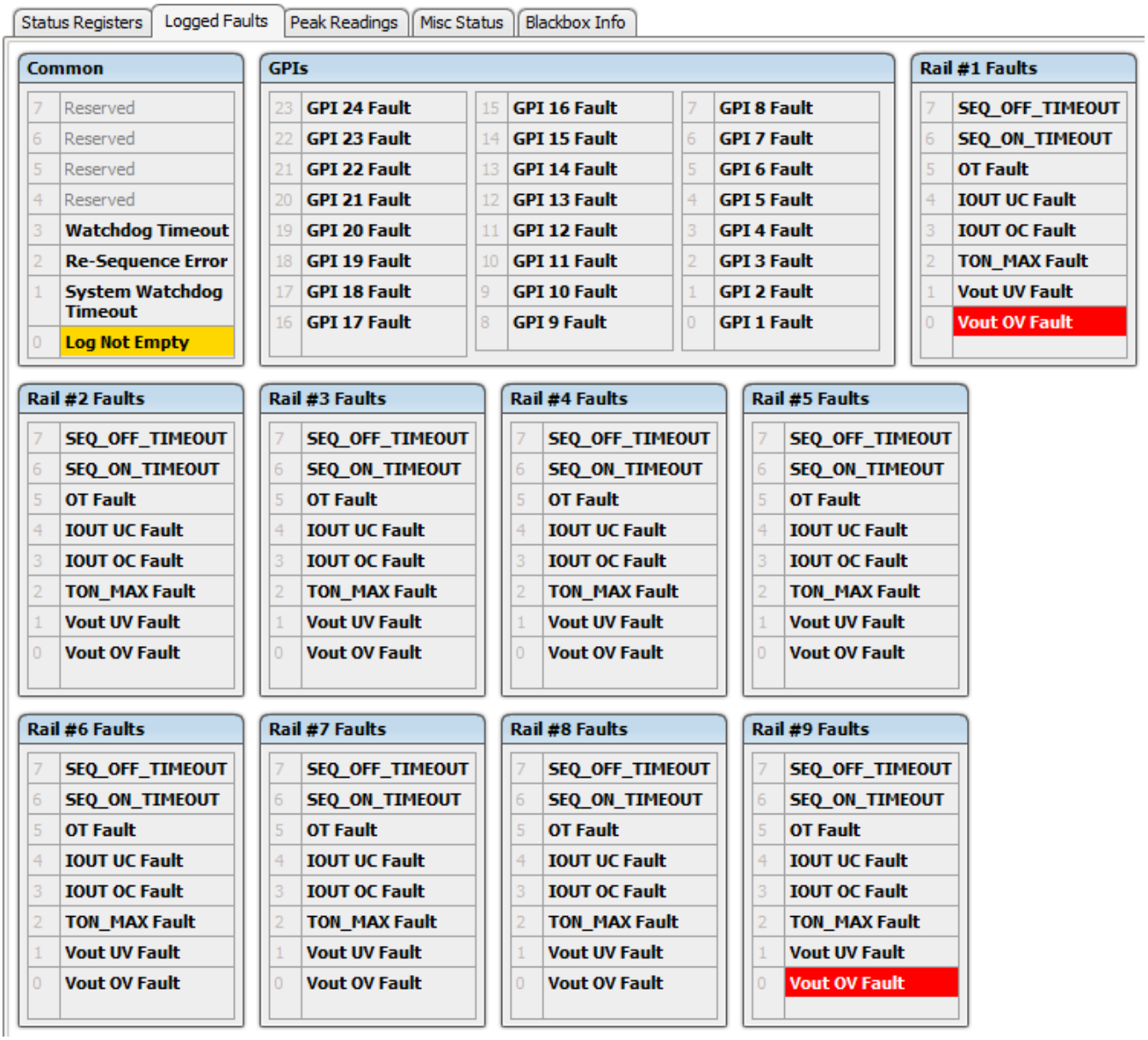


Figure 33. *Fusion Digital Power Designer* Software Logged Faults (Status ►Logged Faults Tab)

8.4.13 Data and Error Logging to EEPROM Memory

The UCD90320 provides fault log, device reset counter, and peak readings for each rail. To reduce stress on the EEPROM memory, a 30-second timer is started if a measured value exceeds the previously logged value. Only the highest value from the 30-second interval is written from RAM to EEPROM.

Faults are stored in EEPROM memory and are accessible over PMBus. Each logged fault includes the following information:

- Rail number
- Fault type
- Fault time since previous device reset
- Last measured rail voltage

The total number of device resets is also stored to EEPROM memory. The value can be reset using PMBus.

The run time clock value is logged into EEPROM when a power down is detected. This allows UCD90320 to preserve the run-time clock value through resets or power cycles.

It is also possible to update and calibrate the UCD90320 internal run-time clock via a PMBus host. For example, a host processor with a real-time clock can periodically update the UCD90320 run-time clock to a value that corresponds to the actual date and time. The host must translate the UCD90320 timer value back into appropriate units, based on the usage scenario chosen. See the REAL_TIME_CLOCK command in the *UCD90320 Sequencer and System Health Controller PMBus Command Reference* for more details.

8.4.14 Black Box First Fault Logging

The first fault in a system failure event is usually critical to diagnose the root cause. An innovative Black Box Fault Logging feature is introduced in the UCD90320 to accelerate the debugging process. When UCD90320 detects the first fault, the device records and saves the status of each rail and I/O pin in a special area of the EEPROM reserved for this function. The device does not save the subsequent faults and monitoring statuses into the Black Box Fault Log, but instead records them into the standard fault log. The Black Box Fault Log must be cleared in order to acknowledge the next fault.

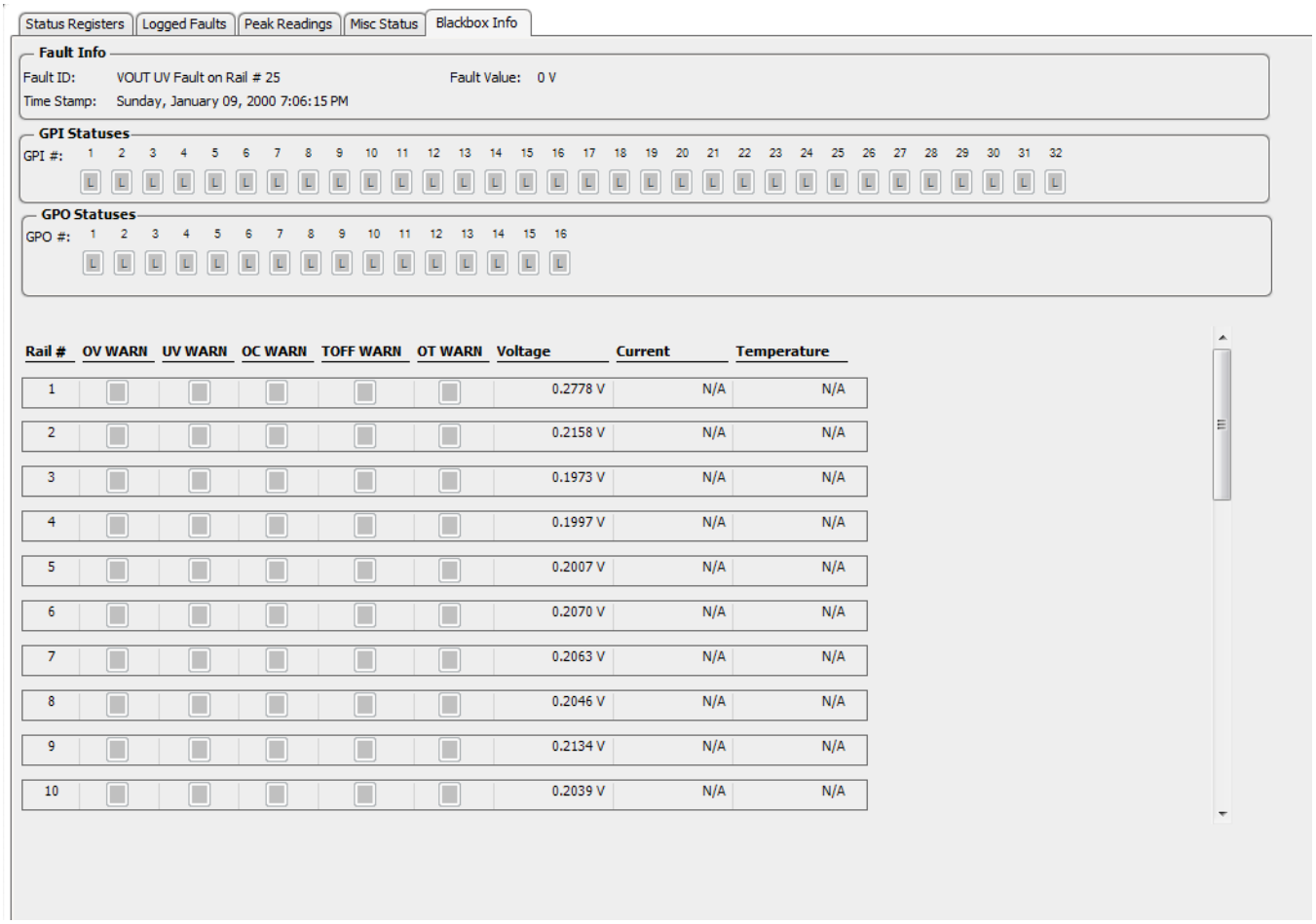


Figure 34. Black Box Fault Logging Window (Status ►Blackbox Info Tab)

8.4.15 PMBus Address Selection

Three digital input pins are allocated to decode the PMBus address. At power up, UCD90320 detects the logic inputs of the three address pins to determine the configured PMBus address.

Table 5. PMBus Address Configuration

PMBUS_ADDR2	PMBUS_ADDR1	PMBUS_ADDR0	PMBUS ADDRESS SELECTED	
L	L	L	17d	0010001b
L	L	H	19d	0010011b
L	H	L	23d	0010111b
L	H	H	49d	0110001b
H	L	L	51d	0110011b
H	L	H	113d	1110001b
H	H	L	115d	1110011b
H	H	H	119d	1110111b

8.4.16 ADC Reference

Using the V33A pin as ADC reference voltage by default provides a cost-effective solution. However, internal voltage reference has a higher Total Unadjusted Error. Also, voltage variations on the V33A pin affect ADC readings, such as when the device is powered down. To achieve better ADC accuracy, an external voltage reference can be connected to the VREFA+ and VREFA- pins. Ensure that the external reference voltage stays in regulation whenever V33D is above VBOR threshold. This limitation allows accurate ADC readings in full V33D operating range.

The external reference voltage level must be configured into the *Fusion Digital Power Designer* software to give correct ADC readings.

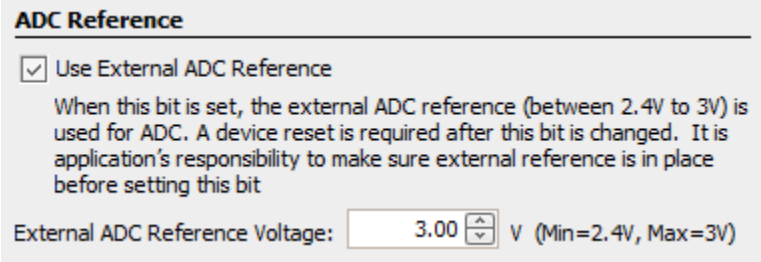


Figure 35. ADC Reference Configuration Window (Global Configuration ► Misc Config)

8.4.17 Device Reset

The UCD90320 device has an integrated power-on reset (POR) circuit which monitors the supply voltage. At power up, the POR detects the V33D pin voltage rise. When the V33D voltage is greater than V_{RESET}, the device comes out of reset.

The device can be forced into the reset state by an external circuit connected to the $\overline{\text{RESET}}$ pin. A logic-low voltage on this pin for longer than t_{RESET} sets the device into reset state. The device comes out of reset within t_{IRT} after $\overline{\text{RESET}}$ is released to logic-high level.

Any time the device comes out of reset, it begins an initialization routine that lasts typically 40 ms. A data flash checksum verification is performed at power up. If the checksum verification does not match, the device configuration settings are cleared, the $\overline{\text{PMBALERT}}$ pin is asserted, and a flag is set in the status register. A fault-log checksum verification in the EEPROM is also performed at power up. Each log entry includes the checksum verification status. Only a corrupted log entry is discarded. During the initialization routine, all I/O pins are held at high impedance state. At the end of initialization, the device begins normal operation as defined by the device configuration.

8.4.18 Brownout

The UCD90320 device triggers brownout event when the V33D pin voltage drops below the brownout threshold voltage, (V_{BOR}). During a brownout event, the device continues to write fault logs into the EEPROM that occurred before the brownout event. As the supply voltage continues to drop, the device fully shuts down when the V33D pin voltage is below the shutdown threshold voltage (V_{SHDN}). Any fault event that has not been written into the EEPROM before the device shutdown is lost.

In the scenario where several faults happen immediately before the brownout event, the device requires a capacitance of 500 µs to write the first fault event into the EEPROM. The write function requires an additional 4 ms to write the Black Box fault log into the EEPROM. Therefore, in order to preserve at least the first fault log, the user must provide enough local capacitance to maintain the V33D rail above VSHDN for 500 µs (or 4.5 ms with the Black Box fault log). Longer holdup time allows more fault events to be written into the EEPROM during brownout.

NOTE

The holdup time is affected by V33D rail capacitance, the UCD90320 supply current and external circuits that source current from the rail (such as LEDs, load current on I/O pins, and other devices powered by the same rail).

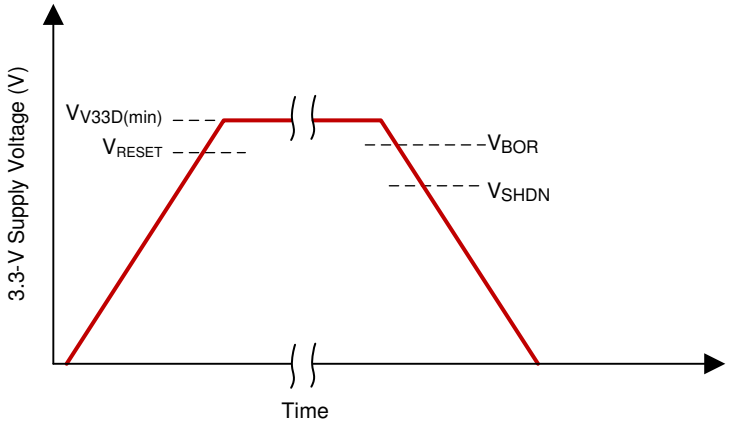


Figure 36. Reset and Brownout Thresholds

8.4.19 Internal Fault Management

The UCD90320 device verifies the firmware by using a checksum algorithm at each power up. If the checksum does not match, the device resets. If the device continues to reset, the SYNC_CLK pin outputs repeated pulses with an approximate 250-ms pulse width that can be observed externally.

The device performs a configuration checksum verification at power up. If the checksum does not match, the device discards all the configuration data. The PMBALERT pin is asserted and a flag is set in the status register.

A fault-log checksum verification in EEPROM is also performed at power up. Each log entry has a checksum. The device discards corrupted log entries.

If the internal firmware watchdog timer times out, the device resets. If the firmware program is corrupted, the device returns to a known state. This return function is normal, so all of the I/O pins are held in high-impedance while the device is in reset. The process confirms each parameter to ensure it falls within the acceptable range.

8.5 Device Configuration and Programming

UCD90320 devices include factory-installed sequencing and monitoring firmware. All I/O pins are pre-configured and high-impedance, with no sequencing or fault-response operation. Use the *Fusion Digital Power Designer* software to configure the device on-line or off-line. Generate a configuration file after configuring the device and import that configuration into other UCD90320 devices.

Devices implement dual-bank mechanism to store the user configurations. The old configurations are erased after the new one is programmed successfully. But if any errors are present in the middle of the programming, devices provide a fail-safe state by reloading the previous configurations after a power cycle or reset.

The ***Configuration Programming of UCD Devices*** section of the Documentation and Help Center offers configuration and programming details and can be accessed under the *Fusion Digital Power Designer* software help menu. In general, the UCD90320 supports two programming methods:

- The **PMBus command over PMBus and I²C** method uses a PMBus host to program the device. The PMBus host can be either a host microcontroller or *Fusion Digital Power Designer* software tools. Each PMBus

Device Configuration and Programming (continued)

command sends a corresponding parameter or parameters into the device. The new parameters are stored in its associated memory (RAM) location. After all the parameters are sent into the device, the PMBus host issues a special command, STORE_DEFAULT_ALL, which writes the RAM data into nonvolatile memory (data flash). Fusion GUI normally uses this method to configure a device. If you are using *Fusion Digital Power Designer* software tools for on-board programming, the *Fusion Digital Power Designer* software tools must have ownership of the PMBus/I^2C bus of the target board. This method can cause unexpected behaviors on GPIO pins which can disable rails that provide power to device. It is not recommended for production programming.

- The **data flash image over PMBus and I^2C** method uses the *Fusion Digital Power Designer* software to export a data flash image in Intel Hex, CSV or S-record format. The image file can be directly downloaded into the data flash of the device through PMBus and I^2C using *Fusion Digital Power Designer* software tools or a dedicated device programmer. The new configuration takes effect after a device reset. It is recommended to use for production programming since GPIO pins are under controlled state.

Device Configuration and Programming (continued)

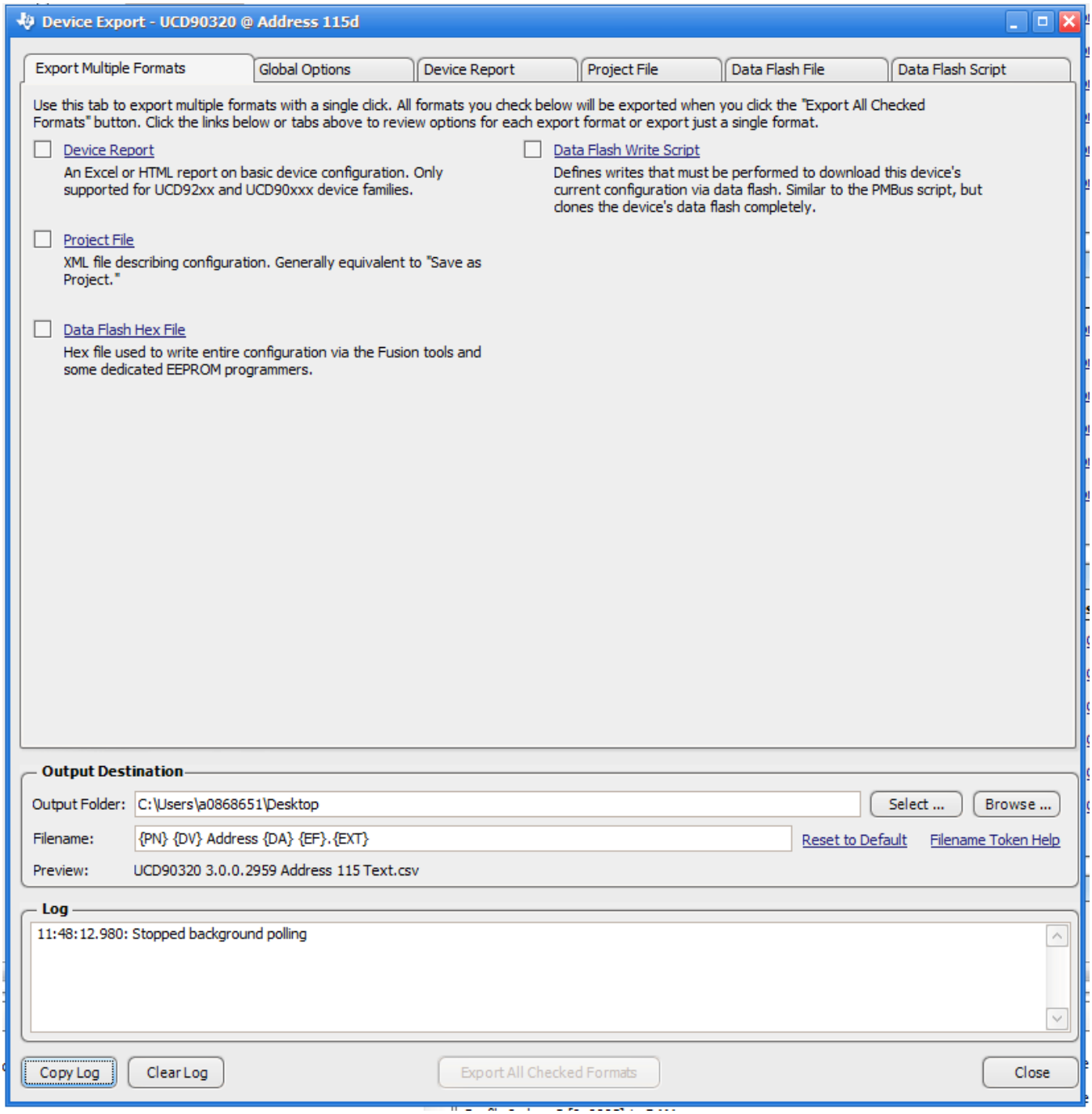


Figure 37. *Fusion Digital Power Designer* Software Configuration Export Tool

The UCD90320 must be powered when it is being programmed via the PMBus or I^2C interface. The PMBus clock and data pins must be accessible and must be pulled high to the same V33D supply that powers the device, with pullup resistors between 1 kΩ and 2 kΩ. Do not introduce additional bus capacitance less than 100 pF. When programming multiple UCD90320 devices over I^2C, programming must be done individually. Specifically, the clock and data lines must be multiplexed such that only one device is written by the programmer at a time.

Device Configuration and Programming (continued)

To update the device configuration in an operating system, the PMBus command method can be used to update thresholds, timeout periods, and dependencies while the system is operating. Because the new configuration is written into RAM, it takes effect immediately. However, pin-function-related configurations (change of rails, change of GPI/GPO functions, for example) may not work correctly until after a device reset. This delay can indicate a problem in an operating system. For example, undesired states in the GPI, GPO, or $\overline{\text{RESET}}$ pin can disable rails that provide power to the UCD90320, and thus terminate the programming process before it is completed. Using the data flash image method can overcomes this problem by directly writing new configuration into the data flash. This method allows a full configuration while the system is operating. It is not required to reset the device immediately but the UCD90320 continues to operate based on previous configuration until a device reset.

The JTAG port is compatible with IEEE Standard 1149.1-1990, *Test-Access Port and Boundary Scan Architecture* specification. The UCD90320 device supports boundary scan. The UCD90320 device supports does not support configuration programming via JTAG.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCD90320 device can be used to sequence, monitor up to 32 rails, and margin up to 24 voltage rails. With the cascading feature, up to four UCD90320 devices can manage up to 128 rails and record synchronized fault responses. Typical applications include automatic test equipment, telecommunication and networking equipment, servers, and storage systems. Device configuration can be performed using the *Fusion Digital Power Designer* software provided by TI. No coding skill is required.

9.2 Typical Application

Figure 38 shows a simplified system diagram. For simplification, this diagram shows only three rails, but each UCD90320 device can manage up to 32 rails.

Typical Application (continued)

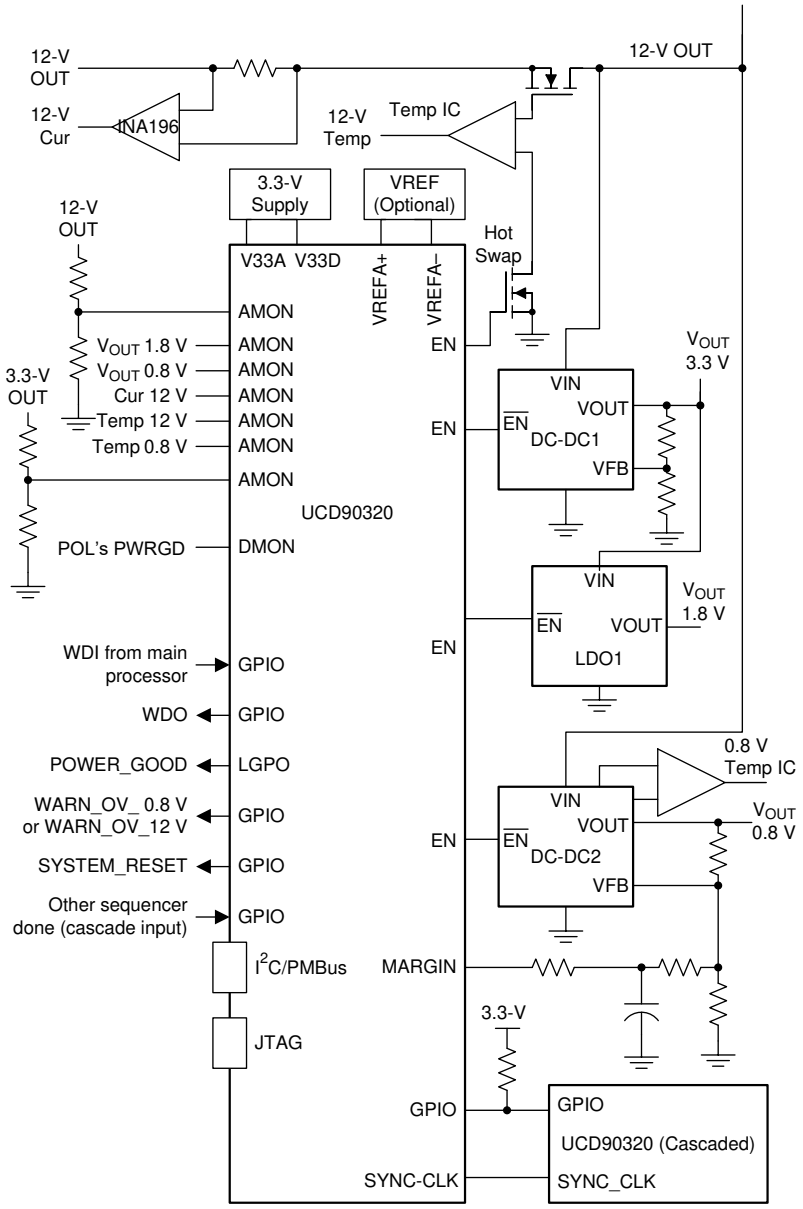


Figure 38. Simplified System Diagram

Typical Application (continued)

9.2.1 Design Requirements

UCD90320 requires decoupling capacitors on the V33D, V33A, BPCAP, and (if applicable) VREFA+ pins. The capacitance values for V33A, BPCAP, and VREFA+ are specified in the *Electrical Characteristics*. Consider these capacitor design configurations as options.

- Three 1-µF X7R ceramic capacitors in parallel with two 0.1-µF X7R ceramic capacitors for BPCAP decoupling
- Two 1-µF X7R ceramic capacitors in parallel with four 0.1-µF X7R ceramic capacitors and two 0.01-µF X7R ceramic capacitors for V33D decoupling
- One 1-µF X7R ceramic capacitor in parallel with one 0.1-µF X7R ceramic capacitor and one 0.01-µF X7R ceramic capacitor for V33A decoupling. A 1-Ω resistor can placed between V33D and V33A to decouple the noise on V33D from V33A.
- One 1-µF X7R ceramic capacitor in parallel with one 0.01-µF X7R ceramic capacitor for VREFA+ decoupling (if used)
- Place decoupling capacitors as close to the device as possible.
- If an application does not use the $\overline{\text{RESET}}$ signal, the $\overline{\text{RESET}}$ pin must be tied to V33D, either by direct connection to the nearest V33D pin (Pin F10), or by a R-C circuit as shown in Figure 39. The R-C circuit in Figure 39 can be also used to delay reset at power up. If an application uses the $\overline{\text{RESET}}$ external pin, the trace of the $\overline{\text{RESET}}$ signal must be kept as short as possible. Be sure to place any components connected to the RESET signal as close to the device as possible.
- TI recommends to maintain at least 200-Ω resistance between a low-impedance analog input and a AMON pin. For example, when monitoring a rail voltage without resistor divider, it is recommended to place a 200-Ω resistor at the AMON pin, as shown in Figure 40.
- PMBus commands (project file, PMBus write script file) method is not recommended for the production programming since GPIO pins can have unexpected behaviors which can disable rails that provide power to device. Data flash hex file or data flash script file shall be used for production programming since GPIO pins are under controlled state.
- It is mandatory that the V33D power be stable and no device reset be fired during the device programming. Data flash can be corrupted if failed to follow these rules.

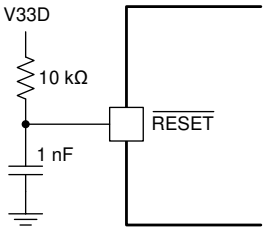


Figure 39. $\overline{\text{RESET}}$ Pin With R-C Network

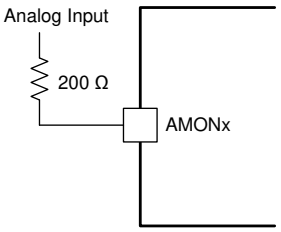


Figure 40. Example of Analog Inputs

9.2.2 Detailed Design Procedure

The *Fusion Digital Power Designer* software can be used to design the device configuration online or offline (with or without a UCD90320 device connected to the computer). In offline mode, the software prompts the user to create or open a project file (.xml) at launch. In online mode, the software automatically detects the device via the PMBus interface and extracts the configuration data from the device. A USB Interface Adapter EVM available from TI is required to connect *Fusion Digital Power Designer* software to PMBus.

The general design steps are included. Details of the steps are described in the *Detailed Description*, and are easily accessed within the *Fusion Digital Power Designer* software.

1. Rail setup
2. Rail monitoring configuration
3. GPI configuration
4. Rail sequence configuration
5. Fault response configuration
6. GPO configuration

Typical Application (continued)

7. Margining configuration
8. Other configurations including but not limited to:
   - Pin Selected Rail States
   - Watchdog Timer
   - System Reset
   - Sync Clock
   - Fault Pins

Click **Write to Hardware** to apply the changes. In online mode, then click **Store RAM to Flash** to permanently store the new configuration into the data flash of the device.

9.2.3 Application Curves

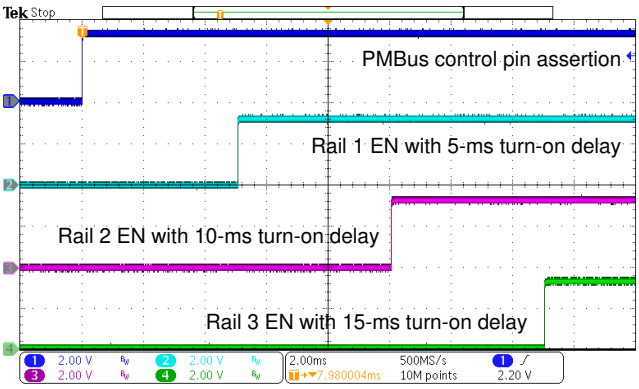


Figure 41. Start-Up Waveforms

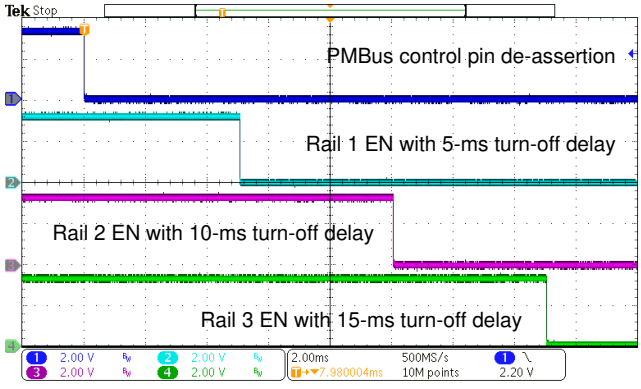


Figure 42. Shut-Down Waveforms

10 Power Supply Recommendations

Power the UCD90320 device from a 3.3-V power supply.

If internal reference is used, V33A acts as ADC reference and is assumed to be exactly 3.3 V. Any input voltage deviation from 3.3 V introduces an error to ADC reference and to the ADC results. Therefore, the 3.3-V power supply must be tightly regulated and allow only a very small voltage fluctuation (including voltage ripple and voltage deviation caused by load transients).

If external reference is used, the 3.3-V power supply needs to meet only the minimum requirements specified in the *Recommended Operating Conditions* and *Electrical Characteristics*.

11 Layout

11.1 Layout Guidelines

- Place the decoupling capacitors as close as possible to the device.
- Connect the BPCAP decoupling capacitors as close as possible to pin D6.
- MARGIN pins output PWM signals that have fast-edges. Route these signals away from sensitive analog signals. It is a good practice to place resistor R4 and capacitor C1 (as shown in Figure 22) as close as possible to the MARGIN pin, minimizing the propagation distance of the fast-edge PWM signals on the PCB.
- Resistor R3 can be placed near the power supply feedback node to isolate the feedback node from noise sources on the PCB. If resistor R4 and capacitor C1 cannot be located close to the MARGIN pin, add a termination resistor in series with a value between 20 Ω and 33 Ω. Locate it near the MARGIN pin.

11.2 Layout Example

The UCD90320 device is available in a 169-pin BGA package. If the design calls for the device to be mounted on the top layer, decoupling capacitors can be placed on the bottom layer to allow room for top-layer trace routing. The following layout example describes this strategy. Figure 43 shows bottom-layer component placement from the top-view. In addition to Figure 43, consider these important suggestions.

1. Use a uniform ground plane to connect DVSS, AVSS, and VREFA– pins.
2. Connect all four BPCAP pins to a common internal-layer copper area.
3. AVSS and VREFA– pins can be connected to a common internal-layer copper area.

Figure 43 shows a typical application with the UCD90320 device mounted on the top layer and the components placed on the bottom layer.

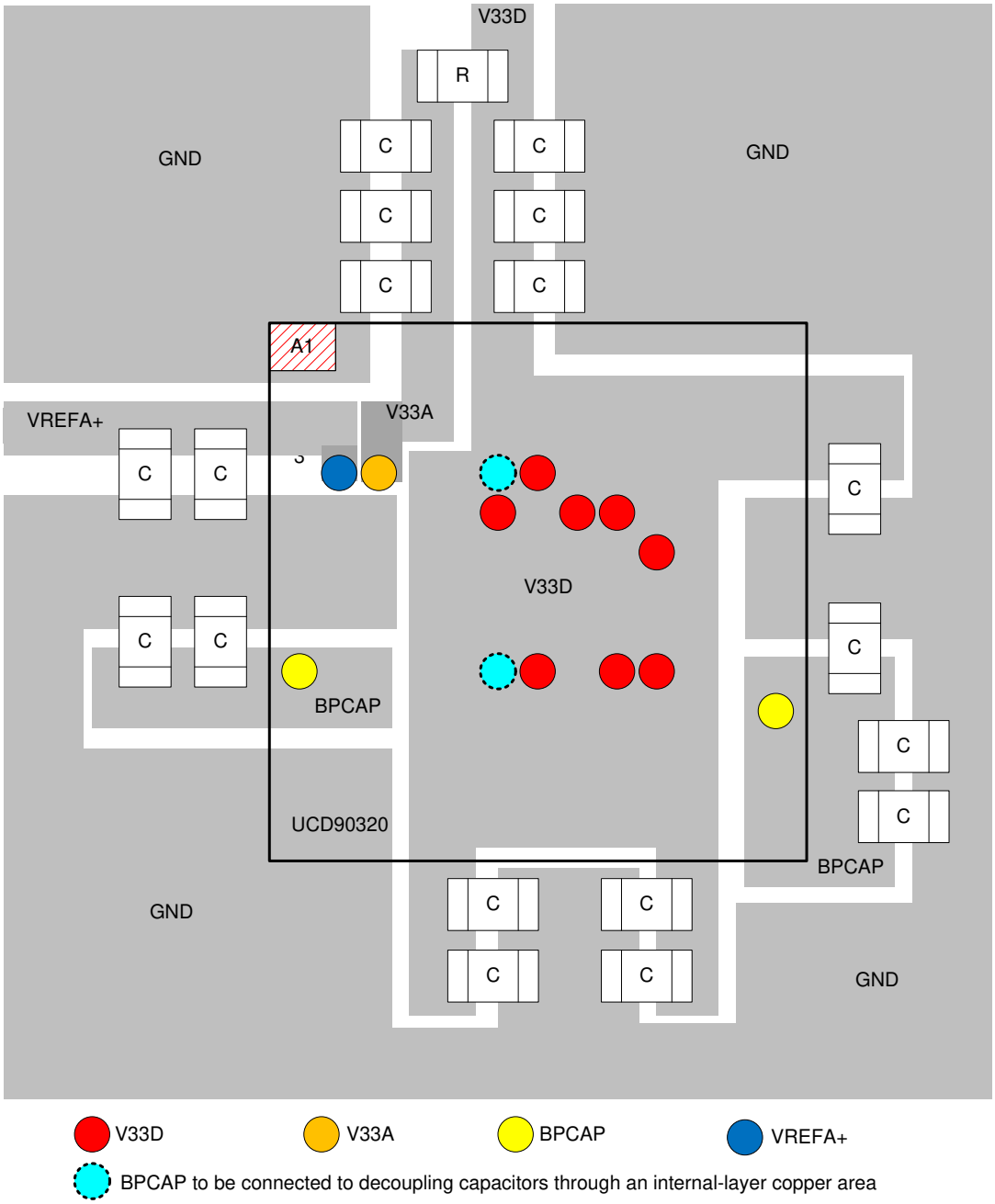


Figure 43. Layout Example

12 Device and Documentation Support

12.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Trademarks

TI Fusion Digital Power, E2E are trademarks of Texas Instruments.
PMBus is a trademark of SMIF, Inc..
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCD90320ZWSR	ACTIVE	NFBGA	ZWS	169	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	UCD90320	Samples
UCD90320ZWST	ACTIVE	NFBGA	ZWS	169	250	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	UCD90320	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

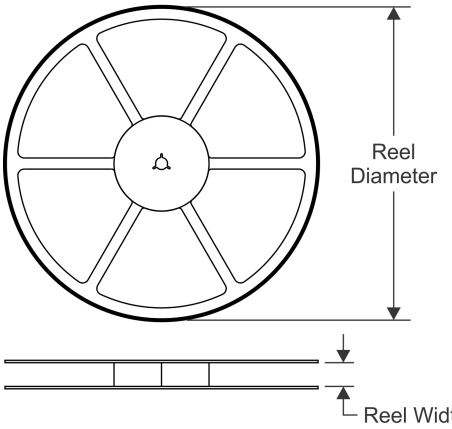
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

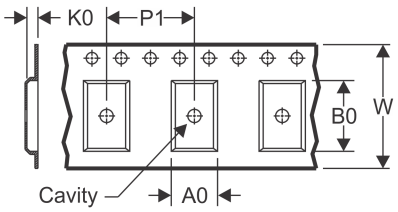
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

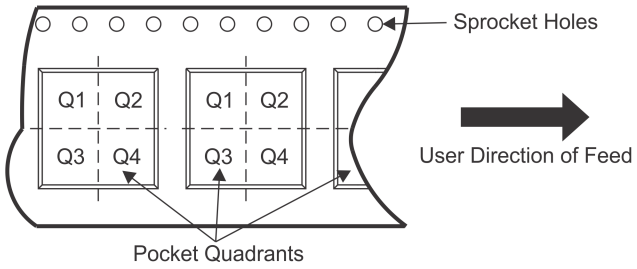


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

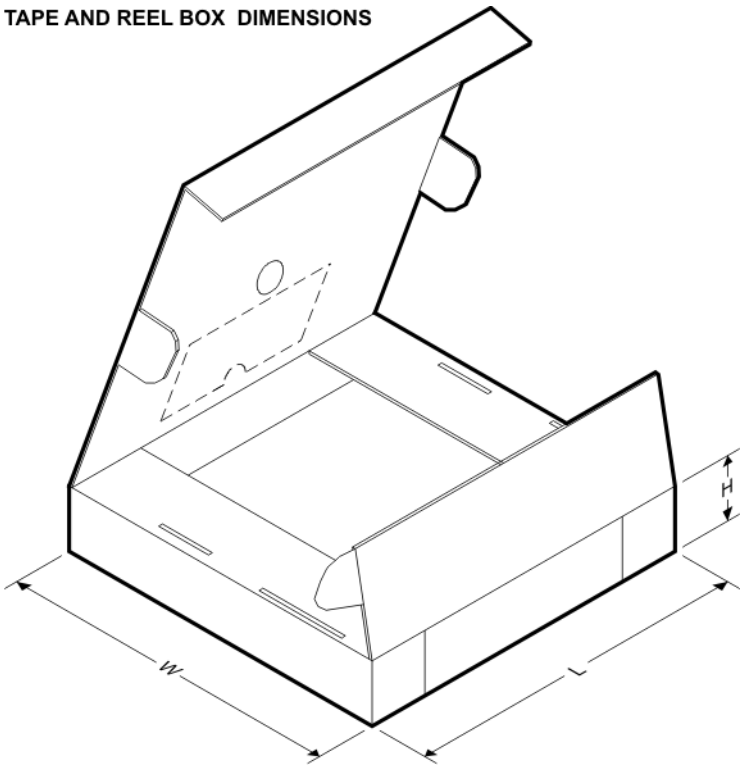
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD90320ZWSR	NFBGA	ZWS	169	1000	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1
UCD90320ZWST	NFBGA	ZWS	169	250	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

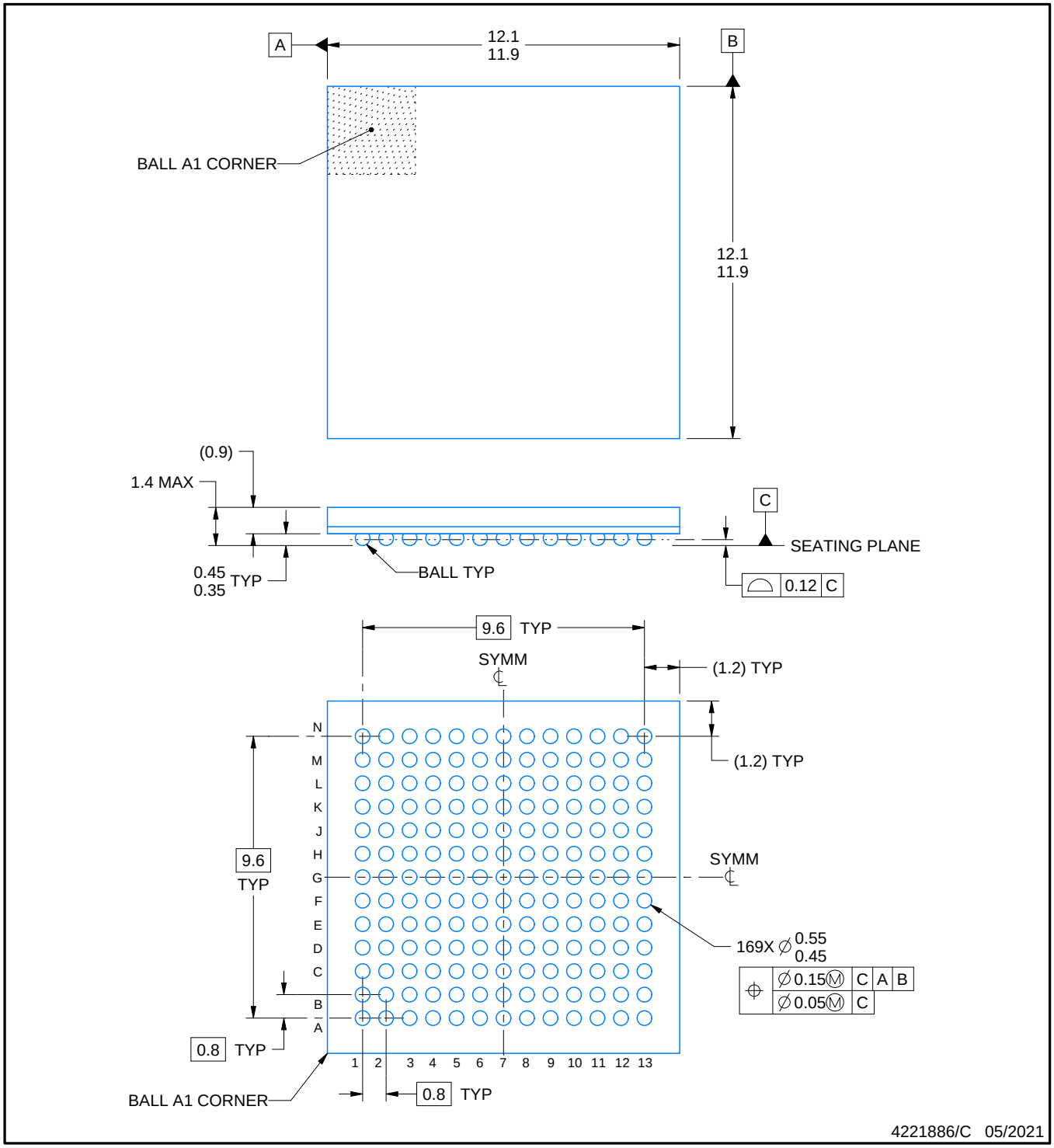
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD90320ZWSR	NFBGA	ZWS	169	1000	336.6	336.6	41.3
UCD90320ZWST	NFBGA	ZWS	169	250	336.6	336.6	41.3

PACKAGE OUTLINE

ZWS0169A

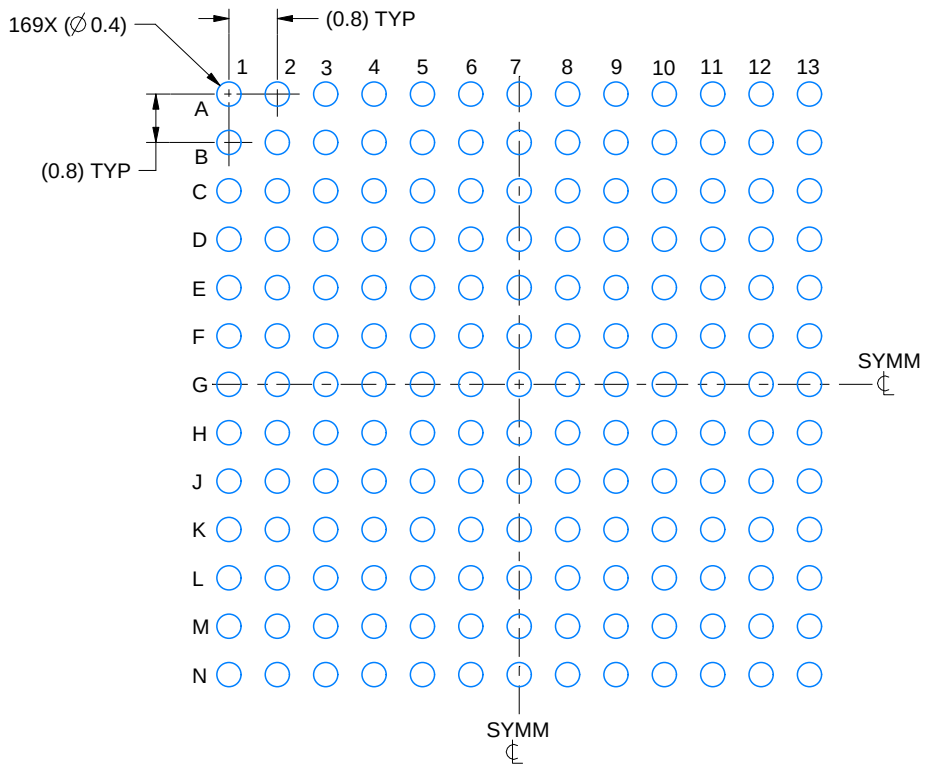
NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY

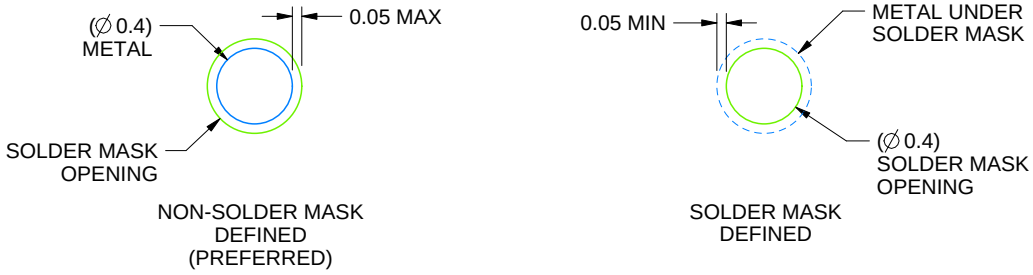


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X

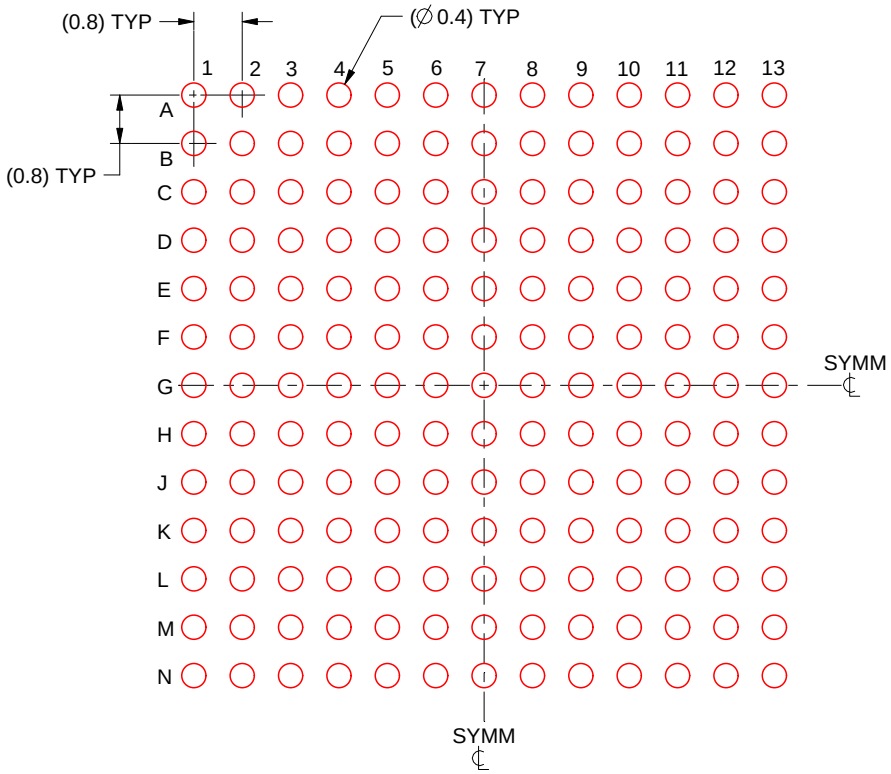


SOLDER MASK DETAILS
NOT TO SCALE

4221886/C 05/2021

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SSZA002 (www.ti.com/lit/ssza002).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4221886/C 05/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265