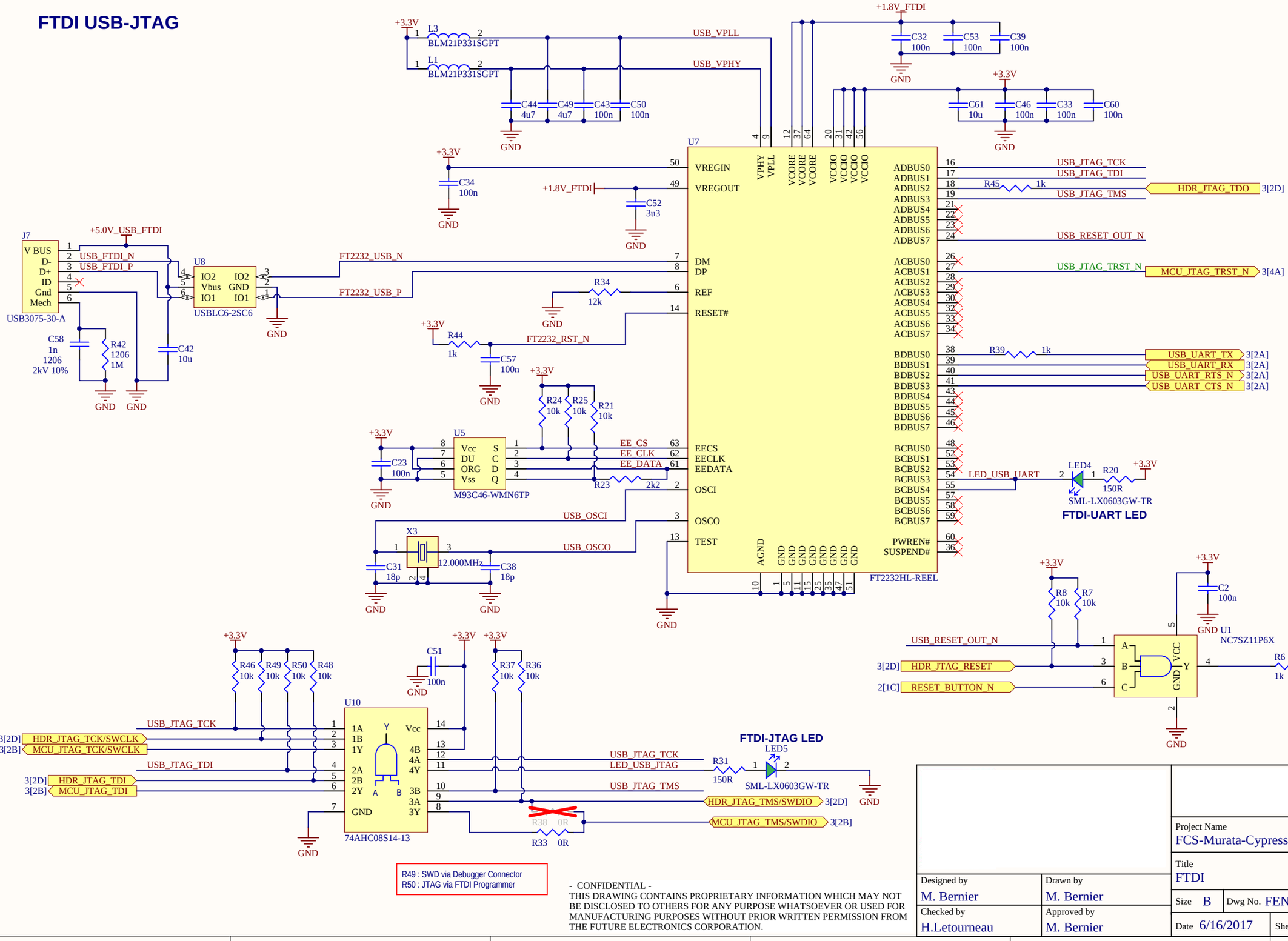
FTDI USB-JTAG



Designed by M. Bernier	Drawn by M. Bernier
Checked by H.Letourneau	Approved by M. Bernier

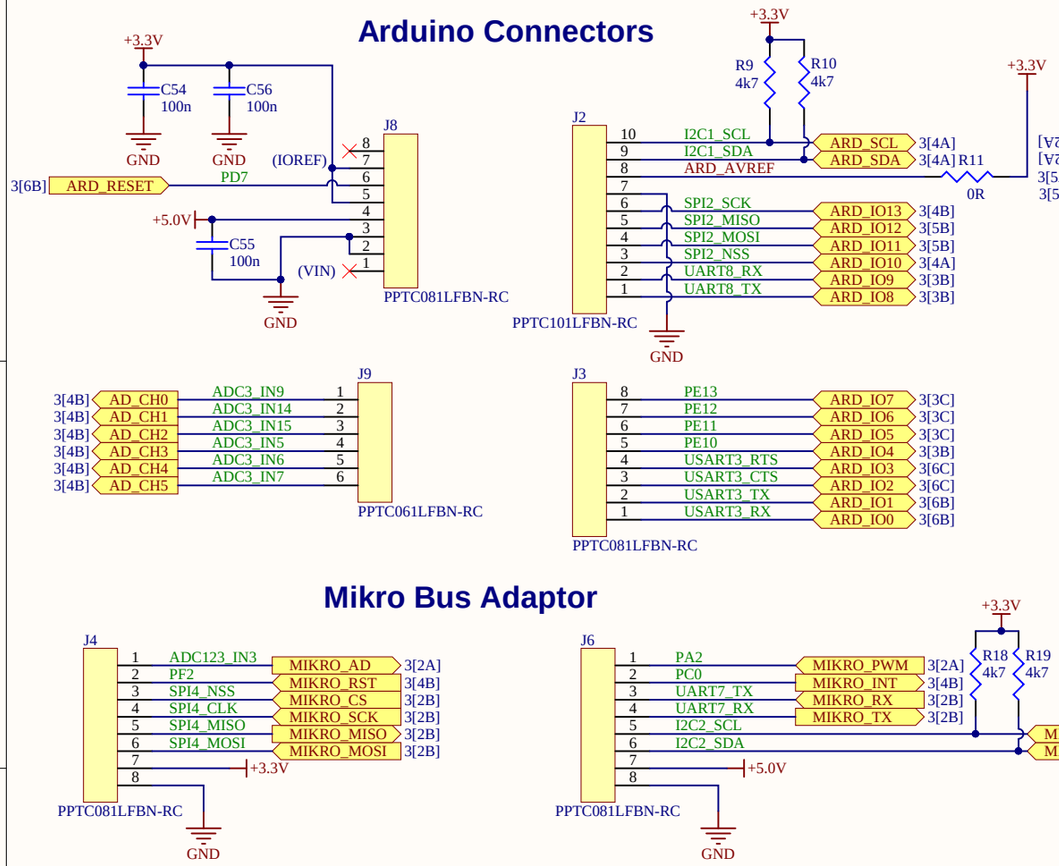
Project Name: FCS-Murata-Cypress Dev kit Rev 1

Title: FTDI

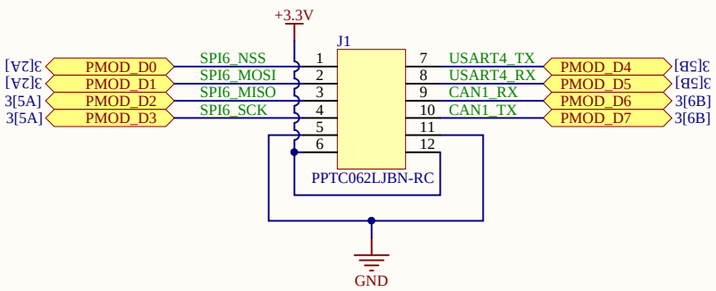
Size B | Dwg No. FEN-413458-SCH-R1 | Rev 1

Date 6/16/2017 | Sheet 1 of 4 | Variant: FCS-Murata-Cypress Dev kit

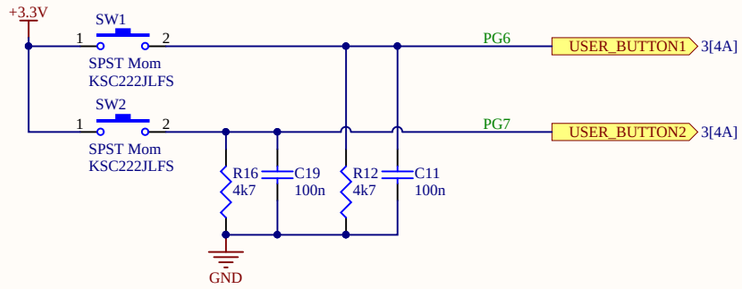
Arduino Connectors



PMOD Connector

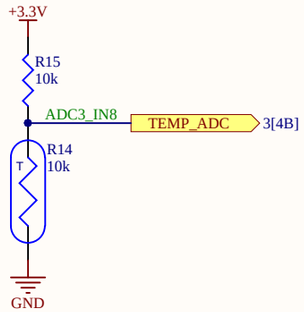


USER Buttons

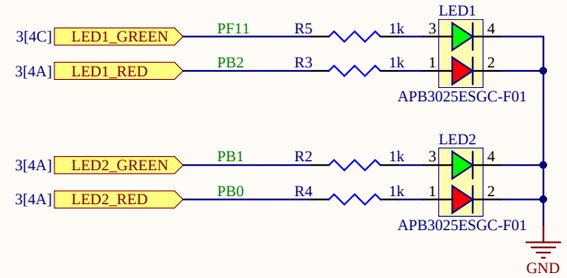


Mikro Bus Adaptor

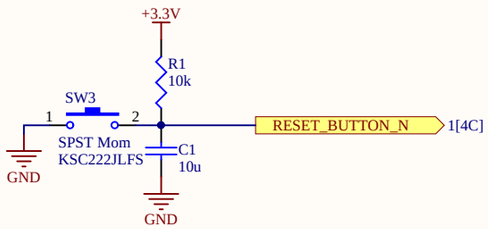
Temperature Sensor



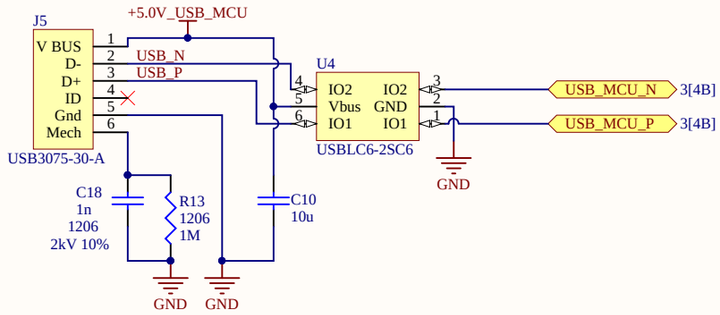
USER LEDs



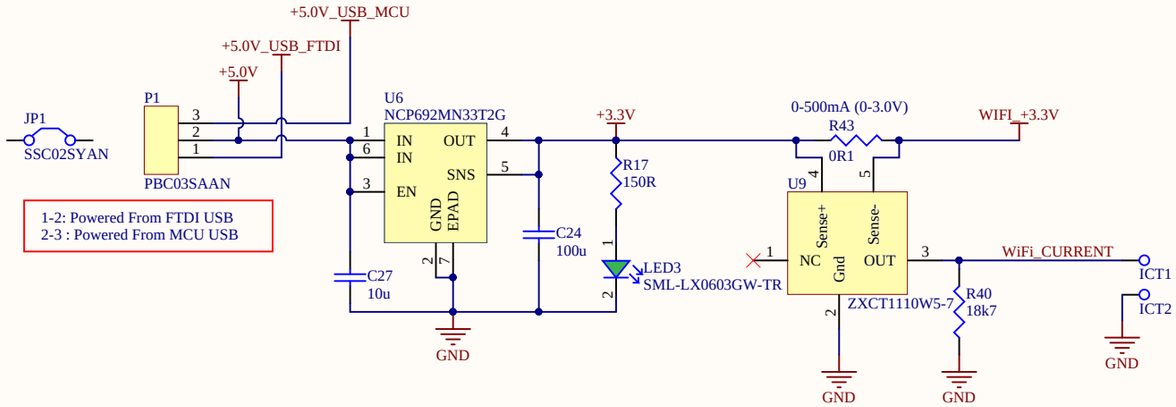
RESET



MCU USB Device



Power Supply



W1 MountHole 120mil

F1 Fiducial

Designed by M. Bernier	Drawn by M. Bernier
Checked by H.Letourneau	Approved by M. Bernier

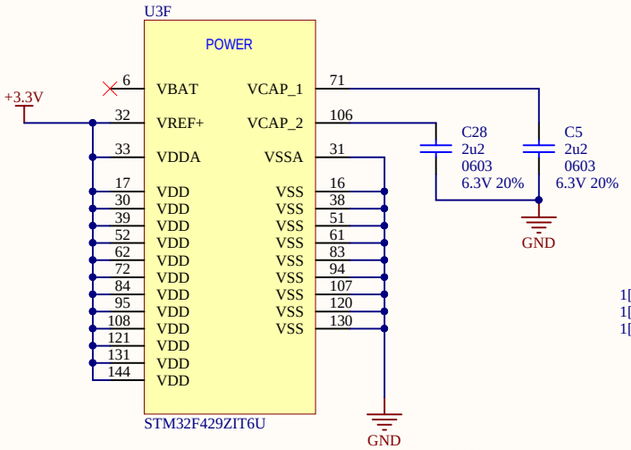
Project Name: FCS-Murata-Cypress Dev kit Rev 1

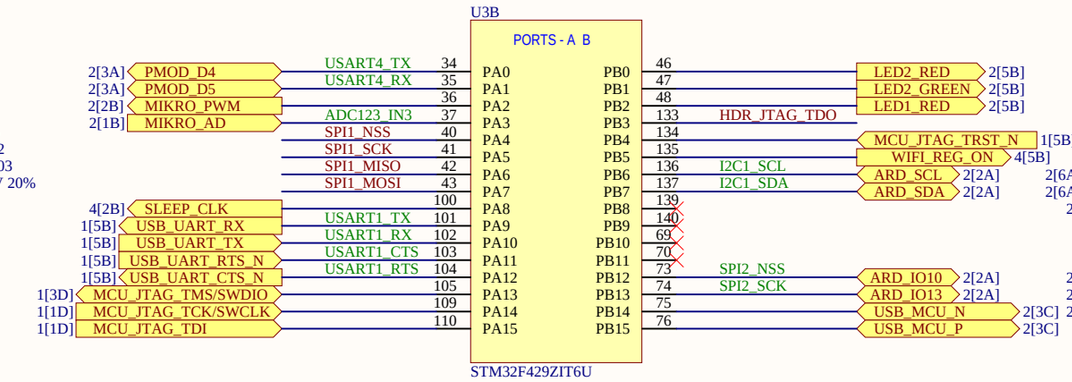
Title: Power and Interconnect

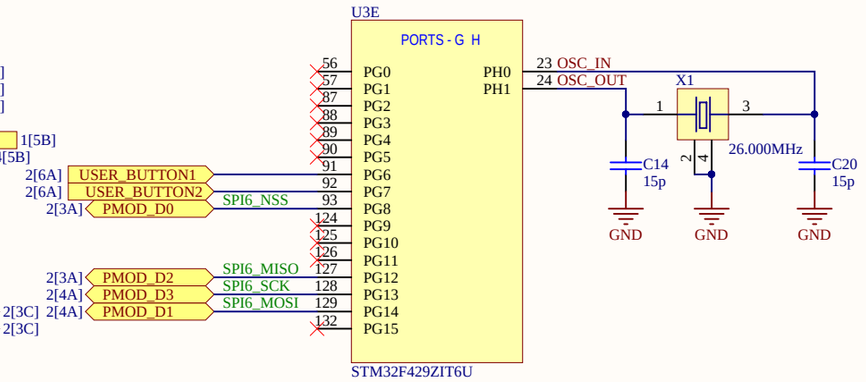
Size B | Dwg No. FEN-413458-SCH-R1 | Rev 1

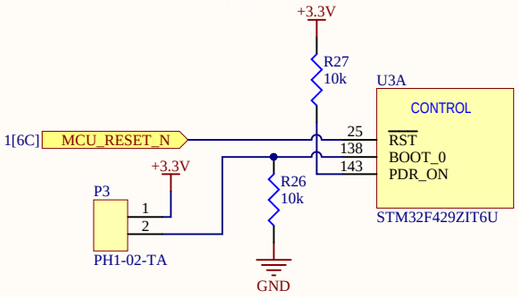
Date 6/20/2017 | Sheet 2 of 4 | Variant: FCS-Murata-Cypress Dev kit

STM32F429ZIT6

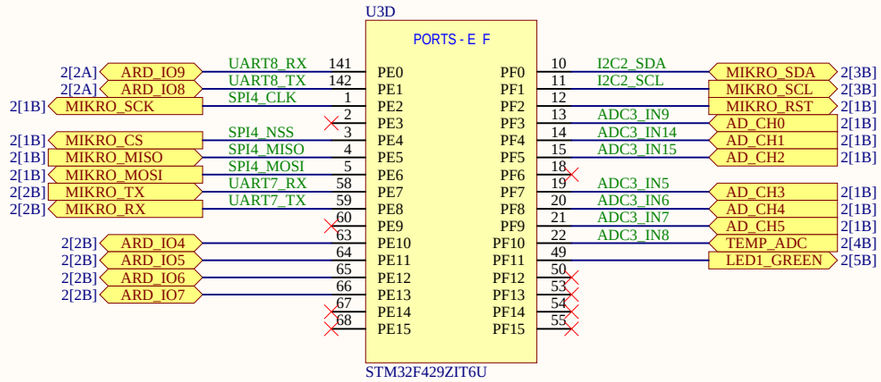


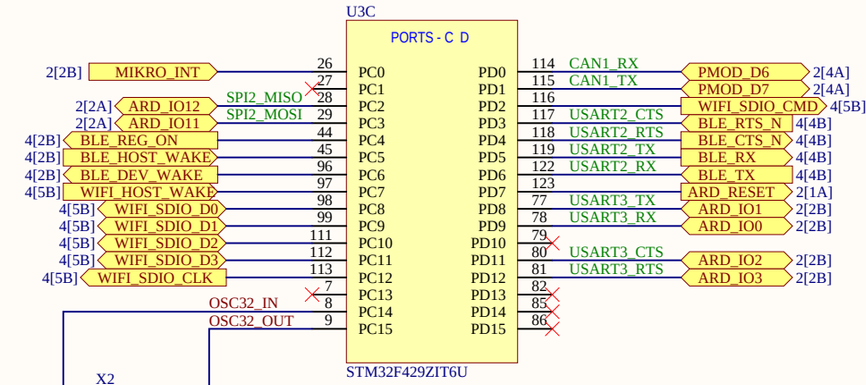




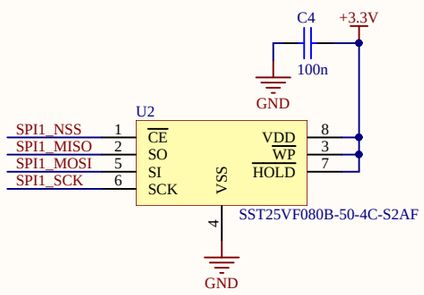


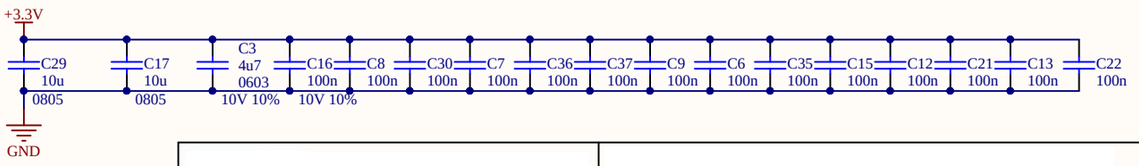
Populate jumper for programming MCU through USB using ST utility



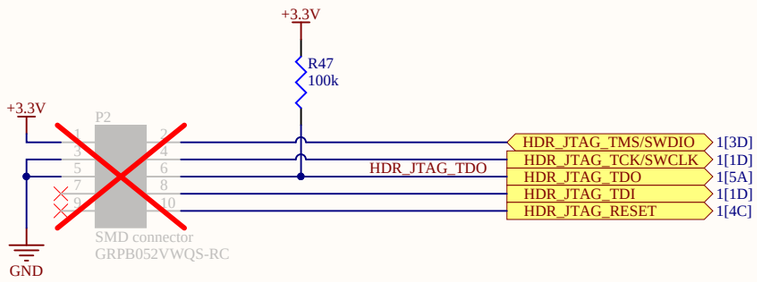


Serial Flash 8Mbit





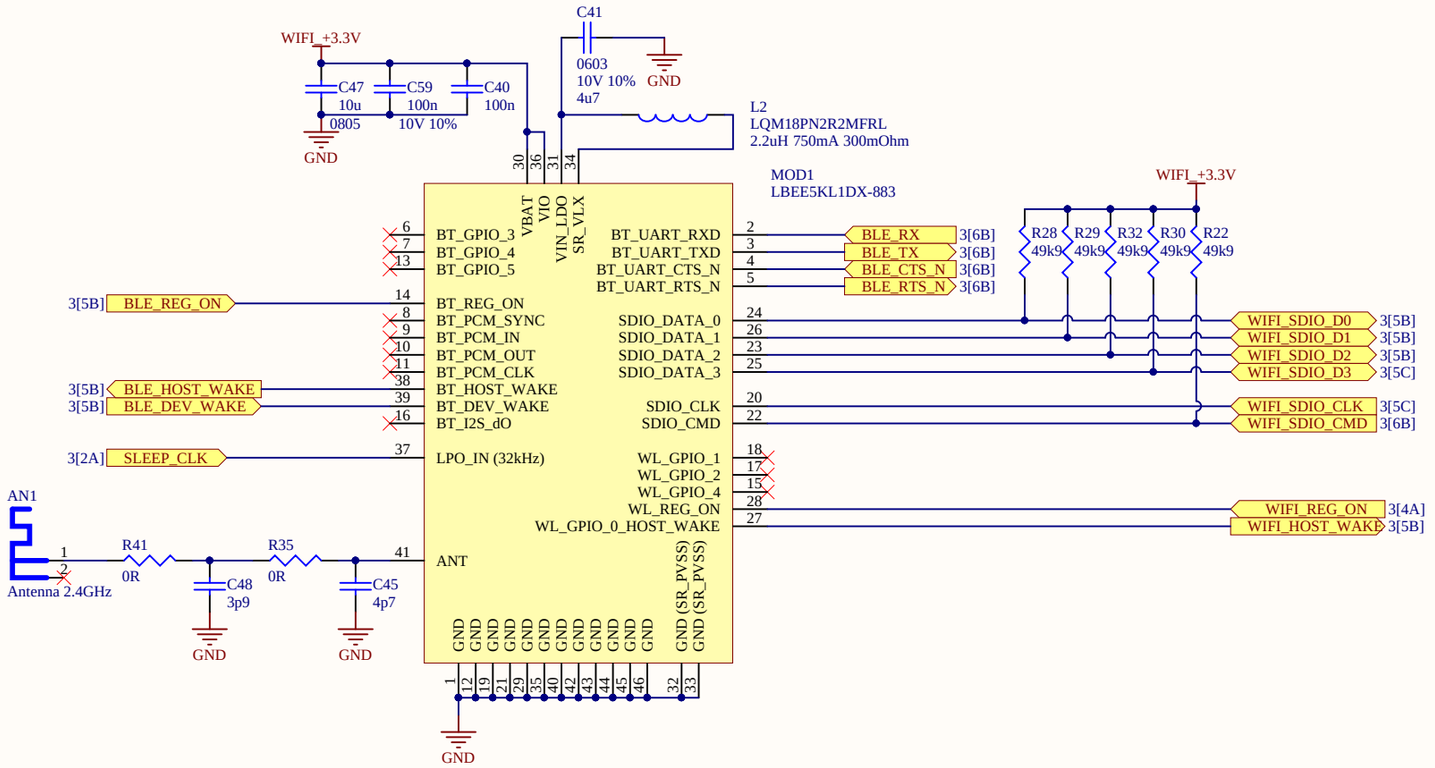
Cortex-M Debug Connector (SWD)



Designed by	M. Bernier
Drawn by	M. Bernier
Checked by	H.Letourneau
Approved by	M. Bernier

Project Name: FCS-Murata-Cypress Dev kit Rev 1
Title: Microcontroller
Size: B | Dwg No. FEN-413458-SCH-R1 | Rev 1
Date: 6/16/2017 | Sheet 3 of 4 | Variant: FCS-Murata-Cypress Dev kit

WiFi and Bluetooth Module



Do not populate matching network components

Designed by	M. Bernier
Drawn by	M. Bernier
Checked by	H.Letourneau
Approved by	M. Bernier

Project Name: FCS-Murata-Cypress Dev kit Rev 1

Title: WIFI

Size: B | Dwg No. FEN-413458-SCH-R1 | Rev 1

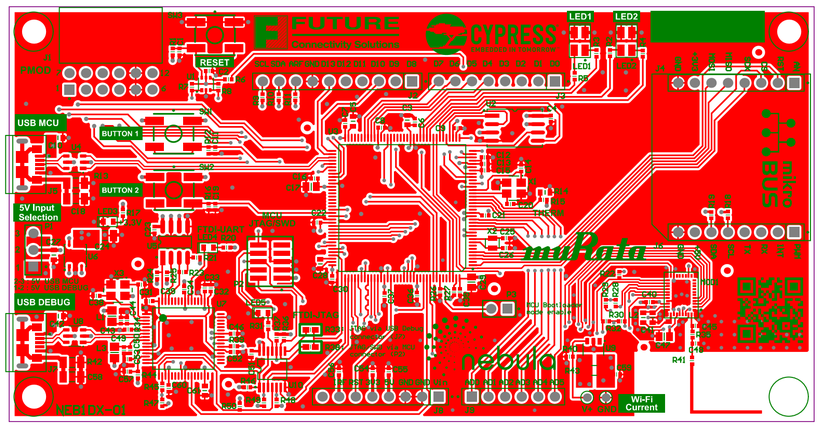
Date: 6/14/2017 | Sheet 4 of 4 | Variant: FCS-Murata-Cypress Dev kit

Layers	Top Layer				Instructions (GM16)	Top Overlay

Impedance Requirements

	Impedance 50 Ohms	Impedance 90 Ohms (Diff)		Co-planar Waveguide : 50 Ohms	
Layer	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
Top Layer	9 mils	8 mils	9 mils	10 mils	30 mils
Bottom Layer	9 mils	8 mils	9 mils	10 mils	30 mils

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	2.10mil		
4	Dielectric1	FR-4 HTg	6.00mil	4.5	
5	GND	Copper	1.40mil		
6	Dielectric3	FR-4 HTg	45.00mil	4.5	
7	Power	Copper	1.40mil		
8	Dielectric2	FR-4 HTg	6.00mil	4.5	
9	Bottom Layer	Copper	2.10mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)

2. BASE MATERIAL - FR4 High Tg [X] Metal Core [ ] Other [ ] _____
   - Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR FINISHED STACK-UP DETAIL

4. PLATING - 0.5oz [ ] 0.75oz [ ] 1oz [X] Other [ ] _____

5. FINISH - HASL RoHS [X] HASL [ ] Immersion Silver [ ] Immersion Tin [ ] ENIG [ ]
   Other [ ] _____

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
   - GREEN [ ] WHITE [ ] BLUE [X] Other [ ] _____

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
   - TOP/BOTTOM [ ] TOP ONLY [X] BOTTOM ONLY [ ] NONE [ ]
   - WHITE [X] BLACK [ ] Other [ ] _____

8. IMPEDANCE CONTROL - NO [ ] YES [X] SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
    - ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED IN THE DRILL LEGEND

14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD TO DIMENSION SHOWN

Designed by: M. Bernier	Drawn by: M. Bernier	Project #	FCS-Murata-Cypress Dev kit
Checked by: H.Letourneau	Approved by: M. Bernier	Title:	FCS-Murata-Cypress Dev kit
		Size: B	DWG NO: FEN-413458-PCB-R1 REV: 1
		Date: 6/20/2017	Sheet 1 of 1

Layers		GND			Instructions (GM16)

Impedance Requirements

	Impedance 50 Ohms	Impedance 90 Ohms (Diff)		Co-planar Waveguide : 50 Ohms	
Layer	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
Top Layer	9 mils	8 mils	9 mils	10 mils	30 mils
Bottom Layer	9 mils	8 mils	9 mils	10 mils	30 mils

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
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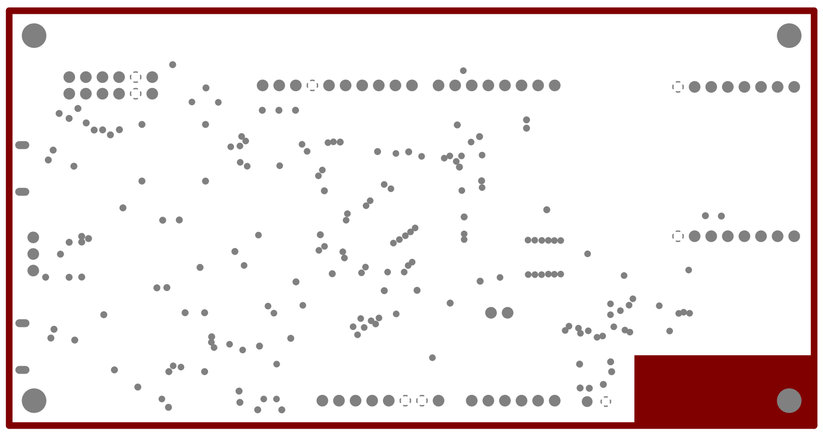
5	GND	Copper	1.40mil		
6	Dielectric3	FR-4 HTg	45.00mil	4.5	
7	Power	Copper	1.40mil		
8	Dielectric2	FR-4 HTg	6.00mil	4.5	
9	Bottom Layer	Copper	2.10mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



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   Other [ ] _____

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
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7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
   - TOP/BOTTOM [ ] TOP ONLY [X] BOTTOM ONLY [ ] NONE [ ]
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Designed by: M. Bernier	Drawn by: M. Bernier
Checked by: H.Letourneau	Approved by: M. Bernier

Project #	FCS-Murata-Cypress Dev kit	
Title:	FCS-Murata-Cypress Dev kit	
Size: B	DWG NO: FEN-413458-PCB-R1	REV: 1
Date: 6/20/2017	Sheet 1 of 1	

Layers			Power		Instructions (GM16)

Impedance Requirements

	Impedance 50 Ohms	Impedance 90 Ohms (Diff)		Co-planar Waveguide : 50 Ohms	
Layer	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
Top Layer	9 mils	8 mils	9 mils	10 mils	30 mils
Bottom Layer	9 mils	8 mils	9 mils	10 mils	30 mils

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
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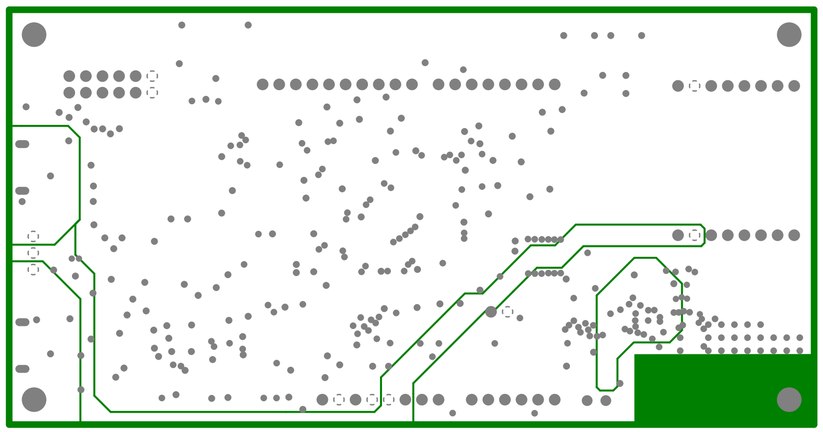
7	Power	Copper	1.40mil		
8	Dielectric2	FR-4 HTg	6.00mil	4.5	
9	Bottom Layer	Copper	2.10mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



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3. COPPER FOIL WEIGHT - SEE TABLE FOR FINISHED STACK-UP DETAIL

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5. FINISH - HASL RoHS [X] HASL [ ] Immersion Silver [ ] Immersion Tin [ ] ENIG [ ]
   Other [ ] _____

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
   - GREEN [ ] WHITE [ ] BLUE [X] Other [ ] _____

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
   - TOP/BOTTOM [ ] TOP ONLY [X] BOTTOM ONLY [ ] NONE [ ]
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Designed by: M. Bernier	Drawn by: M. Bernier
Checked by: H.Letourneau	Approved by: M. Bernier

Project #	FCS-Murata-Cypress Dev kit	
Title:	FCS-Murata-Cypress Dev kit	
Size: B	DWG NO: FEN-413458-PCB-R1	REV: 1
Date: 6/20/2017	Sheet 1 of 1	

Layers				Bottom Layer

Instructions (GM16)

Bottom Overlay

Impedance Requirements

	Impedance 50 Ohms	Impedance 90 Ohms (Diff)		Co-planar Waveguide : 50 Ohms	
Layer	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
Top Layer	9 mils	8 mils	9 mils	10 mils	30 mils
Bottom Layer	9 mils	8 mils	9 mils	10 mils	30 mils

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
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5	GND	Copper	1.40mil		
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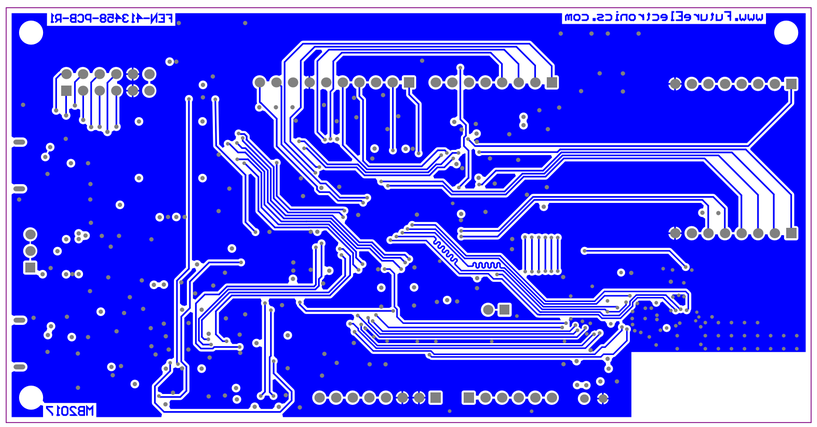
7	Power	Copper	1.40mil		
8	Dielectric2	FR-4 HTg	6.00mil	4.5	
9	Bottom Layer	Copper	2.10mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



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4. PLATING - 0.5oz [ ] 0.75oz [ ] 1oz [X] Other [ ] _____

5. FINISH - HASL RoHS [X] HASL [ ] Immersion Silver [ ] Immersion Tin [ ] ENIG [ ]
   Other [ ] _____

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
   - GREEN [ ] WHITE [ ] BLUE [X] Other [ ] _____

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
   - TOP/BOTTOM [ ] TOP ONLY [X] BOTTOM ONLY [ ] NONE [ ]
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Designed by: M. Bernier	Drawn by: M. Bernier
Checked by: H.Letourneau	Approved by: M. Bernier

Project #	FCS-Murata-Cypress Dev kit	
Title:	FCS-Murata-Cypress Dev kit	
Size: B	DWG NO: FEN-413458-PCB-R1	REV: 1
Date: 6/20/2017	Sheet 1 of 1	

Layers	Top Layer			Bottom Layer	Instructions (GM16) Board Outline (GM14)	Top Overlay Bottom Overlay

Impedance Requirements

	Impedance 50 Ohms	Impedance 90 Ohms (Diff)		Co-planar Waveguide : 50 Ohms	
Layer	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
Top Layer	9 mils	8 mils	9 mils	10 mils	30 mils
Bottom Layer	9 mils	8 mils	9 mils	10 mils	30 mils

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
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5	GND	Copper	1.40mil		
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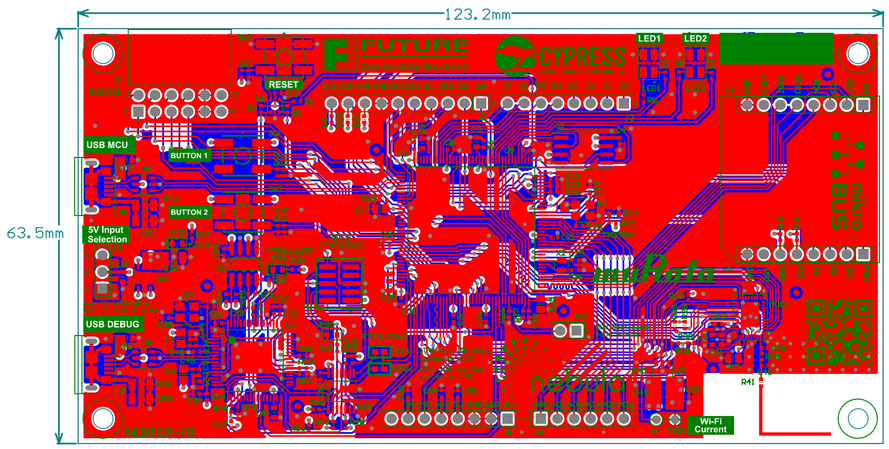
7	Power	Copper	1.40mil		
8	Dielectric2	FR-4 HTg	6.00mil	4.5	
9	Bottom Layer	Copper	2.10mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)

2. BASE MATERIAL - FR4 High Tg [X] Metal Core [ ] Other [ ] _____
   - Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR FINISHED STACK-UP DETAIL

4. PLATING - 0.5oz [ ] 0.75oz [ ] 1oz [X] Other [ ] _____

5. FINISH - HASL RoHS [X] HASL [ ] Immersion Silver [ ] Immersion Tin [ ] ENIG [ ]
   Other [ ] _____

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
   - GREEN [ ] WHITE [ ] BLUE [X] Other [ ] _____

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
   - TOP/BOTTOM [ ] TOP ONLY [X] BOTTOM ONLY [ ] NONE [ ]
   - WHITE [X] BLACK [ ] Other [ ] _____

8. IMPEDANCE CONTROL - NO [ ] YES [X] SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
    - ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

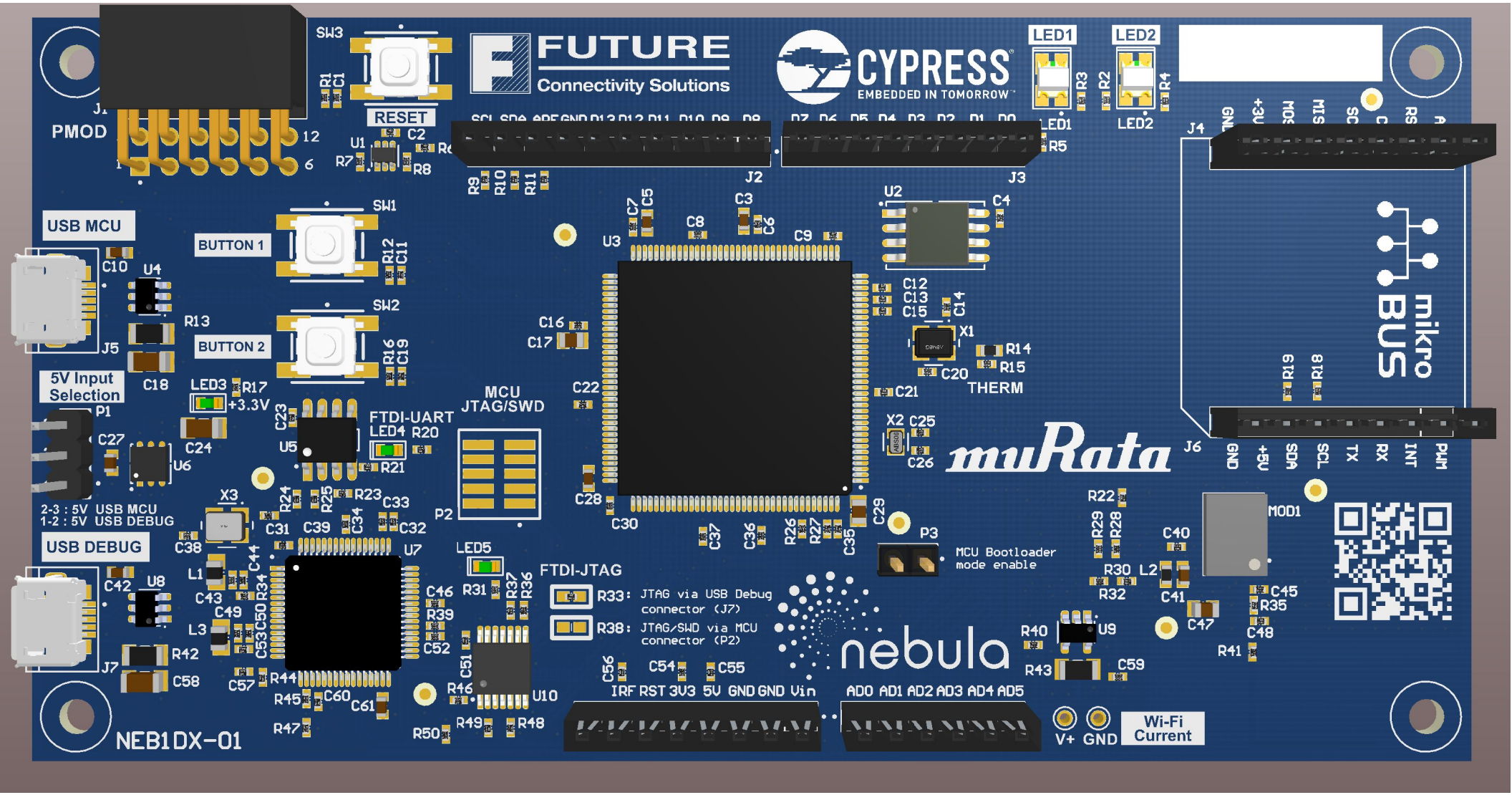
11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED IN THE DRILL LEGEND

14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD TO DIMENSION SHOWN

Designed by: M. Bernier	Drawn by: M. Bernier	Project #	FCS-Murata-Cypress Dev kit
Checked by: H.Letourneau	Approved by: M. Bernier	Title:	FCS-Murata-Cypress Dev kit
		Size: B	DWG NO: FEN-413458-PCB-R1 REV: 1
		Date: 6/20/2017	Sheet 1 of 1


FUTURE
Connectivity Solutions
CYPRESS
EMBEDDED IN TOMORROW™
PMOD
RESET
SW1
BUTTON 1
SW2
BUTTON 2
USB MCU
5V Input Selection
2-3 : 5V USB MCU
1-2 : 5V USB DEBUG
USB DEBUG
LED1
LED2
LED3
LED4
LED5
+3.3V
FTDI-UART
MCU JTAG/SWD
FTDI-JTAG
R33: JTAG via USB Debug connector (J7)
R38: JTAG/SWD via MCU connector (P2)
MCU Bootloader mode enable
THERM
mikro BUS
muRata
nebula
MOD1
Wi-Fi Current
V+
GND
NEB1DX-01