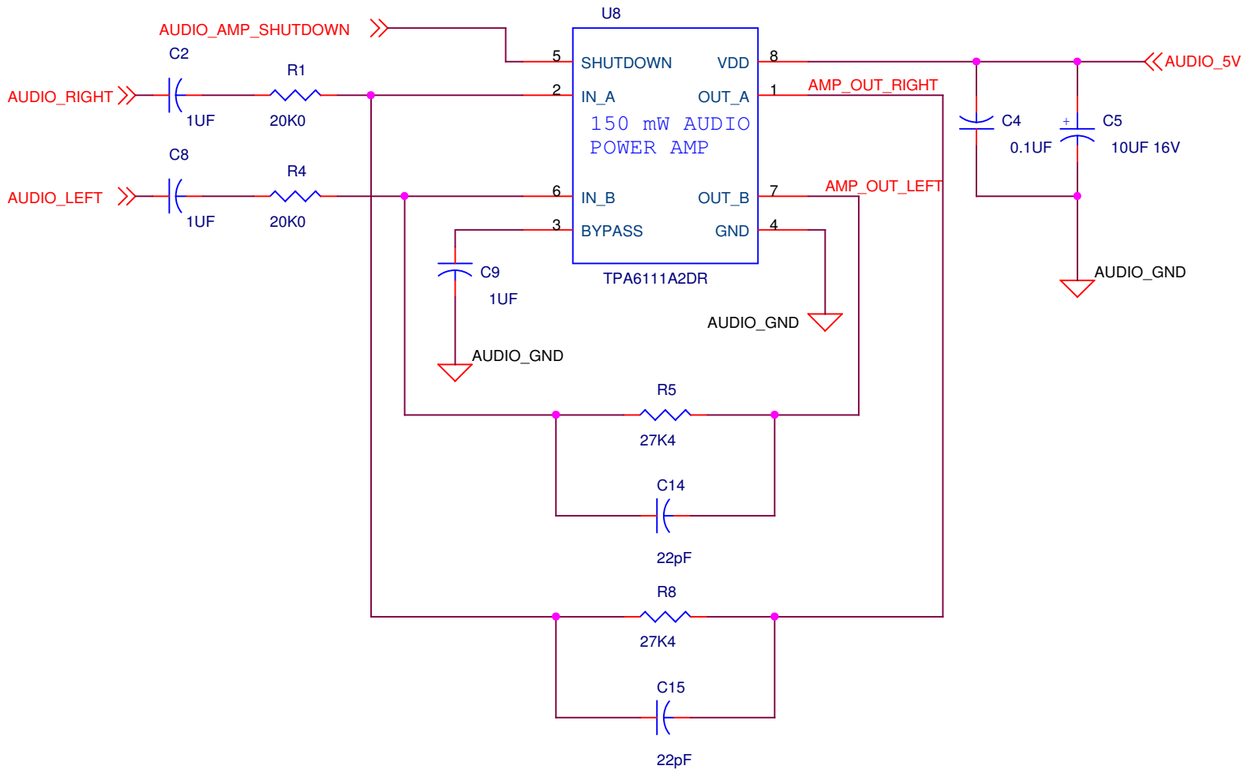

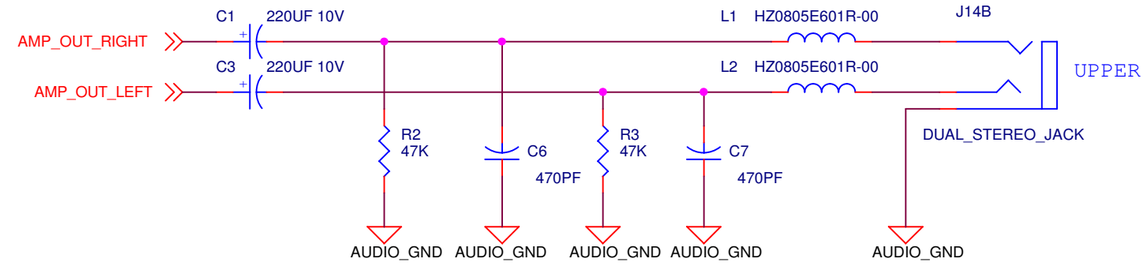

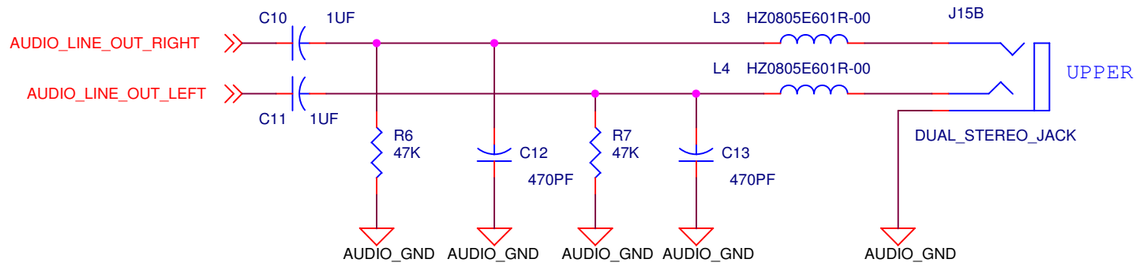

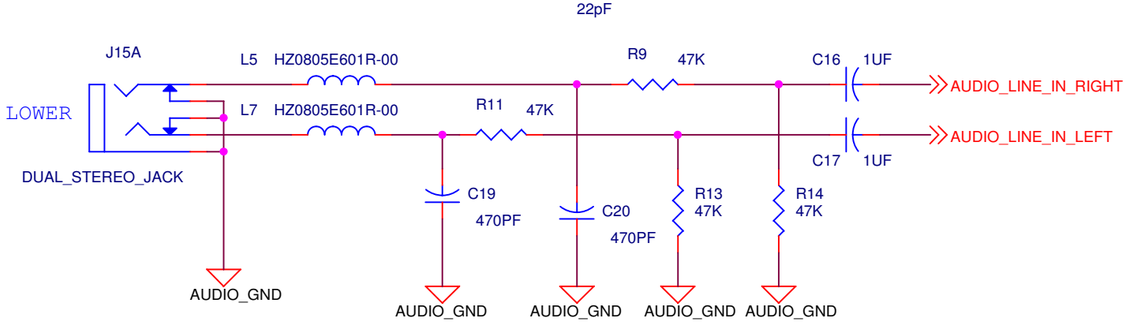

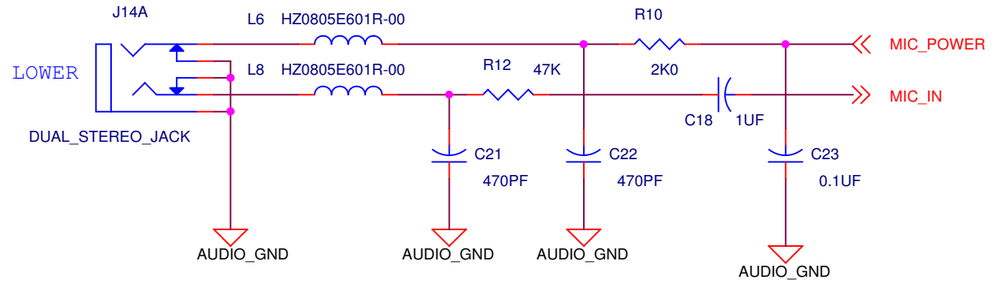

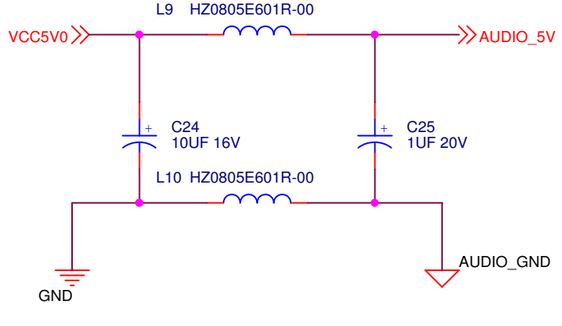

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title

AUDIO POWER AMPLIFIER

Size	Document Number	Rev
B	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

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AUDIO MIXER AND CODEC

AC97 CODEC

U9

AUDIO_5V
VCC3V3
C26 0.1UF
C27 0.1UF
C28 10UF 16V
C29 10UF 16V
C30 0.1UF
C31 0.1UF
C32 1UF
AUDIO_GND
GND
R15 3K3

AVSS0 26
AVSS1 42
AVDD0 25
AVDD1 38
NC0 44
NC1 43
NC2 40
DVDD0 1
DVDD1 9
DVSS0 4
DVSS1 7

BEEP_TONE_IN
R16 6K8
C33 1UF
BEEP_TONE
R17 4K7
AUDIO_GND

AUDIO_LINE_IN_RIGHT
AUDIO_LINE_IN_LEFT
MIC_IN

PC_BEEP 12
LINE_IN_R 24
LINE_IN_L 23
MIC1 21
MIC2 22
CD_R 20
CD_GND 19
CD_L 18
VIDEO_R 17
VIDEO_L 16
AUX_R 15
AUX_L 14
PHONE_IN 13
MONO_OUT 37
SPDIF 48

RESET 11 — AUDIO_RESET_Z
SDATA_OUT 5 — AC97_SDATA_OUT
SDATA_IN 8 — R167 56R2 1% — AC97_SDATA_IN
SYNCH 10 — R168 56R2 1% — AC97_SYNCH
BIT_CLOCK 6 — AC97_BIT_CLOCK
CS0 45
CS1 46 — R18 10K — VCC3V3
AMP_PWR_DWN 47 — AUDIO_AMP_SHUTDOWN
LNLVL_OUT_R 41 — AUDIO_LINE_OUT_RIGHT
LNLVL_OUT_L 39 — AUDIO_LINE_OUT_LEFT
LINE_OUT_R 36 — AUDIO_RIGHT
LINE_OUT_L 35 — AUDIO_LEFT

R169 3K3
R170 3K3

C34 MONO 1UF
R19 47K
C35 0.1UF
AUDIO_GND

AFILT1 29
AFLT2 30
FILT_L 31
FILT_R 32
CX3D 34
RX3D 33
VREF_OUT 28
VREF 27
XTAL_IN 2
XTAL_OUT 3

C36 270PF
C38 270PF
C37 100NF
C39 47NF
C40 1UF
C43 1UF
AUDIO_GND

Y1 24.576 MHz
R20 1M0
C41 22PF
C42 22PF
GND

MIC_POWER
R21 10K
AUDIO_5V
C44 100NF
C45 10UF 16V
AUDIO_GND

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title: **AC97 AUDIO PROCESSOR**

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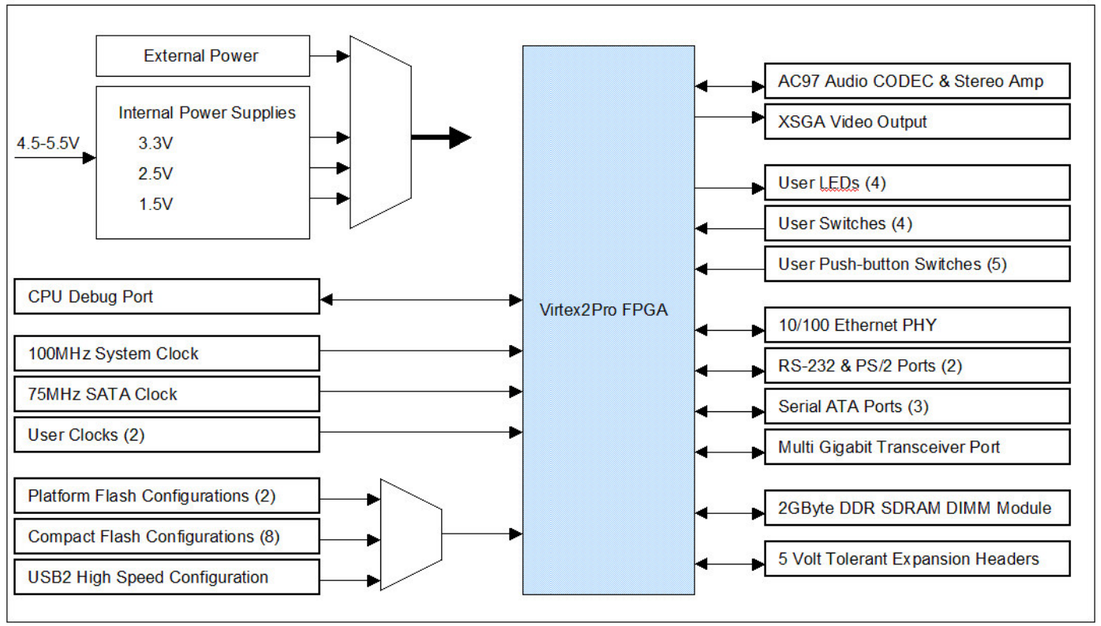

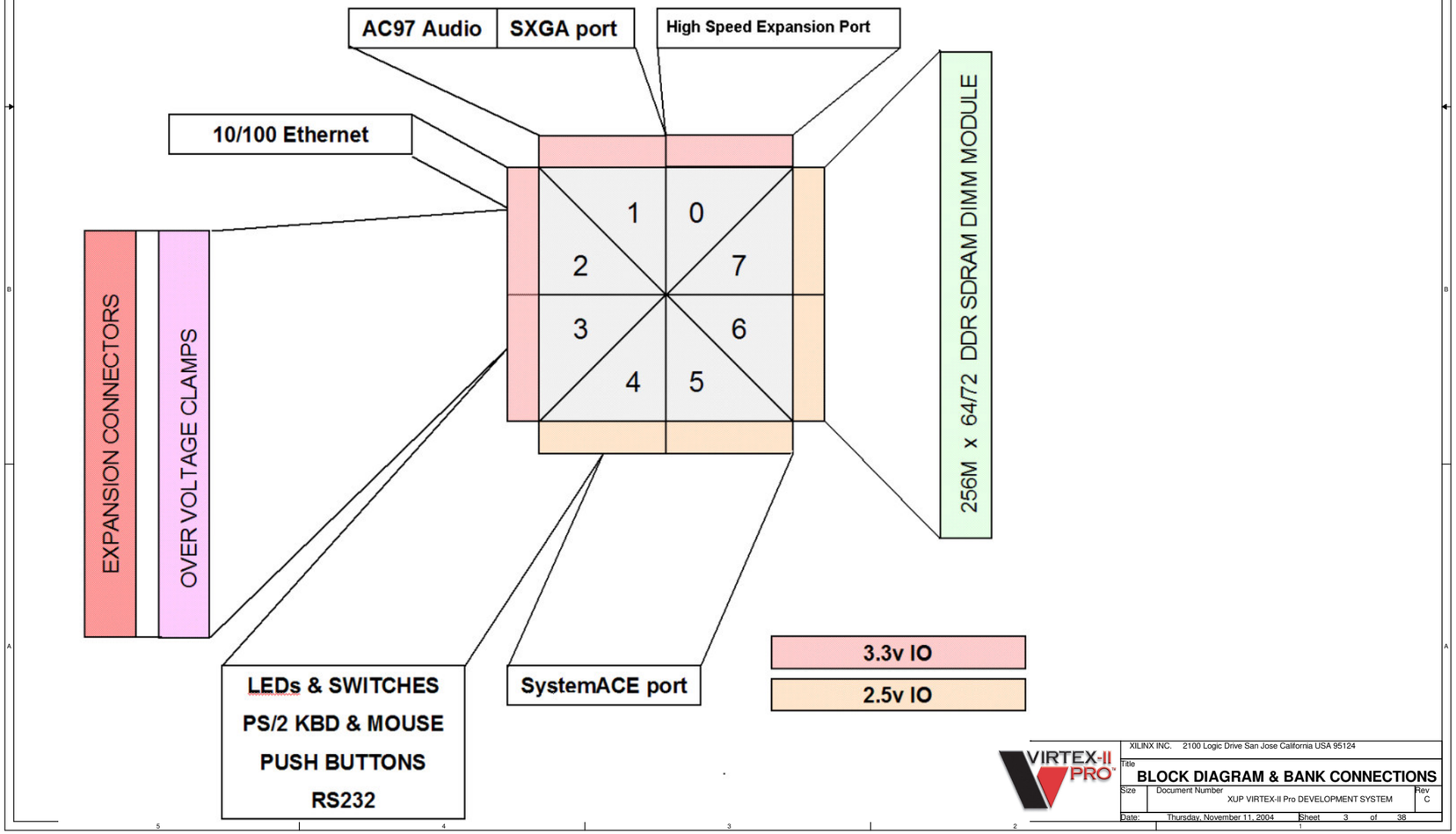

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title: BLOCK DIAGRAM & BANK CONNECTIONS

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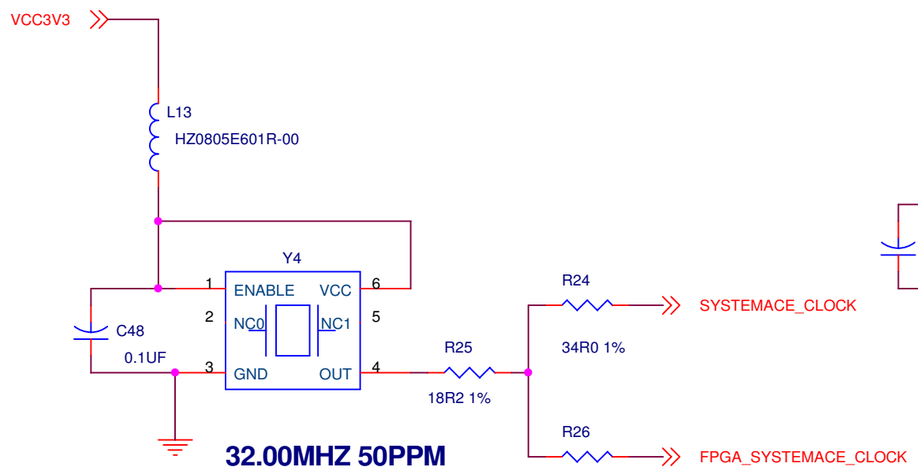

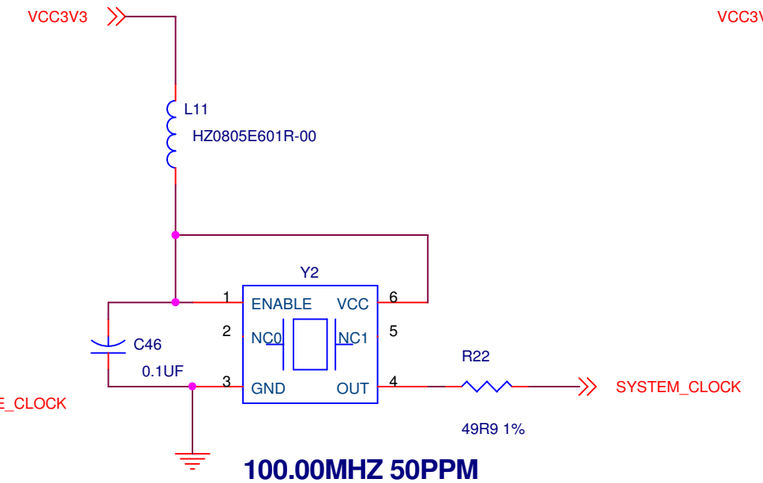

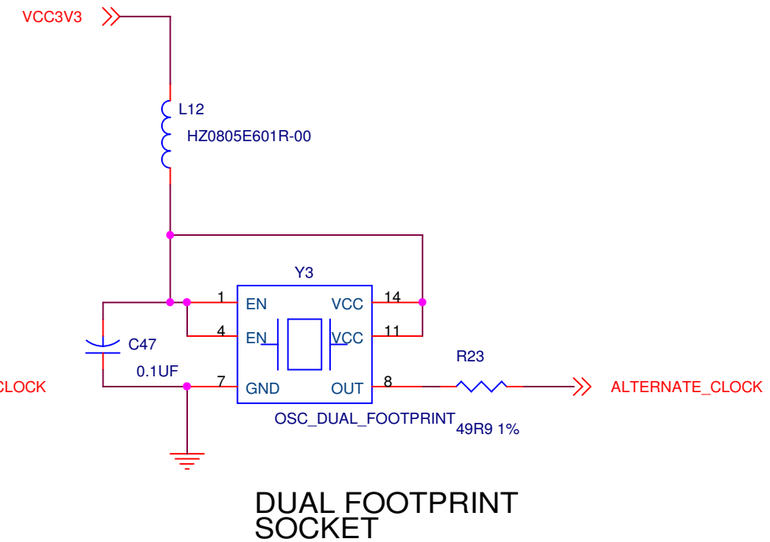

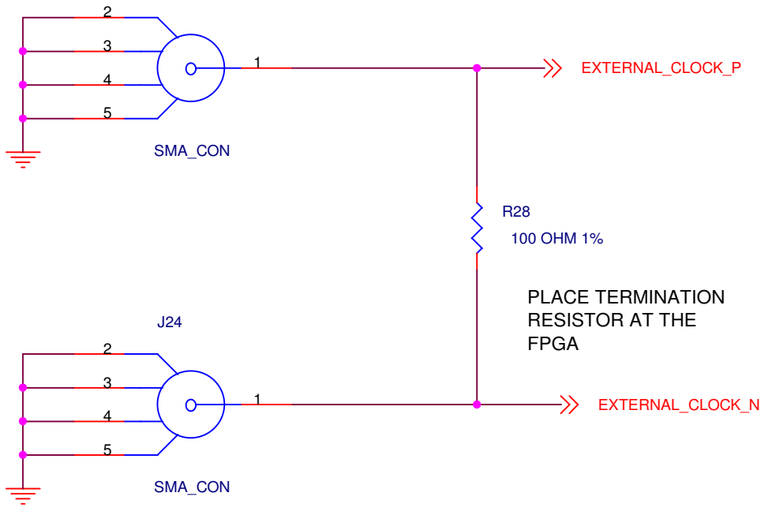

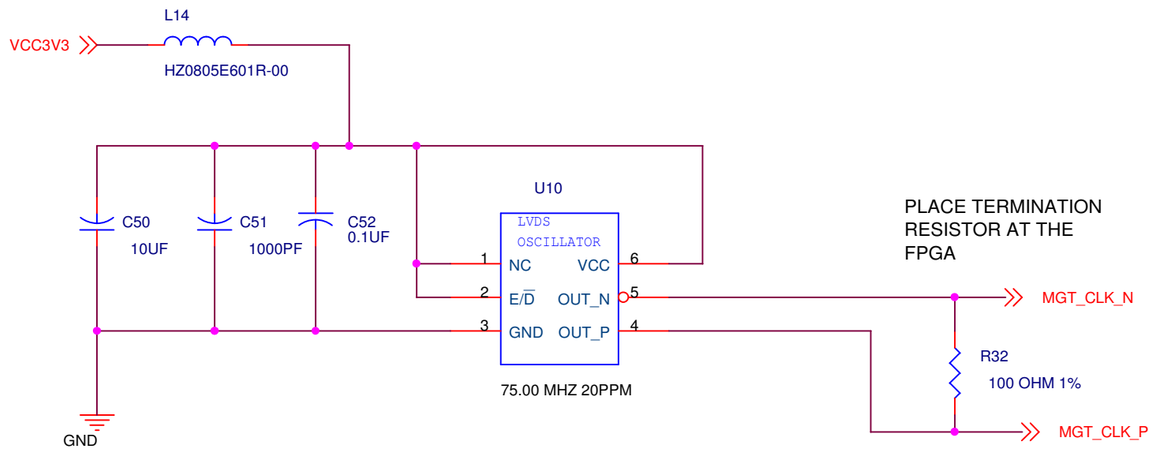

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title: **CLOCKS**

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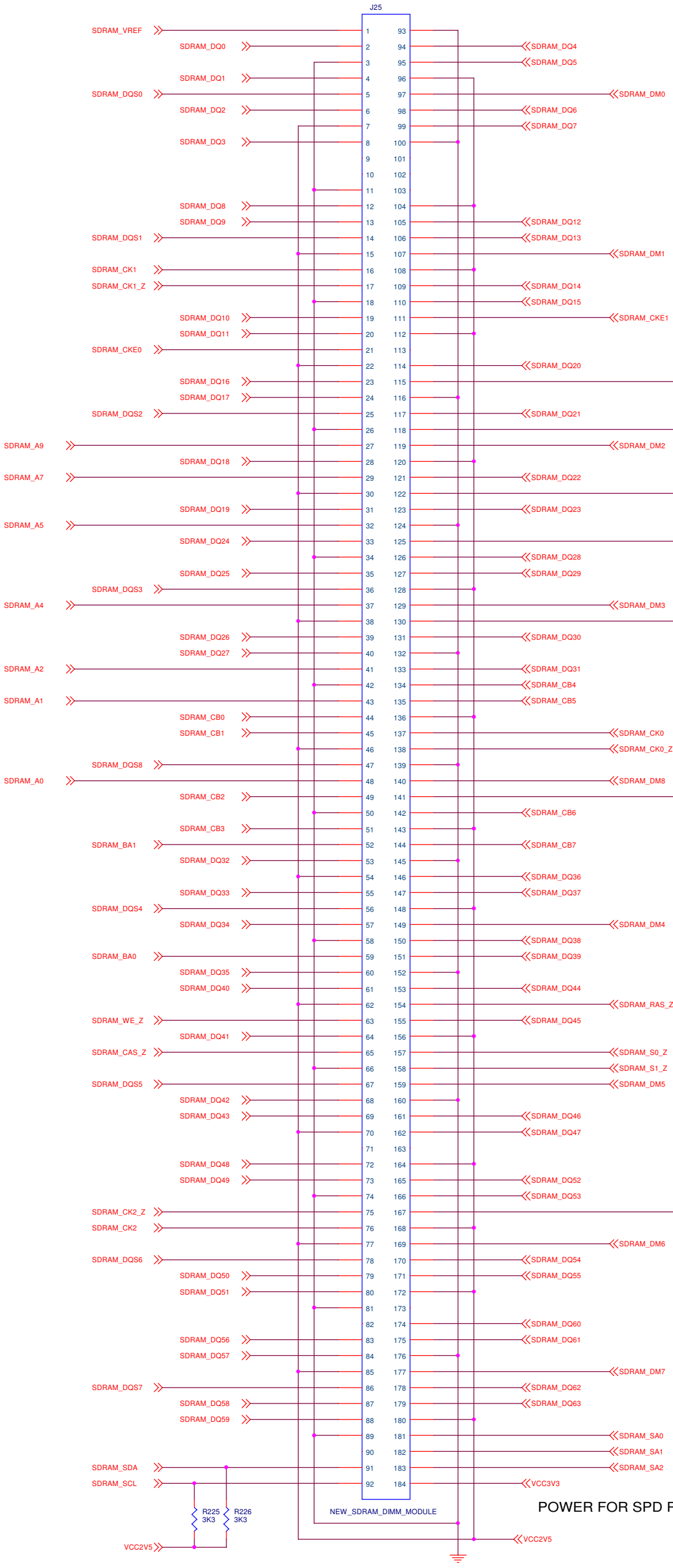
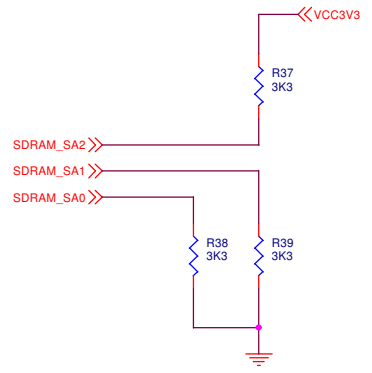
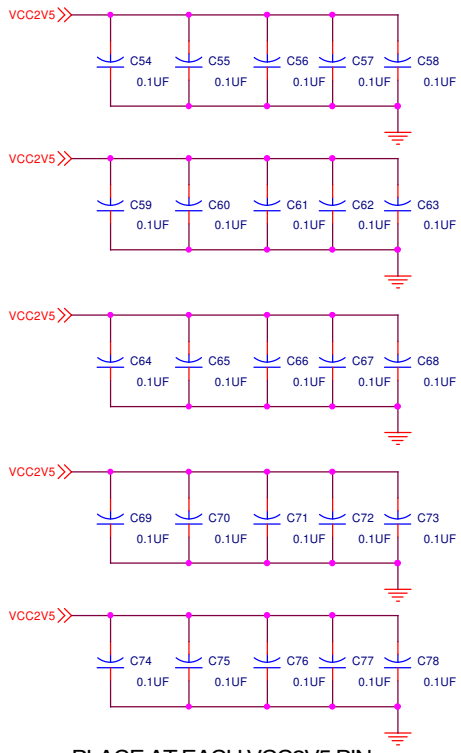


POWER FOR SPD PROM

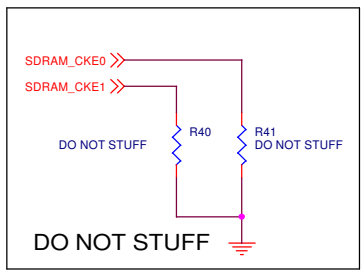


SPD PROM READ ADDRESS A9

FOR 512M/1G/2G MODULES

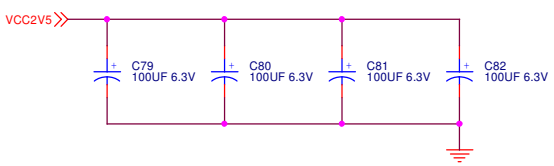


PLACE AT EACH VCC2V5 PIN



DO NOT STUFF

FOR 2G MODULES



PLACE AT EACH CORNER OF THE DIMM SOCKET

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title: **SDRAM DIMM SCOKET**

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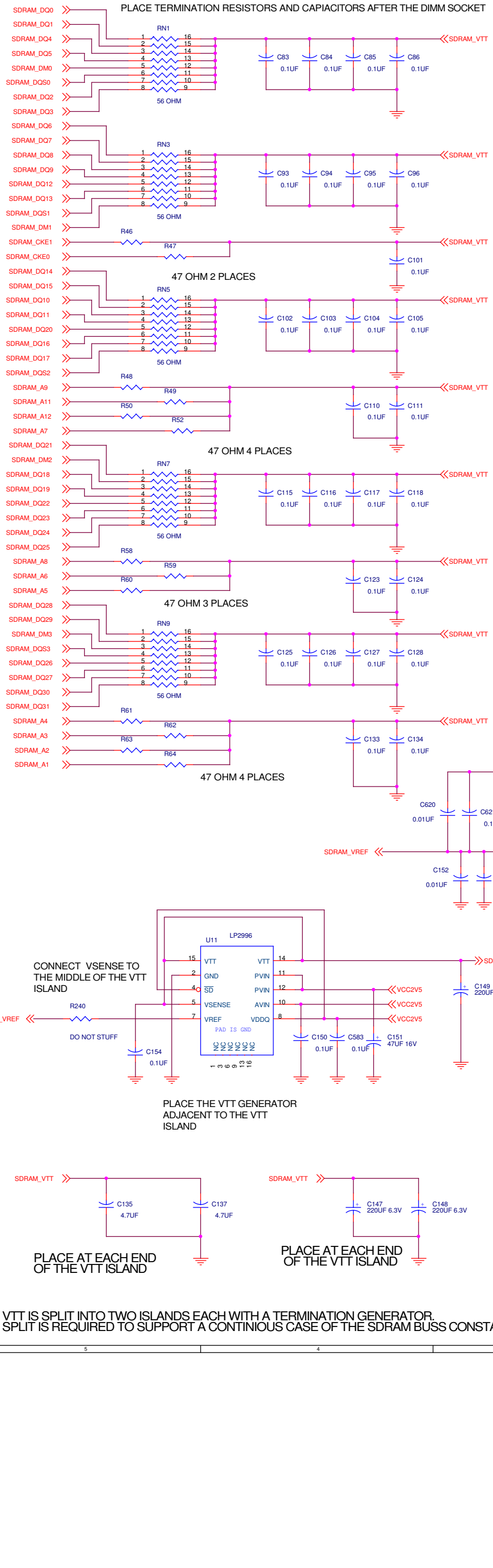
PLACE TERMINATION RESISTORS AND CAPIACITORS AFTER THE DIMM SOCKET
SDRAM_DQ0
SDRAM_DQ1
SDRAM_DQ4
SDRAM_DQ5
SDRAM_DM0
SDRAM_DQS0
SDRAM_DQ2
SDRAM_DQ3
RN1
56 OHM
C83 0.1UF
C84 0.1UF
C85 0.1UF
C86 0.1UF
SDRAM_VTT
SDRAM_DQ6
SDRAM_DQ7
SDRAM_DQ8
SDRAM_DQ9
SDRAM_DQ12
SDRAM_DQ13
SDRAM_DQS1
SDRAM_DM1
SDRAM_CKE1
SDRAM_CKE0
SDRAM_DQ14
SDRAM_DQ15
RN3
56 OHM
C93 0.1UF
C94 0.1UF
C95 0.1UF
C96 0.1UF
R46
R47
C101 0.1UF
47 OHM 2 PLACES
SDRAM_DQ10
SDRAM_DQ11
SDRAM_DQ20
SDRAM_DQ16
SDRAM_DQ17
SDRAM_DQS2
RN5
56 OHM
C102 0.1UF
C103 0.1UF
C104 0.1UF
C105 0.1UF
R48
R49
R50
R52
SDRAM_A9
SDRAM_A11
SDRAM_A12
SDRAM_A7
C110 0.1UF
C111 0.1UF
47 OHM 4 PLACES
SDRAM_DQ21
SDRAM_DM2
SDRAM_DQ18
SDRAM_DQ19
SDRAM_DQ22
SDRAM_DQ23
SDRAM_DQ24
SDRAM_DQ25
RN7
56 OHM
C115 0.1UF
C116 0.1UF
C117 0.1UF
C118 0.1UF
R58
R59
R60
SDRAM_A8
SDRAM_A6
SDRAM_A5
C123 0.1UF
C124 0.1UF
47 OHM 3 PLACES
SDRAM_DQ28
SDRAM_DQ29
SDRAM_DM3
SDRAM_DQS3
SDRAM_DQ26
SDRAM_DQ27
SDRAM_DQ30
SDRAM_DQ31
RN9
56 OHM
C125 0.1UF
C126 0.1UF
C127 0.1UF
C128 0.1UF
R61
R62
R63
R64
SDRAM_A4
SDRAM_A3
SDRAM_A2
SDRAM_A1
C133 0.1UF
C134 0.1UF
47 OHM 4 PLACES
VCC2V5
C620 0.01UF
C621 0.1UF
R238 1K00 1%
SDRAM_VREF
C152 0.01UF
C153 0.1UF
R239 1K00 1%
CONNECT VSENSE TO THE MIDDLE OF THE VTT ISLAND
U11
LP2996
VTT
GND
SD
VSENSE
VREF
PVIN
AVIN
VDDQ
PAD IS GND
R240
DO NOT STUFF
C154 0.1UF
C150 0.1UF
C583 0.1UF
C151 47UF 16V
C149 220UF 6.3V
VCC2V5
PLACE THE VTT GENERATOR ADJACENT TO THE VTT ISLAND
C135 4.7UF
C137 4.7UF
PLACE AT EACH END OF THE VTT ISLAND
C147 220UF 6.3V
C148 220UF 6.3V
PLACE AT EACH END OF THE VTT ISLAND
PLACE TERMINATION RESISTORS AND CAPIACITORS AFTER THE DIMM SOCKET
SDRAM_CB4
SDRAM_CB5
SDRAM_CB0
SDRAM_CB1
SDRAM_DQS8
SDRAM_DM8
SDRAM_CB2
SDRAM_CB3
RN2
56 OHM
C87 0.1UF
C88 0.1UF
C89 0.1UF
C90 0.1UF
SDRAM_VTT2
R42
R43
R44
R45
SDRAM_A0
SDRAM_A10
SDRAM_BA1
SDRAM_BA0
C91 0.1UF
C92 0.1UF
47 OHM 4 PLACES
SDRAM_CB6
SDRAM_CB7
SDRAM_DQ32
SDRAM_DQ33
SDRAM_DQ36
SDRAM_DQ37
SDRAM_DQS4
SDRAM_DM4
RN4
56 OHM
C97 0.1UF
C98 0.1UF
C99 0.1UF
C100 0.1UF
SDRAM_DQ34
SDRAM_DQ38
SDRAM_DQ39
SDRAM_DQ35
SDRAM_DQ40
SDRAM_DQ44
SDRAM_DQ45
SDRAM_DQ41
RN6
56 OHM
C106 0.1UF
C107 0.1UF
C108 0.1UF
C109 0.1UF
R51
R53
R54
R55
R56
R57
SDRAM_RAS_Z
SDRAM_WE_Z
SDRAM_CAS_Z
SDRAM_S0_Z
SDRAM_S1_Z
SDRAM_A13
C112 0.1UF
C113 0.1UF
C114 0.1UF
47 OHM 6 PLACES
SDRAM_DQS5
SDRAM_DM5
SDRAM_DQ42
SDRAM_DQ43
SDRAM_DQ46
SDRAM_DQ47
SDRAM_DQ48
SDRAM_DQ49
RN8
56 OHM
C119 0.1UF
C120 0.1UF
C121 0.1UF
C122 0.1UF
SDRAM_DQ52
SDRAM_DQ53
SDRAM_DM6
SDRAM_DQS6
SDRAM_DQ54
SDRAM_DQ55
SDRAM_DQ50
SDRAM_DQ51
RN10
56 OHM
C129 0.1UF
C130 0.1UF
C131 0.1UF
C132 0.1UF
SDRAM_DQ60
SDRAM_DQ61
SDRAM_DQ56
SDRAM_DQ57
SDRAM_DM7
SDRAM_DQS7
SDRAM_DQ62
SDRAM_DQ63
RN11
56 OHM
C138 0.1UF
C139 0.1UF
C140 0.1UF
C141 0.1UF
R65
R66
SDRAM_DQ58
SDRAM_DQ59
C146 0.1UF
56 OHM 2 PLACES
CONNECT VSENSE TO THE MIDDLE OF THE VTT2 ISLAND
U63
LP2996
C612 0.1UF
C609 0.1UF
C610 0.1UF
C611 47UF 16V
C608 220UF 6.3V
PLACE THE VTT2 GENERATOR ADJACENT TO THE VTT2 ISLAND
C613 220UF 6.3V
C614 220UF 6.3V
PLACE AT EACH END OF THE VTT2 ISLAND
C615 4.7UF
C136 4.7UF
PLACE AT EACH END OF THE VTT2 ISLAND
THE VTT IS SPLIT INTO TWO ISLANDS EACH WITH A TERMINATION GENERATOR.
THE SPLIT IS REQUIRED TO SUPPORT A CONTINIOUS CASE OF THE SDRAM BUSS CONSTANTLY DRIVEN HIGH OR LOW.
VIRTEX-II PRO
XILINX INC. 2100 Logic Drive San Jose California USA 95124
Title
SDRAM DIMM TERMINATION
Size
Document Number
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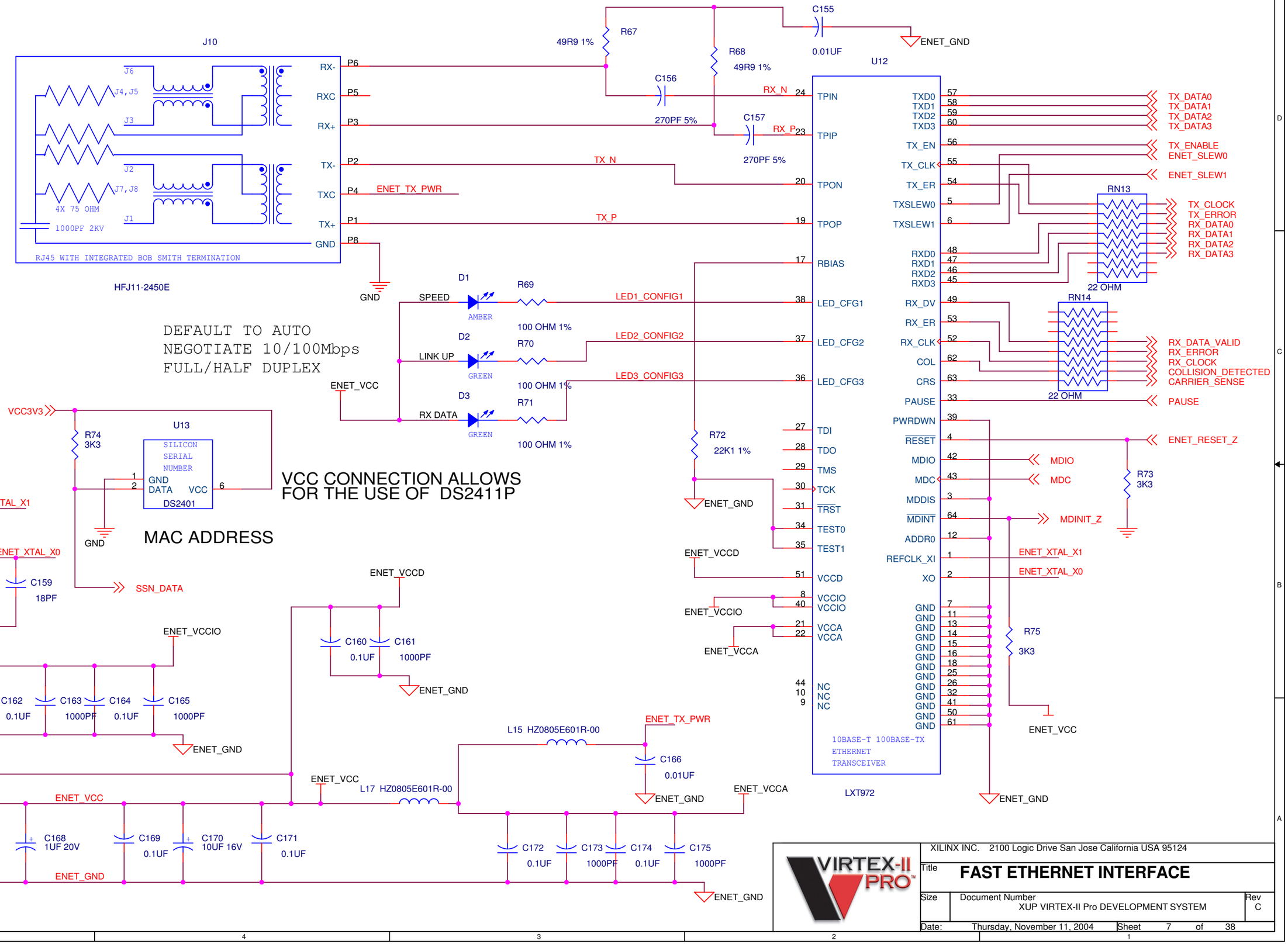
J10
RX-
RXC
RX+
TX-
TXC
TX+
GND
P6
P5
P3
P2
P4
P1
P8
J6
J4,J5
J3
J2
J7,J8
J1
4X 75 OHM
1000PF 2KV
RJ45 WITH INTEGRATED BOB SMITH TERMINATION
HFJ11-2450E
GND
ENET_TX_PWR
49R9 1%
R67
R68
49R9 1%
C155
0.01UF
ENET_GND
C156
270PF 5%
C157
270PF 5%
RX_N
RX_P
TX_N
TX_P
U12
TPIN
TPIP
TPON
TPOP
RBIAS
LED_CFG1
LED_CFG2
LED_CFG3
TDI
TDO
TMS
TCK
TRST
TEST0
TEST1
VCCD
VCCIO
VCCIO
VCCA
VCCA
NC
NC
NC
24
23
20
19
17
38
37
36
27
28
29
30
31
34
35
51
8
40
21
22
44
10
9
TXD0
TXD1
TXD2
TXD3
TX_EN
TX_CLK
TX_ER
TXSLEW0
TXSLEW1
RXD0
RXD1
RXD2
RXD3
RX_DV
RX_ER
RX_CLK
COL
CRS
PAUSE
PWRDWN
RESET
MDIO
MDC
MDDIS
MDINT
ADDR0
REFCLK_XI
XO
GND
57
58
59
60
56
55
54
5
6
48
47
46
45
49
53
52
62
63
33
39
4
42
43
3
64
12
1
2
7
11
13
14
15
16
18
25
26
32
41
50
61
TX_DATA0
TX_DATA1
TX_DATA2
TX_DATA3
TX_ENABLE
ENET_SLEW0
ENET_SLEW1
RN13
22 OHM
TX_CLOCK
TX_ERROR
RX_DATA0
RX_DATA1
RX_DATA2
RX_DATA3
RN14
22 OHM
RX_DATA_VALID
RX_ERROR
RX_CLOCK
COLLISION_DETECTED
CARRIER_SENSE
PAUSE
ENET_RESET_Z
MDIO
MDC
MDINIT_Z
R73
3K3
R75
3K3
ENET_VCC
10BASE-T 100BASE-TX
ETHERNET
TRANSCEIVER
LXT972
ENET_GND
D1
SPEED
AMBER
R69
100 OHM 1%
LED1_CONFIG1
D2
LINK UP
GREEN
R70
100 OHM 1%
LED2_CONFIG2
D3
RX DATA
GREEN
R71
100 OHM 1%
LED3_CONFIG3
R72
22K1 1%
ENET_VCC
DEFAULT TO AUTO
NEGOTIATE 10/100Mbps
FULL/HALF DUPLEX
VCC3V3
R74
3K3
U13
SILICON
SERIAL
NUMBER
GND
DATA
VCC
DS2401
1
2
6
GND
SSN_DATA
VCC CONNECTION ALLOWS
FOR THE USE OF DS2411P
MAC ADDRESS
ENET_XTAL_X1
ENET_XTAL_X0
Y5
C158
18PF
25.000MHZ
C159
18PF
ENET_GND
ENET_VCCIO
C162
0.1UF
C163
1000PF
C164
0.1UF
C165
1000PF
ENET_GND
ENET_VCCD
C160
0.1UF
C161
1000PF
ENET_GND
L15 HZ0805E601R-00
ENET_TX_PWR
C166
0.01UF
ENET_GND
ENET_VCCA
L16 HZ0805E601R-00
L17 HZ0805E601R-00
L18 HZ0805E601R-00
VCC3V3
ENET_VCC
ENET_GND
C167
10UF 16V
C168
1UF 20V
C169
0.1UF
C170
10UF 16V
C171
0.1UF
C172
0.1UF
C173
1000PF
C174
0.1UF
C175
1000PF
ENET_GND
GND
XILINX INC. 2100 Logic Drive San Jose California USA 95124
Title
FAST ETHERNET INTERFACE
Size
Document Number
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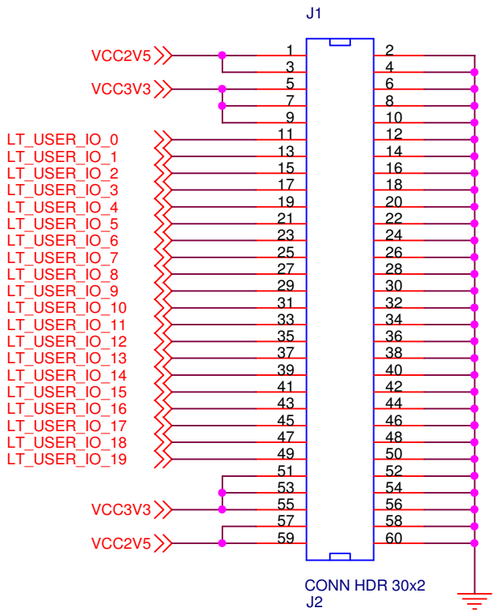
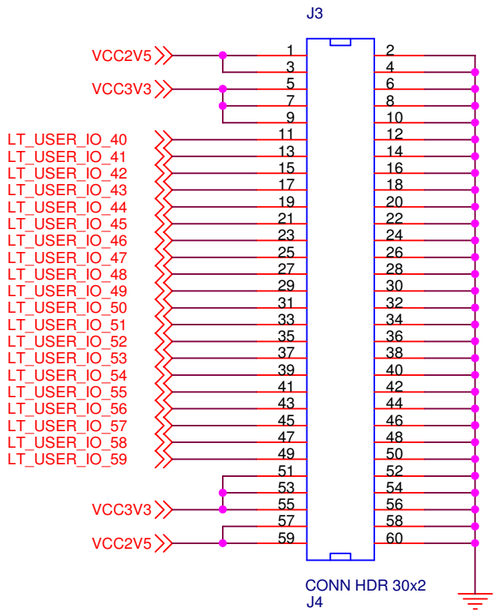
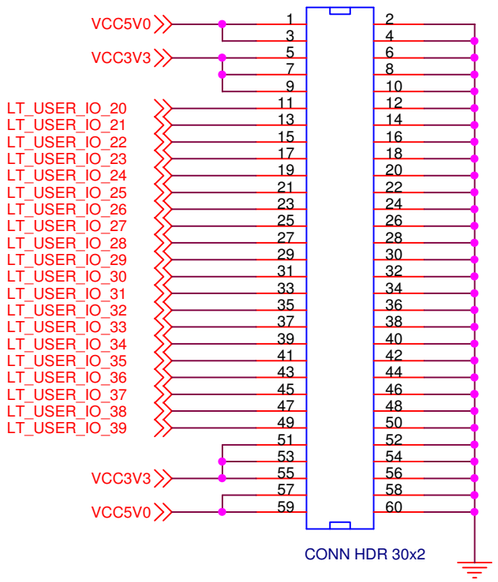
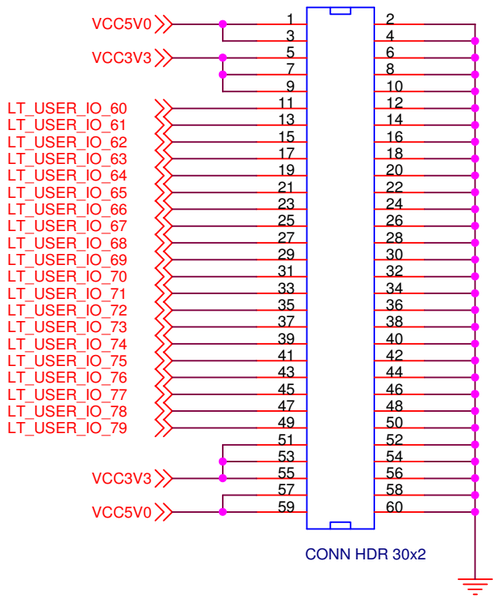
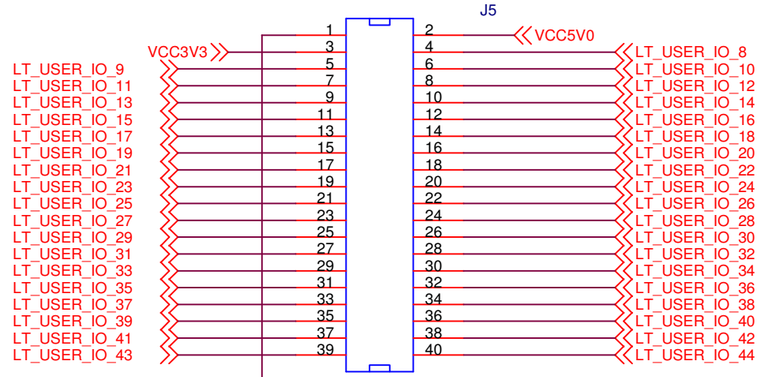




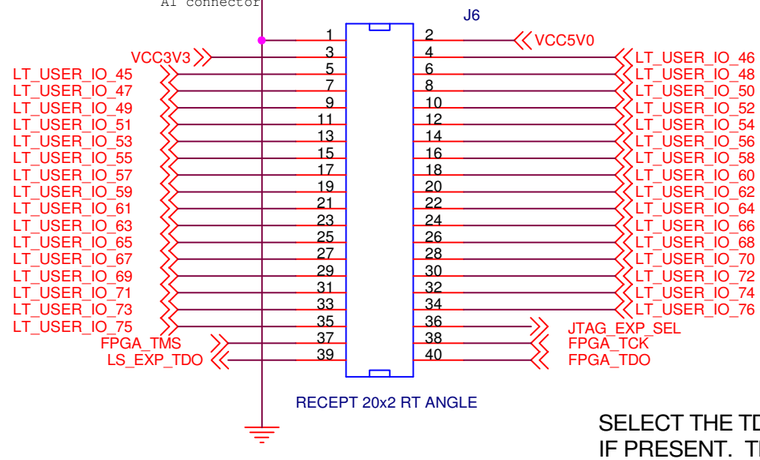




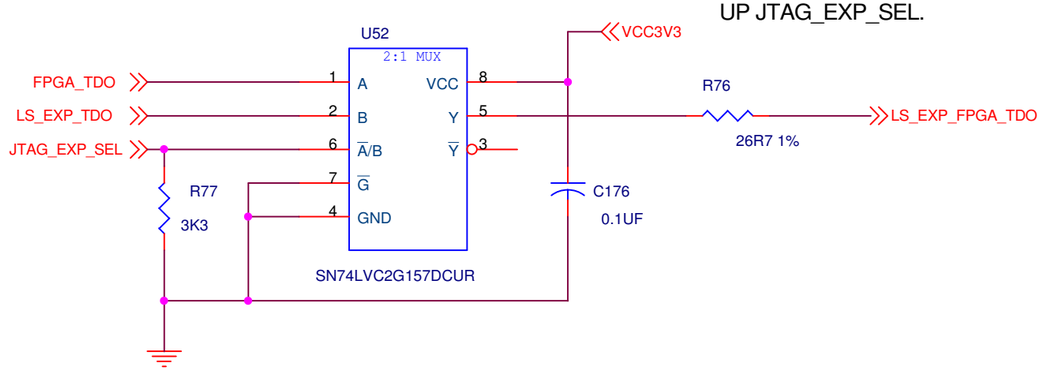
LEFT DIGILENT EXPANSION CONNECTOR
A2 connector



RIGHT DIGILENT EXPANSION CONNECTOR
A1 connector



SELECT THE TDO FROM THE EXPANSION BOARD IF PRESENT. THE EXPANSION BOARD WILL PULL UP JTAG_EXP_SEL.



The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion(if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.

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Title: **EXPANSION PORTS**

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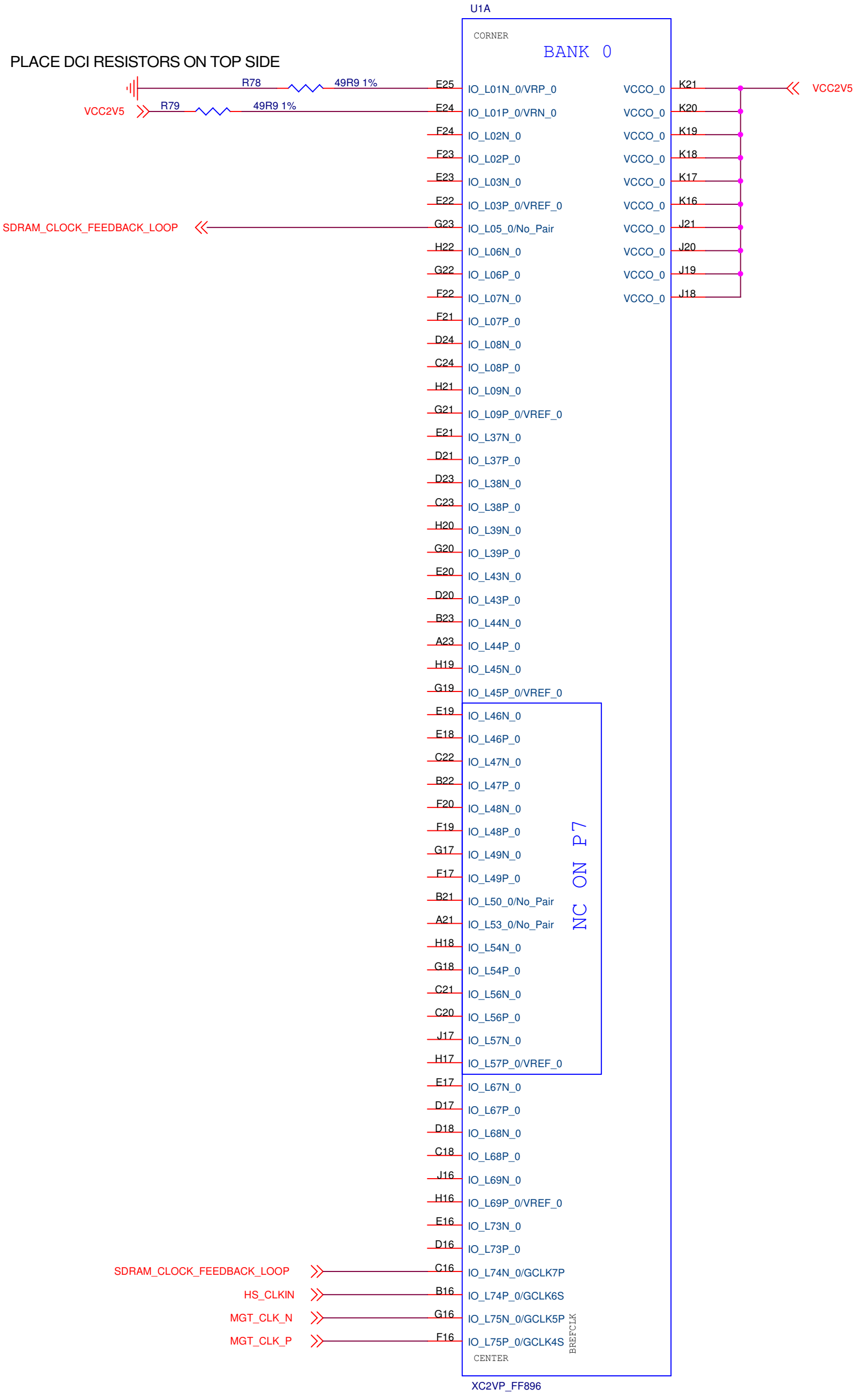
PLACE DCI RESISTORS ON TOP SIDE



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Title
BANK0 IOS

Size	Document Number	Rev
	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

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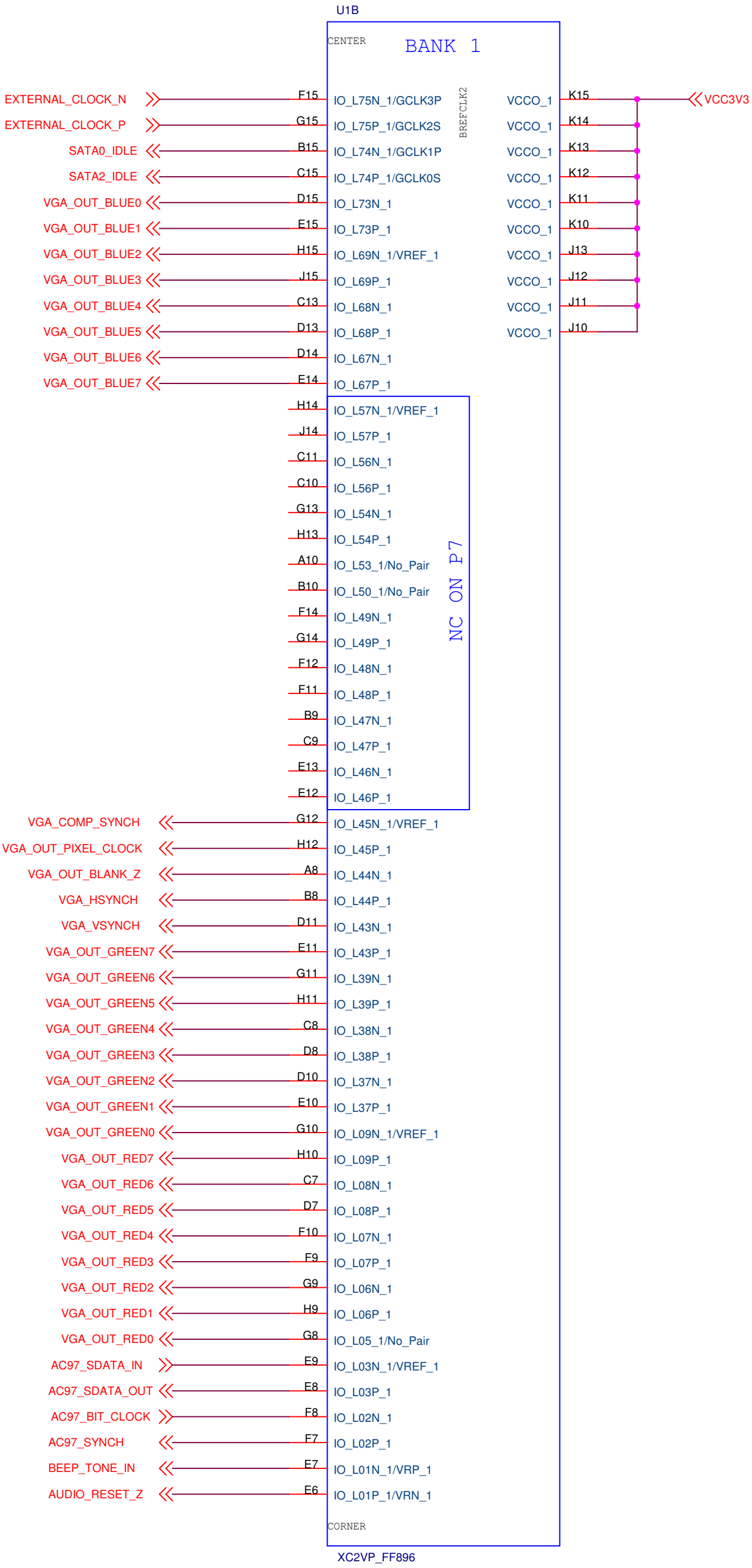

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title
BANK1 IOS

Size	Document Number	Rev
	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

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U1C

CORNER

BANK 2

ENET_SLEW1	A3	IO_L01N_2/VRP_2	VCCO_2	R10	VCC3V3
ENET_SLEW0	B3	IO_L01P_2/VRN_2	VCCO_2	P10	
ENET_RESET_Z	G6	IO_L02N_2	VCCO_2	N10	
MDINIT_Z	G5	IO_L02P_2	VCCO_2	N9	
CARRIER_SENSE	C5	IO_L03N_2	VCCO_2	M10	
COLLISION_DETECTED	D5	IO_L03P_2	VCCO_2	M9	
TX_DATA3	C2	IO_L04N_2/VREF_2	VCCO_2	L10	
TX_DATA2	C1	IO_L04P_2	VCCO_2	L9	
TX_DATA1	J8	IO_L05N_2	VCCO_2	K9	
TX_DATA0	J7	IO_L05P_2	VCCO_2	J9	
TX_ENABLE	C4	IO_L06N_2			
TX_CLOCK	D3	IO_L06P_2			
	D2	IO_L31N_2			
	D1	IO_L31P_2			
	H6	IO_L32N_2			
	H5	IO_L32P_2			
HS_CLKOUT	E4	IO_L33N_2			
HS_CLKIO	E3	IO_L33P_2			
HS_USER_IO_40	E2	IO_L34N_2/VREF_2			
HS_USER_IO_39	E1	IO_L34P_2			
HS_USER_IO_38	K8	IO_L35N_2			
HS_USER_IO_37	K7	IO_L35P_2			
HS_USER_IO_36	F4	IO_L36N_2			
HS_USER_IO_35	F3	IO_L36P_2			
HS_USER_IO_34	F2	IO_L37N_2			
HS_USER_IO_33	F1	IO_L37P_2			
HS_USER_IO_32	J6	IO_L38N_2			
HS_USER_IO_31	J5	IO_L38P_2			
HS_USER_IO_30	G4	IO_L39N_2			
HS_USER_IO_29	G3	IO_L39P_2			
HS_USER_IO_28	G2	IO_L40N_2/VREF_2			
HS_USER_IO_27	G1	IO_L40P_2			
HS_USER_IO_26	L8	IO_L41N_2			
HS_USER_IO_25	L7	IO_L41P_2			
	H4	IO_L42N_2			
	H3	IO_L42P_2			
TX_ERROR	H2	IO_L43N_2			
RX_ERROR	J2	IO_L43P_2			
RX_CLOCK	M8	IO_L44N_2			
RX_DATA_VALID	M7	IO_L44P_2			
RX_DATA0	K6	IO_L45N_2			
RX_DATA1	K5	IO_L45P_2			
RX_DATA2	J1	IO_L46N_2/VREF_2			
RX_DATA3	K1	IO_L46P_2			
MDC	M6	IO_L47N_2			
MDIO	M5	IO_L47P_2			
PAUSE	J4	IO_L48N_2			
SSN_DATA	J3	IO_L48P_2			
EXP_IO_0	K2	IO_L49N_2			
EXP_IO_1	L2	IO_L49P_2			
EXP_IO_2	N8	IO_L50N_2			
EXP_IO_3	N7	IO_L50P_2			
EXP_IO_4	K4	IO_L51N_2			
EXP_IO_5	K3	IO_L51P_2			
EXP_IO_6	L1	IO_L52N_2/VREF_2			
EXP_IO_7	M1	IO_L52P_2			
EXP_IO_8	N6	IO_L53N_2			
EXP_IO_9	N5	IO_L53P_2			
EXP_IO_10	L5	IO_L54N_2			
EXP_IO_11	L4	IO_L54P_2			
EXP_IO_12	M2	IO_L55N_2			
EXP_IO_13	N2	IO_L55P_2			
EXP_IO_14	P9	IO_L56N_2			
EXP_IO_15	R9	IO_L56P_2			
EXP_IO_16	M4	IO_L57N_2			
EXP_IO_17	M3	IO_L57P_2			
EXP_IO_18	N1	IO_L58N_2/VREF_2			
EXP_IO_19	P1	IO_L58P_2			
EXP_IO_20	P8	IO_L59N_2			
EXP_IO_21	P7	IO_L59P_2			
EXP_IO_22	N4	IO_L60N_2			
EXP_IO_23	N3	IO_L60P_2			
EXP_IO_24	P3	IO_L85N_2			
EXP_IO_25	P2	IO_L85P_2			
EXP_IO_26	R8	IO_L86N_2			
EXP_IO_27	R7	IO_L86P_2			
EXP_IO_28	P5	IO_L87N_2			
EXP_IO_29	P4	IO_L87P_2			
EXP_IO_30	R2	IO_L88N_2/VREF_2			
EXP_IO_31	T2	IO_L88P_2			
EXP_IO_32	R6	IO_L89N_2			
EXP_IO_33	R5	IO_L89P_2			
EXP_IO_34	R4	IO_L90N_2			
EXP_IO_35	R3	IO_L90P_2			

NC ON P7

XC2VP_FF896

CENTER

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title: **BANK2 IOS**

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CENTER

BANK 3

EXP_IO_36	U1	IO_L90N_3	VCCO_3	AB9	VCC3V3
EXP_IO_37	V1	IO_L90P_3	VCCO_3	AA9	
EXP_IO_38	T5	IO_L89N_3	VCCO_3	Y10	
EXP_IO_39	T6	IO_L89P_3	VCCO_3	Y9	
EXP_IO_40	T3	IO_L88N_3	VCCO_3	W10	
EXP_IO_41	T4	IO_L88P_3	VCCO_3	W9	
EXP_IO_42	U2	IO_L87N_3/VREF_3	VCCO_3	V10	
EXP_IO_43	U3	IO_L87P_3	VCCO_3	V9	
EXP_IO_44	T7	IO_L86N_3	VCCO_3	U10	
EXP_IO_45	T8	IO_L86P_3	VCCO_3	T10	VCC3V3_MON
EXP_IO_46	U4	IO_L85N_3			
EXP_IO_47	U5	IO_L85P_3			
EXP_IO_48	V2	IO_L60N_3			
EXP_IO_49	W2	IO_L60P_3			
EXP_IO_50	T9	IO_L59N_3			
EXP_IO_51	U9	IO_L59P_3			
EXP_IO_52	V3	IO_L58N_3			
EXP_IO_53	V4	IO_L58P_3			
EXP_IO_54	W1	IO_L57N_3/VREF_3			
EXP_IO_55	Y1	IO_L57P_3			
EXP_IO_56	U7	IO_L56N_3			
EXP_IO_57	U8	IO_L56P_3			
EXP_IO_58	V5	IO_L55N_3			
EXP_IO_59	V6	IO_L55P_3			
EXP_IO_60	Y2	IO_L54N_3			
EXP_IO_61	AA2	IO_L54P_3			
EXP_IO_62	V7	IO_L53N_3			
EXP_IO_63	V8	IO_L53P_3			
EXP_IO_64	W3	IO_L52N_3			
EXP_IO_65	W4	IO_L52P_3			
EXP_IO_66	AA1	IO_L51N_3/VREF_3			
EXP_IO_67	AB1	IO_L51P_3			
EXP_IO_68	W5	IO_L50N_3			
EXP_IO_69	W6	IO_L50P_3			
EXP_IO_70	Y4	IO_L49N_3			
EXP_IO_71	Y5	IO_L49P_3			
EXP_IO_72	AA3	IO_L48N_3			
EXP_IO_73	AA4	IO_L48P_3			
EXP_IO_74	W7	IO_L47N_3			
EXP_IO_75	W8	IO_L47P_3			
EXP_IO_76	AB3	IO_L46N_3			
EXP_IO_77	AB4	IO_L46P_3			
EXP_IO_78	AB2	IO_L45N_3/VREF_3			
EXP_IO_79	AC2	IO_L45P_3			
LED_3	AA5	IO_L44N_3			
LED_2	AA6	IO_L44P_3			
LED_1	AC3	IO_L43N_3			
LED_0	AC4	IO_L43P_3			
HS_USER_IO_24	AD1	IO_L42N_3			
HS_USER_IO_23	AD2	IO_L42P_3			
HS_USER_IO_22	Y7	IO_L41N_3			
HS_USER_IO_21	Y8	IO_L41P_3			
HS_USER_IO_20	AB5	IO_L40N_3			
HS_USER_IO_19	AB6	IO_L40P_3			
HS_USER_IO_18	AE1	IO_L39N_3/VREF_3			
HS_USER_IO_17	AE2	IO_L39P_3			
HS_USER_IO_16	AA7	IO_L38N_3			
HS_USER_IO_15	AA8	IO_L38P_3			
HS_USER_IO_14	AD3	IO_L37N_3			
HS_USER_IO_13	AD4	IO_L37P_3			
HS_USER_IO_12	AF1	IO_L36N_3			
HS_USER_IO_11	AF2	IO_L36P_3			
HS_USER_IO_10	AC5	IO_L35N_3			
HS_USER_IO_9	AC6	IO_L35P_3			
HS_USER_IO_8	AF3	IO_L34N_3			
HS_USER_IO_7	AF4	IO_L34P_3			
HS_USER_IO_6	AE3	IO_L33N_3/VREF_3			
HS_USER_IO_5	AE4	IO_L33P_3			
HS_USER_IO_4	AB7	IO_L32N_3			
HS_USER_IO_3	AB8	IO_L32P_3			
HS_USER_IO_2	AE5	IO_L31N_3			
HS_USER_IO_1	AF6	IO_L31P_3			
KBD_DATA	AG1	IO_L06N_3			
KBD_CLOCK	AG2	IO_L06P_3			
MOUSE_DATA	AD5	IO_L05N_3			
MOUSE_CLOCK	AD6	IO_L05P_3			
PB_DOWN	AG3	IO_L04N_3			
PB_UP	AH4	IO_L04P_3			
PB_LEFT	AH1	IO_L03N_3/VREF_3			
PB_RIGHT	AH2	IO_L03P_3			
PB_ENTER	AG5	IO_L02N_3			
PROCESSOR_RESET_Z	AH5	IO_L02P_3			
TRI_STATE_CPLD_JTAG_CHAIN	AJ3	IO_L01N_3/VRP_3			
SATA1_IDLE	AK3	IO_L01P_3/VRN_3			

MONITOR THE VCC3V3 ON THE DIE

NC ON P7

CORNER

XC2VP_FF896

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Title: **BANK3 IOS**

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PLACE DCI RESISTORS ON TOP SIDE

U1E

BANK 4

FPGA_BUSY	AG6	IO_L01N_4/DOUT	VCCO_4	AB13	VCC2V5
FPGA_INIT	AF7	IO_L01P_4/INIT_B	VCCO_4	AB12	
PROM_DATA0	AC9	IO_L02N_4/D0	VCCO_4	AB11	
PROM_DATA1	AD9	IO_L02P_4/D1	VCCO_4	AB10	
PROM_DATA2	AG7	IO_L03N_4/D2	VCCO_4	AA15	
PROM_DATA3	AH7	IO_L03P_4/D3	VCCO_4	AA14	
FPGA_PROM_CLOCK	AD8	IO_L05_4/No_Pair	VCCO_4	AA13	
R213 49R9 1%	AG8	IO_L06N_4/VRP_4	VCCO_4	AA12	
VCC2V5 R214	AH8	IO_L06P_4/VRN_4	VCCO_4	AA11	
49R9 1%	AC10	IO_L07N_4	VCCO_4	AA10	
RS232_DSR_OUT	AD10	IO_L07P_4/VREF_4			
RS232_TX_DATA	AE7	IO_L08N_4			
RS232_CTS_OUT	AE8	IO_L08P_4			
RS232_RX_DATA	AJ8	IO_L09N_4			
RS232_RTS_IN	AK8	IO_L09P_4/VREF_4			
SW_0	AC11	IO_L37N_4			
SW_1	AD11	IO_L37P_4			
SW_2	AF8	IO_L38N_4			
SW_3	AF9	IO_L38P_4			
CF_MPD15	AF10	IO_L39N_4			
CF_MPD14	AG10	IO_L39P_4			
CF_MPD13	AC12	IO_L43N_4			
CF_MPD12	AD12	IO_L43P_4			
CF_MPD11	AE9	IO_L44N_4			
CF_MPD10	AE10	IO_L44P_4			
CF_MPD9	AH9	IO_L45N_4			
CF_MPD8	AJ9	IO_L45P_4/VREF_4			
	AC13	IO_L46N_4			
	AD13	IO_L46P_4			
	AE11	IO_L47N_4			
	AE12	IO_L47P_4			
	AH10	IO_L48N_4			
	AH11	IO_L48P_4			
	AB14	IO_L49N_4			
	AC14	IO_L49P_4			
	AF11	IO_L50_4/No_Pair			
	AG11	IO_L53_4/No_Pair			
	AJ10	IO_L54N_4			
	AK10	IO_L54P_4			
	AF12	IO_L56N_4			
	AF13	IO_L56P_4			
	AG13	IO_L57N_4			
	AH13	IO_L57P_4/VREF_4			
CF_MPD7	AB15	IO_L67N_4			
CF_MPD6	AC15	IO_L67P_4			
CF_MPD5	AD14	IO_L68N_4			
CF_MPD4	AE14	IO_L68P_4			
CF_MPD3	AF14	IO_L69N_4			
CF_MPD2	AG14	IO_L69P_4/VREF_4			
CF_MPD1	AD15	IO_L73N_4			
CF_MPD0	AE15	IO_L73P_4			
FPGA_CPU_TDI	AF15	IO_L74N_4/GCLK3S			
FPGA_CPU_TCK	AG15	IO_L74P_4/GCLK2P			
FPGA_SYSTEMACE_CLOCK	AH15	IO_L75N_4/GCLK1S			
SYSTEM_CLOCK	AJ15	IO_L75P_4/GCLK0P			

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BREFCLK2

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Title: **BANK4 IOS**

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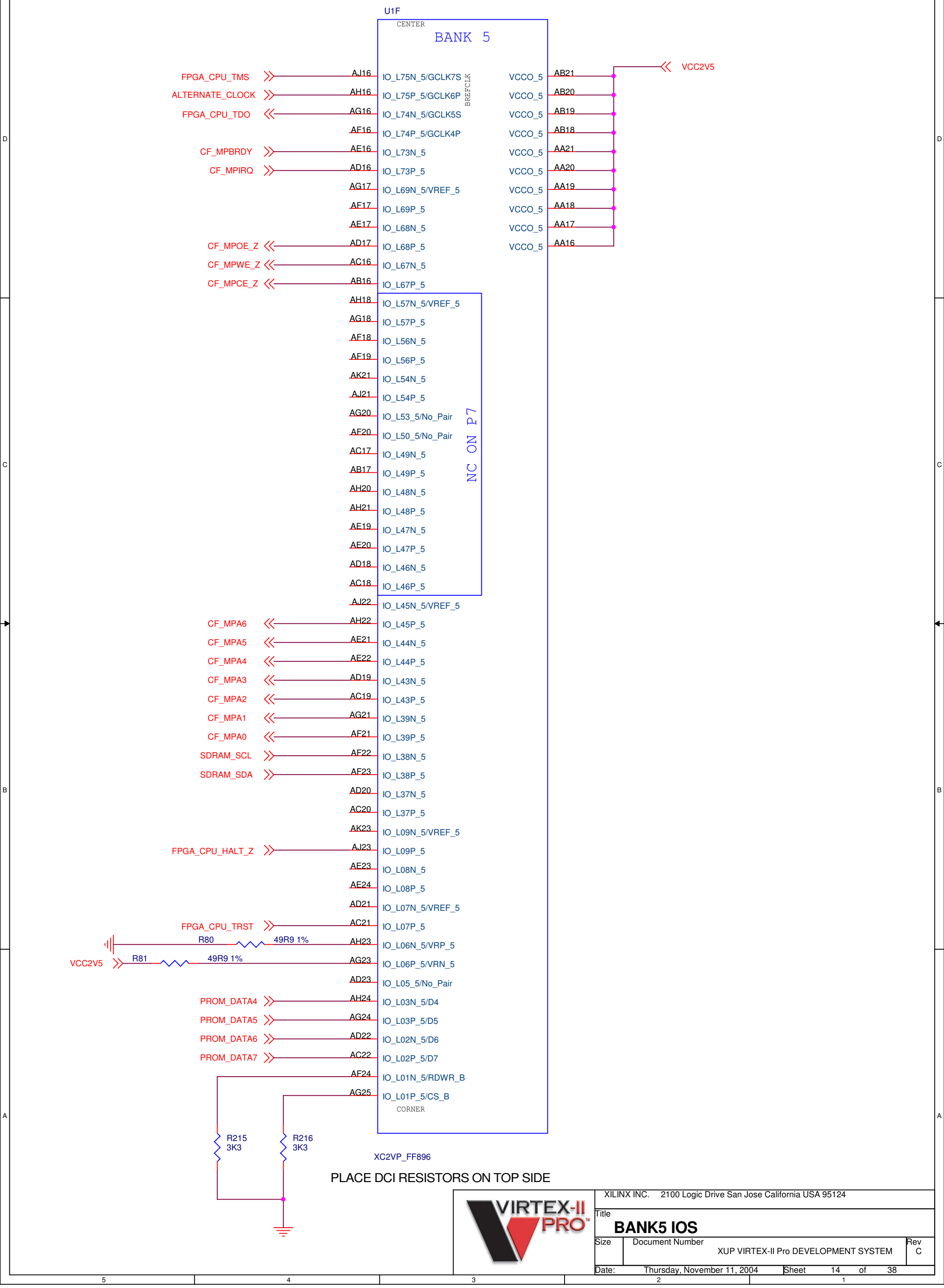

PLACE DCI RESISTORS ON TOP SIDE

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Title: **BANK5 IOS**

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PLACE DCI RESISTORS ON TOP SIDE

U1G

CORNER

BANK 6

VCC2V5	R82 49R9 1%	AK28	IO_L01P_6/VRN_6	VCCO_6	AB22
	R83 49R9 1%	AJ28	IO_L01N_6/VRP_6	VCCO_6	AA22
SDRAM_DQS7		AH26	IO_L02P_6	VCCO_6	Y22
		AG26	IO_L02N_6	VCCO_6	Y21
SDRAM_DQ63		AH29	IO_L03P_6	VCCO_6	W22
		AH30	IO_L03N_6/VREF_6	VCCO_6	W21
SDRAM_DQ62		AH27	IO_L04P_6	VCCO_6	V22
SDRAM_DQ61		AG28	IO_L04N_6	VCCO_6	V21
SDRAM_DQ60		AD25	IO_L05P_6	VCCO_6	U21
SDRAM_DQ59		AD26	IO_L05N_6	VCCO_6	T21
SDRAM_DQ58		AG29	IO_L06P_6		
SDRAM_DQ57		AG30	IO_L06N_6		
SDRAM_DQ56		AF25	IO_L31P_6		
		AE26	IO_L31N_6		
SDRAM_CK2		AB23	IO_L32P_6		
SDRAM_CK2_Z		AB24	IO_L32N_6		
		AE27	IO_L33P_6		
		AE28	IO_L33N_6/VREF_6		
		AF27	IO_L34P_6		
		AF28	IO_L34N_6		
SDRAM_DQS6		AC25	IO_L35P_6		
		AC26	IO_L35N_6		
SDRAM_DQ55		AF29	IO_L36P_6		
SDRAM_DQ54		AF30	IO_L36N_6		
SDRAM_DQ53		AD27	IO_L37P_6		
SDRAM_DQ52		AD28	IO_L37N_6		
SDRAM_DQ51		AA23	IO_L38P_6		
SDRAM_DQ50		AA24	IO_L38N_6		
SDRAM_DQ49		AE29	IO_L39P_6		
		AE30	IO_L39N_6/VREF_6		
SDRAM_DQ48		AB25	IO_L40P_6		
		AB26	IO_L40N_6		
		Y23	IO_L41P_6		
		Y24	IO_L41N_6		
SDRAM_CK1		AD29	IO_L42P_6		
SDRAM_CK1_Z		AD30	IO_L42N_6		
SDRAM_CK0		AC27	IO_L43P_6		
SDRAM_CK0_Z		AC28	IO_L43N_6		
SDRAM_DQS5		AA25	IO_L44P_6		
		AA26	IO_L44N_6		
SDRAM_DQ47		AC29	IO_L45P_6		
		AB29	IO_L45N_6/VREF_6		
SDRAM_DQ46		AB27	IO_L46P_6		
SDRAM_DQ45		AB28	IO_L46N_6		
SDRAM_DQ44		W23	IO_L47P_6		
SDRAM_DQ43		W24	IO_L47N_6		
SDRAM_DQ42		AA27	IO_L48P_6		
SDRAM_DQ41		AA28	IO_L48N_6		
SDRAM_DQ40		Y26	IO_L49P_6		
		Y27	IO_L49N_6		
SDRAM_DM7		W25	IO_L50P_6		
SDRAM_DM6		W26	IO_L50N_6		
		AB30	IO_L51P_6		
		AA30	IO_L51N_6/VREF_6		
SDRAM_DM5		W27	IO_L52P_6		
SDRAM_DM4		W28	IO_L52N_6		
SDRAM_DQS4		V23	IO_L53P_6		
		V24	IO_L53N_6		
SDRAM_DQ39		AA29	IO_L54P_6		
SDRAM_DQ38		Y29	IO_L54N_6		
SDRAM_DQ37		V25	IO_L55P_6		
SDRAM_DQ36		V26	IO_L55N_6		
SDRAM_DQ35		U23	IO_L56P_6		
SDRAM_DQ34		U24	IO_L56N_6		
SDRAM_DQ33		Y30	IO_L57P_6		
		W30	IO_L57N_6/VREF_6		
SDRAM_DQ32		V27	IO_L58P_6		
		V28	IO_L58N_6		
SDRAM_DM8		U22	IO_L59P_6		
SDRAM_DM3		T22	IO_L59N_6		
SDRAM_DM2		W29	IO_L60P_6		
SDRAM_DM1		V29	IO_L60N_6		
SDRAM_DM0		U26	IO_L85P_6		
		U27	IO_L85N_6		
SDRAM_DQS8		T23	IO_L86P_6		
		T24	IO_L86N_6		
SDRAM_CB7		U28	IO_L87P_6		
		U29	IO_L87N_6/VREF_6		
SDRAM_CB6		T27	IO_L88P_6		
SDRAM_CB5		T28	IO_L88N_6		
SDRAM_CB4		T25	IO_L89P_6		
SDRAM_CB3		T26	IO_L89N_6		
SDRAM_CB2		V30	IO_L90P_6		
SDRAM_CB1		U30	IO_L90N_6		

NC ON P7

CENTER

XC2VP_FF896

VCC2V5

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Title: **BANK6 IOS**

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BANK 7

SDRAM_VREF					
SDRAM_CB0	R28	IO_L90P_7	VCCO_7	R21	VCC2V5
	R27	IO_L90N_7	VCCO_7	P21	
SDRAM_CKE0	R26	IO_L89P_7	VCCO_7	N22	
SDRAM_CKE1	R25	IO_L89N_7	VCCO_7	N21	
	T29	IO_L88P_7	VCCO_7	M22	
	R29	IO_L88N_7/VREF_7	VCCO_7	M21	
RST_DQS_DIV	P27	IO_L87P_7	VCCO_7	L22	
	P26	IO_L87N_7	VCCO_7	L21	
SDRAM_S0_Z	R24	IO_L86P_7	VCCO_7	K22	
SDRAM_S1_Z	R23	IO_L86N_7	VCCO_7	J22	VCC2V5_MON
SDRAM_DQS3	P29	IO_L85P_7			
	P28	IO_L85N_7			
SDRAM_DQ31	N28	IO_L60P_7			
SDRAM_DQ30	N27	IO_L60N_7			
SDRAM_DQ29	P24	IO_L59P_7			
SDRAM_DQ28	P23	IO_L59N_7			
SDRAM_DQ27	P30	IO_L58P_7			
	N30	IO_L58N_7/VREF_7			
SDRAM_DQ26	M28	IO_L57P_7			
SDRAM_DQ25	M27	IO_L57N_7			
SDRAM_DQ24	R22	IO_L56P_7			
	P22	IO_L56N_7			
SDRAM_RAS_Z	N29	IO_L55P_7			
SDRAM_A3	M29	IO_L55N_7			
SDRAM_CAS_Z	L27	IO_L54P_7			
SDRAM_A2	L26	IO_L54N_7			
SDRAM_WE_Z	N26	IO_L53P_7			
SDRAM_A1	N25	IO_L53N_7			
SDRAM_DQS2	M30	IO_L52P_7			
	L30	IO_L52N_7/VREF_7			
SDRAM_DQ23	K28	IO_L51P_7			
SDRAM_DQ22	K27	IO_L51N_7			
SDRAM_DQ21	N24	IO_L50P_7			
SDRAM_DQ20	N23	IO_L50N_7			
SDRAM_DQ19	L29	IO_L49P_7			
SDRAM_DQ18	K29	IO_L49N_7			
SDRAM_DQ17	J28	IO_L48P_7			
SDRAM_DQ16	J27	IO_L48N_7			
SDRAM_BA0	M26	IO_L47P_7			
SDRAM_A0	M25	IO_L47N_7			
SDRAM_A4	K30	IO_L46P_7			
	J30	IO_L46N_7/VREF_7			
SDRAM_BA1	K26	IO_L45P_7			
	K25	IO_L45N_7			
SDRAM_A12	M24	IO_L44P_7			
SDRAM_A13	M23	IO_L44N_7			
SDRAM_DQS1	J29	IO_L43P_7			
	H29	IO_L43N_7			
SDRAM_DQ15	H28	IO_L42P_7			
SDRAM_DQ14	H27	IO_L42N_7			
SDRAM_DQ13	L24	IO_L41P_7			
SDRAM_DQ12	L23	IO_L41N_7			
SDRAM_DQ11	G30	IO_L40P_7			
	G29	IO_L40N_7/VREF_7			
SDRAM_DQ10	G28	IO_L39P_7			
SDRAM_DQ9	G27	IO_L39N_7			
SDRAM_DQ8	J26	IO_L38P_7			
	J25	IO_L38N_7			
SDRAM_A11	F30	IO_L37P_7			
	F29	IO_L37N_7			
SDRAM_A10	F28	IO_L36P_7			
	F27	IO_L36N_7			
SDRAM_A9	K24	IO_L35P_7			
	K23	IO_L35N_7			
SDRAM_DQS0	E30	IO_L34P_7			
	E29	IO_L34N_7/VREF_7			
SDRAM_DQ7	E28	IO_L33P_7			
SDRAM_DQ6	E27	IO_L33N_7			
SDRAM_DQ5	H26	IO_L32P_7			
SDRAM_DQ4	H25	IO_L32N_7			
SDRAM_DQ3	D30	IO_L31P_7			
SDRAM_DQ2	D29	IO_L31N_7			
SDRAM_DQ1	D28	IO_L06P_7			
SDRAM_DQ0	C27	IO_L06N_7			
SDRAM_A8	J24	IO_L05P_7			
	J23	IO_L05N_7			
	C30	IO_L04P_7			
	C29	IO_L04N_7/VREF_7			
SDRAM_A7	D26	IO_L03P_7			
	C26	IO_L03N_7			
SDRAM_A6	G26	IO_L02P_7			
SDRAM_A5	G25	IO_L02N_7			
VCC2V5 R84 49R9 1%	B28	IO_L01P_7/VRN_7			
R85 49R9 1%	A28	IO_L01N_7/VRP_7			

NC ON P7

CORNER

PLACE DCI RESISTORS ON TOP SIDE

XC2VP_FF896

VCC2V5_MON
MONITOR THE VCC2V5 ON THE DIE

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Title
BANK7 IOS

Size | Document Number: XUP VIRTEX-II Pro DEVELOPMENT SYSTEM | Rev: C

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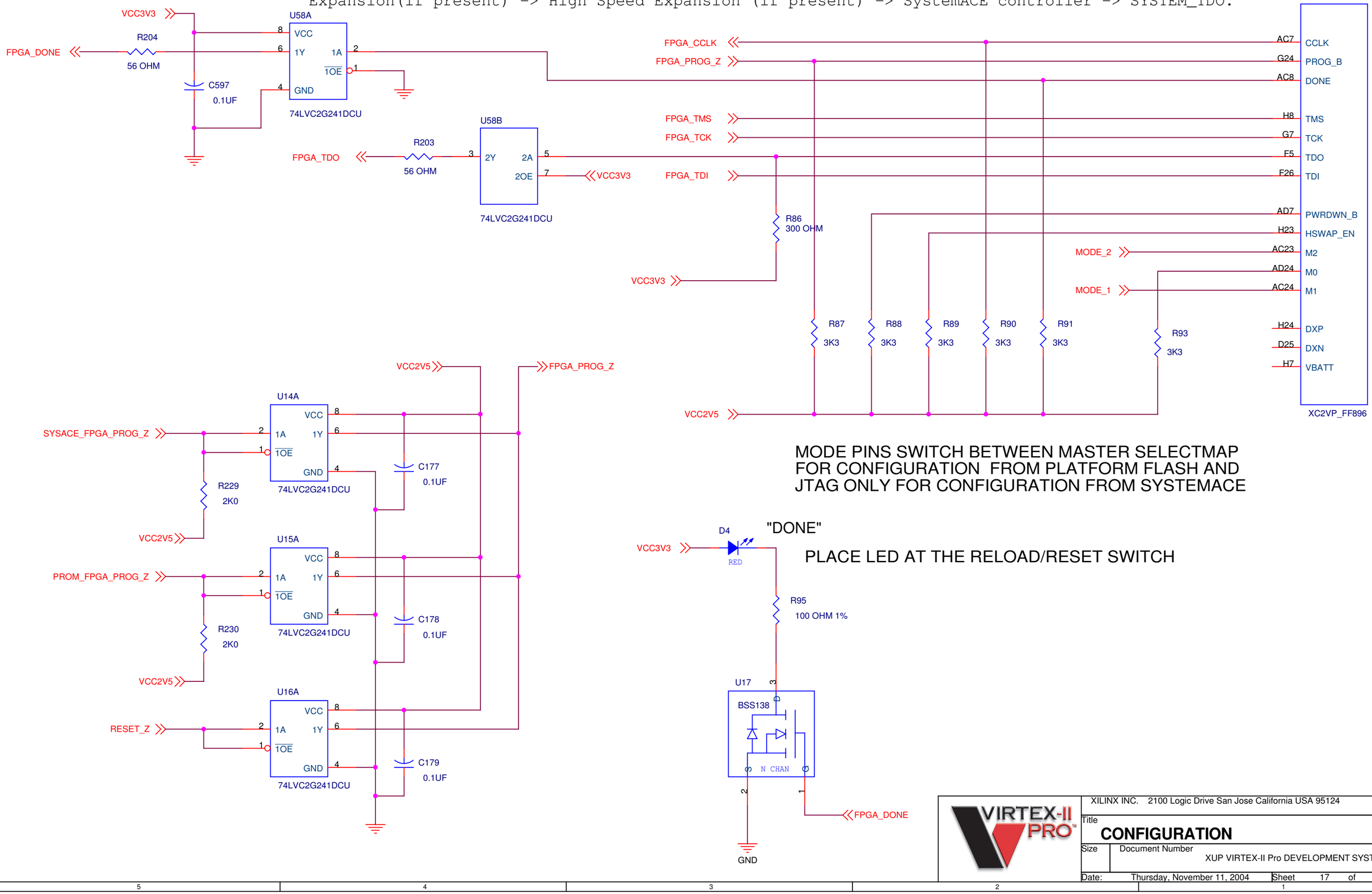
The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion(if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.



MODE PINS SWITCH BETWEEN MASTER SELECTMAP FOR CONFIGURATION FROM PLATFORM FLASH AND JTAG ONLY FOR CONFIGURATION FROM SYSTEMACE

"DONE"

PLACE LED AT THE RELOAD/RESET SWITCH

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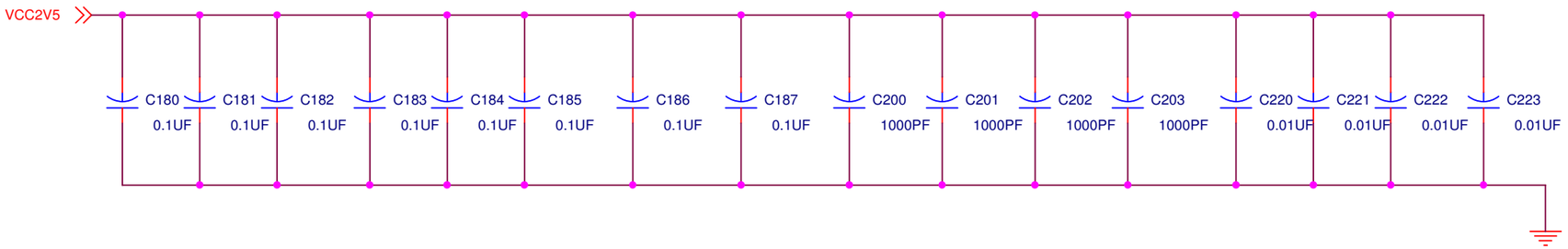
Title: **CONFIGURATION**

Size | Document Number: XUP VIRTEX-II Pro DEVELOPMENT SYSTEM | Rev C

Date: Thursday, November 11, 2004 | Sheet 17 of 38



DISTRIBUTE CAPS EVENLY ON ALL BANKS

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Title: **FPGA VAUX CAPS**

Size | Document Number: XUP VIRTEX-II Pro DEVELOPMENT SYSTEM | Rev: C

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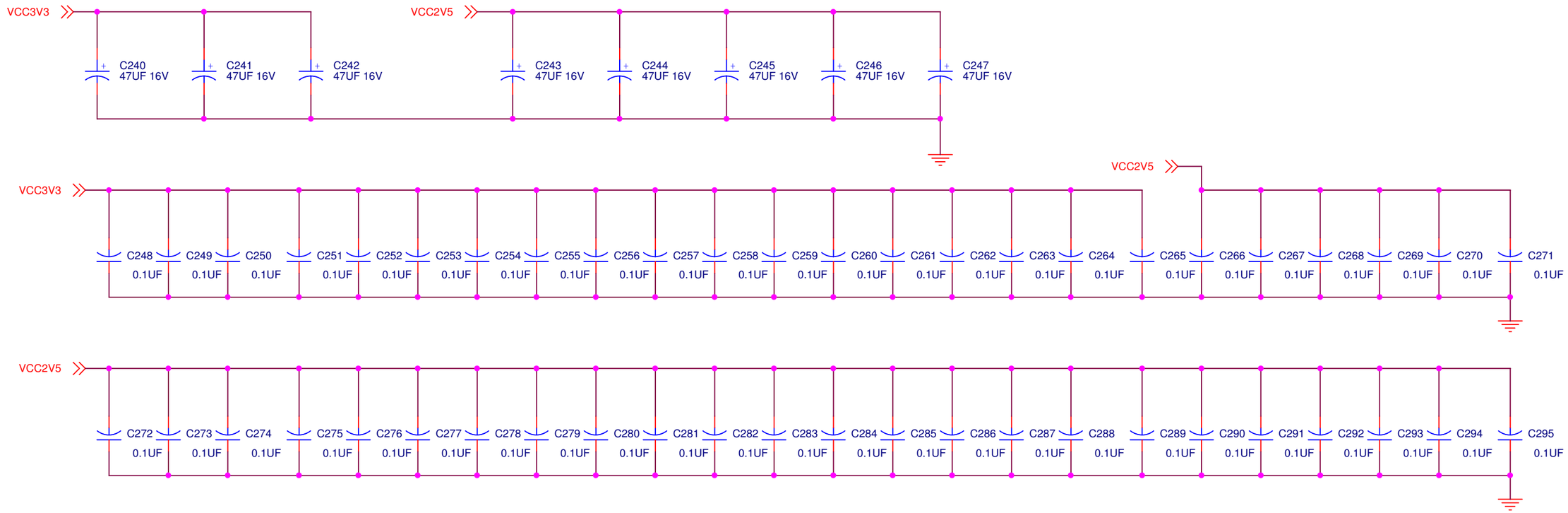

DISTRIBUTE CAPS EVENLY ON ALL BANKS

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title: **FPGA VCCO CAPS**

Size | Document Number: XUP VIRTEX-II Pro DEVELOPMENT SYSTEM | Rev: C

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"1.5V OK"

D5
GREEN
VCC5V0
R96
200 OHM
U18
BSS138
N CHAN
GND

R97
3K3

VCC5V0

C344
100UF 10V
C345
100UF 10V
C346
100UF 10V
C347
10UF
GND

U19
TPS54613
1.5 V FIXED
SYNCHRONOUS
REGULATOR
POWERPAD

RT
SYNC
SS/ENA
VBIAS
PWRGD
COMP
VSENSE
AGND
VIN0
VIN1
VIN2
VIN3
VIN4
PH0
PH1
PH2
PH3
PH4
PH5
PH6
PH7
PH8
BOOT
PGND0
PGND1
PGND2
PGND3
PGND4

C348
0.033UF
C349
0.1UF
AGND2

VCCINT_MON

C353
0.047UF

L19
6.0 uH
1V5

C350
330UF 6.3V
C351
330UF 6.3V
C352
330UF 6.3V

PLACE TERMINALS AT THE BOARD EDGE
J28
J29
TERMINAL
TERMINAL
GND

FPGA_VINT
1.5V @ 6A

FOR NORMAL OPERATION
INSTALL 3 SHORTING PLUGS

REMOVE SHORTING PLUGS
FOR CURRENT MONITORING OR
APPLICATION OF EXTERNAL POWER
AT THE TERMINALS

JP5
JUMPER_3X2

JP6
"1.5V DISABLE"
INSTALL SHORTING PLUG
TO DISABLE THE POWER SUPPLY
FOR APPLICATION OF EXTERNAL POWER
HDR_1X2

THE POWERPAD IS TIED TO AGND
FOLLOW THE LAYOUT GUIDELINES IN THE DATA SHEET
CONNECT AGND2 TO GND AT PIN 1
PROVIDE A COPPER HEATSINK OF AT LEASE 2 SQ
INCHES ON TOP AND BOTTOM LAYERS

SP7
SP8
SP9
SHORTING PLUG
SHORTING PLUG
SHORTING PLUG

VIRTEX-II PRO™

XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title
FPGA VINT

Size	Document Number	Rev
	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

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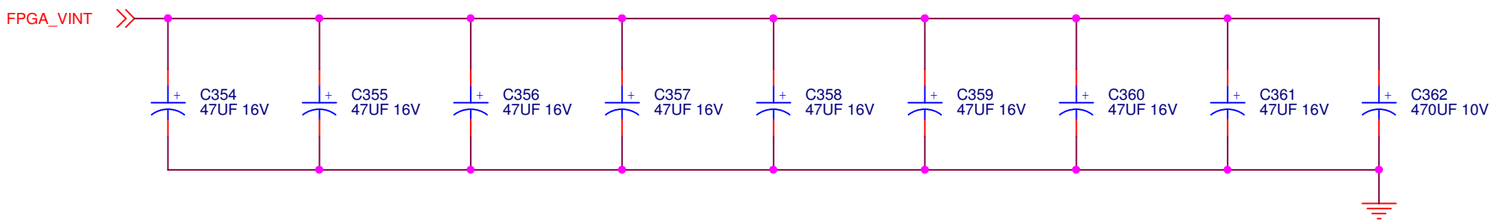

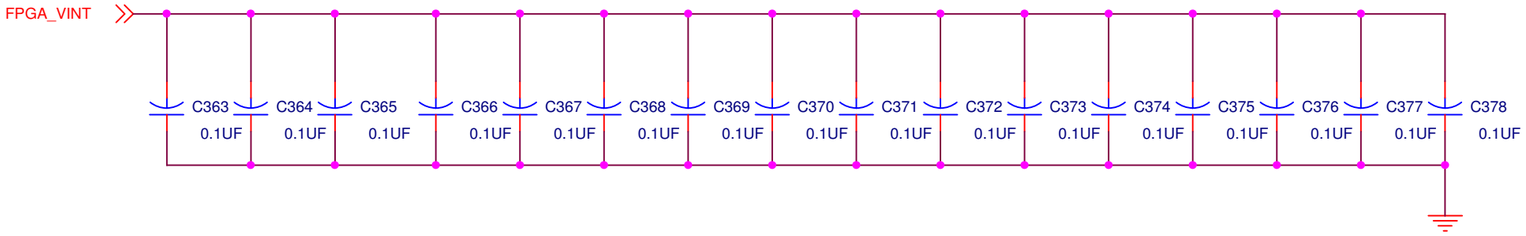

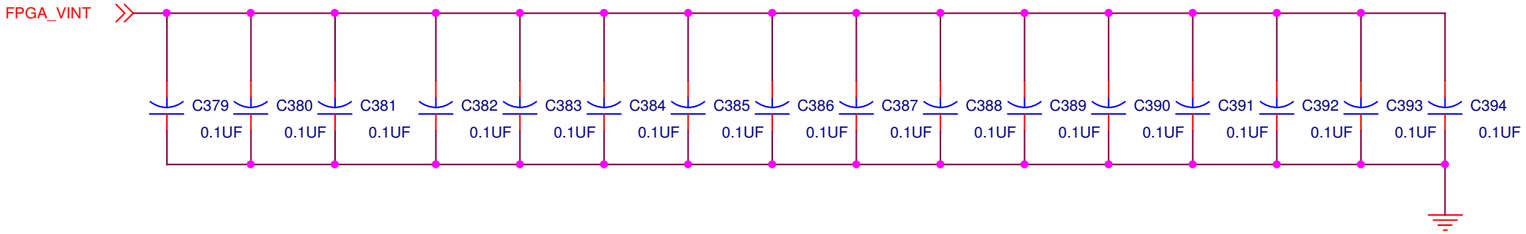

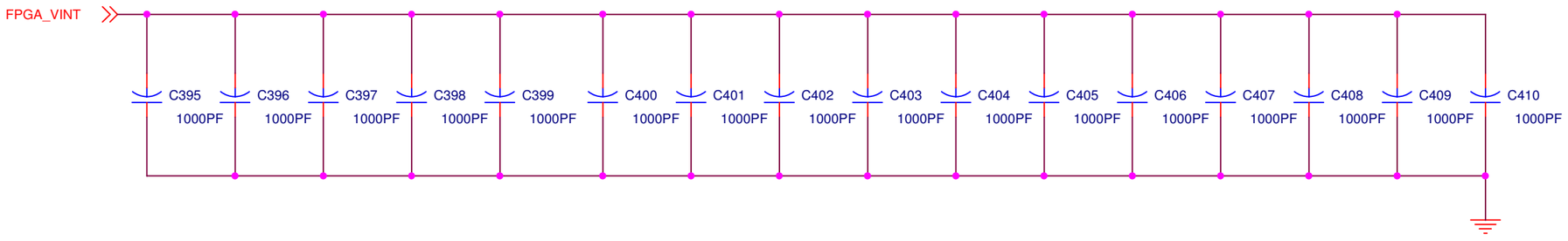

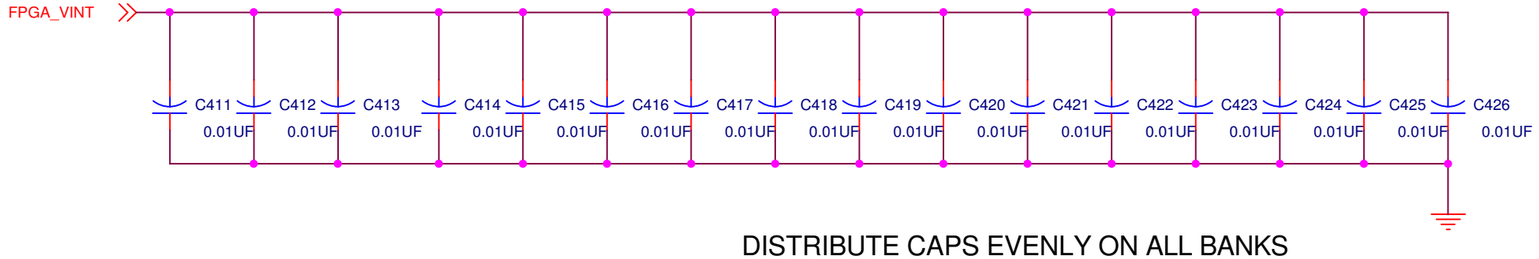

DISTRIBUTE CAPS EVENLY ON ALL BANKS

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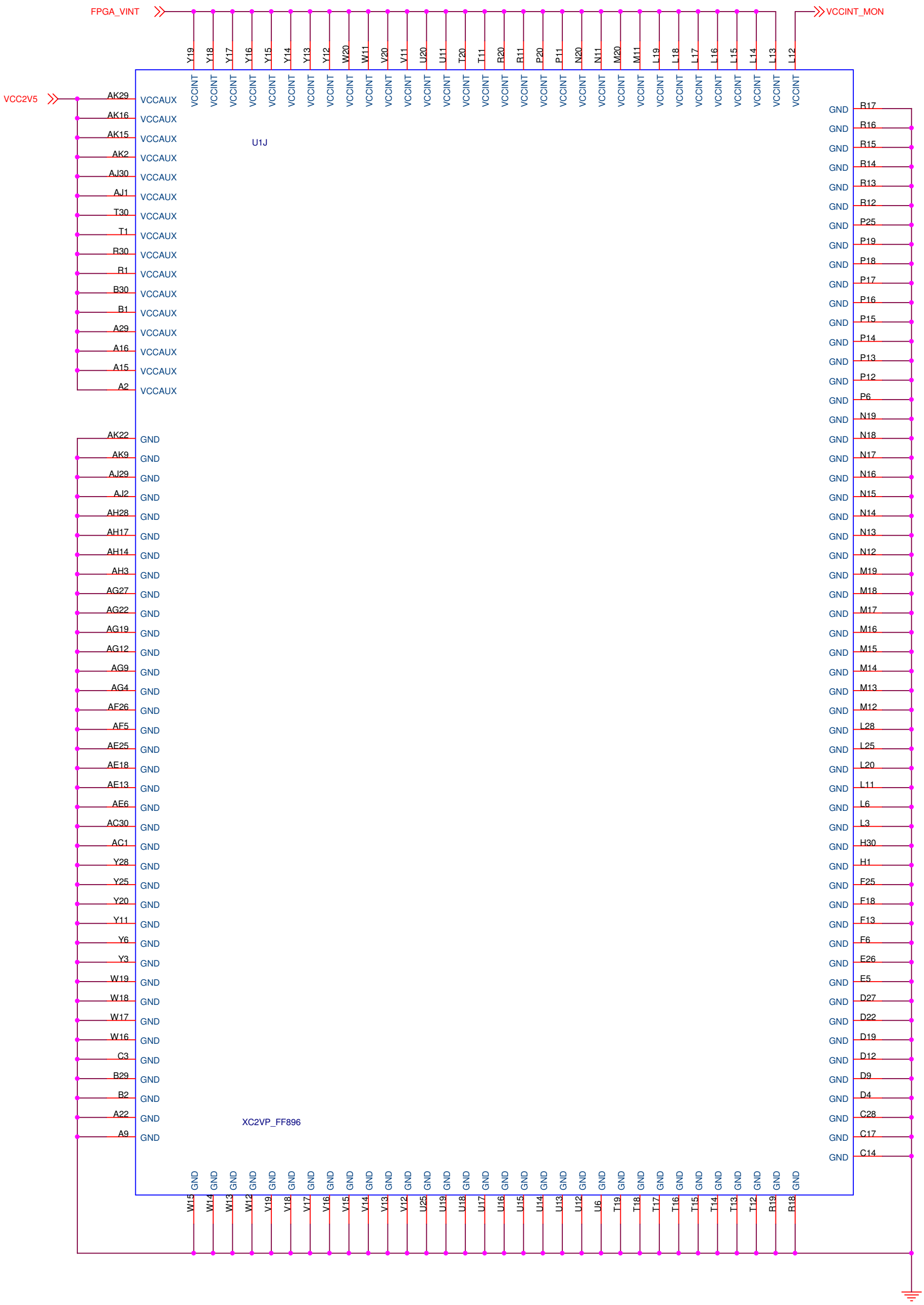
Title: **FPGA VINT CAPS**

Size | Document Number: XUP VIRTEX-II Pro DEVELOPMENT SYSTEM | Rev: C

Date: Thursday, November 11, 2004 | Sheet 21 of 38



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Title: **FPGA 0 VINT VAUX GND**

Size | Document Number: XUP VIRTEX-II Pro DEVELOPMENT SYSTEM | Rev: C

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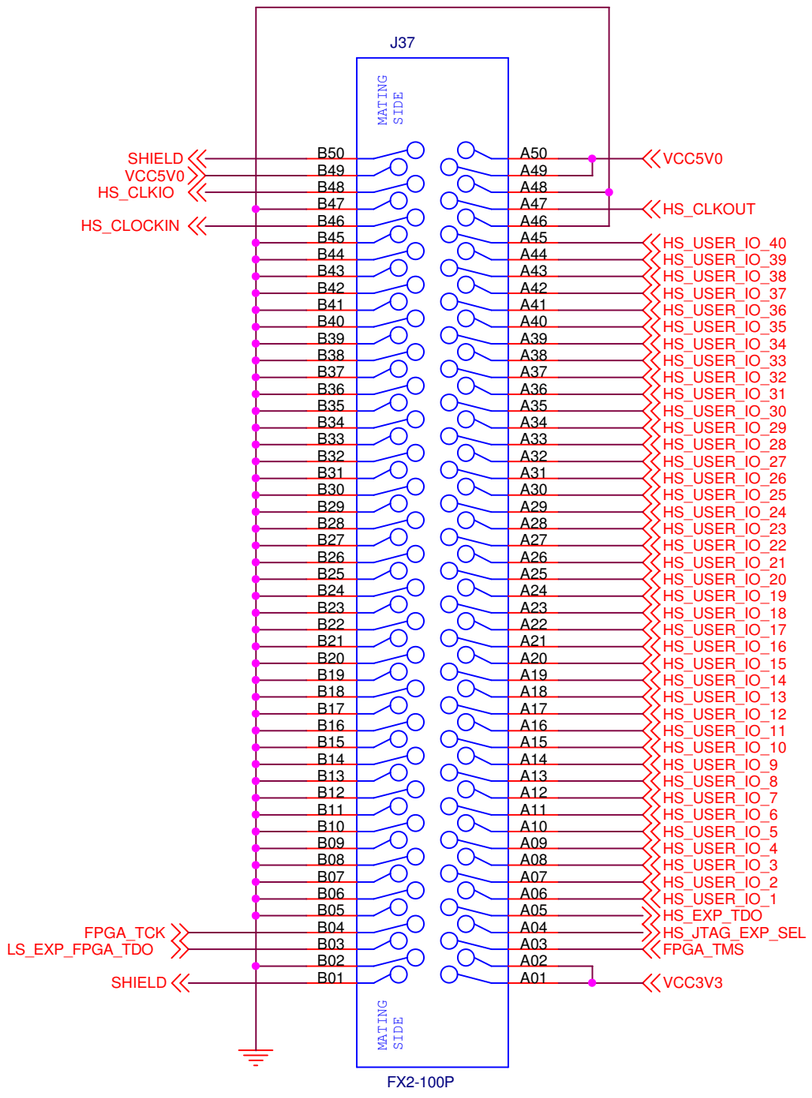
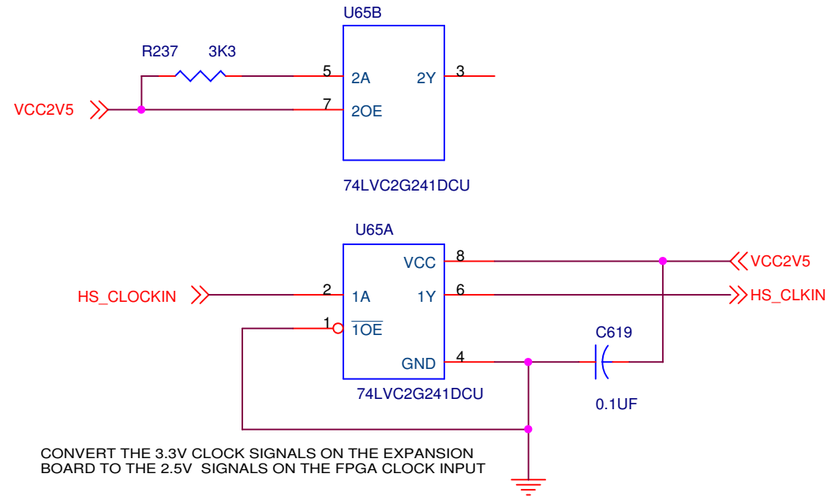
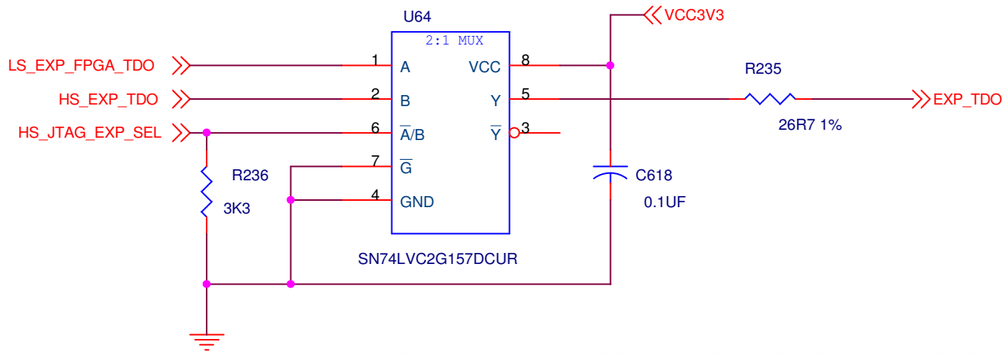
The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion(if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.







SELECT THE TDO FROM THE HIGH SPEED EXPANSION BOARD IF PRESENT. THE EXPANSION BOARD WILL PULL UP HS_JTAG_EXP_SEL.

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Title
HIGH SPEED EXPANSION PORT

Size	Document Number	Rev
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SDRAM NET LENGTH MATCHING

SIGNAL GROUP	MIN LENGTH	MAX LENGTH	NOTES
Command to Clock SDRAM_A[13:0] to SDRAM_CKn SDRAM_DM[7:0] to SDRAM_CKn SDRAM_RAS_Z to SDRAM_CKn SDRAM_CAS_Z to SDRAM_CKn SDRAM_WE_Z to SDRAM_CKn SDRAM_BA0 to SDRAM_CKn SDRAM_BA1 to SDRAM_CKn	SDRAM_CKn (MAX) - 2"	SDRAM_CKn (MIN) - 0.5"	MIN SPACING TO NON SDRAM SIGNALS 20 mils TRACE WIDTH 5 mils TRACE SPACING 12 mils (edge to edge)
Control to Clock SDRAM_CKE0 to SDRAM_CKn SDRAM_CKE1 to SDRAM_CKn SDRAM_S0_Z to SDRAM_CKn SDRAM_S1_Z to SDRAM_CKn	SDRAM_CKn (MAX) - 2"	SDRAM_CKn (MIN) - 0.5"	MIN SPACING TO NON SDRAM SIGNALS 20 mils TRACE WIDTH 5 mils TRACE SPACING 12 mils (edge to edge)
Strobe to Clock SDRAM_DQS8 to SDRAM_CKn SDRAM_DQS7 to SDRAM_CKn SDRAM_DQS6 to SDRAM_CKn SDRAM_DQS5 to SDRAM_CKn SDRAM_DQS4 to SDRAM_CKn SDRAM_DQS3 to SDRAM_CKn SDRAM_DQS2 to SDRAM_CKn SDRAM_DQS1 to SDRAM_CKn SDRAM_DQS0 to SDRAM_CKn	SDRAM_CKn (MAX) - 2"	SDRAM_CKn (MIN) + 1"	MIN SPACING TO NON SDRAM SIGNALS 20 mils TRACE WIDTH 5 mils TRACE SPACING 15 mils (edge to edge)
Data to Strobe SDRAM_CB[7:0] to SDRAM_DQS8 SDRAM_DQ[63:56] to SDRAM_DQS7 SDRAM_DQ[55:48] to SDRAM_DQS6 SDRAM_DQ[47:40] to SDRAM_DQS5 SDRAM_DQ[39:32] to SDRAM_DQS4 SDRAM_DQ[31:24] to SDRAM_DQS3 SDRAM_DQ[23:16] to SDRAM_DQS2 SDRAM_DQ[15:8] to SDRAM_DQS1 SDRAM_DQ[7:0] to SDRAM_DQS0	SDRAM_DQS8 - 25 mils SDRAM_DQS7 - 25 mils SDRAM_DQS6 - 25 mils SDRAM_DQS5 - 25 mils SDRAM_DQS4 - 25 mils SDRAM_DQS3 - 25 mils SDRAM_DQS2 - 25 mils SDRAM_DQS1 - 25 mils SDRAM_DQS0 - 25 mils	SDRAM_DQS8 + 25 mils SDRAM_DQS7 + 25 mils SDRAM_DQS6 + 25 mils SDRAM_DQS5 + 25 mils SDRAM_DQS4 + 25 mils SDRAM_DQS3 + 25 mils SDRAM_DQS2 + 25 mils SDRAM_DQS1 + 25 mils SDRAM_DQS0 + 25 mils	MIN SPACING TO NON SDRAM SIGNALS 20 mils TRACE WIDTH 5 mils TRACE SPACING 12 mils (edge to edge) MINIMUM TRACE LENGTH 1.5"
Differential Clock Length SDRAM_CK0_Z to SDRAM_CK0 SDRAM_CK1_Z to SDRAM_CK1 SDRAM_CK2_Z to SDRAM_CK2	SDRAM_CK0 - 10 mils SDRAM_CK1 - 10 mils SDRAM_CK2 - 10 mils	SDRAM_CK0 + 10 mils SDRAM_CK1 + 10 mils SDRAM_CK2 + 10 mils	ROUTE AS 100 OHM DIFFERENTIAL MIN SPACING TO OTHER SDRAM SIGNALS 20 mils MIN SPACING TO NON SDRAM SIGNALS 20 mils TRACE WIDTH 8 mils TRACE SPACING 5 mils (edge to edge)
Clock to Clock Length SDRAM_CKm to SDRAM_CKn SDRAM_CLOCK_FEEDBACK_LOOP	SDRAM_CKn - 20 mils	SDRAM_CKn + 20 mils	MINIMUM TRACE LENGTH 3.5"

SIGNAL GROUP	MIN LENGTH	MAX LENGTH	NOTES
Differential Net Lengths MGT_CLK_N to MGT_CLK_P EXTERNAL_CLOCK_N to EXTERNAL_CLOCK_P MGT_TXN to MGT_TXP MGT_RXN to MGT_RXP SATA_PRT0_TXN to SATA_PRT0_TXP SATA_PRT0_RXN to SATA_PRT0_RXP SATA_PRT1_TXN to SATA_PRT1_TXP SATA_PRT1_RXN to SATA_PRT1_RXP SATA_PRT2_TXN to SATA_PRT2_TXP SATA_PRT2_RXN to SATA_PRT2_RXP SATA_PORT0_TXN to SATA_PORT0_TXP SATA_PORT1_TXN to SATA_PORT1_TXP SATA_PORT2_TXN to SATA_PORT2_TXP	MGT_CLK_P - 10 mils EXTERNAL_CLOCK_P - 10 mils MGT_TXP - 10 mils MGT_RXP - 10 mils SATA_PRT0_TXP - 10 mils SATA_PRT0_RXP - 10 mils SATA_PRT1_TXP - 10 mils SATA_PRT1_RXP - 10 mils SATA_PRT2_TXP - 10 mils SATA_PRT2_RXP - 10 mils SATA_PORT0_TXP - 10 mils SATA_PORT1_TXP - 10 mils SATA_PORT2_TXP - 10 mils	MGT_CLK_P + 10 mils EXTERNAL_CLOCK_P + 10 mils MGT_TXP + 10 mils MGT_RXP + 10 mils SATA_PRT0_TXP + 10 mils SATA_PRT0_RXP + 10 mils SATA_PRT1_TXP + 10 mils SATA_PRT1_RXP + 10 mils SATA_PRT2_TXP + 10 mils SATA_PRT2_RXP + 10 mils SATA_PORT0_TXP + 10 mils SATA_PORT1_TXP + 10 mils SATA_PORT2_TXP + 10 mils	ROUTE AS 100 OHM DIFFERENTIAL MIN SPACING TO OTHER SIGNALS 20 mils TRACE WIDTH 8 mils TRACE SPACING 5 mils (edge to edge) INCLUDE THE "R", "C" and FPGA ballout lengths

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Title: **LENGTH MATCHING RULES**

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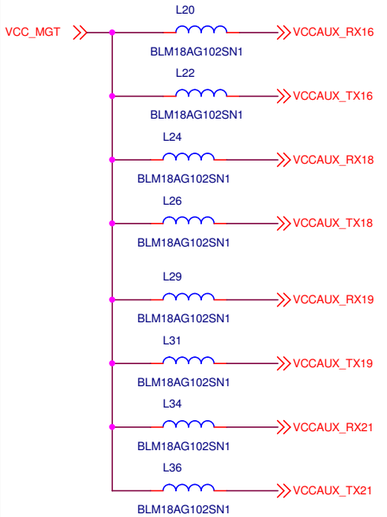

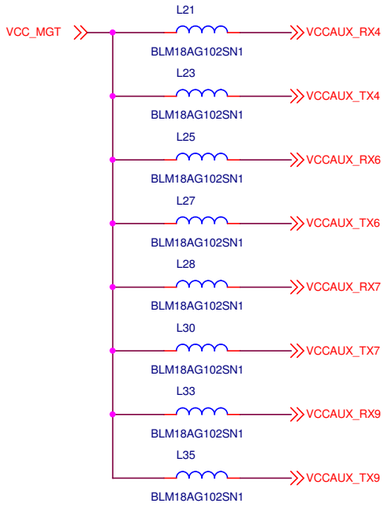

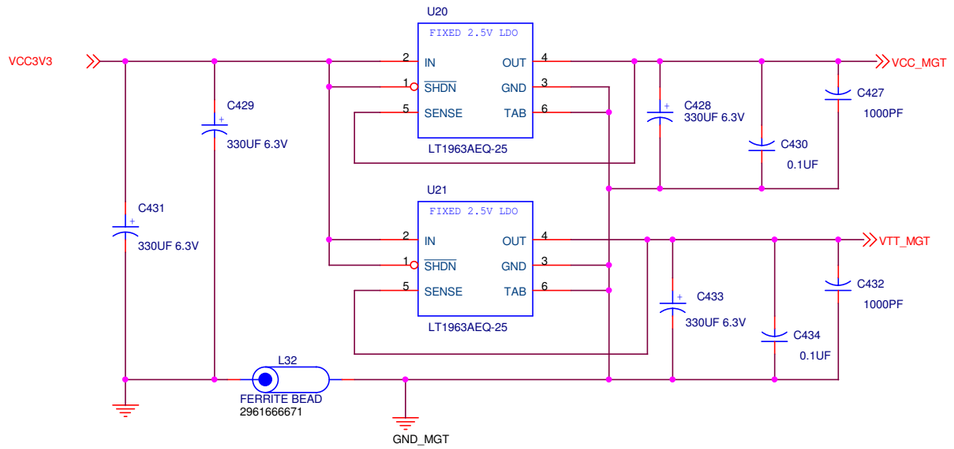

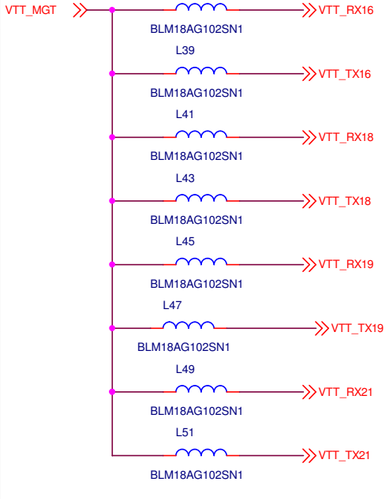

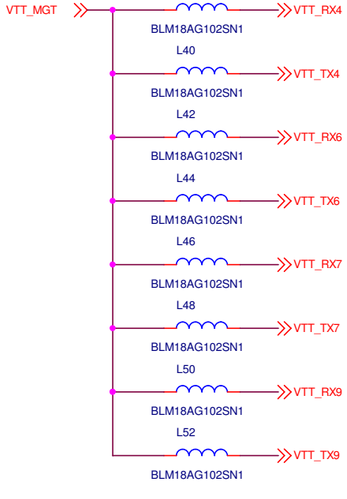

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Title: **MGT FILTERS & POWER**

Size | Document Number: XUP VIRTEX-II Pro DEVELOPMENT SYSTEM | Rev: C

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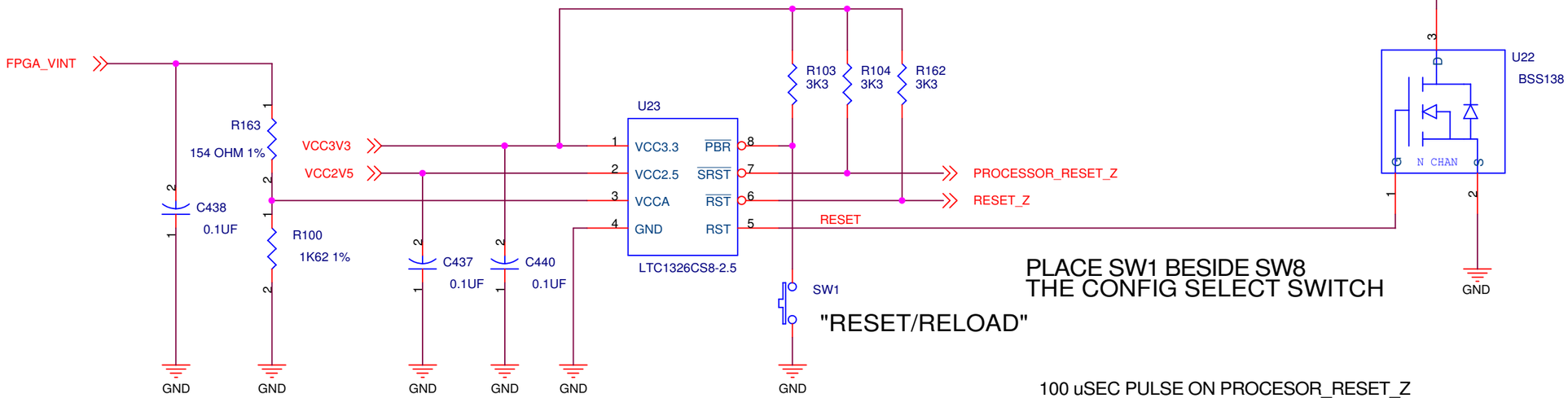
PLACE LED AT THE RELOAD/RESET SWITCH

"RELOAD PS ERROR"

R98
348 OHM 1%



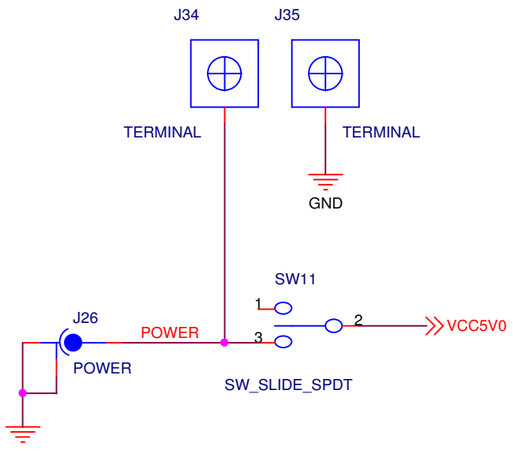
"RESET/RELOAD"

PLACE SW1 BESIDE SW8
THE CONFIG SELECT SWITCH

100 uSEC PULSE ON PROCESOR_RESET_Z
WHEN SW1 IS PRESSED FOR LESS THAN 2 SEC.

200 mSEC PULSE ON RESET_Z ON POWER UP
OR WHEN SW1 IS PRESSED FOR MORE THAN 2
SEC.

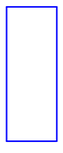
PLACE TERMINALS AT THE BOARD EDGE



X2

0.375 8-32 HEX STANDOFF

X4

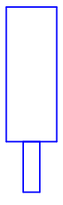


0.375 8-32 HEX STANDOFF

X5

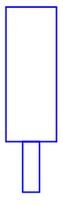
1.750 8-32 HEX STANDOFF

X6



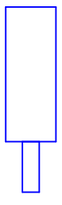
1.750 8-32 HEX STANDOFF

X7



1.750 8-32 HEX STANDOFF

X8

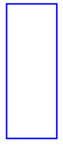


1.750 8-32 HEX STANDOFF

X1

0.375 8-32 HEX STANDOFF

X3



0.375 8-32 HEX STANDOFF

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Title
POWER MONITOR & RESET GENERATION

Size	Document Number	Rev
	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

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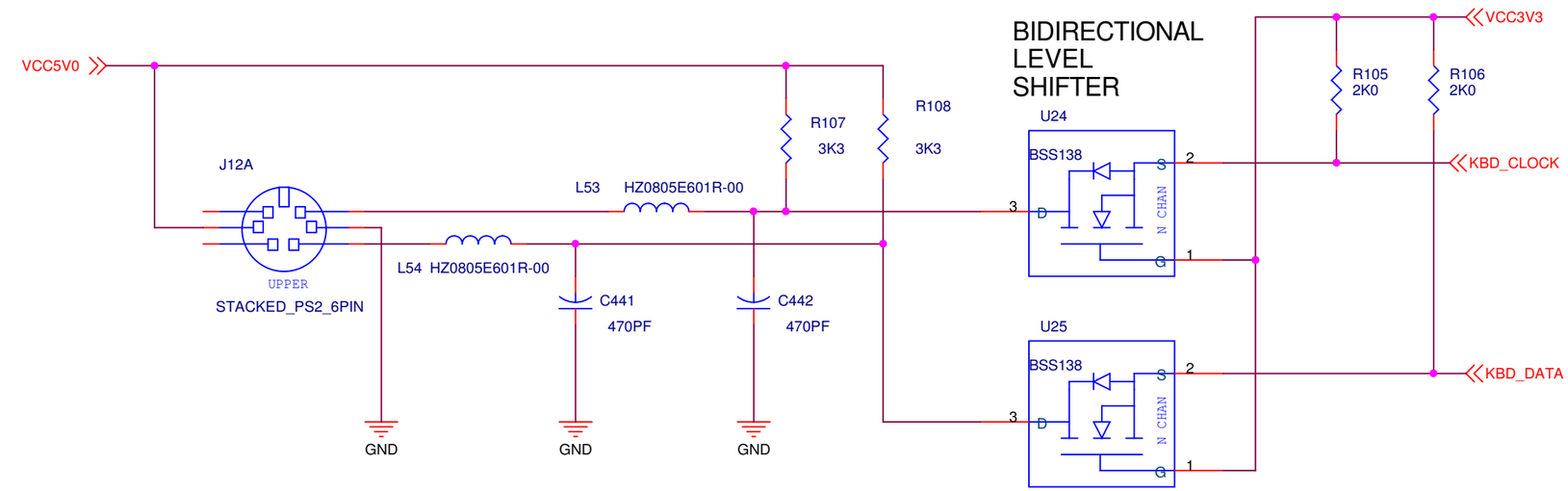

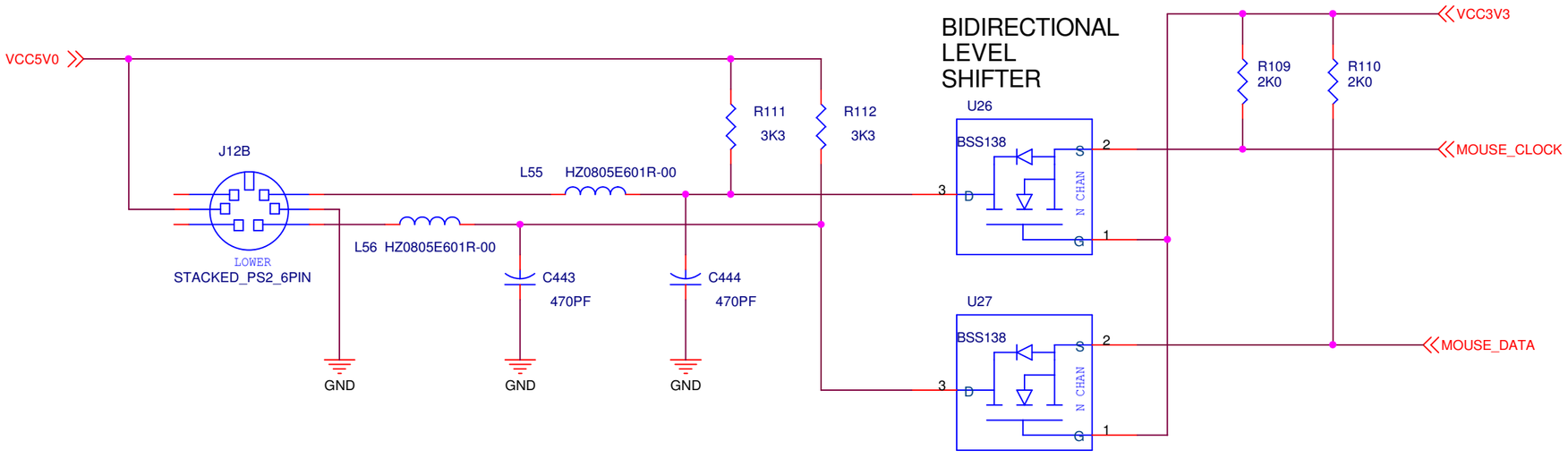

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Title: **PS/2 PORTS**

Size	Document Number	Rev
B	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

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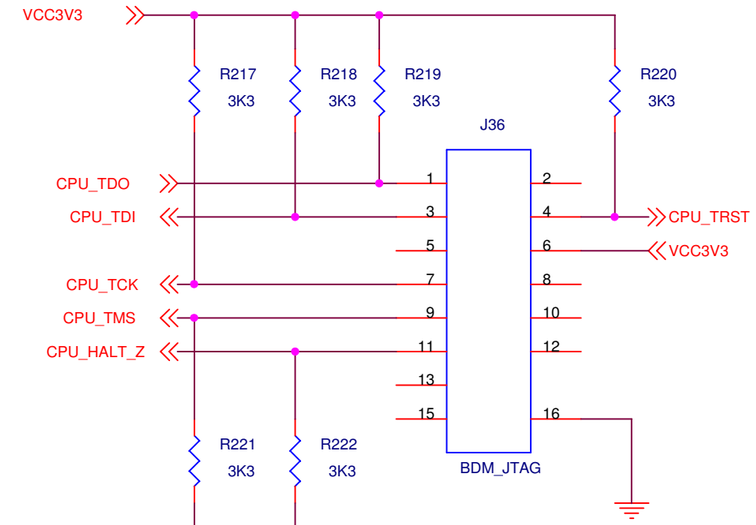

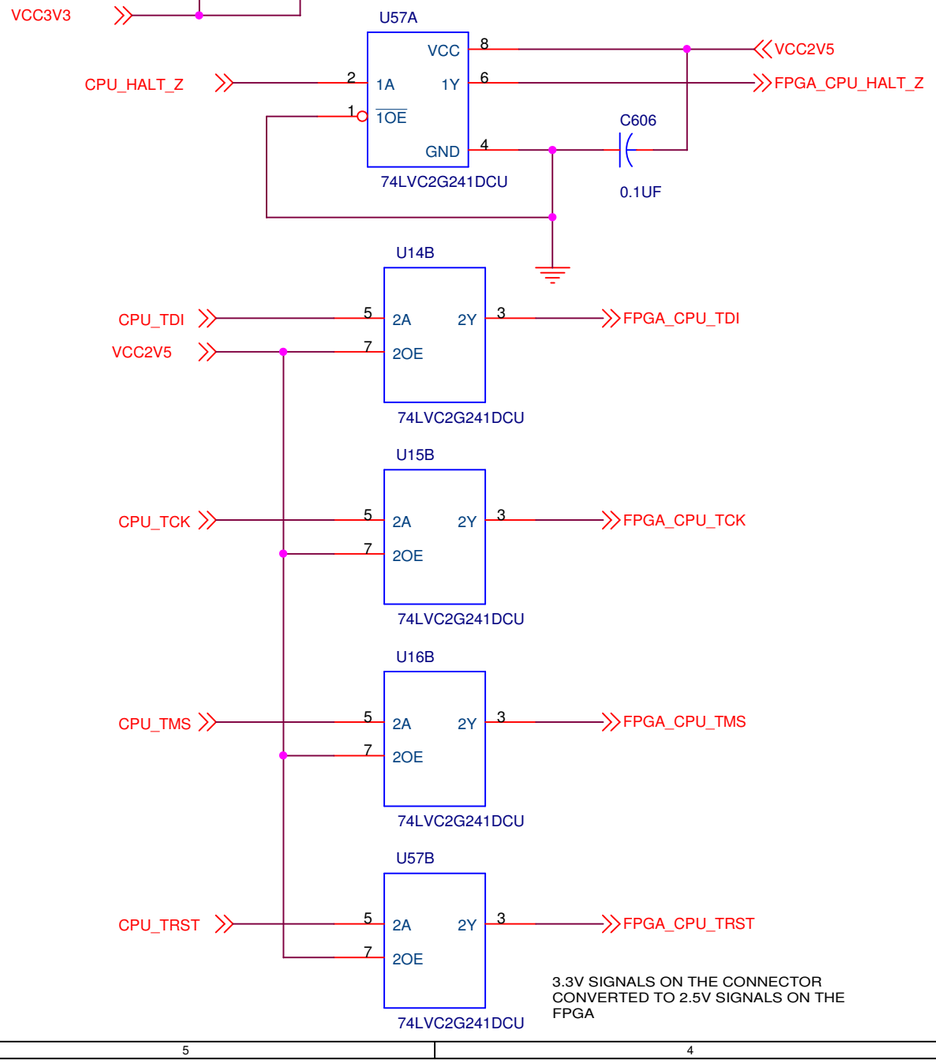

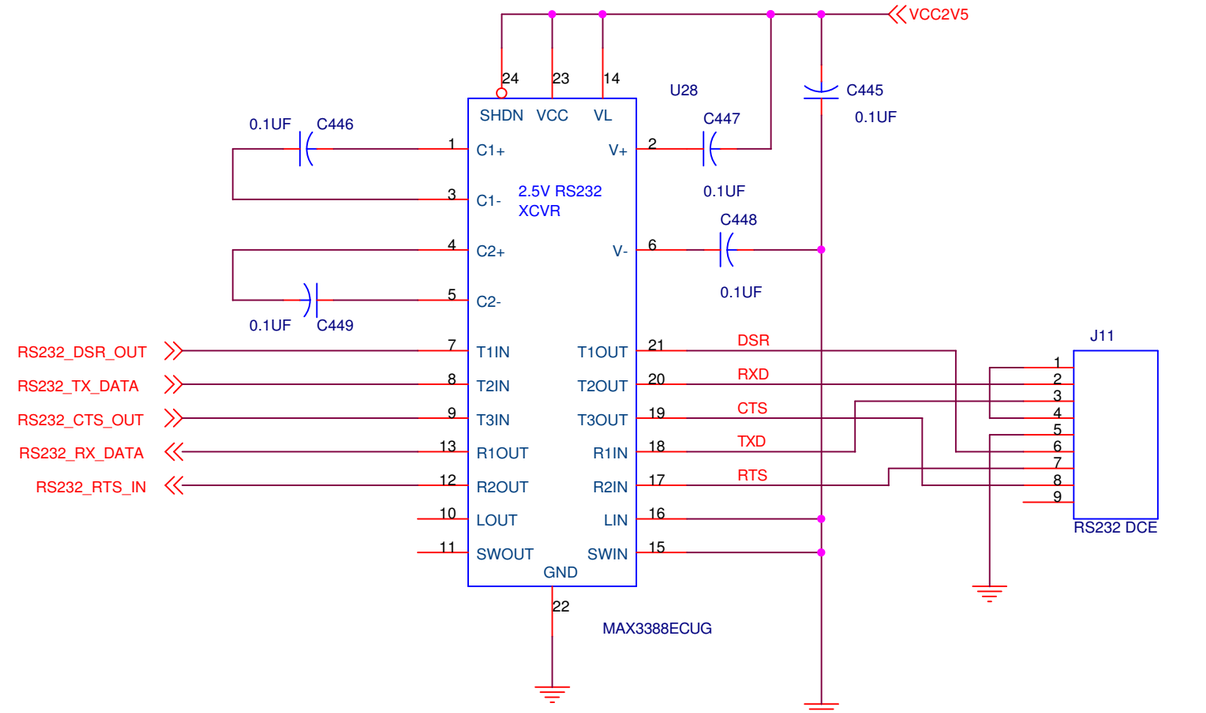

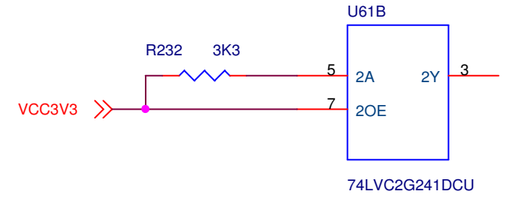

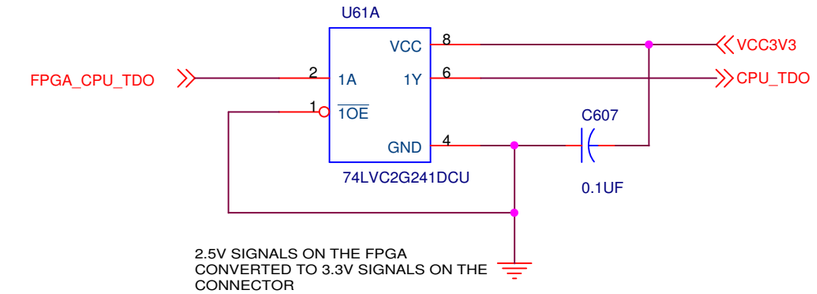

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Title

SERIAL PORT & DEBUG PORT

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ALL TX/RX PAIRS TO BE MATCHED IN LENGTH AND ROUTED AS 100 OHM DIFFERENTIAL PAIRS

THE BOTTOM SIDE MGTS ARE UNUSED

J16 — HOST — SERIAL ATA — SATA
KEY
GND_1 1
HT+ 2 SATA_PRT0_TXP
HT- 3 SATA_PRT0_TXN
GND_2 4
HR- 5 SATA_PRT0_RXN
HR+ 6 SATA_PRT0_RXP
GND_3 7

J17 — TARGET — SERIAL ATA — SATA
KEY
GND_1 1
HT+ 2 SATA_PRT1_RXP
HT- 3 SATA_PRT1_RXN
GND_2 4
HR- 5 SATA_PRT1_TXN
HR+ 6 SATA_PRT1_TXP
GND_3 7

J18 — HOST — SERIAL ATA — SATA
KEY
GND_1 1
HT+ 2 SATA_PRT2_TXP
HT- 3 SATA_PRT2_TXN
GND_2 4
HR- 5 SATA_PRT2_RXN
HR+ 6 SATA_PRT2_RXP
GND_3 7

U1L — BOTTOM MGTs — XC2VP_FF896

AK4	RXNPAD16	AVCCAUXRX16	AJ4 — VCCAUX_RX16
AK5	RXPPAD16	VTRXPAD16	AJ5 — VTT_RX16
AK6	TXPPAD16	GNDA16	AH6
AK7	TXNPAD16	VTTXPAD16	AJ7 — VTT_TX16
		AVCCAUXTX16	AJ6 — VCCAUX_TX16
AK11	RXNPAD18	AVCCAUXRX18	AJ11 — VCCAUX_RX18
AK12	RXPPAD18	VTRXPAD18	AJ12 — VTT_RX18
AK13	TXPPAD18	GNDA18	AH12
AK14	TXNPAD18	VTTXPAD18	AJ14 — VTT_TX18
		AVCCAUXTX18	AJ13 — VCCAUX_TX18
AK17	RXNPAD19	AVCCAUXRX19	AJ17 — VCCAUX_RX19
AK18	RXPPAD19	VTRXPAD19	AJ18 — VTT_RX19
AK19	TXPPAD19	GNDA19	AH19
AK20	TXNPAD19	VTTXPAD19	AJ20 — VTT_TX19
		AVCCAUXTX19	AJ19 — VCCAUX_TX19
AK24	RXNPAD21	AVCCAUXRX21	AJ24 — VCCAUX_RX21
AK25	RXPPAD21	VTRXPAD21	AJ25 — VTT_RX21
AK26	TXPPAD21	GNDA21	AH25
AK27	TXNPAD21	VTTXPAD21	AJ27 — VTT_TX21
		AVCCAUXTX21	AJ26 — VCCAUX_TX21

GND_MGT

U1K — TOP MGTs — XC2VP_FF896

A27	TXNPAD4	AVCCAUXTX4	B26 — VCCAUX_TX4
A26	TXPPAD4	VTTXPAD4	B27 — VTT_TX4
A25	RXPPAD4	GNDA4	C25
A24	RXNPAD4	VTRXPAD4	B25 — VTT_RX4
		AVCCAUXRX4	B24 — VCCAUX_RX4
A20	TXNPAD6	AVCCAUXTX6	B19 — VCCAUX_TX6
A19	TXPPAD6	VTTXPAD6	B20 — VTT_TX6
A18	RXPPAD6	GNDA6	C19
A17	RXNPAD6	VTRXPAD6	B18 — VTT_RX6
		AVCCAUXRX6	B17 — VCCAUX_RX6
A14	TXNPAD7	AVCCAUXTX7	B13 — VCCAUX_TX7
A13	TXPPAD7	VTTXPAD7	B14 — VTT_TX7
A12	RXPPAD7	GNDA7	C12
A11	RXNPAD7	VTRXPAD7	B12 — VTT_RX7
		AVCCAUXRX7	B11 — VCCAUX_RX7
A7	TXNPAD9	AVCCAUXTX9	B6 — VCCAUX_TX9
A6	TXPPAD9	VTTXPAD9	B7 — VTT_TX9
A5	RXPPAD9	GNDA9	C6
A4	RXNPAD9	VTRXPAD9	B5 — VTT_RX9
		AVCCAUXRX9	B4 — VCCAUX_RX9

GND_MGT

SATA_PRT0_TXN — C598 0.1UF — R182 49R9 1% — SATA_PORT0_TXN — A27
SATA_PRT0_TXP — C599 0.1UF — R183 49R9 1% — SATA_PORT0_TXP — A26
SATA_PORT0_RXP — A25
SATA_PORT0_RXN — C450 0.1UF — C451 0.1UF — A24

SATA_PRT1_TXN — C600 0.1UF — R205 49R9 1% — SATA_PORT1_TXN — A20
SATA_PRT1_TXP — C601 0.1UF — R206 49R9 1% — SATA_PORT1_TXP — A19
SATA_PORT1_RXP — A18
SATA_PORT1_RXN — C452 0.1UF — C453 0.1UF — A17

SATA_PRT2_TXN — C602 0.1UF — R184 49R9 1% — SATA_PORT2_TXN — A14
SATA_PRT2_TXP — C603 0.1UF — R185 49R9 1% — SATA_PORT2_TXP — A13
SATA_PORT2_RXP — A12
SATA_PORT2_RXN — C454 0.1UF — C455 0.1UF — A11

MGT_TXN — A7
MGT_TXP — A6
MGT_RXP — A5
MGT_RXN — A4

VCC3V3

R186 1K0 — U50 — SATA0_IDLE — SATA_PORT0_TXP — SATA_PORT0_TXN — C586 0.1UF
R187 1K0 — U51 — SATA1_IDLE — SATA_PORT1_TXP — SATA_PORT1_TXN — C587 0.1UF
R207 1K0 — U59 — SATA2_IDLE — SATA_PORT2_TXP — SATA_PORT2_TXN — C604 0.1UF

FET SWITCH: OE, VCC, A, GND, B
74CBTLV1G125DBV

J19 — SMA_CON — MGT_TXP
J20 — SMA_CON — MGT_TXN
J21 — SMA_CON — MGT_RXP
J22 — SMA_CON — MGT_RXN

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Title: **SERIAL ATA MGTs**

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XILINX INC. 2100 Logic Drive San Jose California USA 95124

Title: **SVGA OUTPUT**

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B	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

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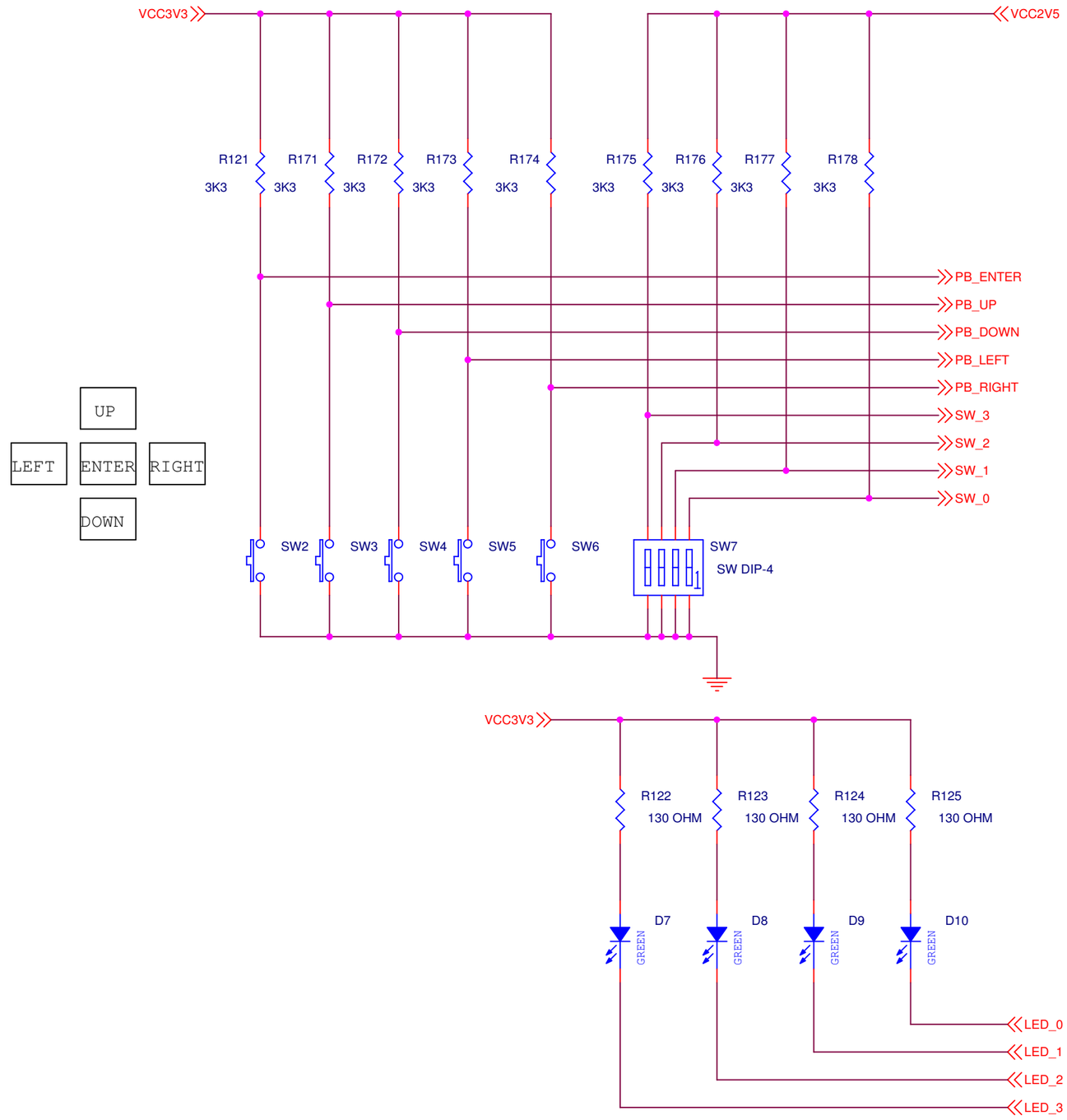

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Title

SWITCHES & LEDS

Size	Document Number	Rev
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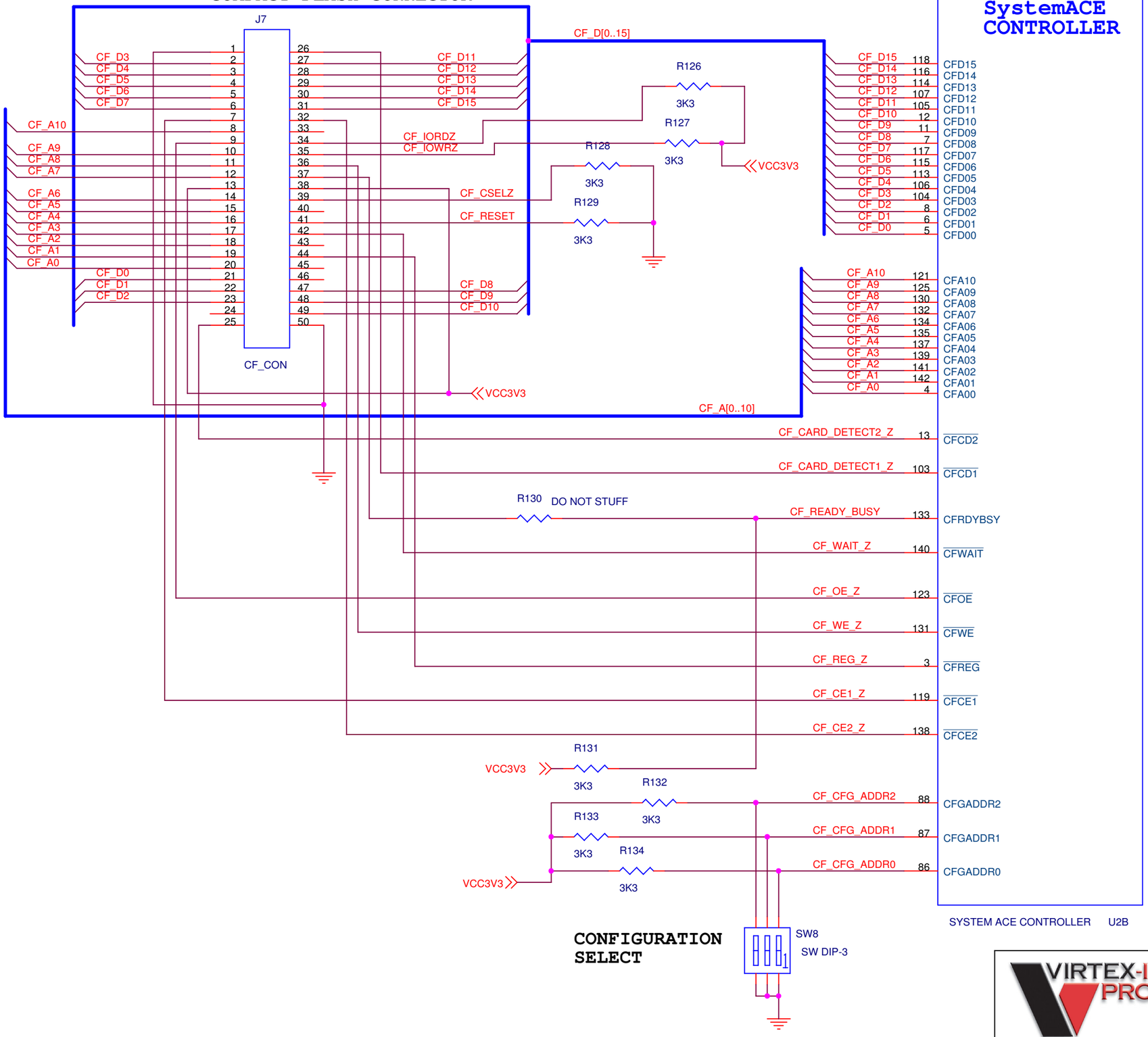
COMPACT FLASH CONNECTOR



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Title: **SYSTEMACE COMPACT FLASH PORT**

Size	Document Number	Rev
	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C

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The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion(if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.

U2A

SystemACE CONTROLLER

SYSTEM_TDO — R164 56 OHM — 97 TSTTDO
PROM_SYSACE_TMS — 98 TSTTMS
PROM_SYSACE_TCK — 101 TSTTCK
PROM_TDO — 102 TSTTDI

FPGA_INIT — 78 CFGINIT0
SYSACE_FPGA_PROG_Z — R135 56 OHM — 79 CFGPROG0
FPGA_TMS — R136 56 OHM — 85 CFGTMS0
FPGA_TCK — R137 56 OHM — 80 CFGTCK0
EXP_TDO — 81 CFGTDI0
FPGA_TDI — R138 56 OHM — 82 CFGTDO0

R139 3K3, R140 3K3, R141 3K3, R142 3K3, R143 3K3 — VCC3V3

16 CFGINIT3
124 CFGPROG3
127 CFGTMS3
14 CFGTCK3
20 CFGTDI3
122 CFGTDO3

19 CFGINIT2
22 CFGPROG2
23 CFGTMS2
24 CFGTCK2
27 CFGTDI2
21 CFGTDO2

90 CFGINIT1
29 CFGPROG1
30 CFGTMS1
31 CFGTCK1
32 CFGTDI1
28 CFGTDO1

VCC3V3 — R146 3K3 — 89 CFGMODE

SYSTEM ACE CONTROLLER

MPA00 70 CF_MPA0
MPA01 69 CF_MPA1
MPA02 68 CF_MPA2
MPA03 67 CF_MPA3
MPA04 45 CF_MPA4
MPA05 44 CF_MPA5
MPA06 43 CF_MPA6

RN16 47 OHM
MPD00 66 CF_MPD0_T — 1 16 CF_MPD0
MPD01 65 CF_MPD1_T — 2 15 CF_MPD1
MPD02 63 CF_MPD2_T — 3 14 CF_MPD2
MPD03 62 CF_MPD3_T — 4 13 CF_MPD3
MPD04 61 CF_MPD4_T — 5 12 CF_MPD4
MPD05 60 CF_MPD5_T — 6 11 CF_MPD5
MPD06 59 CF_MPD6_T — 7 10 CF_MPD6
MPD07 58 CF_MPD7_T — 8 09 CF_MPD7

RN17 47 OHM
MPD08 56 CF_MPD8_T — 1 16 CF_MPD8
MPD09 53 CF_MPD9_T — 2 15 CF_MPD9
MPD10 52 CF_MPD10_T — 3 14 CF_MPD10
MPD11 51 CF_MPD11_T — 4 13 CF_MPD11
MPD12 50 CF_MPD12_T — 5 12 CF_MPD12
MPD13 49 CF_MPD13_T — 6 11 CF_MPD13
MPD14 48 C0_MPD14_T — 7 10 CF_MPD14
MPD15 47 CF_MPD15_T — 8 09 CF_MPD15

MPCE 42 CF_MPCE_Z
MPWE 76 CF_MPWE_Z
MPOE 77 CF_MPOE_Z
MPIRQ 41 CF_MPIRQ
MPBRDY 39 CF_MPBRDY

ERRLED 96 — SYSACE_ERROR — D11 RED — "SYSTEMACE ERROR" — R144
STATLED 95 — SYSACE_STATUS — D12 GREEN — "SYSTEMACE STATUS" — R145 130 OHM — 130 OHM — VCC3V3
RESET 33 RESET_Z
CLK 93 SYSTEMACE_CLOCK

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Title: **SYSTEMACE MICRO PORT & JTAG TEST PORT**

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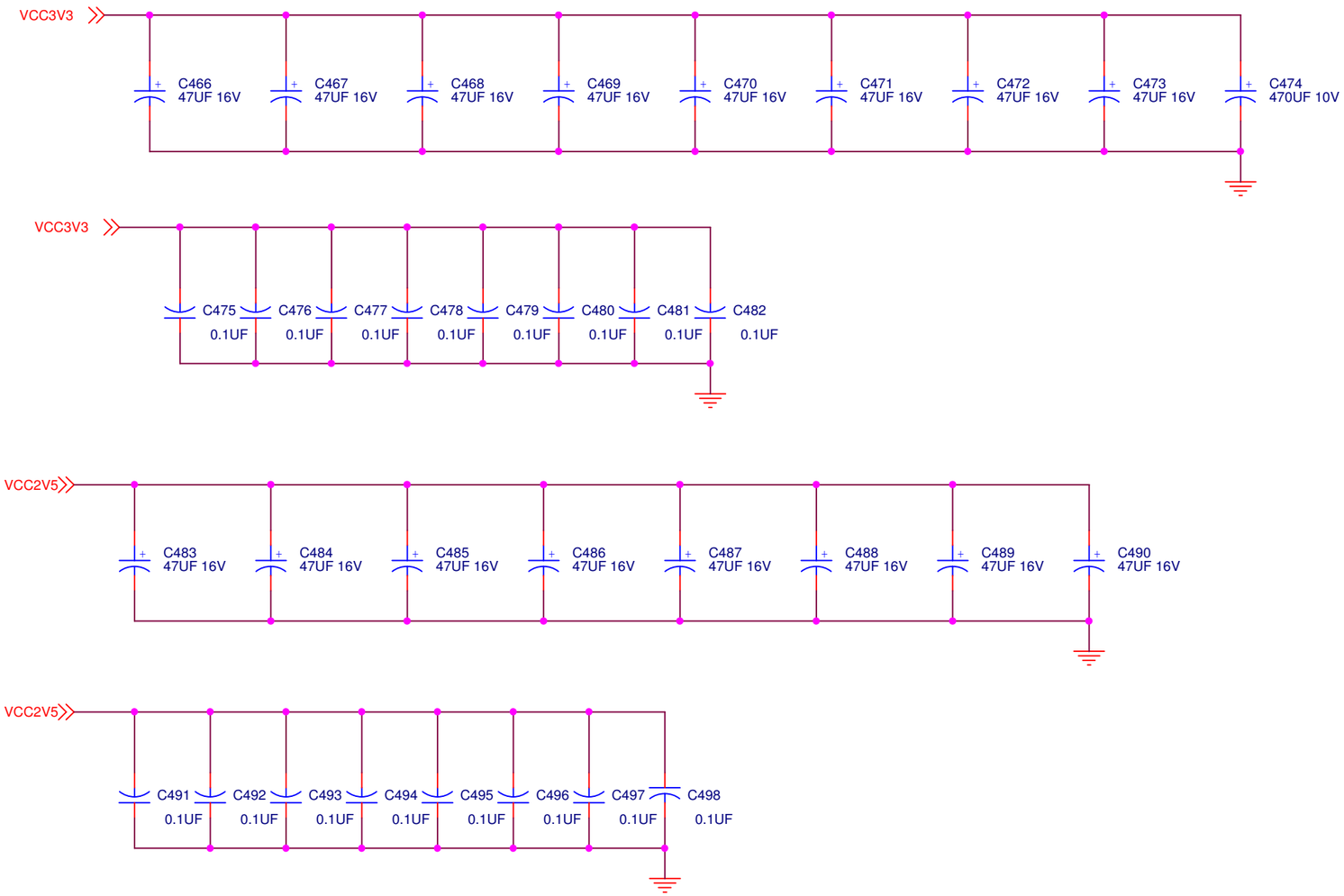

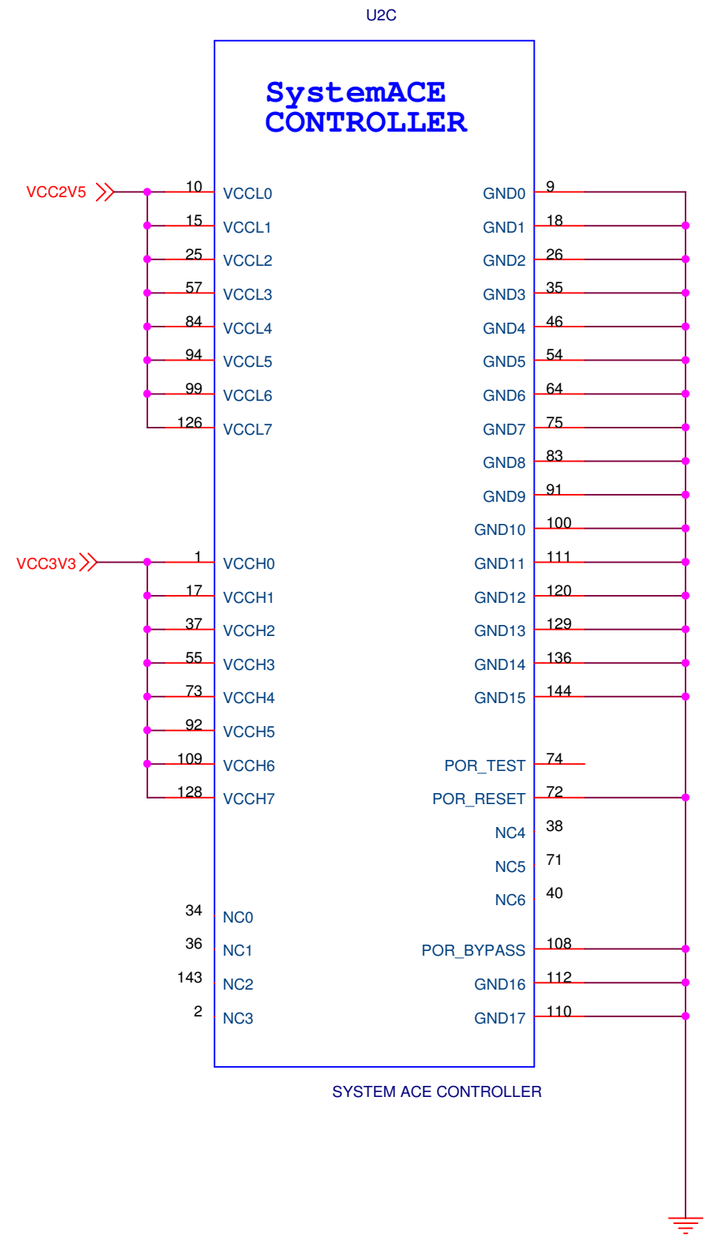

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Title: **SYSTEMACE CONTROLLER POWER**

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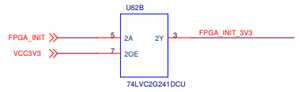
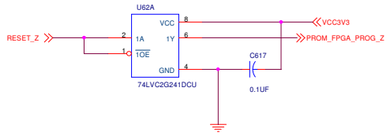
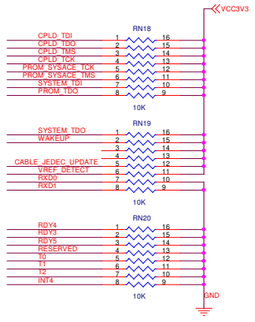
The JTAG programming chain is SYSTEM_TDI -> Platform FLASH -> SystemACE controller -> FPGA -> Digilent Expansion(if present) -> High Speed Expansion (if present) -> SystemACE controller -> SYSTEM_TDO.

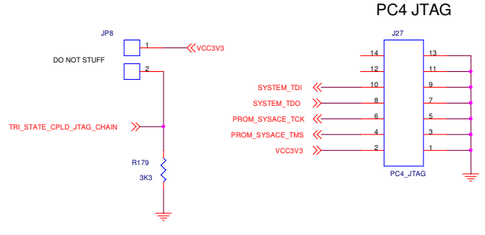


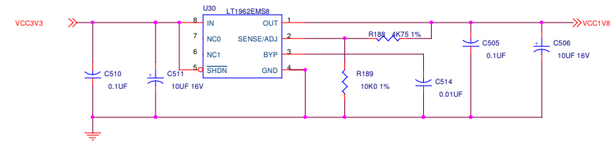


Drive the CF pin on the PROM LOW during reset to resample the version pins.

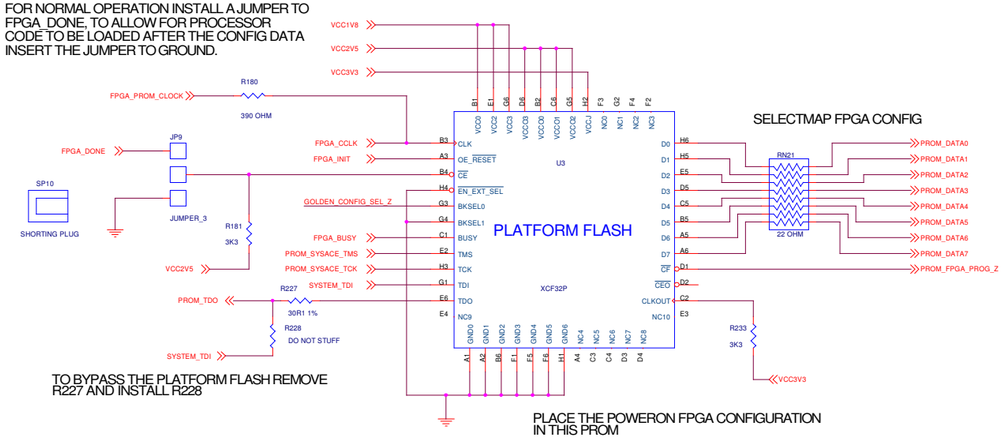
THE PLATFORM USB CABLE DETAILS HAVE BEEN REMOVED FROM THIS SCHEMATIC BECAUSE IT IS XILINX CONFIDENTIAL

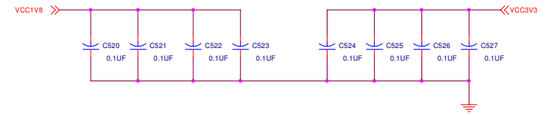


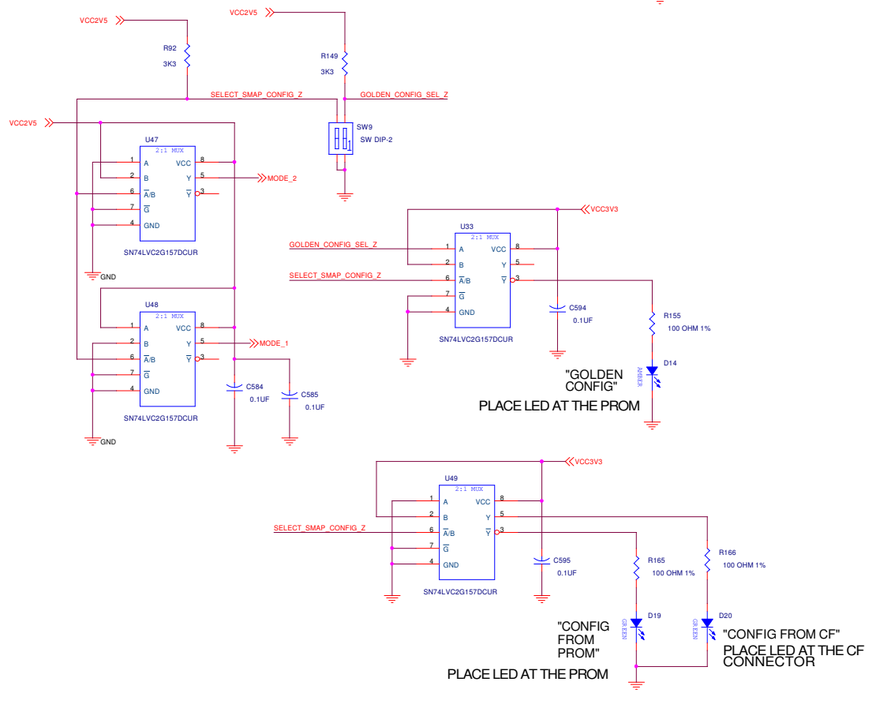




FOR NORMAL OPERATION INSTALL A JUMPER TO FPGA_DONE, TO ALLOW FOR PROCESSOR CODE TO BE LOADED AFTER THE CONFIG DATA INSERT THE JUMPER TO GROUND.







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Title: **USB CABLE EMULATION & PLATFORM FLASH**

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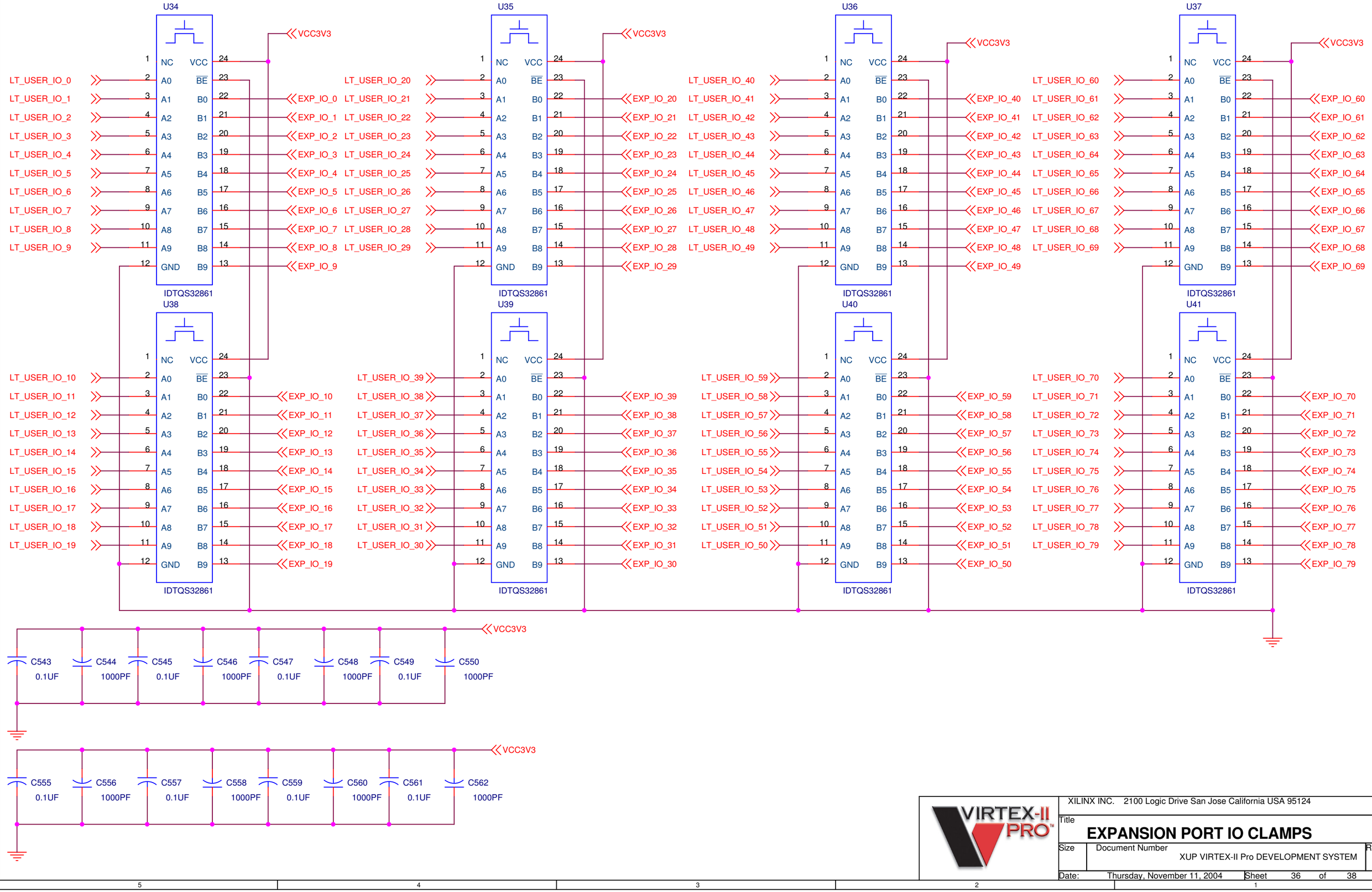

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Title

EXPANSION PORT IO CLAMPS

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	XUP VIRTEX-II Pro DEVELOPMENT SYSTEM	C
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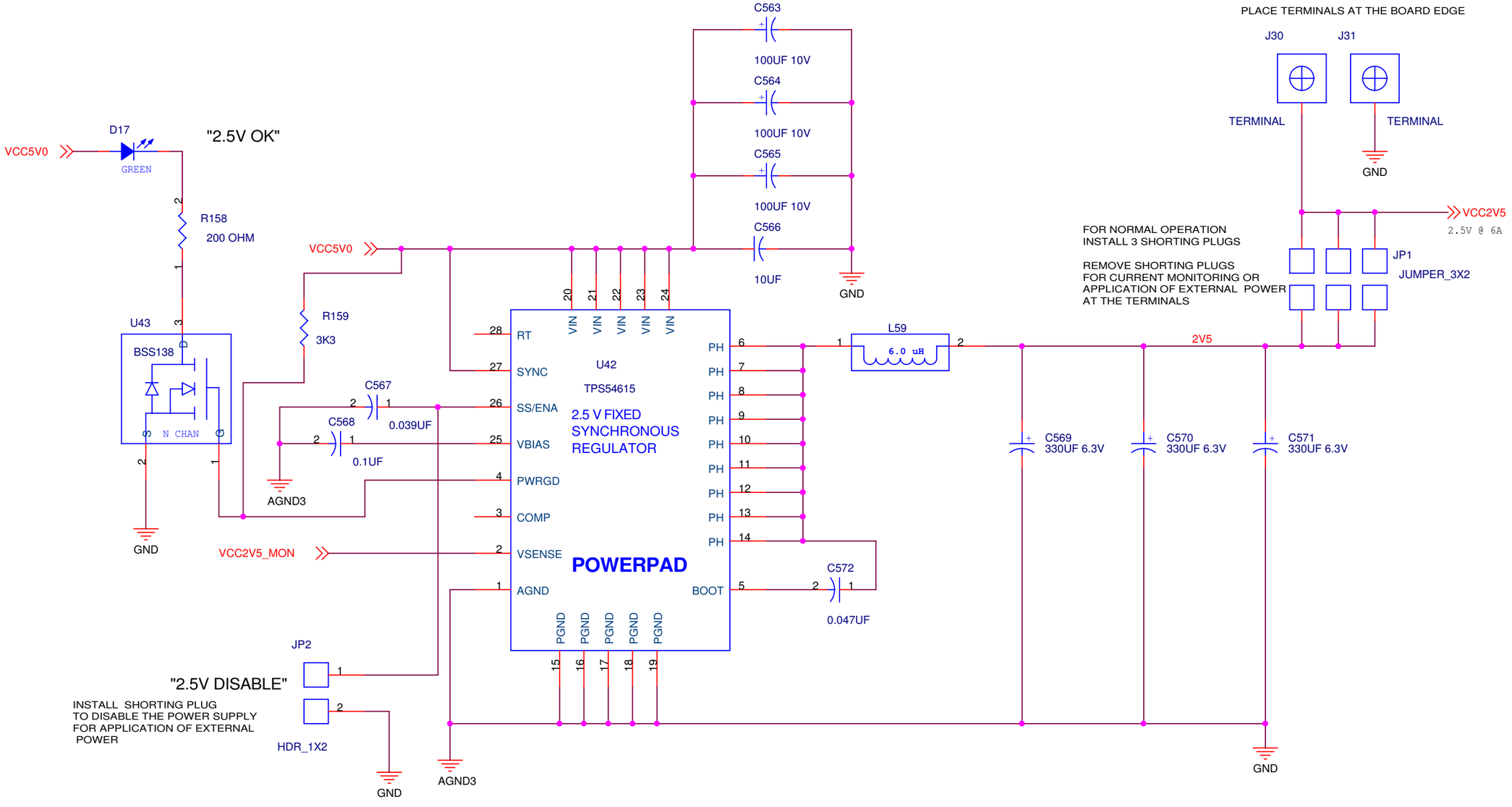
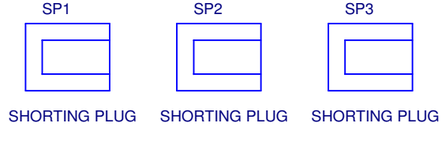


THE POWERPAD IS TIED TO AGND
FOLLOW THE LAYOUT GUIDELINES IN THE DATA SHEET
CONNECT AGND3 TO GND AT PIN 1
PROVIDE A COPPER HEATSINK OF AT LEASE 2 SQ
INCHES ON TOP AND BOTTOM LAYERS



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Title: **VCC2V5**

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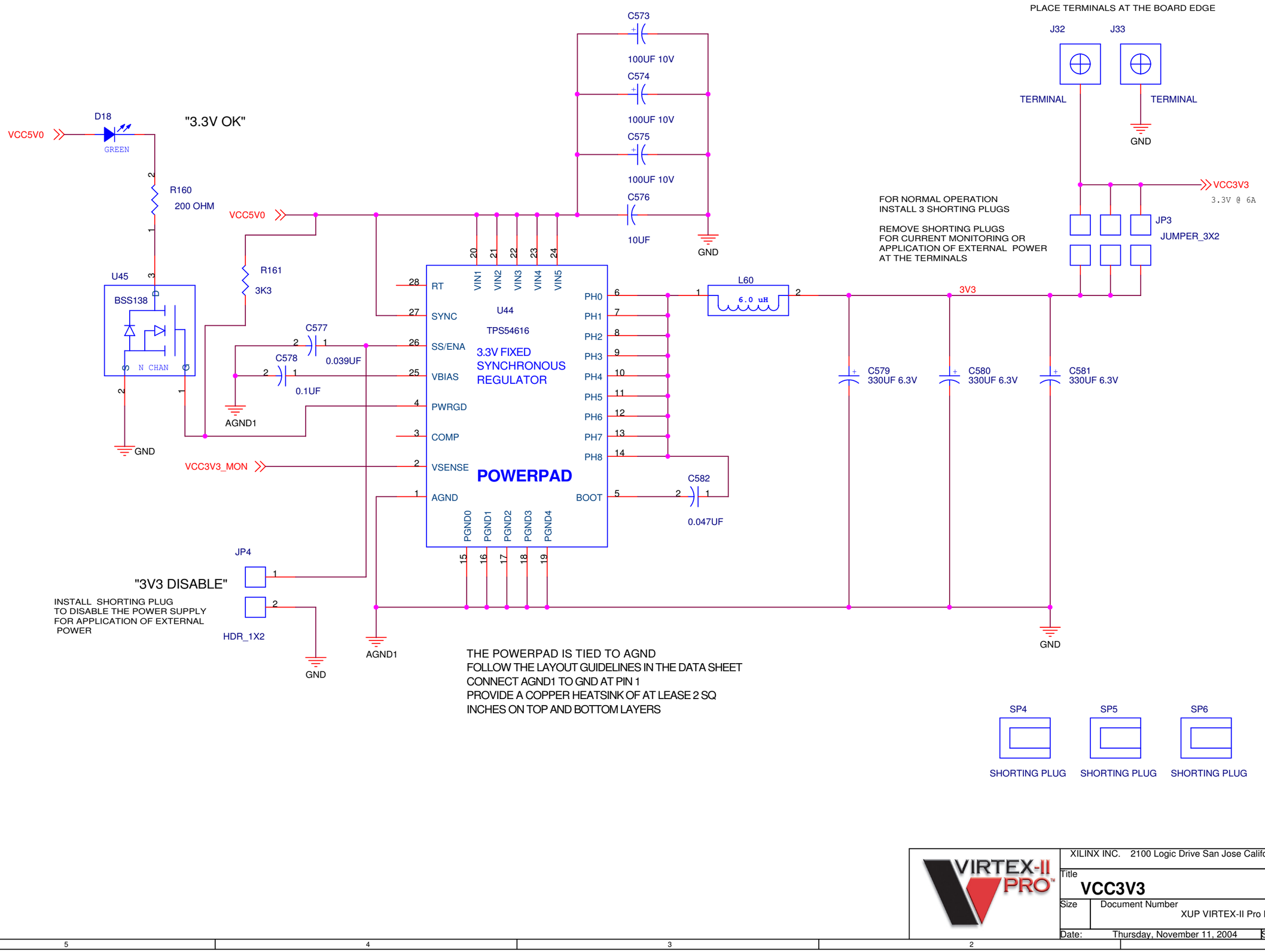

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Title: **VCC3V3**

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