1. Features

Category	Parameter	Value
LoRa®	Transceiver	Semtech SX1262 Long Range Low Power LoRa® Transceiver +22dBm, global frequency coverage
	Frequency	Europe: 863 – 870 MHz US: 902 – 928 MHz
	Maximum Transmit Power	21.7 dBm
	Receiver Sensitivity	-147.6 dBm (BW=10.4kHz, SF=12)
Bluetooth® Low Energy	Specification	Bluetooth 5 low-energy
	Frequency	2.402 – 2.480 GHz
	Maximum Transmit Power	2 dBm
	Receiver Sensitivity	-95 dBm
Host Processor	Architecture	Ambiq Apollo3 ARM® Cortex® M4 with FPU Up to 96MHz
	Memory	Flash: 1 MB on-chip with external flash support RAM: 384 kB
	Interfaces	50x GPIO 1x Dual/Quad/Octal SPI master 6x SPI/I2C master 1x SPI/I2C slave 1x I2C slave 2x UART with flow control 1x PDM Master 1x I2S slave
	Security	ISO 7816 secure interface Secure Key Storage Secure Boot Secure OTA External Flash Inline Encryption/Decryption
	Peripherals	15-Channel 14-bit ADC at 1.2MS/s Voltage Comparator Temperature Sensor
Power	Supply Voltage	2.8 – 3.6V
	Current Consumption	Processor 6uA / MHz BT Tx 0 dBm: 3mA, Rx: 3 mA LoRa Tx 22 dBm: 143 mA, LoRa Rx 125 kHz: 8.8 mA Sleep: 5uA in deep sleep mode 2, RAM retention, and RF section OFF
Environmental	Operating Temperature	-40° to 85°C
Physical	Dimensions	LGA 81 pads 12.8 mm x 12.8 mm x 2.4 mm

2. Contents

3. List of Figures

4. List of Tables

5. Pin Definition

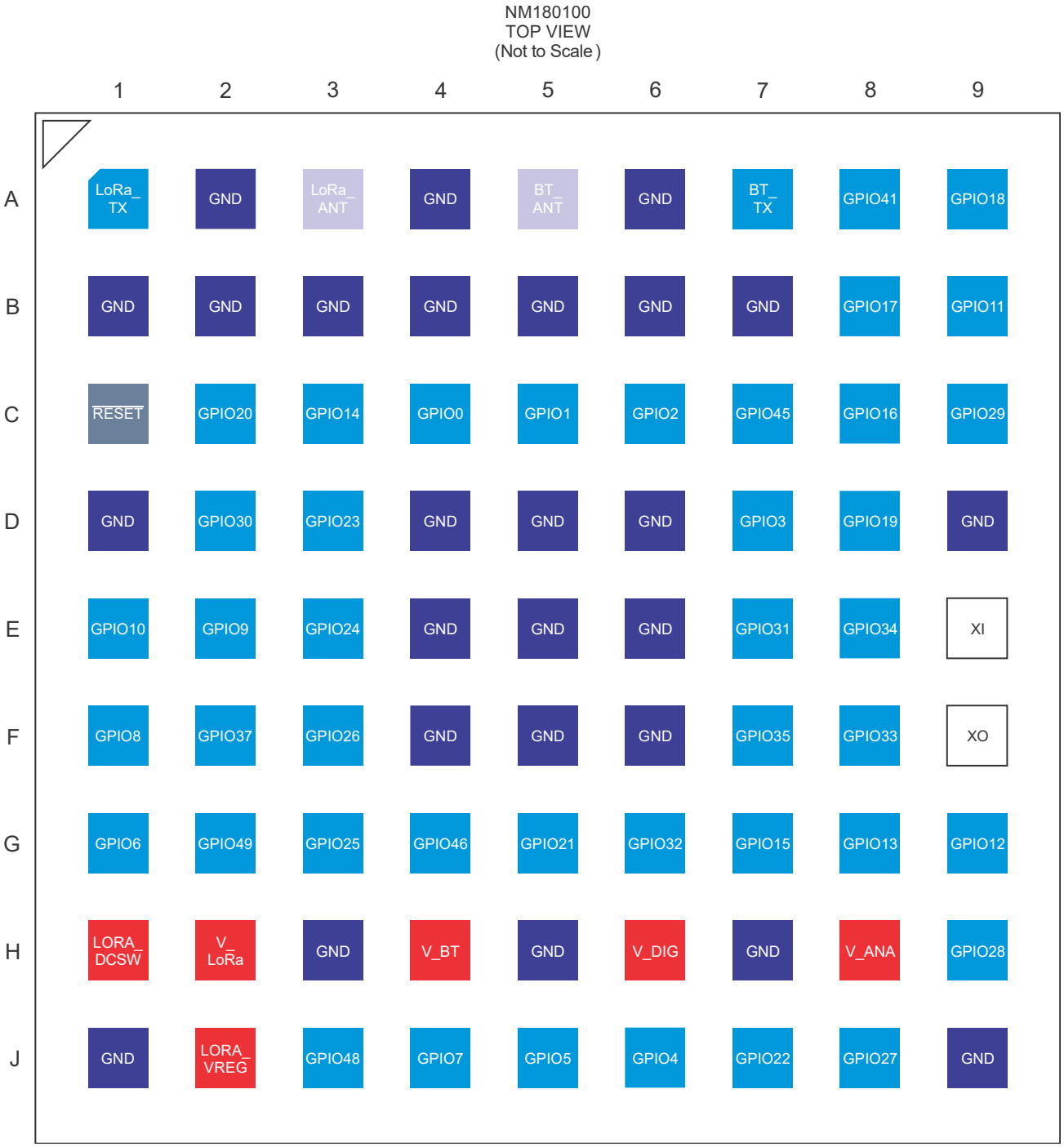

Figure 1 Pin Diagram

Table 1 NM180100 Pin definitions.

Pin Number	Type	Name	Description
A2, A4, A6, B1, B2, B3, B4, B5, B6, B7, D1, D4, D5, D6, D9, E4, E5, E6, F4, F5, F6, H3, H5, H7, J1, J9	Power	GND	Ground.
H6	Power	V_DIG	Supply input for the Apollo3 digital section.
H8	Power	V_ANA	Supply input for the Apollo3 analog section.
H4	Power	V_BT	Supply input for the Apollo3 BT section.
H2	Power	V_LoRa	Supply input for the LoRa transceiver.
C1	I	$\overline{\text{RESET}}$	Apollo3 active low chip reset.
E9	I	XI	
F9	O	XO	
A3	RF	LoRa_ANT	LoRa antenna connection.
A1	O	LoRa_TX	LoRa transmit indicator.
A5	RF	BT_ANT	Bluetooth antenna connection.
A7	O	BT_TX	Bluetooth transmit indicator.
A8, A9 B8, B9 C2, C3, C4, C5, C6, C7, C8, C9 D2, D3, D7, D8 E1, E2, E3, E7, E8 F1, F2, F3, F7, F8 G1, G2, G3, G4, G5, G6, G7, G8, G9 H9 J3, J4, J5, J6, J7, J8	I/O	GPIO0 to GPIO49	General purpose inputs and outputs.
H1	Power	LORA_DCSW	SX1262 DC/DC switcher output
J2	Power	LORA_VREG	SX1262 regulated output voltage from the internal regulator

6. Electrical Characteristics

Table 2 Absolute maximum ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_DIG	Supply input for the digital section			3.63	V
V_ANA	Supply input for the analog section			3.63	V
V_BT	Supply input for the BLE section			3.63	V
V_LoRa	Supply input for the LoRa section			3.9	V
T_S	Storage Temperature		-55	125	°C
T_OP	Operating Temperature		-40	85	°C
ESD_LU	Latch-up	JEDEC standard JESD78 B, Class I Level A		100	mA
ESD_HBM	ESD Human Body Model	ANSI/ESDA/JEDEC Standard JS-001-2014 Class 2		2.0	kV
ESD_CDM	ESD Charged Device Model	JEDEC Standard JESD22-C101D, Class 3		250	V
T_REFLOW	Reflow temperature	Reflow Profile per JEDEC J-STD-020D.1		260	°C

Table 3 Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_DIG	Supply input for the digital section		1.8	3.3	3.6	V
V_ANA	Supply input for the analog section		1.8	3.3	3.6	V
V_BT	Supply input for the BLE section		1.8	3.3	3.6	V
V_LoRa	Supply input for the LoRa section		1.8		3.6	V
f_XTAL	Low frequency external crystal			32.768		kHz
T_A	Ambient operating temperature		-40	-	85	°C

6.1. RF Performance Characteristics

6.1.1. Bluetooth RF Characteristics

Table 4 Bluetooth transmitter characteristics.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BT_P_{OUT}_MAX	Maximum transmit power		1.7	2	2.5	dBm
BT_P_{OUT}_MIN	Minimum active transmit power	CW	-11	-	-	dBm
BT_P_{OUT}_STEP	Output power step size		-	1	-	dB
BT_P_{OUT}_VAR_V	Output power variation vs supply at BT_POUT_MAX		-	TBD	-	dB
BT_P_{OUT}_VAR_T	Output power variation vs temperature at BT_POUT_MAX		-	TBD	-	dB
BT_P_{OUT}_VAR_F	Output power variation vs RF frequency at BT_POUT_MAX		-0.5	-	0.5	dB
	Second harmonic			-40	-30	dBm
	Third harmonic			-40	-30	dBm
BT_F_RANGE	RF tuning frequency range		2400	-	2483.5	MHz

Table 5 Bluetooth receiver characteristics.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BT_SAT	Max usable receiver input level at 0.1% BER		-	0	-	dBm
BT_SENS	30.8% Packet Error Rate		-92	-93	-94	dBm
BT_C/I_CC	Signal to co-channel interferer, 0.1% BER		-	7	-	dB
BT_BLOCK_OOB	Blocking, 0.1% BER, Desired is reference signal at -67 dBm. Interferer is CW in OOB range.	30 MHz to 2000 MHz	-	-5	-	dBm
		2003 MHz to 2399 MHz		-15		dBm
		2484 MHz to 2997 MHz		-15		dBm
		3000 MHz to 12.75 GHz		-5		dBm
BT_RSSI_MAX	Upper limit of input power range over which RSSI resolution is maintained		-	-	0	dBm
BT_RSSI_MIN	Lower limit of input power range over which RSSI resolution is maintained		-94	-	-	dBm
BT_RSSI_RES	RSSI resolution			1		dB

6.1.2. LoRa RF Characteristics

Table 6 LoRa transmitter characteristics.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
LORA_POUT_MAX	Maximum transmit power	matching and RF switch loss included	21.0	-	21.7	dBm
LORA_POUT_MIN	Minimum active transmit power	CW	-9	-	-	dBm
LORA _POUT_STEP	Output power step size		-	1	-	dB
LORA _POUT_VAR_V	Output power variation vs supply at LORA_POUT_MAX		-	0.5	-	dB
LORA _POUT_VAR_T	Output power variation vs temperature at LORA_POUT_MAX		-	1	-	dB
LORA _POUT_VAR_F	Output power variation vs RF frequency at LORA_POUT_MAX		-0.5	-	0.5	dB
LORA_SPUR_HRM	Second harmonics	CW at 864.1 MHz, 22 dBm	-	-35	-30	dBm
		CW at 868.5 MHz, 22 dBm	-	-35	-30	dBm
		CW at 902.3 MHz, 22 dBm	-	-35	-30	dBm
		CW at 914.9 MHz, 22 dBm	-	-35	-30	dBm
		CW at 927.5 MHz, 22 dBm	-	-35	-30	dBm
	Third harmonics	CW at 864.1 MHz, 22 dBm	-	-35	-30	dBm
		CW at 868.5 MHz, 22 dBm	-	-35	-30	dBm
		CW at 902.3 MHz, 22 dBm	-	-35	-30	dBm
		CW at 914.9 MHz, 22 dBm	-	-35	-30	dBm
		CW at 927.5 MHz, 22 dBm	-	-35	-30	dBm
LORA _F_RANGE	RF tuning frequency range		830	-	930	MHz

Table 7 LoRa receiver characteristics.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
LORA_SAT	Max usable receiver input level		-	10	-	dBm
LORA _RSSI_MAX	Upper limit of input power range over which RSSI resolution is maintained		-		0	dBm
LORA _RSSI_MIN	Lower limit of input power range over which RSSI resolution is maintained	10.4 kHz bandwidth and spreading factor of 12	-148		-	dBm
LORA _RSSI_RES	RSSI resolution			0.5		dB

6.2. Current Consumption

6.2.1. LoRa Radio Current Consumption at 3.3V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
LORA_I_TX	Current consumption in transmit mode, continuous carrier wave at 914.9 MHz	0 dBm		41		mA
		5 dBm		55		mA
		10 dBm		73		mA
		15 dBm		98		mA
		22 dBm		143		mA

6.2.2. BLE Radio Current Consumption at 3.3V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BLE_I_TX	Current consumption in transmit mode, continuous carrier wave at 2.44 GHz	0 dBm programmed		7		mA
		3 dBm programmed		8		mA
		4 dBm programmed		9		mA

7. Functional Description

7.1. Introduction

The NM180100 is a highly integrated LoRa module with an Ambiq Apollo3 microcontroller and a Semtech SX1262 LoRa transceiver supporting the 868MHz and 915MHz ISM bands. Bluetooth 5 Low Energy is integrated with the Apollo3 microcontroller. The Apollo 3 possesses a secure interface (ISO 7816) including secure boot and secure OTA firmware upgrade over Bluetooth. The operating system, radio drivers and wireless communication protocol stacks are provided in the form of source code. This enables the system integrator to fully leverage the module's existing regulatory grants (such as IC or FCC) where applicable. Full programmability allows the module to function as a host while maintaining all RF, mixed-signals, and digital functions in a single device without the need for additional microcontrollers.

7.2. Block Diagram

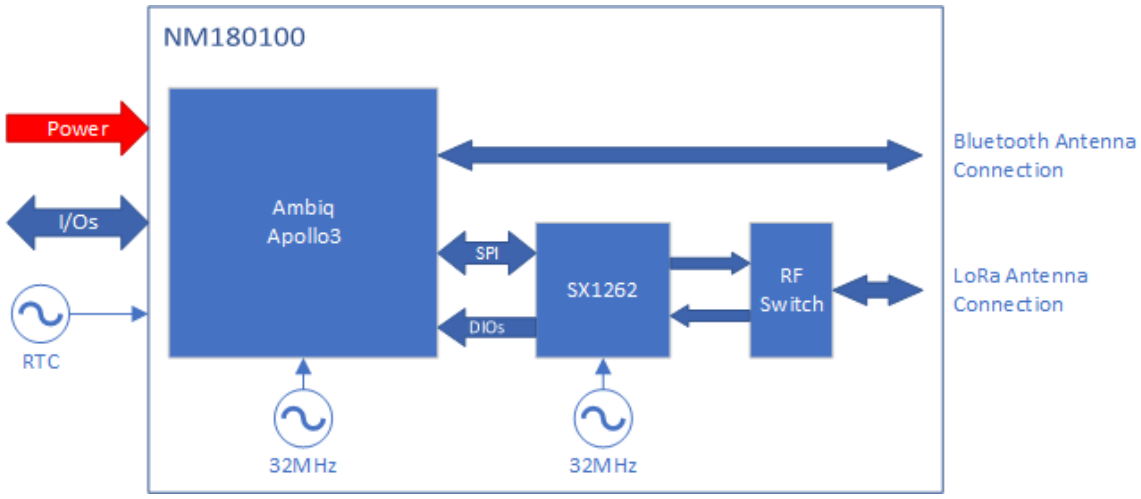

Figure 2 NM180100 block diagram.

7.3. LoRa Radio

The NM180100 utilizes the Semtech SX1262 transceiver for LoRa communications with a maximum output power of 22dBm. An 32MHz crystal is integrated as the frequency reference for the SX1262 radio and also serve as the main clock source for the baseband controller. The SX1262 interfaces with the Apollo 3 as an SPI slave and communicate through IOM module 3 in SPI mode [1]. The DIO pins of the SX1262 [2] are connected to the Apollo 3 as interruptible GPIO lines. The interface pins assignment between Apollo 3 and SX1262 are shown in Table 8.

The LoRa RF front end consists of a transmit and a receive path. Transmit and receive selection of the RF switch is controlled by the SX1262 through the DIO2 pin. The DIO2 signal is exposed externally to the module in order to facilitate system integration of multi-radios applications where transmit co-existence is a requirement.

An impedance transforming filter is connected to the SX1262 transmitter output. The filter is conjugately matched to the maximum output power impedance of the power amplifier. It serves to provide optimal power transfer to the antenna and reduction in higher harmonics in order to meet regulatory emission requirements.

A lattice-type balun circuit is connected between the RF switch and the SX1262 receiver. The circuit provides transformation from a single-ended mode signal into a differential mode that is required by the SX1262 receiver. The balun circuit also provides optimal noise figure matching of the LNA input in order to maximize the receiver sensitivity performance.

Table 8 Apollo 3 and SX1262 interface pin assignments.

Apollo 3		SX1262		
Pin Number	Name	Pin Number	Name	Description
H6	GPIO 36	19	NSS	SPI slave select
J6	GPIO 38	17	MOSI	SPI slave input
J5	GPIO 43	16	MISO	SPI slave output
H5	GPIO 42	18	SCK	SPI clock input
J8	GPIO 39	14	BUSY	Radio busy indicator
J9	GPIO 40	13	DIO1	Multipurpose digital I/O
H9	GPIO 47	6	DIO3	Multipurpose digital I/O
J7	GPIO 44	15	NRESET	Radio reset signal, active low

7.4. Bluetooth Low Energy Radio

The NM180100 module includes a Bluetooth low energy radio that is integrated into the Apollo 3 MCU. The BLE controller supports up to eight simultaneous connections. The BLE presents to the host as a Host Controller Interface. It also supports extended PDU length and enhanced security.

7.5. Low Frequency Clock Input

The NM180100 provides an optional low frequency real-time clock connection for the Apollo3 processor. The RTC clock source must be an external 32.768kHz crystal having a maximum loading capacitance of 7pF.

7.6. Power Supply Sequence

There are a total four supply rails to the NM180100 module. In the optimal power-up sequence, V_DIG and V_ANA power up first and together. V_BT can be power up simultaneously with V_DIG and V_ANA or later. Finally, the LoRa power rail V_LoRa can come up last. Note that no device damage occurs if this sequence is not followed. However, failure to follow this sequence may result in higher than expected power-up currents. If BLE is not used, V_BT can be power down without impact to other functionalities.

The power-down sequence is not critical. If a power-down sequence is followed, remove the V_LoRa supply first to avoid indeterminant output states of the digital control lines from the Apollo3.

In the event that the system enters a long period of inactivity, the LoRa and BLE sections can be independently shutdown by removing the V_LoRa and V_BT supply for further power savings.

7.7. Debugging, Real-time Tracing, and System Analysis

The NM180100 combines multiple different technologies available on the Apollo 3 to enable real-time tracing and system analysis including: Serial Wire Debug, Serial Wire Output, Instrumentation Trace Macrocell, and Serial Wire Viewer.

7.7.1. Serial Wire Debug

Serial Wire Debug (SWD) port consists of a clock and a bi-directional data pin that offers target debugging and low bandwidth trace connectivity. SWD uses an ARM standard bi-directional wire protocol [3] to pass data to and from the debugger and the target system. While the SWD provides real-time access to the system memory without halting the processor, it does not provide real-time tracing.

7.7.2. Serial Wire Output

The Serial Wire Output (SWO) is a trace data drain with no formatter and no pattern generator. It is meant to be used as a part of the Serial Wire Viewer to enable real-time tracing.

7.7.3. Instrumentation Trace Macrocell

The Instrumentation Trace Macrocell (ITM) is a software application driven trace source. The main uses for this block are to provide:

- printf style debugging
- OS and application events tracing
- system diagnostic information

7.7.4. Serial Wire Viewer

Serial Wire Viewer (SWV) is a real-time tracing technology that uses the SWD port and the SWO pin. SWV provides advanced system analysis and real-time tracing without the need to halt the processor to extract certain types of debug information. With debuggers supporting SWV, the following types of information can be retrieved:

- Periodic samples of the program counter value
- Event notification on memory accesses (such as reading or writing of a variable)
- Event notification on exception entry and exit
- Event counters
- Timestamp and CPU cycle information

7.7.5. Debug Port Pin Configuration

On power up, the clock (SWDCK) and data signals (SWDIO) of the SWD port must be connected to GPIO 20 and GPIO 21 respectively. Alternatively, GPIO 14 and 15 can be used for SWDCK or SWDIO respectively. However, these pins are not selected by default. Table 9 shows the REG_GPIO_PADREG fields and values for the SWD port pin configuration.

Table 9 Debug port pin configuration options.

Function	Pin Number	Pin Name	Register Field	Value
SWDCK (default)	C2	GPIO 20	PAD20FNCSEL	0
			PAD20INPEN	1
			PAD20PULL	1
SWDIO (default)	G5	GPIO 21	PAD21FNCSEL	0
			PAD21INPEN	1
			PAD21PULL	1
SWDCK (alternative)	C3	GPIO 14	PAD14FNCSEL	6
			PAD14INPEN	1
			PAD14PULL	1
SWDIO (alternative)	G7	GPIO 15	PAD15FNCSEL	6
			PAD15INPEN	1
			PAD15PULL	1

The optional SWO pin may be configured on a variety of pin as shown in Table 10. The default SWO pin assigned by the boot loader is GPIO 46. However, this can be re-configured dynamically at runtime after the Apollo 3 is booted into the application code.

Table 10 SWO pin configuration options.

Pin Number	Pin Name	Register Field	Value
G7	GPIO 15	PAD15FNCSEL	7
J7	GPIO 22	PAD22FNCSEL	7
E3	GPIO 24	PAD24FNCSEL	7
F8	GPIO 33	PAD33FNCSEL	7
A8	GPIO 41	PAD41FNCSEL	7
C7	GPIO 45	PAD45FNCSEL	7
G4	GPIO 46	PAD46FNCSEL	7

8. Package Information

8.1. Mechanical Specifications

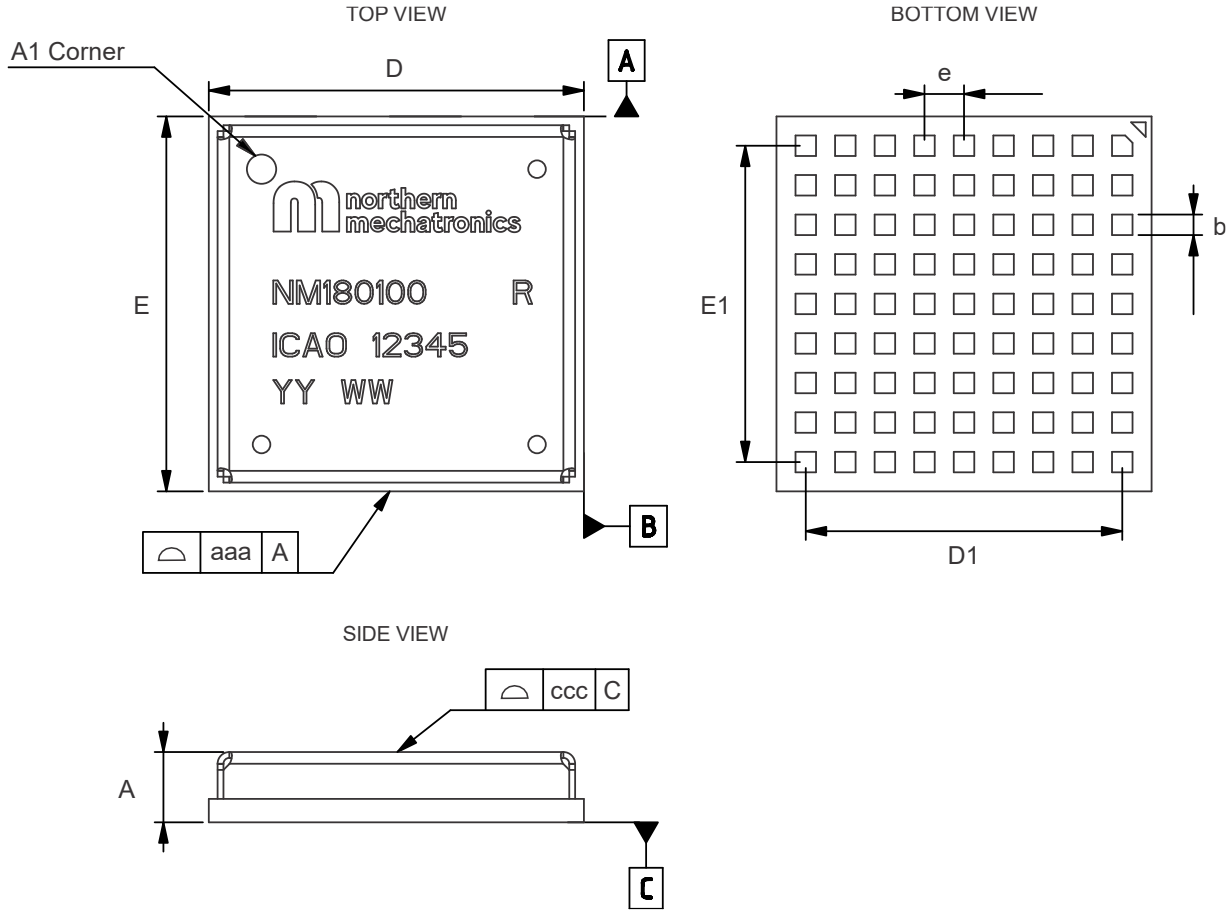

Figure 3 LGA 81 pad, 12.8mm x 12.8mm package outline.

Table 11 LGA 81 pad, 12.8mm x 12.8mm, 1.35mm pitch, package mechanical data.

Symbol	millimeters		
	Min	Typ	Max
A	2.3	2.4	2.5
b	-	0.7	-
D	12.6	12.8	13.0
D1	10.7	10.8	10.9
E	12.6	12.8	13.0
E1	10.7	10.8	10.9
e	-	1.35	-
aaa	-	0.08	-
ccc	-	0.08	-

8.2. Recommended Footprint

A non-solder mask defined (NSMD) land pattern is recommended as shown in Figure 4. NSMD pads have a solder mask opening that is larger than the pad and thereby allowing a tighter control of the copper artwork registration compared to the positional tolerance of the solder masking process. Furthermore, NSMD pad definition introduces less stress concentration points in solder joints that may otherwise crack under extreme fatigue conditions.

NSMD pads require a clearance between the copper pad and the solder mask to avoid overlapping between the solder joint and the solder mask. The clearance amount (typically 3 mils) is dependent on the solder mask registration tolerances and may vary from one PCB vendor to another.

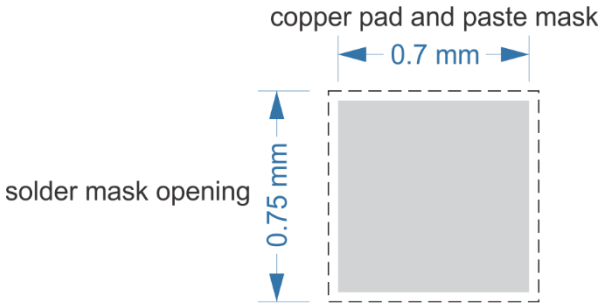

Figure 4 NSMD land pattern recommendation.

8.3. Device Marking

Figure 5 provides an example of the topside marking with respect to the A1 position identifier. Other markings, which are depend on supply chain operations, will vary from device to device.

Parts that are marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and are therefore not approved for use in production. Northern Mechatronics is not responsible for any consequences resulting from such use. In no event will Northern Mechatronics be liable for customers using any of these engineering samples in production.

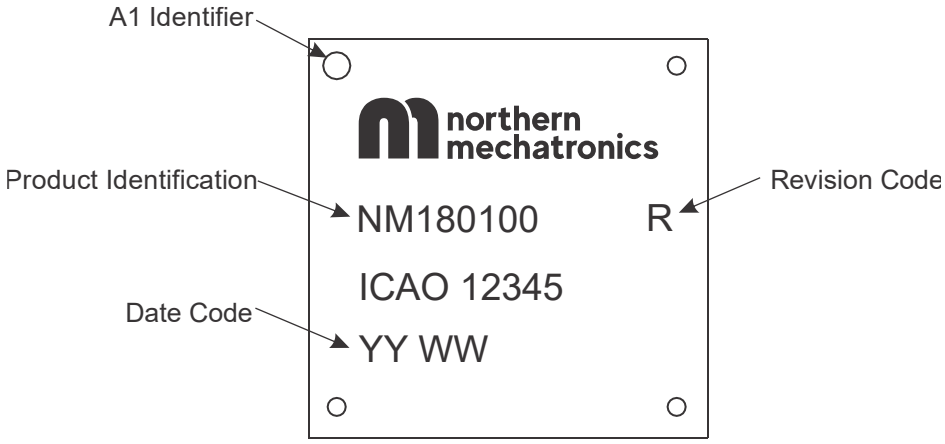

Figure 5 LGA81 marking example (package top view).

9. Packaging Specifications

9.1. Reel Specifications

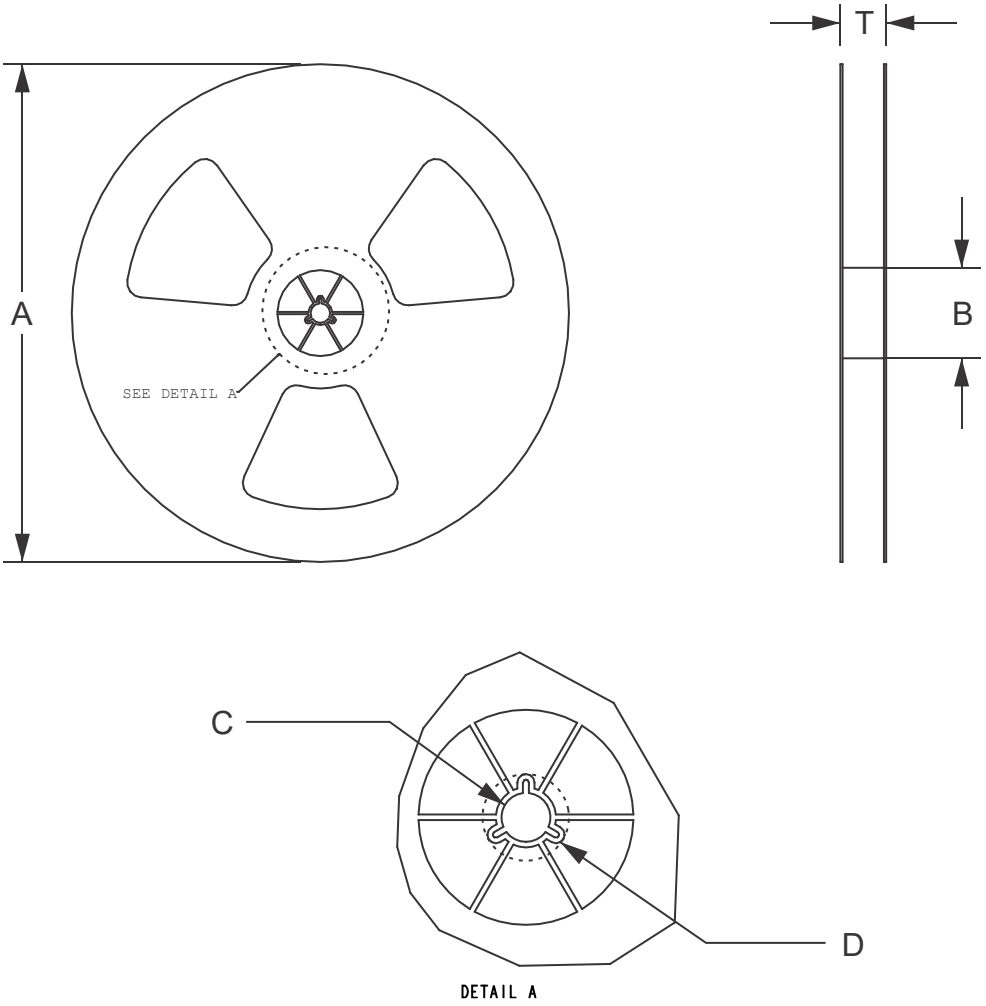

Figure 6 Reel specifications.

Reel Diameter	Tape Size	A	B	C	D	T
330	24 mm	330 mm	50 mm	13 mm	20 mm	30.4 mm

9.2. Embossed Tape Specifications

The carrier tape conforms to the ANSI/EIA-481-D standard for automatic handling of surface mount components.

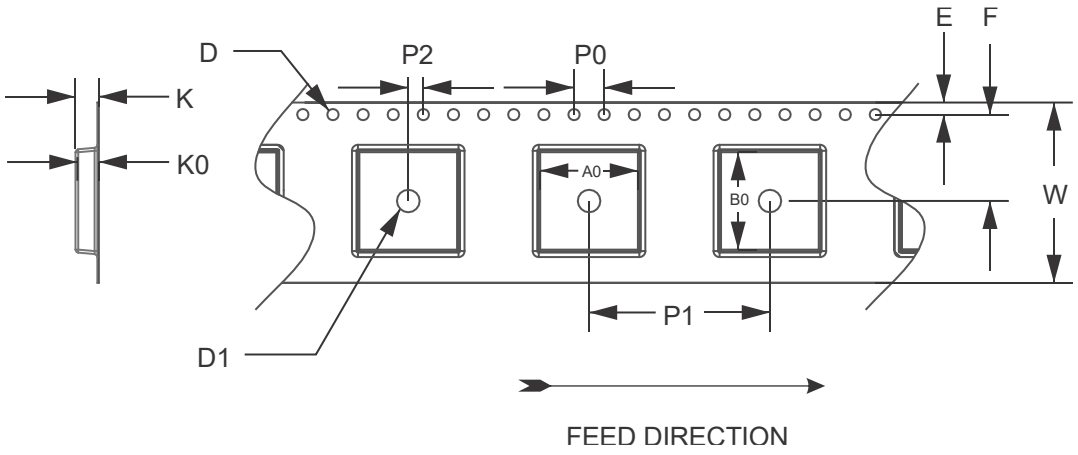

Figure 7 Tape specifications.

Tape Size (W)	D	D1	E	F	P0	P1	P2
24 mm	1.5 mm	3 mm	1.75 mm	11.5 mm	4.0 mm	24 mm	2.0 mm

9.3. Tape Ends for Finished Goods

The trailer is a minimum of 160 mm in length and it consists of empty cavities with sealed cover tape. The leader is a minimum of 400 mm in length and it consists of empty cavities with sealed cover tape.

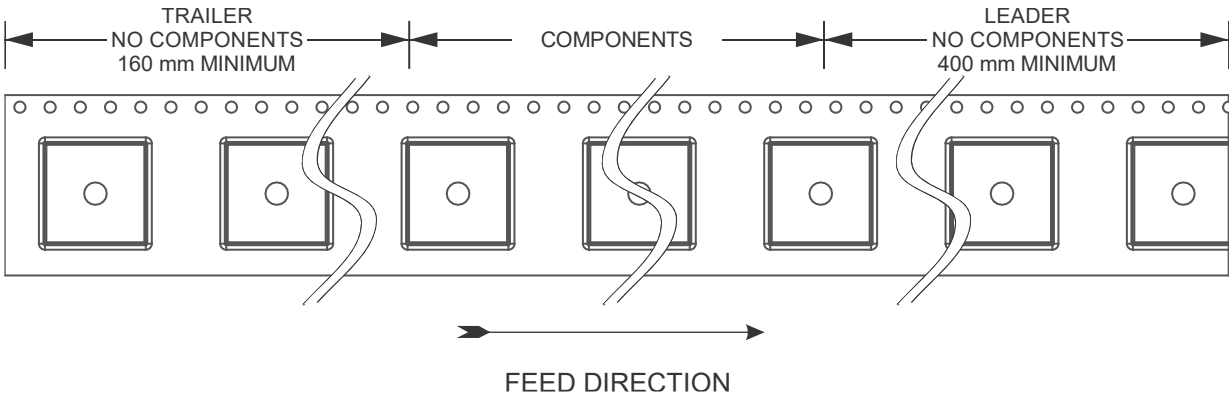

Figure 8 Tape ends specifications.

9.4. Components Orientation

Pad A1 orientation is oriented towards the upper left corner with respect to the feed direction as illustrated below.

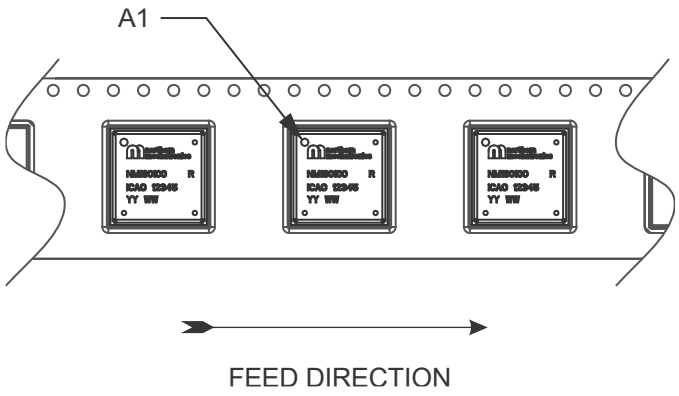

Figure 9 Component orientation.

10.Ordering Information

Model	Temperature Range	Package Description	Package Option
NM180100LTR	-40°C to +85°C	81 pad land grid array	Tape and Reel
NM180100EVB		Evaluation board, with NM180100 LoRa® and Bluetooth® 5 Low Energy Module	

11. References

[1] Ambiq Micro, Inc., "Apollo 3 Blue Datasheet," February 2019. [Online]. Available: https://ambiqmicro.com.

[2] Semtech Corporation, "SX1261-SX1262 Product Datasheet," December 2017. [Online]. Available: http://www.semtech.com.

[3] ARM Limited, "ARM Debug Interface Architecture Specification ADIv6.0," 9 March 2017. [Online]. Available: https://static.docs.arm.com/ihi0074/a/debug_interface_v6_0_architecture_specification_IHI0074A.pdf.

[4] EIA-481-D, *8 mm through 200 mm Embossed Carrier Taping and 8 mm & 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling,* 2008.

12. Revision History

Revision	Date	Description
A.1	November 4, 2019	Initial release.
A.2	October 10, 2020	Updated footprint land pattern specification

13. Document Details

Parameter	Value
Name	NM180100 Datasheet
Number	2000005
Revision	A.2
Life Cycle State	In Work