

# Memory FRAM

## 128K (16K × 8) Bit SPI

# MB85RS128TY

### ■ DESCRIPTION

MB85RS128TY is a FRAM (Ferroelectric Random Access Memory) chip in a configuration of 16,384 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells. This product is specifically targeted for high-temperature environment such as automotive applications.

MB85RS128TY adopts the Serial Peripheral Interface (SPI).

The MB85RS128TY is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85RS128TY can be used for  $10^{13}$  read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E<sup>2</sup>PROM.

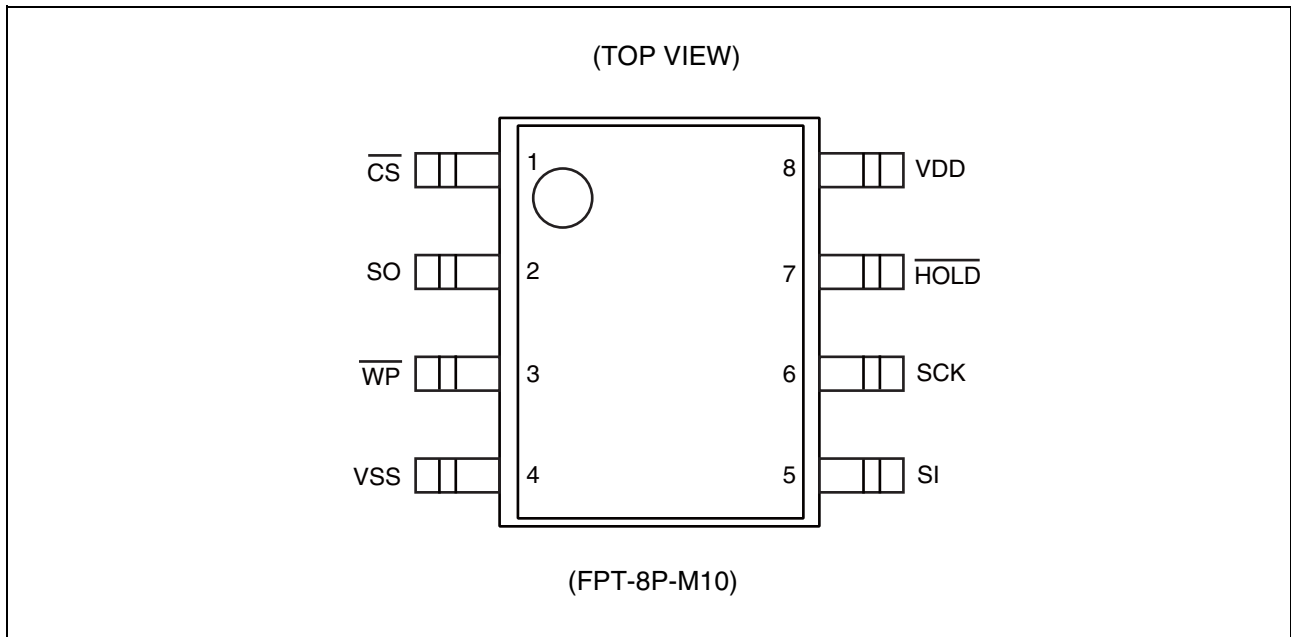
As MB85RS128TY does not need any waiting time in writing process, the write cycle time of MB85RS128TY is much shorter than that of Flash memories or E<sup>2</sup>PROM.

### ■ FEATURES

- Bit configuration : 16,384 words × 8 bits
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)  
Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 33 MHz (Max)
- High endurance :  $10^{13}$  times / byte
- Data retention : 10 years (+85 °C),  
1 year (+125 °C) or more  
Under evaluation for more than 1 year(+125 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low power consumption : Operating power supply current 2.3 mA (Max@33 MHz)  
Standby current 45 μA (Max)  
Sleep current 12 μA (Max)
- Operation ambient temperature range : - 40 °C to +125 °C
- Package : 8-pin plastic SOP (FPT-8P-M10)  
RoHS compliant

# MB85RS128TY

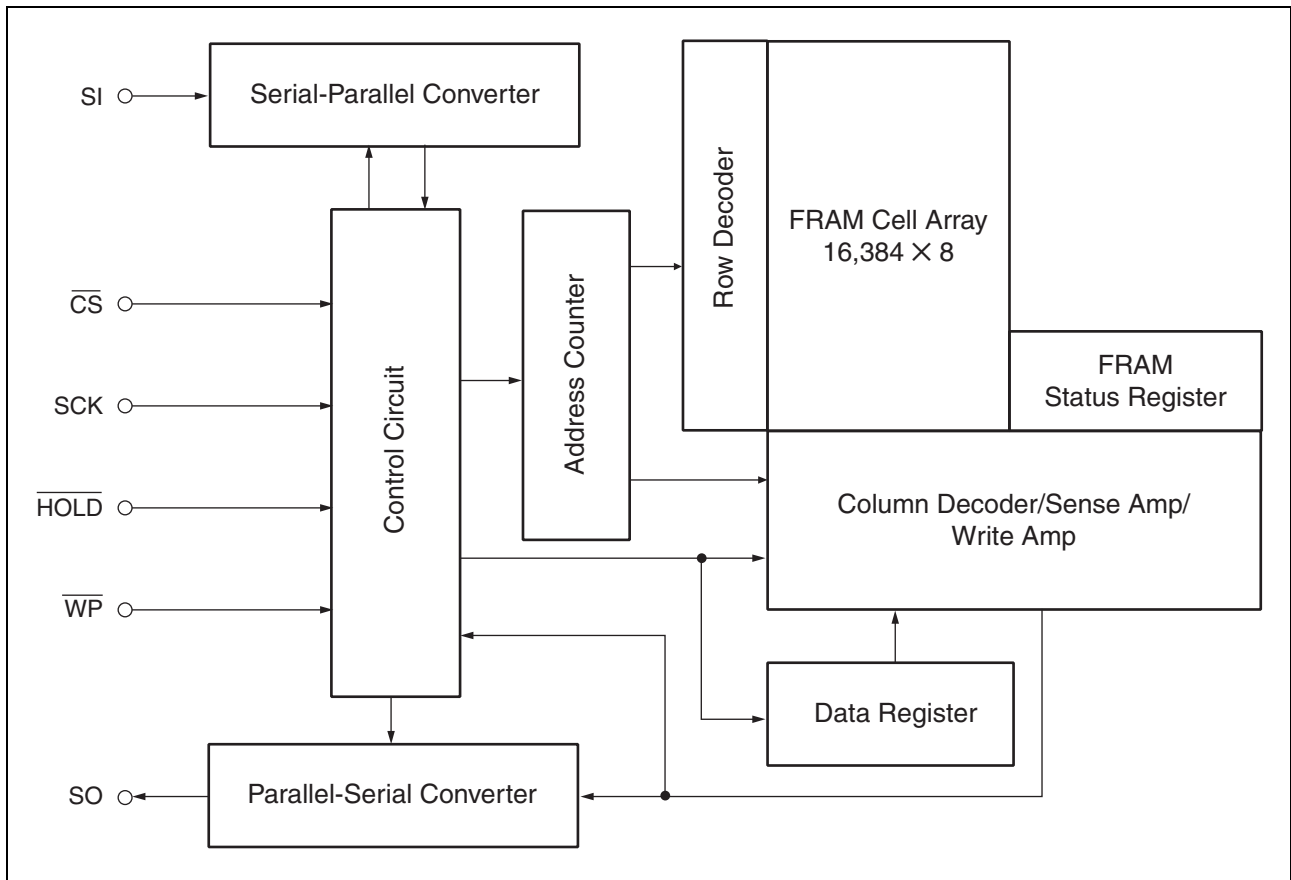
## ■ PIN ASSIGNMENT



## ■ PIN FUNCTIONAL DESCRIPTIONS

Pin No.	Pin Name	Functional description
1	$\overline{CS}$	Chip Select pin This is an input pin to make chips select. When $\overline{CS}$ is "H" level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{CS}$ is "L" level, device is in select (active) status. $\overline{CS}$ has to be "L" level before inputting op-code. The Chip Select pin is pulled up internally to the VDD pin.
3	$\overline{WP}$	Write Protect pin This is a pin to control writing to a status register. The writing of status register (see "■ STATUS REGISTER") is protected in related with $\overline{WP}$ and WPEN. See "■ WRITING PROTECT" for detail.
7	$\overline{HOLD}$	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When $\overline{HOLD}$ is "L" level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. While the hold operation, $\overline{CS}$ has to be retained "L" level.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin

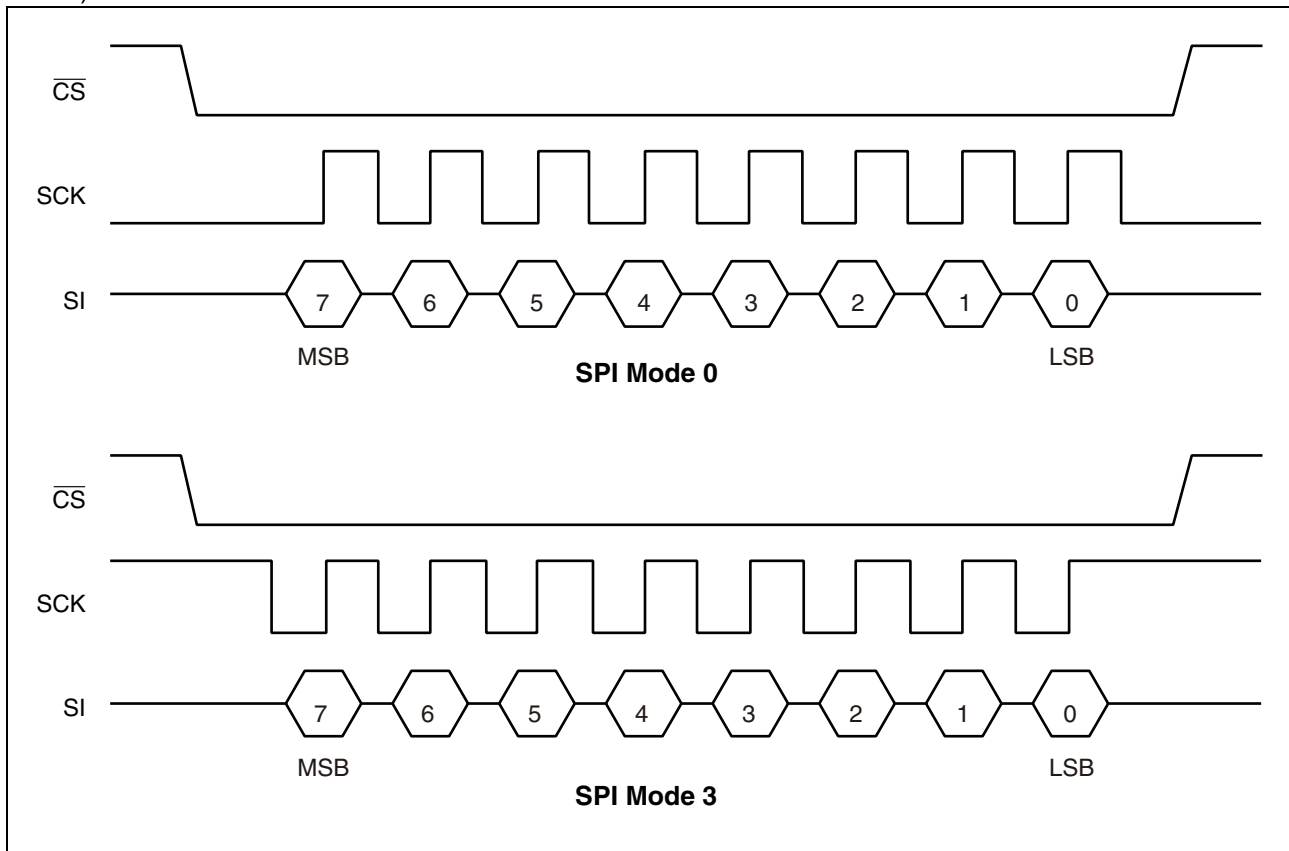
## ■ BLOCK DIAGRAM



# MB85RS128TY

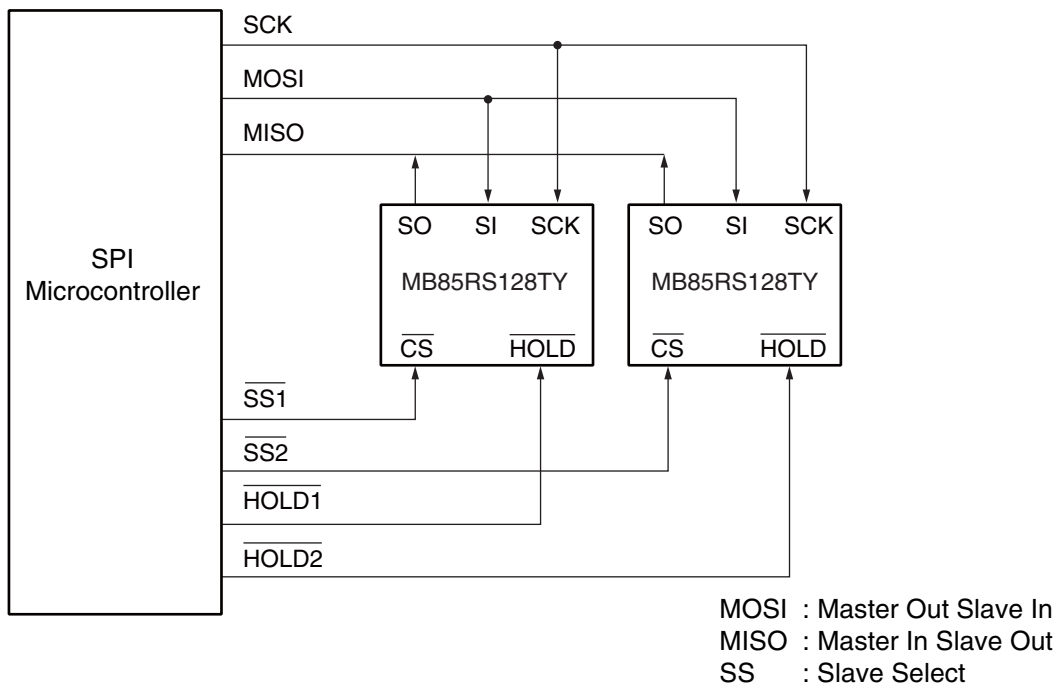
## ■ SPI MODE

MB85RS128TY corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0), and SPI mode 3 (CPOL = 1, CPHA = 1).

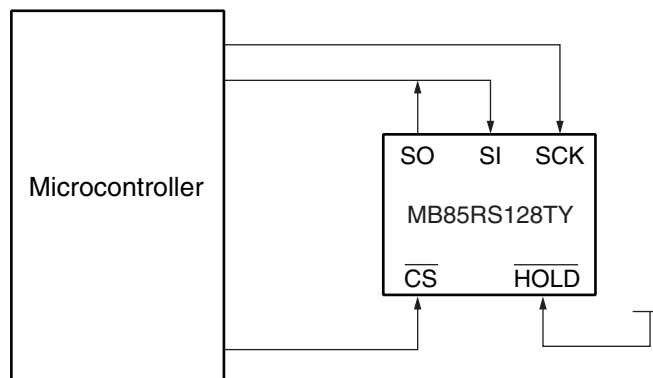


## ■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS128TY works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.



**System Configuration with SPI Port**



**System Configuration without SPI Port**

## ■ STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FRAM). WPEN protects writing to a status register (refer to "■ WRITING PROTECT") relating with $\overline{WP}$ input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to "■ BLOCK PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. After power ON. After WRDI command recognition. The following rising edges do not reset WEL. The rising edge of $\overline{CS}$ after WRSR command recognition. The rising edge of $\overline{CS}$ after WRITE command recognition.
0	0	This is a bit fixed to "0".

## ■ OP-CODE

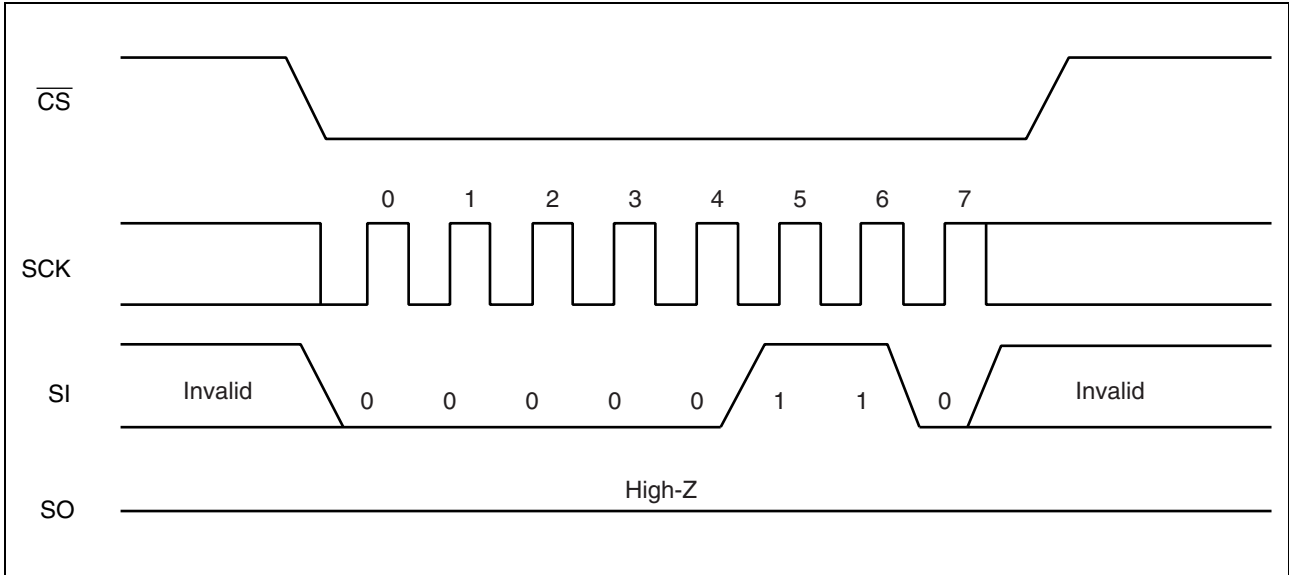
MB85RS128TY accepts 8 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If  $\overline{CS}$  is risen while inputting op-code, the command are not performed.

Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110 <sub>B</sub>
WRDI	Reset Write Enable Latch	0000 0100 <sub>B</sub>
RDSR	Read Status Register	0000 0101 <sub>B</sub>
WRSR	Write Status Register	0000 0001 <sub>B</sub>
READ	Read Memory Code	0000 0011 <sub>B</sub>
WRITE	Write Memory Code	0000 0010 <sub>B</sub>
RDID	Read Device ID	1001 1111 <sub>B</sub>
SLEEP	Sleep Mode	1011 1001 <sub>B</sub>

## ■ COMMAND

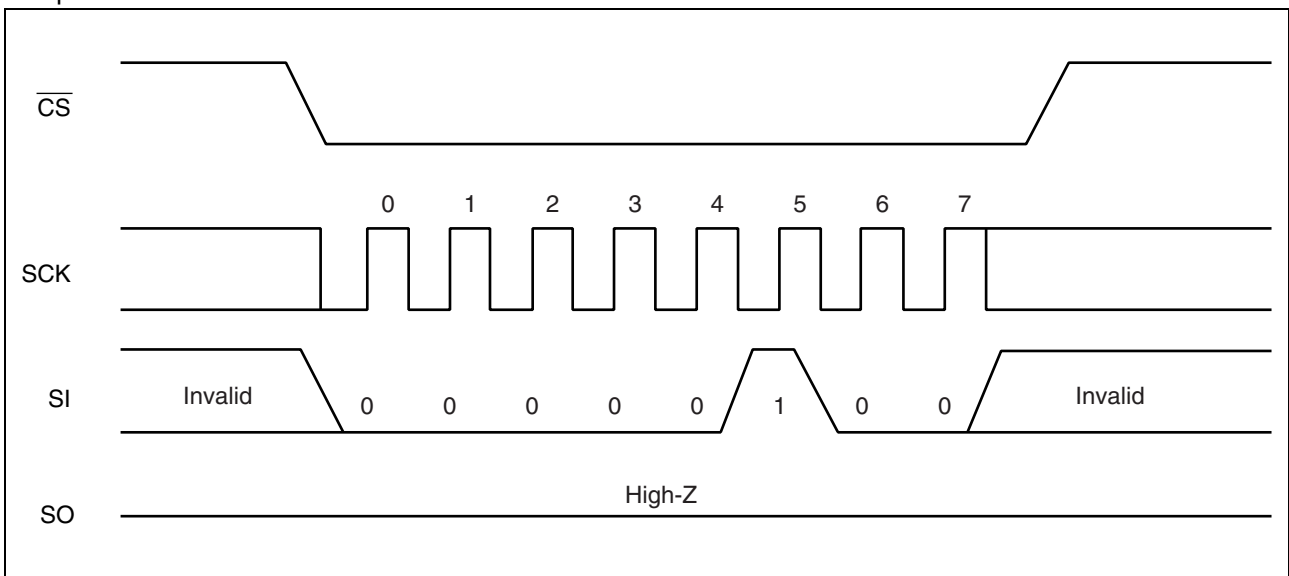
### • WREN

The WREN command sets WEL (Write Enable Latch) bit to 1. WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command). WREN command is applicable to "Up to 33 MHz operation".



### • WRDI

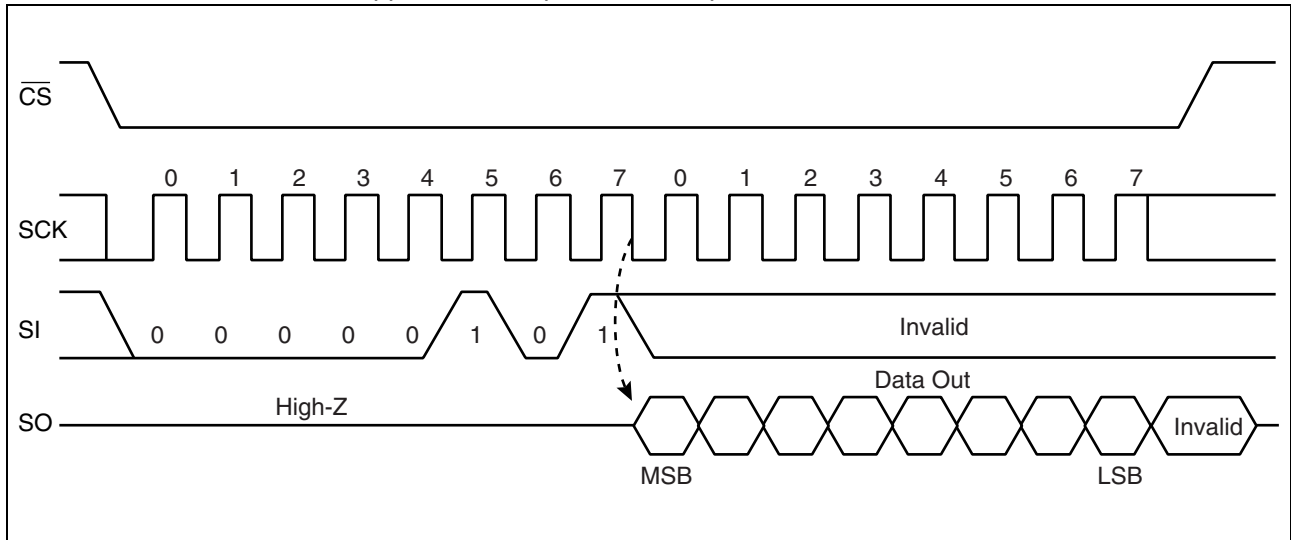
The WRDI command resets WEL (Write Enable Latch) bit to 0. Writing operation (WRSR command and WRITE command) are not performed when WEL is reset. WRDI command is applicable to "Up to 33 MHz operation".



# MB85RS128TY

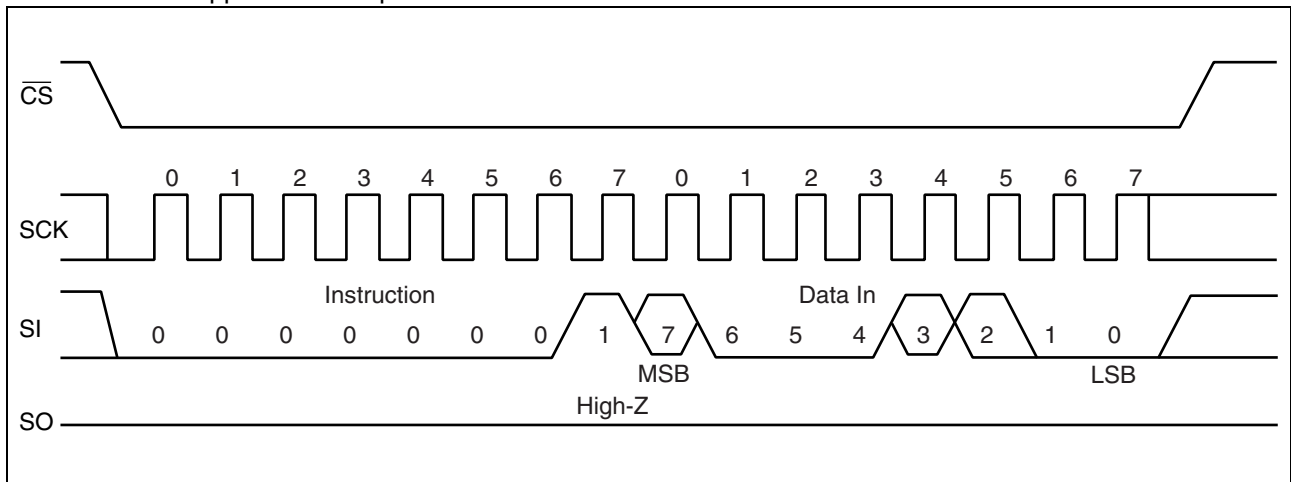
## • RDSR

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of  $\overline{CS}$ . RDSR command is applicable to "Up to 33 MHz operation".



## • WRSR

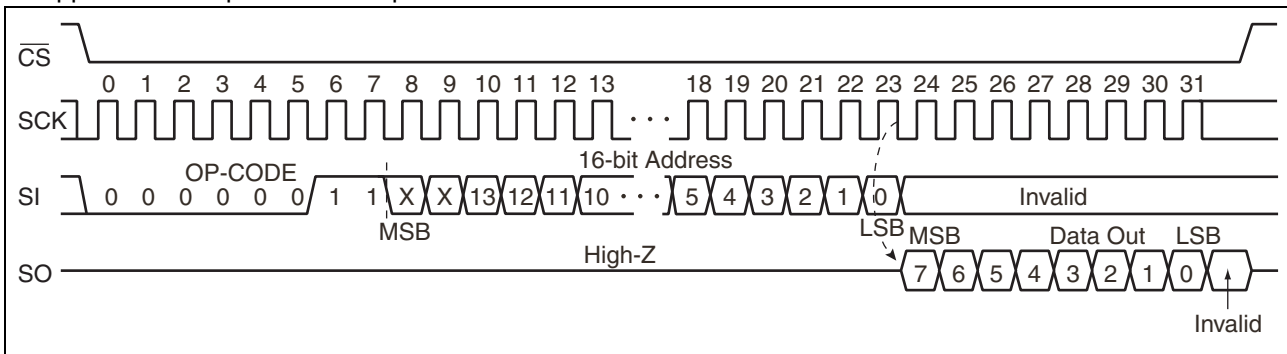
The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to "0" and cannot be written. The SI value corresponding to bit 0 is ignored.  $\overline{WP}$  signal level shall be fixed before performing WRSR command, and do not change the  $\overline{WP}$  signal level until the end of command sequence. WRSR command is applicable to "Up to 33 MHz".





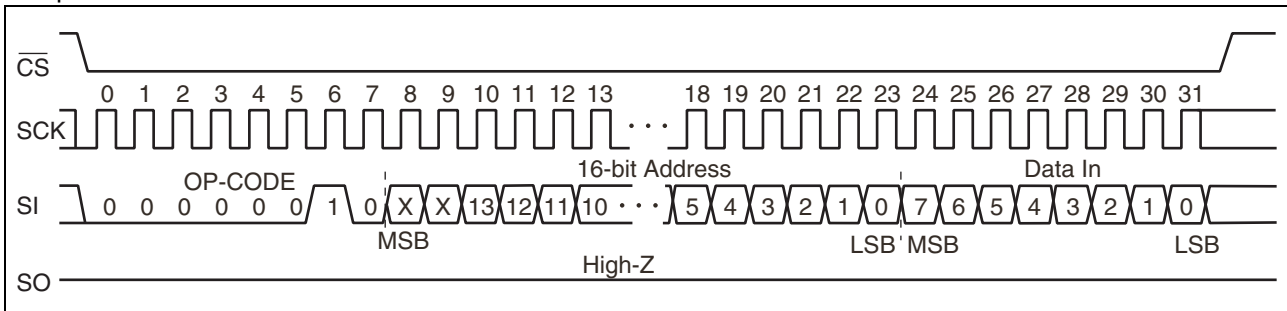
## • READ

The READ command reads FRAM memory cell array data. Arbitrary 16 bits address and op-code of READ are input to SI. The upper two address bits are invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When  $\overline{CS}$  is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before  $\overline{CS}$  rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely. READ command is applicable to “Up to 33 MHz operation”.



## • WRITE

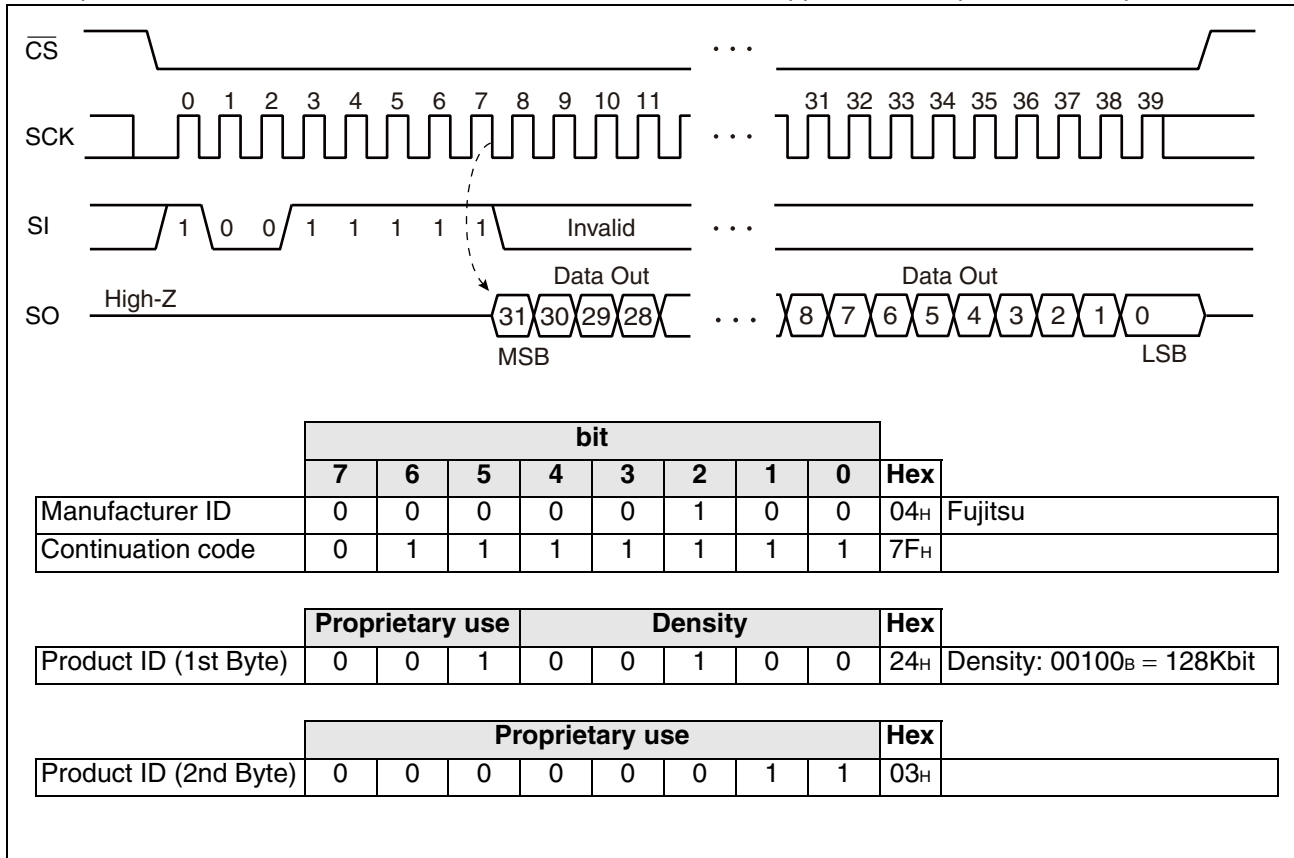
The WRITE command writes data to FRAM memory cell array. WRITE op-code, arbitrary 16 bits of address and 8 bits of writing data are input to SI. The upper two address bits are invalid. When 8 bits of writing data is input, data is written to FRAM memory cell array. Risen  $\overline{CS}$  will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before  $\overline{CS}$  rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely. WRITE command is applicable to “Up to 33 MHz operation”.



# MB85RS128TY

## • RDID

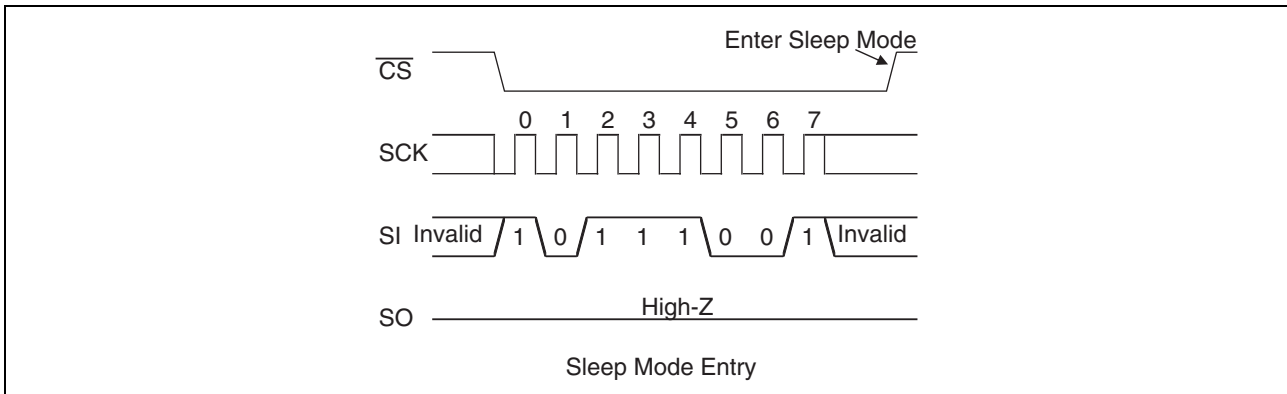
The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, 32-bit Device ID is output by continuously sending SCK clock, and SO holds the output state of the last bit until CS is risen. RDID command is applicable to "Up to 33 MHz operation".



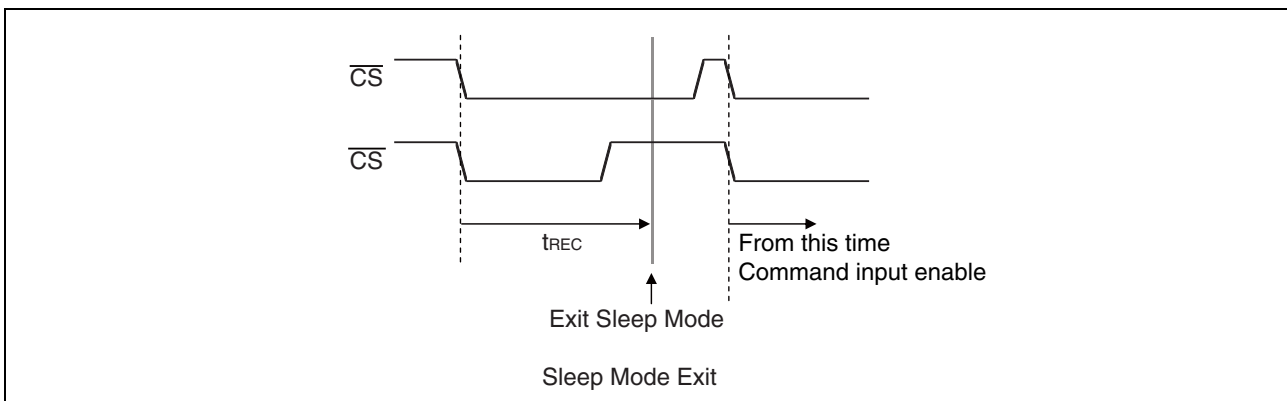
## • SLEEP

The SLEEP command shifts the LSI to a low power mode called "SLEEP mode". The transition to the SLEEP mode is carried out at the rising edge of  $\overline{CS}$  after operation code in the SLEEP command. However, when at least one SCK clock is inputted before the rising edge of  $\overline{CS}$  after operation code in the SLEEP command, this SLEEP command is canceled.

After the SLEEP mode transition, SCK and SI inputs are ignored and SO changes to a High-Z state.



Returning to a normal operation from the SLEEP mode is carried out after  $t_{REC}$  (Max 400  $\mu$ s) time from the falling edge of  $\overline{CS}$  (see the figure below). It is possible to return  $\overline{CS}$  to H level before  $t_{REC}$  time. However, it is prohibited to bring down  $\overline{CS}$  to L level again during  $t_{REC}$  period.



## ■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	3000 <sub>H</sub> to 3FFF <sub>H</sub> (upper 1/4)
1	0	2000 <sub>H</sub> to 3FFF <sub>H</sub> (upper 1/2)
1	1	0000 <sub>H</sub> to 3FFF <sub>H</sub> (all)

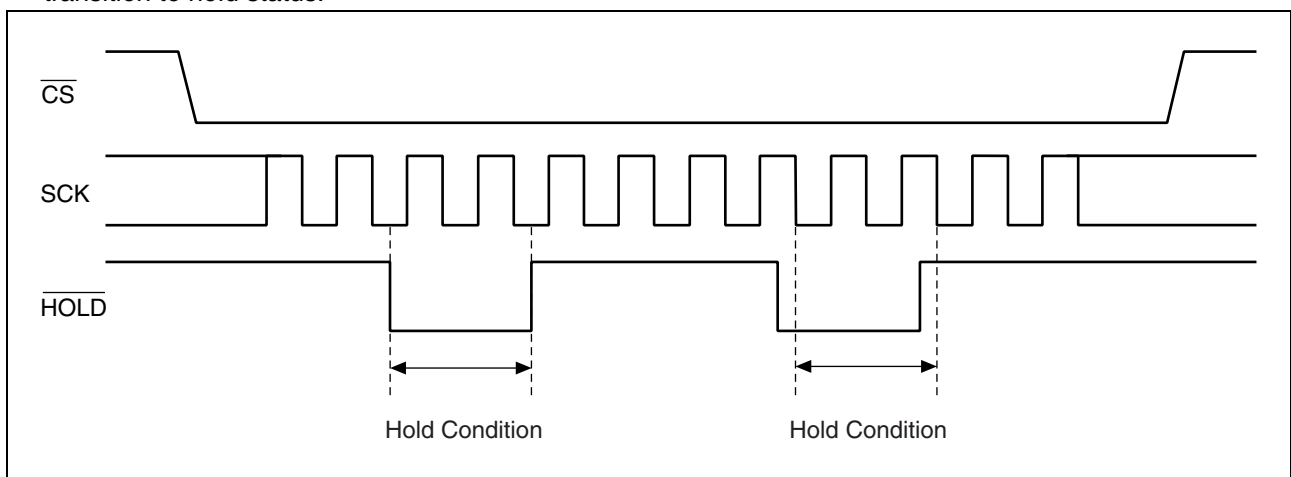
## ■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, WP as shown in the table.

WEL	WPEN	WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

## ■ HOLD OPERATION

Hold status is retained without aborting a command if  $\overline{\text{HOLD}}$  is "L" level while  $\overline{\text{CS}}$  is "L" level. The timing for starting and ending hold status depends on the SCK to be "H" level or "L" level when a  $\overline{\text{HOLD}}$  pin input is transitioned to the hold condition as shown in the diagram below. In case the  $\overline{\text{HOLD}}$  pin transitioned to "L" level when SCK is "L" level, return the  $\overline{\text{HOLD}}$  pin to "H" level at SCK being "L" level. In the same manner, in case the  $\overline{\text{HOLD}}$  pin transitioned to "L" level when SCK is "H" level, return the  $\overline{\text{HOLD}}$  pin to "H" level at SCK being "H" level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, READ). If  $\overline{\text{CS}}$  is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.



## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	$V_{DD}$	- 0.5	+ 4.0	V
Input voltage*	$V_{IN}$	- 0.5	$V_{DD} + 0.5$	V
Output voltage*	$V_{OUT}$	- 0.5	$V_{DD} + 0.5$	V
Operation ambient temperature	$T_A$	- 40	+ 125	°C
Storage temperature	$T_{stg}$	- 55	+ 150	°C

\*: These parameters are based on the condition that  $V_{SS}$  is 0 V.

**WARNING:** Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*1	$V_{DD}$	1.8	3.3	3.6	V
Operation ambient temperature*2	$T_A$	- 40	—	+ 125	°C

\*1: These parameters are based on the condition that  $V_{SS}$  is 0 V.

\*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit	
			Min	Typ	Max		
Input leakage current*1	I <sub>LIL</sub>	$0 \leq \overline{CS} < V_{DD}$	—	—	200	μA	
		$\overline{CS} = V_{DD}$	25 °C	—	—		1
			125 °C	—	—		2
		$\overline{WP}, \overline{HOLD}, SCK$ SI = 0 V to V <sub>DD</sub>	25 °C	—	—		1
125 °C	—		—	2			
Output leakage current*2	I <sub>LOL</sub>	SO = 0 V to V <sub>DD</sub>	25 °C	—	—	1	μA
			125 °C	—	—	2	
Operating power supply current*3	I <sub>DD</sub>	SCK = 33 MHz	—	—	2.3	mA	
Standby current	I <sub>SB</sub>	SCK = SI = $\overline{CS}$ = $\overline{WP} = \overline{HOLD} = V_{DD}$	—	—	45	μA	
Sleep current	I <sub>ZZ</sub>	$\overline{CS} = V_{DD}$ All inputs V <sub>SS</sub> or V <sub>DD</sub>	—	—	12	μA	
Input high voltage	V <sub>IH</sub>	V <sub>DD</sub> = 1.8 V to 3.6 V	V <sub>DD</sub> × 0.8	—	V <sub>DD</sub> + 0.5	V	
Input low voltage	V <sub>IL</sub>	V <sub>DD</sub> = 1.8 V to 3.6 V	- 0.5	—	V <sub>DD</sub> × 0.2	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = - 2 mA	V <sub>DD</sub> - 0.5	—	—	V	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2 mA	—	—	0.4	V	
Pull up resistance for $\overline{CS}$	R <sub>P</sub>	—	18	33	80	kΩ	

\*1 : Applicable pin :  $\overline{CS}$ ,  $\overline{WP}$ ,  $\overline{HOLD}$ , SCK, SI

\*2 : Applicable pin : SO

\*3 : Input voltage magnitude : V<sub>DD</sub> - 0.2 V or V<sub>SS</sub>

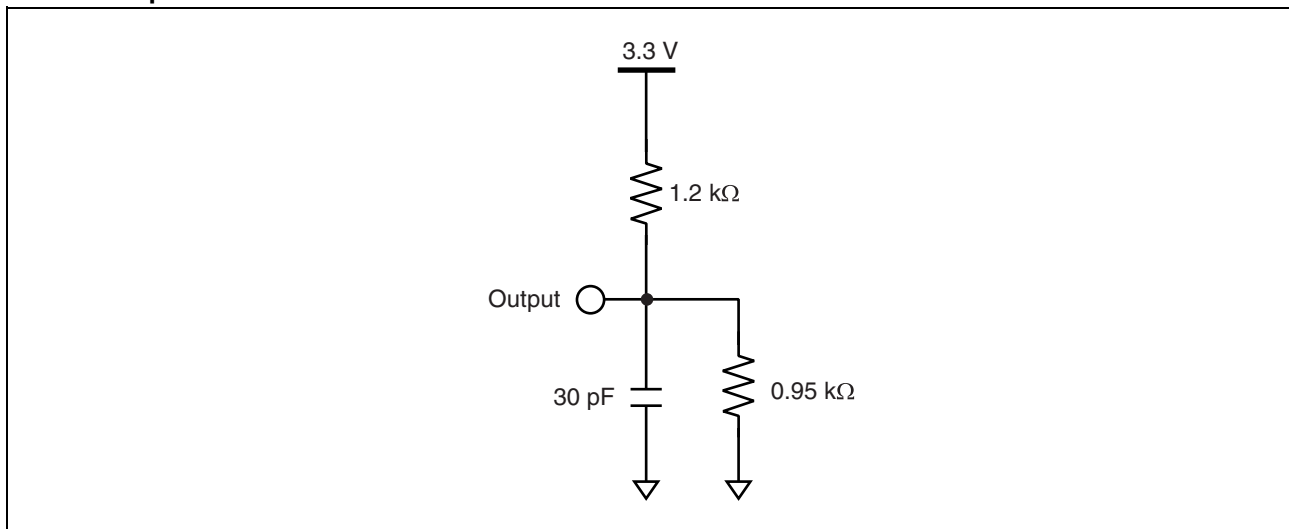
## 2. AC Characteristics

Parameter	Symbol	Value		Unit
		Min	Max	
SCK clock frequency	f <sub>CK</sub>	0	33	MHz
Clock high time	t <sub>CH</sub>	13	—	ns
Clock low time	t <sub>CL</sub>	13	—	ns
Chip select set up time	t <sub>CSU</sub>	10	—	ns
Chip select hold time	t <sub>CSH</sub>	10	—	ns
Output disable time	t <sub>OD</sub>	—	16	ns
Output data valid time	t <sub>ODV</sub>	—	13	ns
Output hold time	t <sub>OH</sub>	0	—	ns
Deselect time	t <sub>D</sub>	40	—	ns
Data in rising time	t <sub>R</sub>	—	50	ns
Data falling time	t <sub>F</sub>	—	50	ns
Data set up time	t <sub>SU</sub>	5	—	ns
Data hold time	t <sub>H</sub>	5	—	ns
$\overline{\text{HOLD}}$ set uptime	t <sub>HS</sub>	10	—	ns
$\overline{\text{HOLD}}$ hold time	t <sub>HH</sub>	10	—	ns
$\overline{\text{HOLD}}$ output floating time	t <sub>HZ</sub>	—	20	ns
$\overline{\text{HOLD}}$ output active time	t <sub>LZ</sub>	—	20	ns
SLEEP recovery time	t <sub>REC</sub>	—	400	μs

### AC Test Condition

Power supply voltage : 1.8 V to 3.6 V Operation  
 Operation ambient temperature : - 40 °C to + 125 °C  
 Input voltage magnitude :  $V_{DD} \times 0.8 \leq V_{IH} \leq V_{DD}$   
    $0 \leq V_{IL} \leq V_{DD} \times 0.2$   
 Input rising time : 5 ns  
 Input falling time : 5 ns  
 Input judge level :  $V_{DD}/2$   
 Output judge level :  $V_{DD}/2$

## AC Load Equivalent Circuit



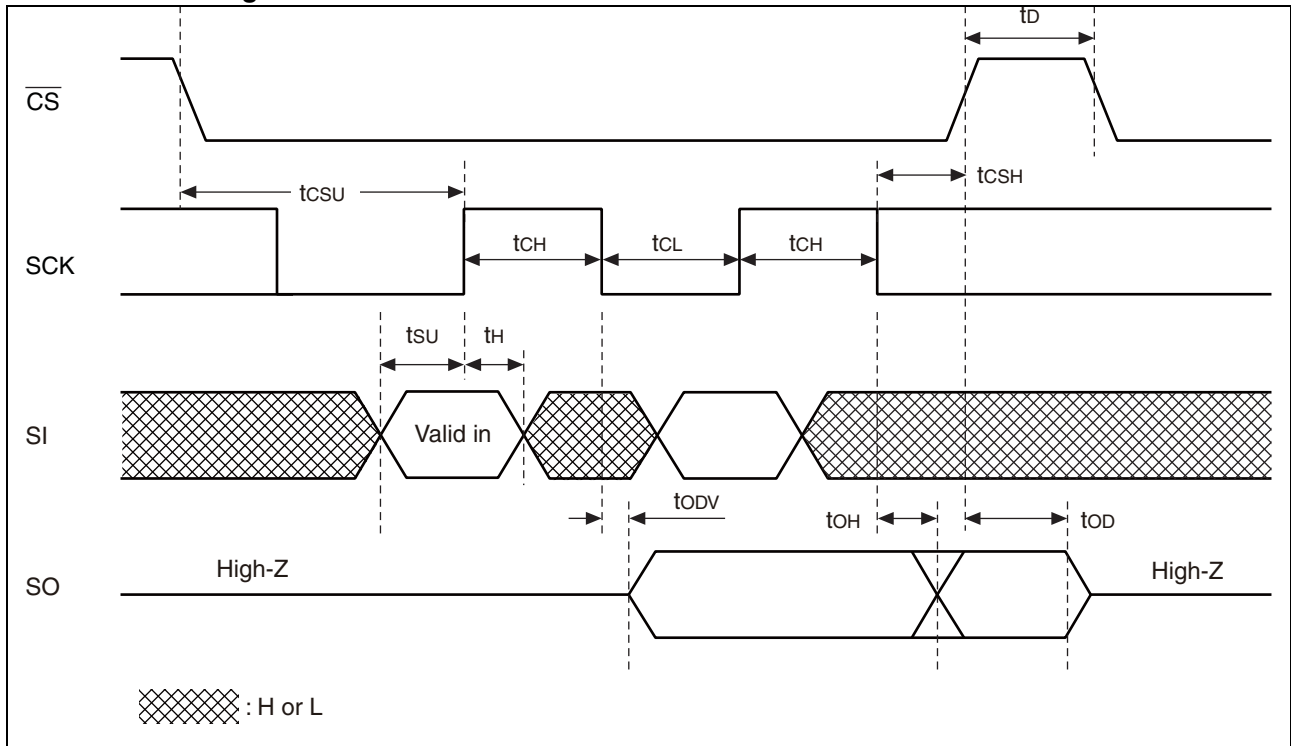
## 3. Pin Capacitance

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output capacitance	$C_o$	$V_{DD} = 3.3 \text{ V}$ , $V_{IN} = V_{OUT} = 0 \text{ V to } V_{DD}$ , $f = 1 \text{ MHz}$ , $T_A = +25 \text{ }^\circ\text{C}$	—	8	pF
Input capacitance	$C_i$		—	6	pF

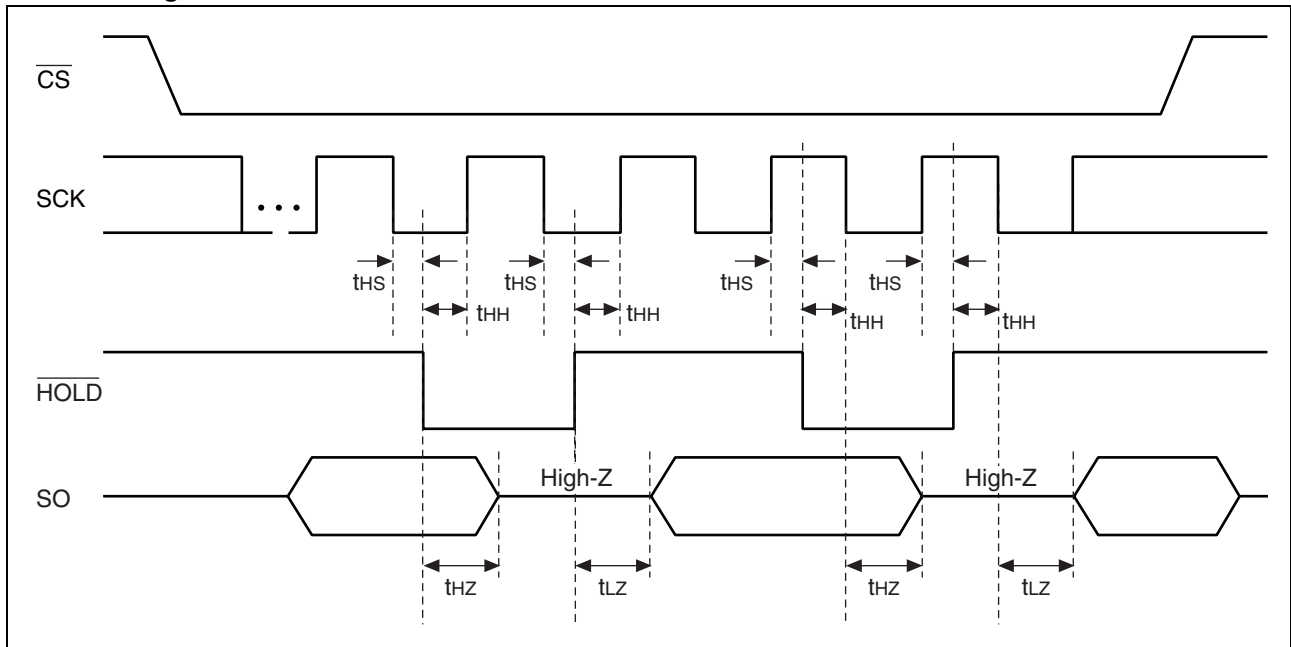


## ■ TIMING DIAGRAM

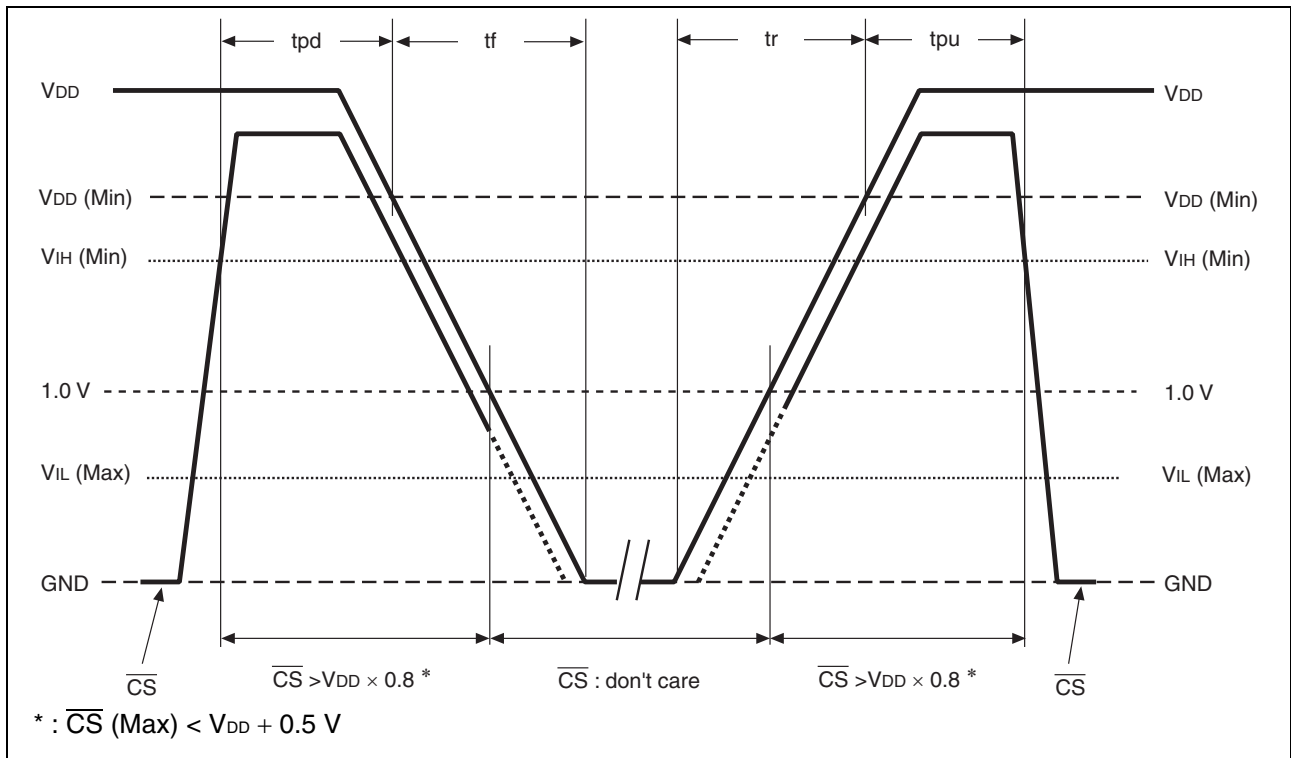
### • Serial Data Timing



### • Hold Timing



## POWER ON/OFF SEQUENCE



Parameter	Symbol	Value		Unit
		Min	Max	
$\overline{CS}$ level hold time at power OFF	tpd	400	—	ns
$\overline{CS}$ level hold time at power ON	tpu	250	—	$\mu\text{s}$
Power supply rising time	tr	0.05	—	ms/V
Power supply falling time	tf	0.1	—	ms/V

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

## FRAM CHARACTERISTICS

Parameter	Value		Unit	Remarks
	Min	Max		
Read/Write Endurance <sup>*1</sup>	$10^{13}$	—	Times/byte	Operation Ambient Temperature $T_A = +85\text{ }^\circ\text{C}$
Data Retention <sup>*2</sup>	1 or more <sup>*3</sup>	—	Years	Operation Ambient Temperature $T_A = +125\text{ }^\circ\text{C}$
	10	—		Operation Ambient Temperature $T_A = +85\text{ }^\circ\text{C}$

\*1 : Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

\*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

\*3: Under evaluation for more than 1 year(+125 °C).

## NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

## ■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RS128TYPNF-G-BCE1	$\geq  2000 \text{ V} $
ESD MM (Machine Model) JESD22-A115 compliant		$\geq  200 \text{ V} $
ESD CDM (Charged Device Model) JESD22-C101 compliant		$\geq  1000 \text{ V} $
Latch-Up (I-test) JESD78 compliant		$\geq  125 \text{ mA} $
Latch-Up ( $V_{\text{supply}}$ overvoltage test) JESD78 compliant		$\geq 5.4\text{V}$

## ■ REFLOW CONDITIONS AND FLOOR LIFE

[ JEDEC MSL ] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

## ■ Current status on Contained Restricted Substances

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

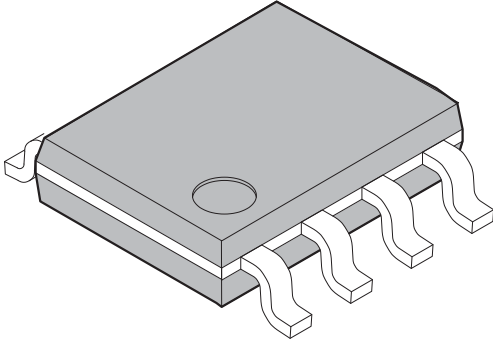
# MB85RS128TY

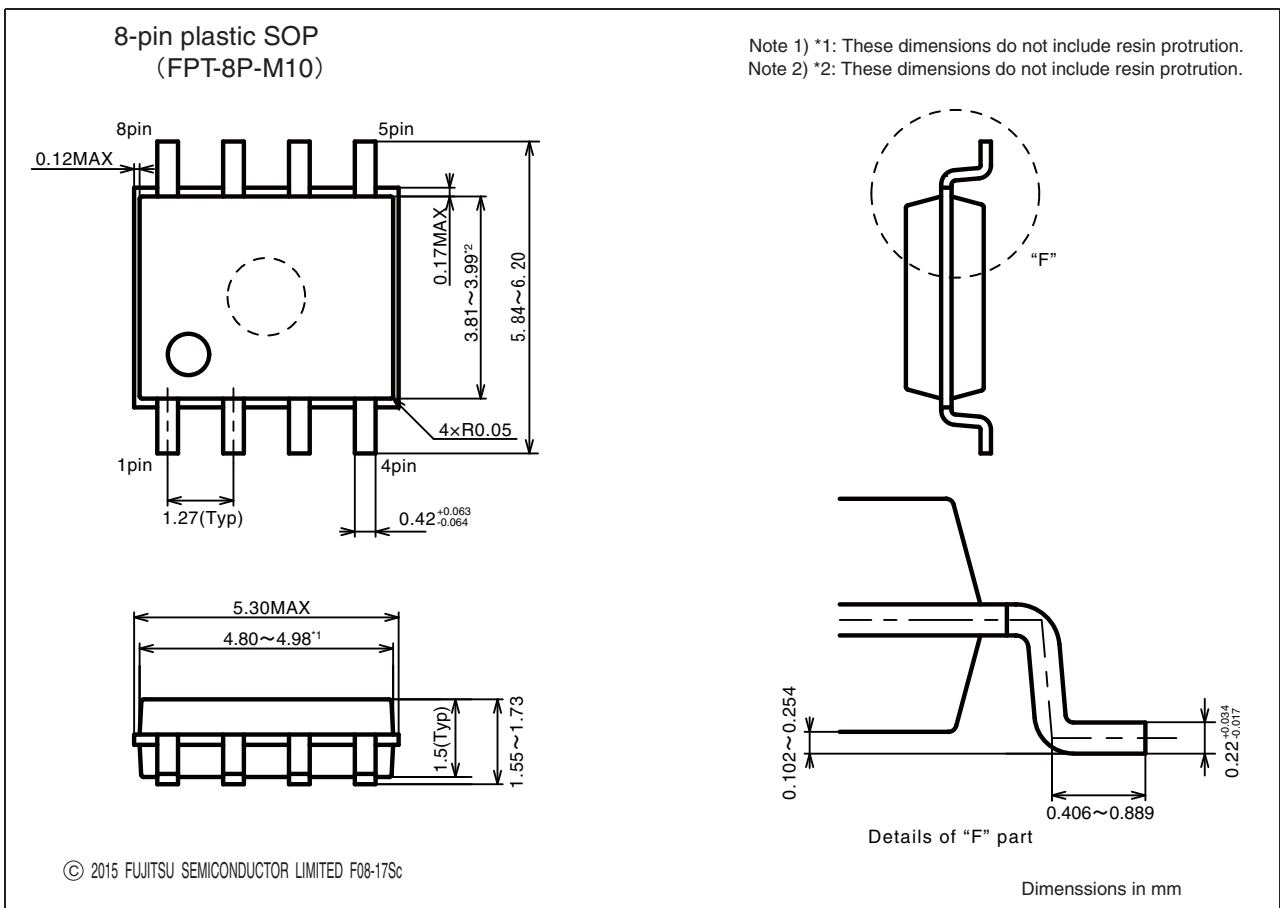
## ■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RS128TYPNF-G-BCE1	8-pin plastic SOP (FPT-8P-M10)	Tube	— *
MB85RS128TYPNF-G-BCERE1	8-pin plastic SOP (FPT-8P-M10)	Embossed Carrier tape	1500

\* : Please contact our sales office about minimum shipping quantity.

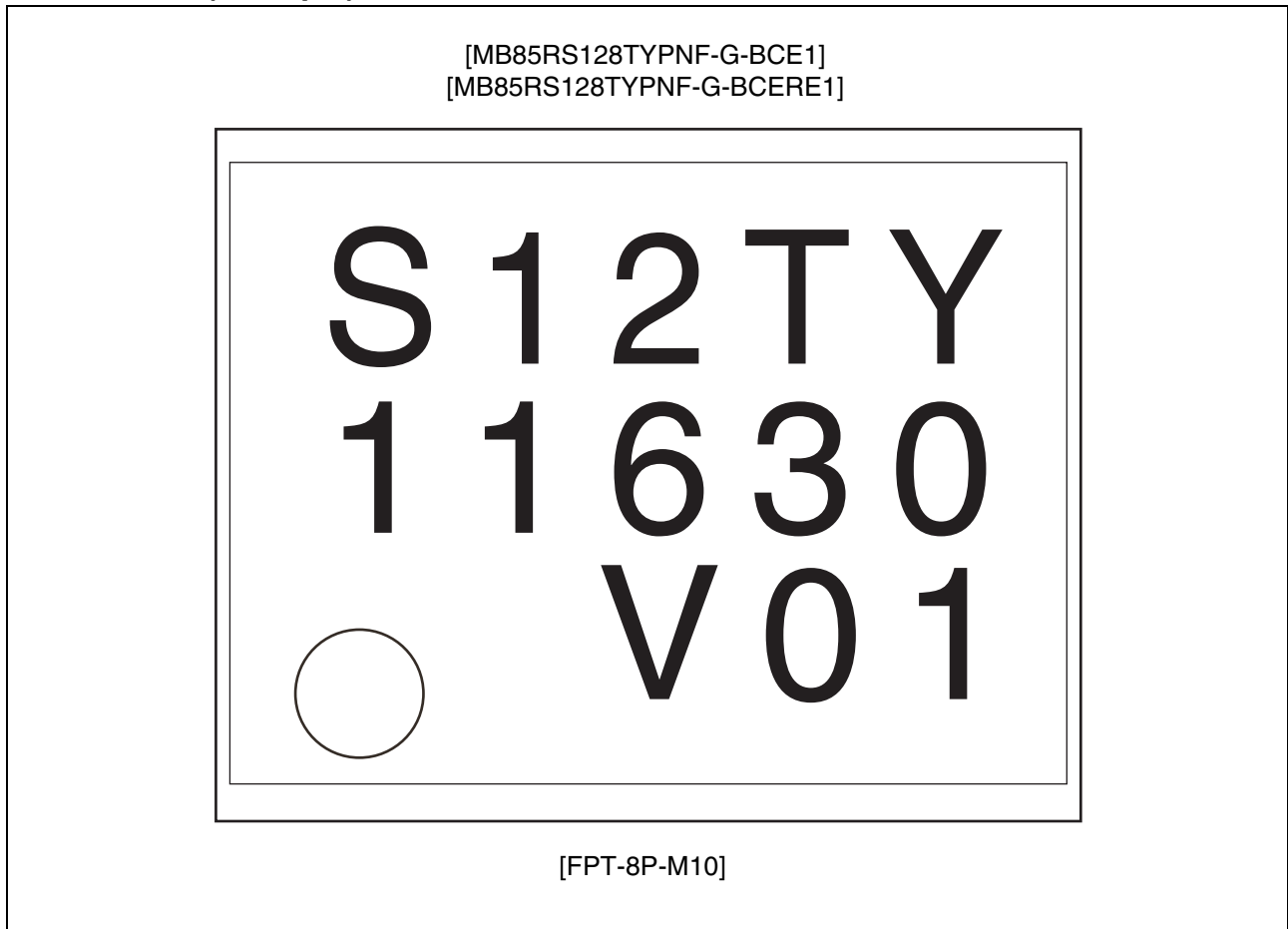
## ■ PACKAGE DIMENSION

 <p>8-pin plastic SOP</p> <p>(FPT-8P-M10)</p>	Lead pitch	1.27 mm
	Package width × package length	3.9 mm × 4.89 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.73 mm MAX
	Weight	0.08 g



# MB85RS128TY

## ■ MARKING (Example)



**MEMO**

## FUJITSU SEMICONDUCTOR LIMITED

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