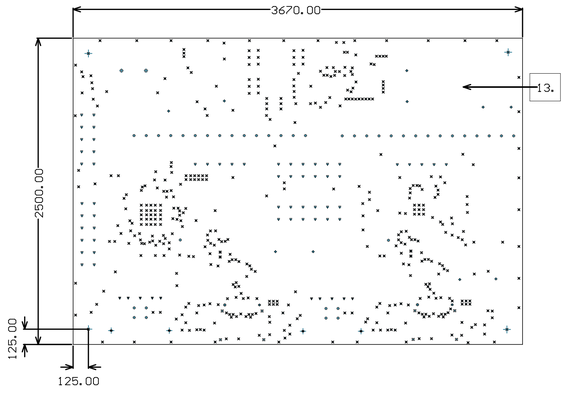
REV	ECO	Comments	Date

NOTE UNLESS OTHERWISE SPECIFIED:

1. Base Material 370HR, RoHS compliant and compatible.
2. PCB Lay-up: 0.062 inches +/-0.007" Finished Board Thickness.
3. PCB Construction: 4 layers. This construction shall be as detailed per Layer Stackup Table.
4. Conductive Pattern Finish: IPC ENIG (Au over Ni).
5. Soldermask: Soldermask over bare copper, *RED* both sides.
   Soldermask shall be in accordance with IPC-SM-840 Class T.
   There shall be no soldermask on any land.
6. Silkscreen: DO NOT clear silkscreen (legend) from tented vias.
   Top side with white, permanent, non-conductive ink.
   Bottom side is to be the same, if present.
   There shall be no ink on any exposed land.
7. Board fabrication acceptance shall meet IPC-6012-B Class 2 workmanship requirements.
8. Minimum copper plate in all holes to be 0.001 inches.
9. Copper thieving may be added by the PCB fabricator on inner and outer signal layers to assist the plating process ONLY IF:
   A. All thieving pads are kept at least 55 mils from other features,
   B. The thieving pattern is made up of individual and separate pads. (No hatching, grids, or lines allowed.)
10. Ref.: Minimum Conductor Width/Spacing: 7mil/6mil.
11. All Artwork is viewed through the PC Board.
12. PCB must be tested per IPC-9252 Class 2. Any deviation from this requirement must have written authorization from Microchip Technology Inc.
13. Vendor ID, UL rating, date code and/or lot number must appear on this board in copper located as shown on bottom side.
14. Finished drill hole size tolerances unless otherwise specified:
    Under 0.021 inches - +0.003/-0.006
    0.021 to 0.090 inches - +/-0.003
    Over 0.090 inches - +/-0.006
15. Traces shall finish at the artwork width, +/- 1 mil.



3.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer	Copper	1.40mil		
	Dielectric1	370HR(1PLY 1080&1PLY 106)	4.30mil	4.2	
2	Layer 2	Copper	1.42mil		
	Dielectric 3	370 HR	46.00mil	4.3	
3	Layer 3	Copper	1.42mil		
	Dielectric 2	370HR(1PLY 1080&1PLY 106	4.30mil	4.3	
4	Bottom Layer	Copper	1.40mil		
	Bottom Solder	Solder Resist	0.39mil	3.5	
	Bottom Overlay				

M4 FAB 3.0

Microchip Technology Inc.
10900-B Stonelake Blvd.
Suite 100
Austin, TX 78759

TITLE: **UPD301 EVB (SRC)**

PROJECT PART NUMBER: EVB-UPD301-SRC

PCB DESIGNER: Jennifer Hancock

GERBER FILE: Fab Drawing (Bottom,Top Layer)

ENGINEER: Mick Davis

BOARD NUMBER: 04-11033

DOCUMENT NUMBER: 04-11033-D

DATE: 8/22/2019

PCB FILE NAME: UNG_8170_EVB_UPD301_SRC_C.PcbDoc

LAYER NAME:

REV: 3.0