PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017

DATA SHEET

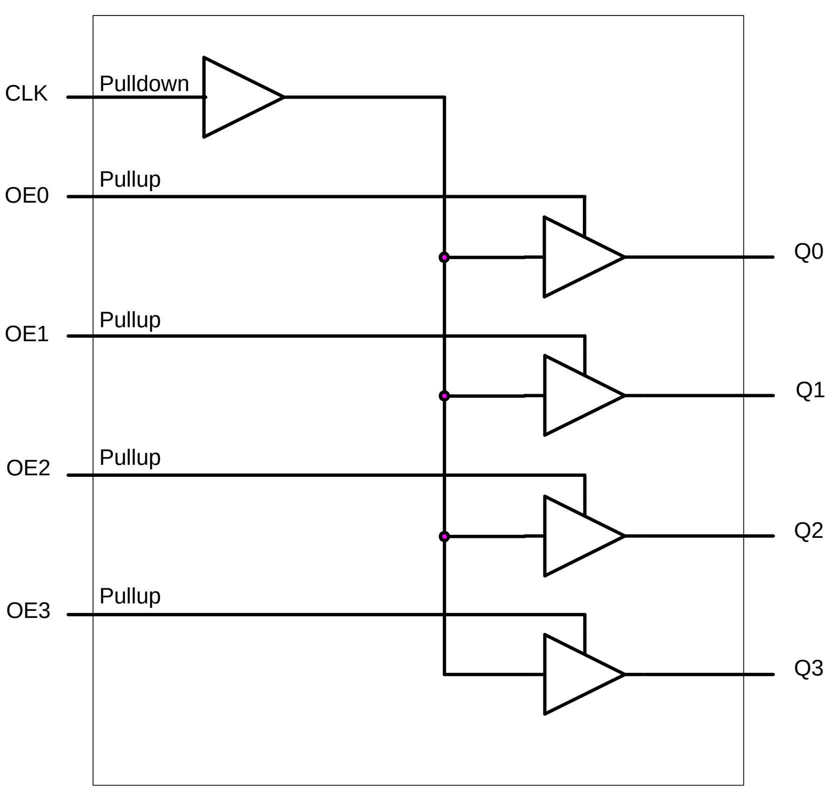
General Description

The ICS8304-02 is a low skew, high performance, 1-to-4 Fanout Buffer with individual output enables. The ICS8304-02 is characterized at full 3.3V and 2.5V for input (V_{DD}), and mixed 3.3V and 2.5V for output operating supply modes (V_{DDO}). Guaranteed output and part-to-part skew characteristics make the ICS8304-02 ideal for those clock distribution applications demanding well defined performance and repeatability.

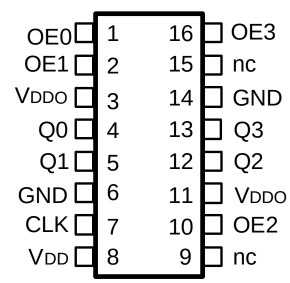
Features

- Four LVCMOS / LVTTL outputs, 15Ω output impedance
- LVCMOS / LVTTL clock input
- Maximum output frequency: 250MHz
- Output skew: 30ps (typical)
- Part-to-part skew: 400ps (maximum)
- Small 16 lead TSSOP package saves board space
- Power supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- Individual output enable control
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging
- For functional replacement part use 8305

Block Diagram



Pin Assignment



ICS8304-02

16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm package body
G Package
Top View

Pin Descriptions and Pin Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2, 10, 16	OE0, OE1, OE2, OE3	Input	Pullup	Output enable pins. Active HIGH. If pin is LOW, output is high impedance. LVCMOS/LVTTL interface levels. See Table 3.
3, 11	V_{DDO}	Power		Output supply pins.
4, 5, 12, 13	Q0, Q1, Q2, Q3	Output		Single-ended clock outputs. 15Ω output impedance. LVCMOS/LVTTL interface levels.
6, 14	GND	Power		Power supply ground.
7	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
8	V_{DD}	Power		Power supply pin.
9, 15	nc	Unused		No connect.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.465V or 2.625V		5		pF
		V_{DD} = 3.465V, V_{DDO} = 2.625V		3		pF
R_{OUT}	Output Impedance	V_{DDO} = 3.465V		15		Ω
		V_{DDO} = 2.625V		17		Ω

Function Table

Table 3. OEx Function Table

Inputs	Outputs
OE3, OE2, OE1, OE0	**Q3, Q2, Q1, Q0**
0	Hi-Z
1	Active (default)

NOTE: Asynchronous output enables.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO}+ 0.5V
Package Thermal Impedance, θ_{JA}	100.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 3.3V ± 5% or 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current			16	20	mA
I_{DDO}	Output Supply Current			6	10	mA

Table 4B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			14	17	mA
I_{DDO}	Output Supply Current			5	10	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2		V_{DD} + 0.3	V
			V_{DD} = 2.625V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		0.8	V
			V_{DD} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
		OE3, OE2, OE1, OE0	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		OE3, OE2, OE1, OE0	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage		V_{DDO} = 3.3V ± 5%; I_{OH} = -12mA	2.6			V
			V_{DDO} = 2.5V ± 5%; I_{OH} = -12mA	1.8			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.3V ± 5%; I_{OL} = 12mA			0.5	V
			V_{DDO} = 2.5V ± 5%; I_{OL} = 12mA			0.5	V
I_{OZL}	Output Hi-Z Current Low			-5			µA
I_{OZH}	Output Hi-Z Current High					5	µA

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V ± 5%, T_A = 0°C to 70°C

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	CLK		2.0	2.5	4.0	ns
*t*sk(o)	Output Skew; NOTE 2, 5		Measured on the Rising Edge		30	60	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5					400	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	400	600	1000	ps
odc	Output Duty Cycle		Output Frequency < 150MHz	45	50	55	%
			Output Frequency ≥150MHz	40	47	60	%
t_{EN}	Output Enable Time; NOTE 4				3	5	ns
t_{DIS}	Output Disable Time; NOTE 4				4	6	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	CLK		2.0	2.7	4.0	ns
*t*sk(o)	Output Skew; NOTE 2, 5		Measured on the Rising Edge		30	60	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5					425	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	400	750	1200	ps
odc	Output Duty Cycle		Output Frequency < 150MHz	45	50	55	%
			Output Frequency ≥150MHz	40	47	60	%
t_{EN}	Output Enable Time; NOTE 4				3	5	ns
t_{DIS}	Output Disable Time; NOTE 4				4	6	ns

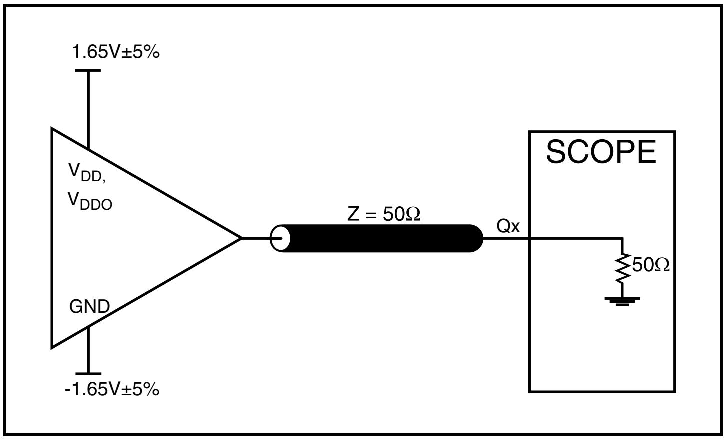
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Table 5C. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

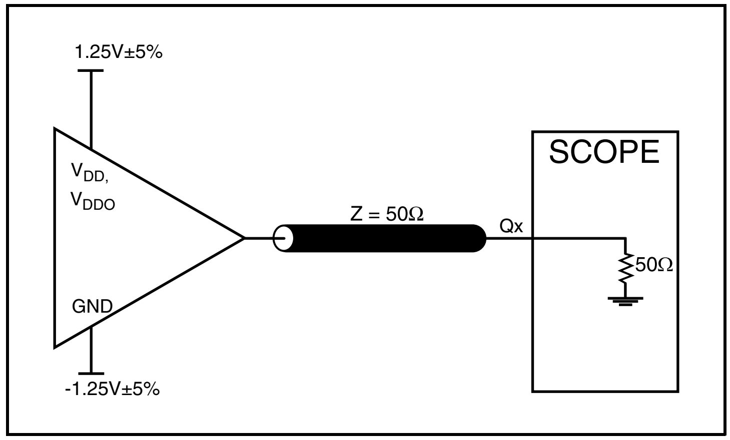
Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency					250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	CLK		2.0	2.8	4.0	ns
*t*sk(o)	Output Skew; NOTE 2, 5		Measured on the Rising Edge		30	60	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5					425	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	400	750	1200	ps
odc	Output Duty Cycle		Output Frequency < 150MHz	45	50	55	%
			Output Frequency ≥150MHz	40	47	60	%
t_{EN}	Output Enable Time; NOTE 4				3	5	ns
t_{DIS}	Output Disable Time; NOTE 4				4	6	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

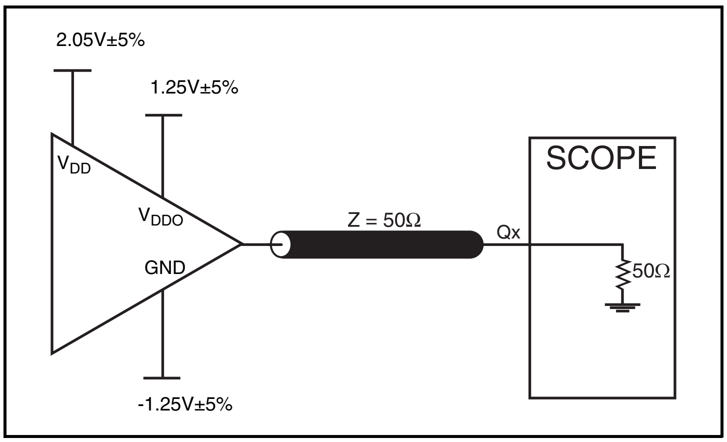
Parameter Measurement Information



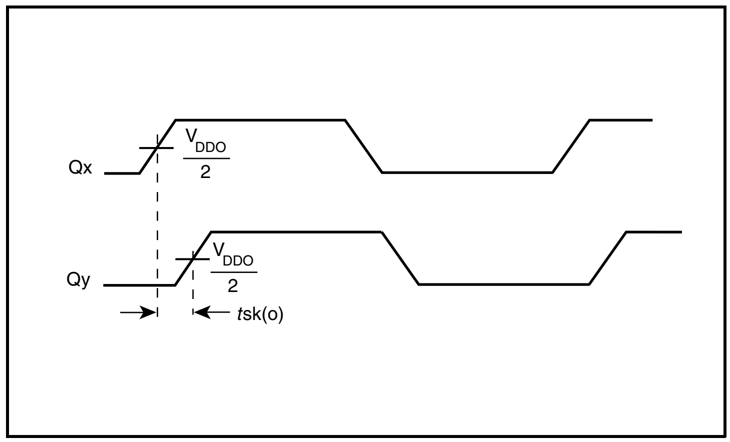
3.3V Core/3.3V LVCMOS Output Load Test Circuit



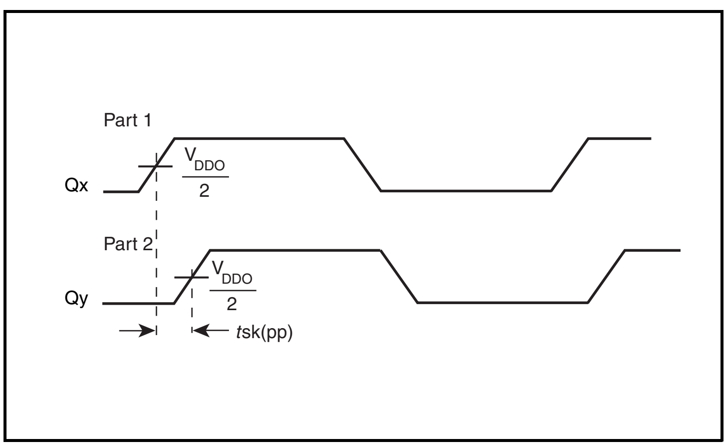
2.5V Core/2.5V LVCMOS Output Load Test Circuit



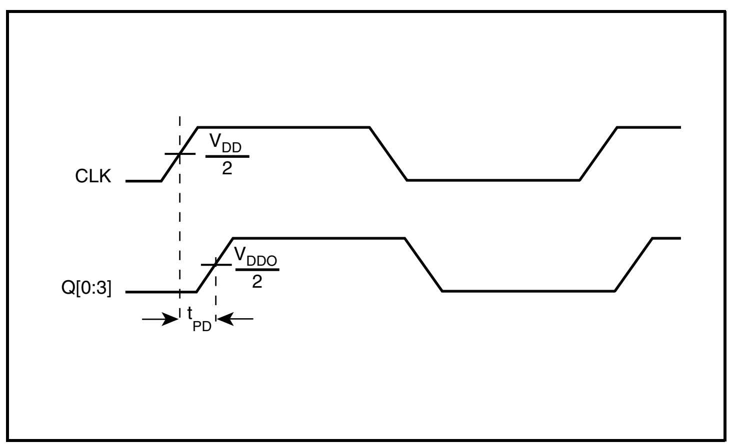
3.3V Core/2.5V LVCMOS Output Load Test Circuit



Output Skew

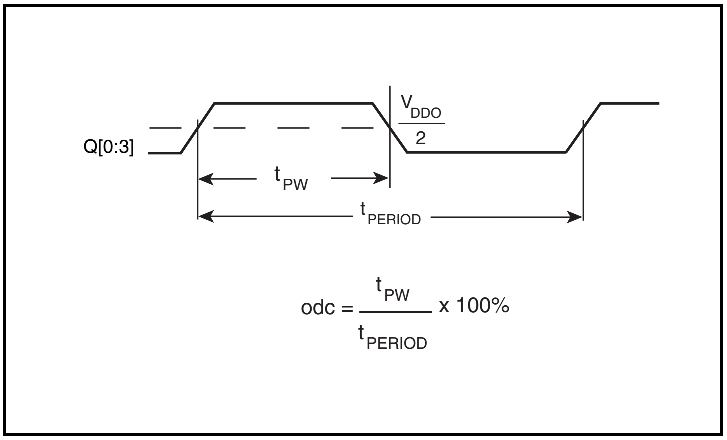


Part-to-Part Skew

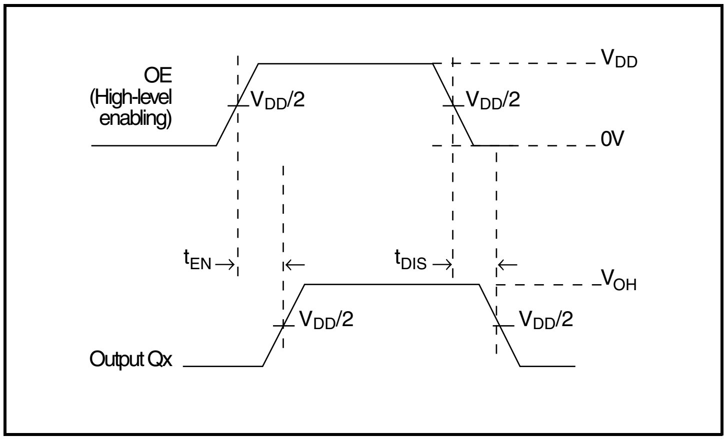


Propagation Delay

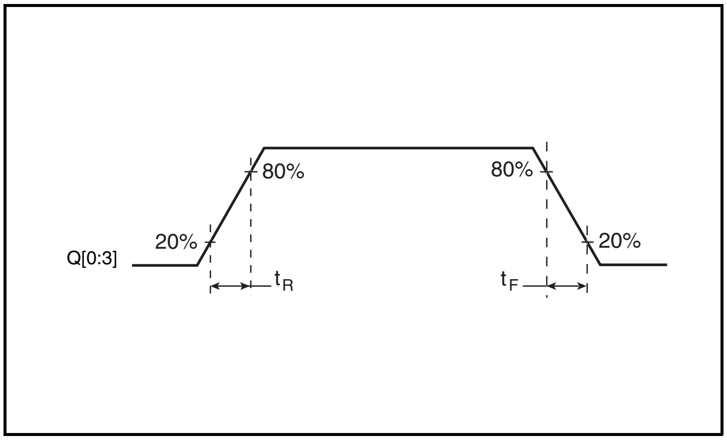
Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period



Output Enable/Disable Time



Output Rise/Fall Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullup resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8304-02.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8304-02 is the sum of the core power plus the power dissipated due to loading. The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX}$ = V_{DD_MAX} * (I_{DD} + I_{DDO}) = 3.465V *(20mA + 17mA) = **128.21mW**
- Output Impedance R_{OUT} Current due to Loading 50Ω to V_{DD}/2
  Output Current I_{OUT} = V_{DD_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 15Ω)] = **26.7mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * $(I_{OUT})^2$ = 15Ω * $(26.7mA)^2$ = **10.7mW per output**
- Total Power (R_{OUT}) = 10.7mW * 4 = **42.8mW**

Dynamic Power Dissipation at 250MHz

Power (250MHz) = C_{PD} * Frequency * $(V_{DD})^2$ = 5pF * 250MHz * $(3.465V)^2$ = **15mW per output**

Total Power (250MHz) = 15mW * 4 = **60mW**

Total Power Dissipation

- **Total Power**
  = Power $(core)_{MAX}$ + Power (R_{OUT}) + Power (250MHz)
  = 128.21mW + 42.8mW + 60mW
  = 231.01mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 100.3°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0231W *100.3°C/W = 93.17°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

Transistor Count

The transistor count for ICS8304-02: 2690

Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

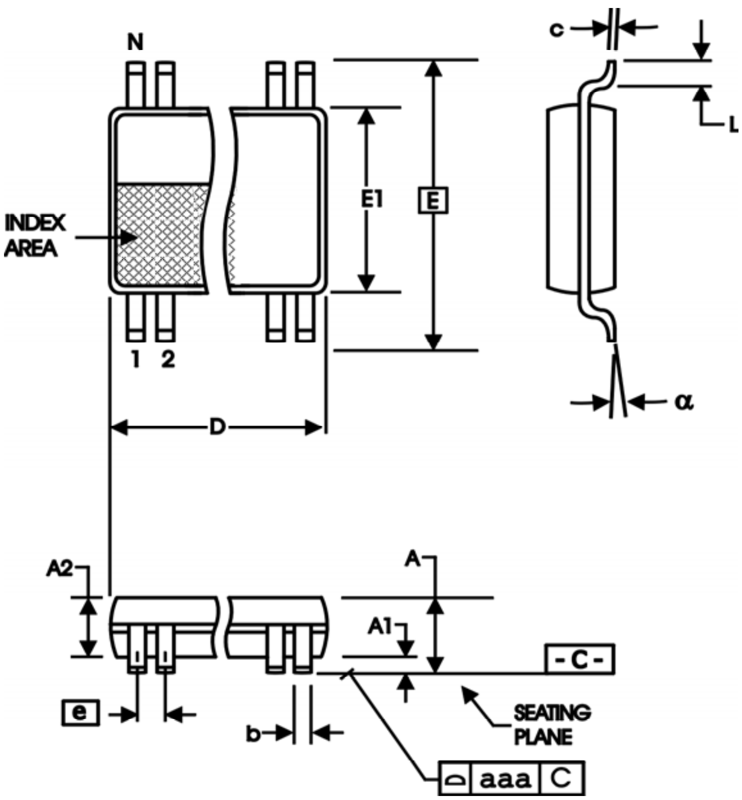


Table 8. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8304AG-02LF	8304A02L	“Lead-Free” 16 Lead TSSOP	Tube	0°C to 70°C
8304AG-02LFT	8304A02L	“Lead-Free” 16 Lead TSSOP	Tape & Reel	0°C to 70°C

Revision History

]

Revision Date	Description of Change
May 6, 2016	▪ Product Discontinuation Notice - Last time buy expires May 6, 2017. ▪ PDN CQ-16-01

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