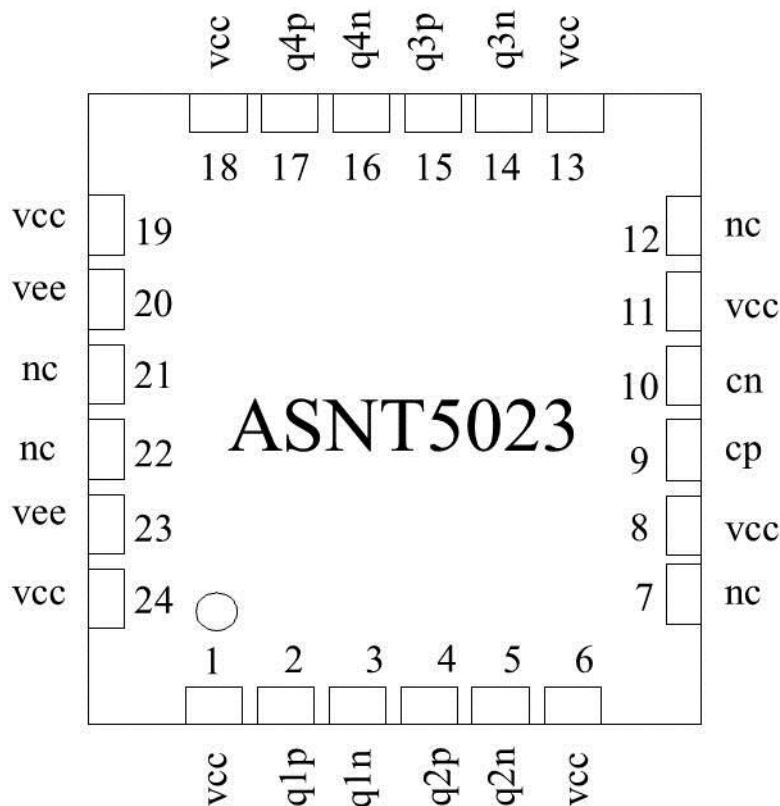# ASNT5023-PQC
DC-28*Gbps*/17*GHz* Signal Distributor 1-to-4

- High-speed broadband Data/Clock Amplifier and Distributor

- Exhibits low jitter and limited temperature variation over industrial temperature range

- One differential input signal port and four differential amplified output signal ports

- Matched phase delays for all outputs

- Fully differential CML input interface

- Fully differential CML output interfaces with 600*mV* single-ended swing

- Linearized output buffers for minimized undershoot/overshoot

- Single +3.3*V* or -3.3*V* power supply

- Power consumption: 1.22*W*

- Fabricated in SiGe for high performance, yield, and reliability

- Standard MLF/QFN 24-pin package

ADSANTEC

ASNT

Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
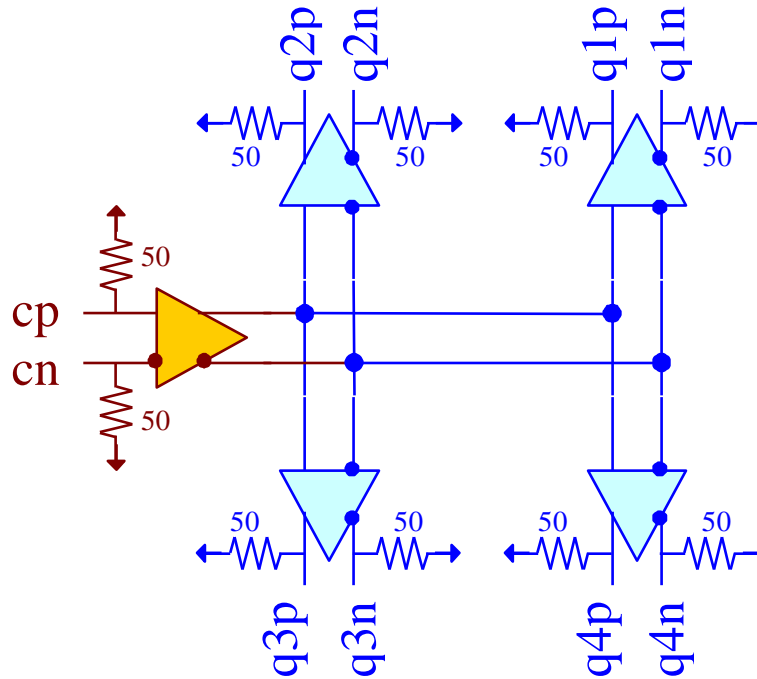*www.adsantec.com*

DESCRIPTION

Fig. 1. Functional Block Diagram

The temperature stable ASNT5023-PQC SiGe IC provides active broadband data/clock signal splitting and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can deliver four phase-matched copies of the broadband data/clock input signal cp/cn to four high-speed differential outputs q1p/q1n, q2p/q2n, q3p/q3n, q4p/q4n.

The part's I/O's support the CML logic interface with on chip $50Ohm$ termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = $0.0V$ = ground and vee = $−3.3V$), or positive supply (vcc = $+3.3V$ and vee = $0.0V$ = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with $50Ohm$ termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = $0.0V$ and vee = -$3.3V$.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		1.17	*W*
RF Input Voltage Swing (SE)		1.4	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
cp	9	CML input	Differential high speed data/clock inputs with internal SE 50*Ohm* termination to vcc
cn	10		
q1p	2	CML output	Differential high speed data/clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
q1n	3		
q2p	4	CML output	Differential high speed data/clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
q2n	5		
q3p	15	CML output	Differential high speed data/clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
q3n	14		
q4p	17	CML output	Differential high speed data/clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
q4n	16		
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	Positive power supply (+3.3*V* or 0)		1, 6, 8, 11, 13, 18, 19, 24
vee	Negative power supply (0*V* or -3.3*V*)		20, 23
nc	Not connected pins		7, 12, 21, 22

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
Ivee		370		mA	
Power consumption		1220		mW	
Junction temperature	-40	25	125	$°C$	
HS data/clock input (cp/cn)					
Data rate	DC		28	$Gbps$	
Frequency	DC		17	GHz	
Swing	50	300	600	mV	Differential or SE, p-p
Common mode level	vcc -0.6	vcc -0.5	vcc	mV	Must match for both inputs
Duty cycle	40	50	60	$\%$	For clock signal
HS data/clock output (q1p/q1n, q2p/q2n, q3p/q3n, q4p/q4n)					
Data rate	DC		28	$Gbps$	
Frequency	DC		17	GHz	
Latency		100		ps	From any input to any output
Phase mismatch			2	ps	Between any two SE outputs
Logic "1" level		vcc-0.1		V	
Logic "0" level		vcc-0.7		V	With external $50Ohm$ DC termination
Rise/Fall Times	15		19	ps	20%-80%
Additive Jitter			5	ps	Peak-to-peak

PACKAGE INFORMATION

The chip die is housed in a standard 24-pin QFN package shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to the vee plain that is ground for the positive supply or power for the negative supply.

The part's identification label is ASNT5023-PQC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.
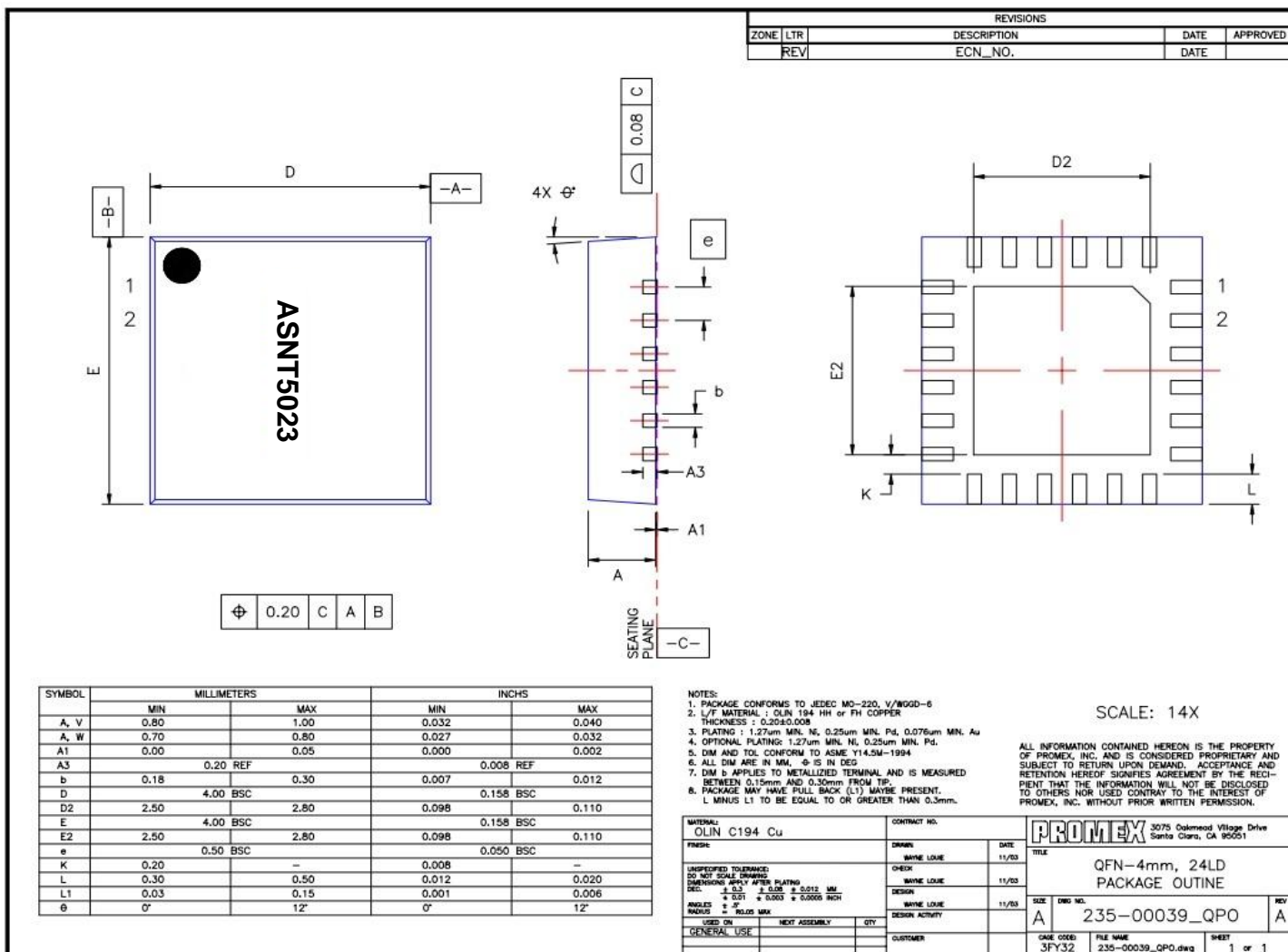
SYMBOL	MILLIMETERS		INCHS	
	MIN	MAX	MIN	MAX
A, V	0.80	1.00	0.032	0.040
A, W	0.70	0.80	0.027	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	4.00 BSC		0.158 BSC	
D2	2.50	2.80	0.098	0.110
E	4.00 BSC		0.158 BSC	
E2	2.50	2.80	0.098	0.110
e	0.50 BSC		0.050 BSC	
K	0.20	–	0.008	–
L	0.30	0.50	0.012	0.020
L1	0.03	0.15	0.001	0.006
θ	0°	12°	0°	12°

NOTES:
1. PACKAGE CONFORMS TO JEDEC MO-220, V/WGGD-6
2. L/F MATERIAL : OLIN 194 HH or FH COPPER
   THICKNESS : 0.20±0.008
3. PLATING : 1.27um MIN. Ni, 0.25um MIN. Pd, 0.076um MIN. Au
4. OPTIONAL PLATING: 1.27um MIN. Ni, 0.25um MIN. Pd.
5. DIM AND TOL. CONFORM TO ASME Y14.5M-1994
6. ALL DIM ARE IN MM, θ IS IN DEG
7. DIM b APPLIES TO METALLIZIED TERMINAL AND IS MEASURED
   BETWEEN 0.15mm AND 0.30mm FROM TIP.
8. PACKAGE MAY HAVE PULL BACK (L1) MAYBE PRESENT.
   L MINUS L1 TO BE EQUAL TO OR GREATER THAN 0.3mm.

MATERIAL:
OLIN C194 Cu

SCALE: 14X

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QFN-4mm, 24LD
PACKAGE OUTINE

DWG. NO. 235-00039_QPO   REV A

Fig. 2. QFN 24-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
2.1.2	02-2020	Updated Package Information
2.0.2	07-2019	Corrected output logic levels
1.9.2	07-2019	Updated Letterhead
1.9.1	08-2018	Corrected latency specifications
1.8.1	08-2018	Added latency specifications
1.7.1	05-2013	Corrected supply current and power
1.6.1	03-2013	Added phase mismatch specifications Updated description
1.5.1	02-2013	Revised title Revised pin out diagram Revised description Revised power supply configuration Corrected absolute maximum ratings table Corrected terminal functions table Corrected electrical characteristics table Updated package information
1.4	05-2012	Corrected parameters
1.3	02-2012	Modified description Modified title Added maximum ratings table Added packaging information Added revision history table
1.2	01-2012	Modified title and description
1.0	11-2011	Initial release