MAX77680/MAX77681 Programmer's Guide

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Abstract

The MAX77680/MAX77681 provide highly integrated power supply solutions for low-power applications where size and efficiency are critical. The MAX77680/MAX77681 device data sheet provides the complete hardware and electrical description for these devices. This Programmer's Guide focuses on the register map for the devices and provides general advice for programmers.

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1 OTP Options

Each register table that appears within this programmer's guide has a column for the register default value. If the default value is fixed for all versions of this device, then the value appears as "0" or "1." If the default value is one-time factory programmable (OTP), it varies depending on the version of device you are using and is listed as "x." See the "OTP Registers Quick Reference Table" to determine the default values for a given device.

2 OTP Registers Quick Reference Table

	MAX77680AEWV	**MAX77681A**EWV
CID	0x0	0x0
DIDM	0x0	0x01
SBIA_LPM_DEF	normal mode	normal mode
DBEN_nEN	30ms	30ms
MRT_OTP	8s reset	8s reset
IP_SBB0	1.0A	1.0A
TV_SBB0	1.8V	1.8V
EN_SBB0	FPS slot 1	FPS slot 1
ADE_SBB0	enabled	enabled
IP_SBB1	1.0A	1.0A
TV_SBB1	1.2V	3.3V
EN_SBB1	FPS slot 0	FPS slot 3
ADE_SBB1	enabled	enabled
IP_SBB2	1.0A	1.0A
TV_SBB2	3.3V	5.0V
EN_SBB2	FPS slot 3	FPS slot 0
ADE_SBB2	enabled	enabled

3 Register Reset Conditions

3.1 System Power-On Reset Comparator (POR)

The SYS POR comparator monitors V_{SYS} and generates a power-on reset signal (POR). When V_{SYS} is below V_{POR}, the device is held in reset (SYSRST = 1). When V_{SYS} rises above V_{POR}, internal signals and on-chip memory stabilize and the device is released from reset (SYSRST = 0).

3.2 System Reset (SYSRST)

The majority of the registers within the device have the reset condition of SYSRST = 1. The SYSRST signal is created by the “On/Off Controller” logic and is continuously high when the system voltage is lower than the power-on reset threshold ($V_{SYS}<V_{POR}$). Additionally, SYSRST is pulsed high to reset the registers during the on/off controller’s “immediate shutdown” routine and “power-down sequence” routine (refer to the IC data sheet’s *On/Off Controller* section for more information).

4 Baseline Initialization

Each time the system's microprocessor boots, execute initialization code for the device per the following guidelines:

A) To maximize performance, set the main bias circuits to operate in normal power mode (SBIA_LPM = 0).
   a. See the *Managing Main-Bias Circuits* section for more information.
B) The default ONKEY style is for push-button. If your system is using a slide-switch style ONKEY, then set nEN_MODE = 1.
C) The default ONKEY debounce time is factory programmable with OTP. If your system prefers a time that is different that the factory programmed value program DBEN_nEN accordingly.
D) Read the DIDM[1:0] and CID[2:0] to make sure that the correct version of the device is installed in your hardware.
   a. This version checking routine is highly recommended to catch any issues during the manufacturing process. For example, some manufacturers stock multiple versions of this device and this step help protect against any mixing of the stock.
E) Read the ERCFLAG register and take any necessary actions based on its information.
F) Read the interrupt and status registers INT_GLBL, STAT_GLBL and take any necessary actions based on their information.
G) Set interrupt mask INT_GLBLM as desired.
H) Configure the active discharge bits per your preference: ADE_SBB0, ADE_SBB1, ADE_SBB2.
I) To maximize efficiency, program the SIMO drive strength to the highest setting (DRV_SBB = 0b00).
   a. If noise issues appear in the system, experiment with slower setting options.
J) Adjust the SIMO current limits per your systems output current requirements (IP_SBB0[1:0], IP_SBB1[1:0], IP_SBB2[1:0]).
   a. Note that it is generally recommended to keep the SIMO current limits as low as possible. See the *Managing SIMO Current Limits* section for more information.
K) To get the best quiescent current performance, set the main bias circuits to operate in low-power mode (SBIA_LPM = 1) before finishing the initialization routine.

5 Managing SIMO Current Limits (IP_SBBx)

The available output current on a given SIMO channel is a function of the input voltage, the output voltage, the peak current limit setting, and the output current of the other SIMO channels. Maxim offers a SIMO calculator that outlines the available capacity for specific conditions. Visit the product page at www.maximintegrated.com/MAX77680 for more information on support documents.

Generally speaking, applications should use the lowest possible SIMO peak current limit for a given mode of operation. Lower SIMO peak current settings give better efficiency, lower output voltage ripple, and lower noise. For example, if a system has increasing power states of OFF>>HIBERNATE>>STANDBY>> ACTIVE, then it is recommended to tailor the SIMO current limits for the power needs of each particular state. HIBERNATE can use 500mA for each SIMO channel, STANDBY can use 0.866A, 0.707A, and 0.5A for SIMO SBB0, SBB1, and SBB2, while ACTIVE can use 1A for each SIMO channel. Once again, see the SIMO calculator for guidance on how to size the current limits for a given set of power needs.

6 Managing Main-Bias Circuits (SBIA_LPM)

1) Applications that are not concerned about quiescent current can leave the main-bias circuits in their normal-power mode indefinitely (SBIA_LPM = 0).
2) Applications that are concerned about quiescent current and want to have a simple software structure can leave the main-bias circuits in their low-power mode indefinitely (SBIA_LPM = 1).
3) Applications that want to maximize performance and have low quiescent current should dynamically control the main-bias circuits (SBIA_LPM).
    a) To maximize performance, set the main bias circuits to operate in normal power mode (SBIA_LPM = 0) whenever the system is doing a significant task. A tasks' significance is judged according to how much quiescent current is consumed current is consumed by the system in order to accomplish that task relative to the quiescent current of the MAX77680/81 when it is in its low-power mode. Since the MAX77680/81 consumes ~3.0µA when all resources are enabled and its bias circuits in are low-power mode, then any task that is expected to consume more than ~2mA is significant.
    b) To get the best quiescent current performance, set the main bias circuits to operate in low-power mode (SBIA_LPM = 1) whenever the system's current consumption is less than ~2mA.

7 Changing Regulator Output Voltages

The regulator output voltages are programmable. When a regulator is off, the output voltage can be directly programmed. However, when the regulator is on and the output voltage needs to be increased or decrease program a voltage ramp from the existing voltage to the new desired voltage. Programming a ramp is recommended for voltage increases to minimize inrush current. Programming a ramp is recommended on voltage decreases to minimize regulator undershoot when it reaches its target voltage.

Example 1: Enabling a regulator to a static output voltage

1. When the regulator is disabled, program the output voltage to the desired value.
2. To maximize performance, set the main bias circuits to operate in normal-power mode. (SBIA_LPM = 0), wait 100us afterwards for the bias circuits to settle (not really needed but still a good idea).
3. Turn the regulator on.
4. To get the best quiescent current performance, wait for 2ms for the regulator to stabilize (enable delay + soft-start ramp + margin), and then program the main bias circuits to operate in low-power mode (SBIA_LPM = 1).

Example 2: Ramping a regulator output voltage while it is enabled

1. To maximize performance, set the main bias circuits to operate in normal-power mode (SBIA_LPM = 0), wait 100us afterwards for the bias circuits to settle (not really needed but still a good idea).
2. Ramp the regulator output voltage one LSB at a time (increasing or decreasing) until the target voltage is reached.
    a. Note that for all regulators except the MAX77681 SBB1 the target voltage code tables are linear so, to step one LSB at a time, software can simply increment or decrement the bitfield value. However, for the MAX77681 SBB1, the code table is not linear and software should ensure that the output voltage is being stepped 50mV at a time. See Section 8.2.7 *MAX77681 TV_SBB1 Code Table* for more information.
3. To get the best quiescent current performance, wait for 2ms for the regulator to stabilize (enable delay + soft-start ramp + margin), and then program the main bias circuits to operate in low-power mode (SBIA_LPM = 1).

8 Register Description

The following tables detail the registers for the MAX77680/MAX77681. Undocumented register locations are reserved.

8.1 Register Descriptions: Top Level/ Global Resources

8.1.1 CNFG_GLBL

Register Name	CNFG_GLBL
I2C Slave Address	function of ADDR OTP bit
Register Address	0x10
Reset Value (HEX)	OTP
Reset Value (BIN)	0b00x00x00
Reset Condition	SYSRST = 1
Access Type	Mixed
Register Type	Configuration

<table>
<tr><th>Bit</th><th>Default</th><th>Bit Name</th><th>Description</th><th>Reset</th><th>Access Type</th></tr>
<tr><td>7</td><td>0</td><td>RESERVED</td><td>Reserved. Unutilized bit. Write to 0. Reads are don't care.</td><td>SYSRST = 1</td><td>R/W</td></tr>
<tr><td>6</td><td>0</td><td>BOK</td><td>Main Bias Okay Status Bit
0 = Main Bias not ready.
1 = Main Bias enabled and ready.</td><td>SYSRST = 1</td><td>R</td></tr>
<tr><td>5</td><td>x</td><td>SBIA_LPM</td><td>Main Bias Low-Power Mode software request
0 = Main Bias requested to be in Normal Power Mode by software.
1 = Main Bias request to be in Low Power Mode by software.</td><td>SYSRST = 1</td><td>R/W</td></tr>
<tr><td>4</td><td>0</td><td>SBIA_EN</td><td>Main Bias Enable Software Request
0 = Main Bias not enabled by software. Note that the main bias can be on via the on/off controller circuitry.
1 = Main Bias force enabled by software</td><td>SYSRST = 1</td><td>R/W</td></tr>
<tr><td>3</td><td>0</td><td>nEN_MODE</td><td>nEN Input (ONKEY) Default Configuration Mode
0 = Push-Button Mode
1 = Slide-Switch Mode</td><td>SYSRST = 1</td><td>R/W</td></tr>
<tr><td>2</td><td>x</td><td>DBEN_nEN</td><td>Debounce Timer Enable for the nEN Pin
0 = 100us Debounce
1 = 30ms Debounce</td><td>SYSRST = 1</td><td>R/W</td></tr>
<tr><td>1</td><td>0</td><td rowspan="2">SFT_RST[1:0]</td><td rowspan="2">Software Reset Functions. See the "On/Off Controller" section of the datasheet for more information.
0b00 = No Action
0b01 = Software Cold Reset (SFT_CRST). The device powers down, resets, and the powers up again.
0b10 = Software Off (SFT_OFF). The device powers down, resets, and then remains off and waiting for a wakeup event.
0b11 = Reserved

Note that unlike most every other I2C write in this device that happens virtually immediately after the I2C acknowledge, the ST_CRST and SFT_OFF commands go through the power down sequence flow as described in the datasheet. This power down sequence flow has delay elements that add up to 205.24ms (60ms delay + 10.24ms nRST assert delay + 4x2.56ms power down slot delays + 125ms output discharge delay). If issuing the SFT_CRST and/or SFT_OFF functions in software, wait for >300ms before trying to issue any additional commands via I2C.</td><td>SYSRST = 1</td><td>R/W</td></tr>
<tr><td>0</td><td>0</td><td>SYSRST = 1</td><td>R/W</td></tr>
</table>

8.1.2 INT_GLBL

Register Name	INT_GLBL
I2C Slave Address	function of ADDR OTP bit
Register Address	0x00
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Condition	SYSRST = 1
Access Type	RC
Register Type	Interrupt

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	RC
6	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	RC
5	0	TJAL2_R	Thermal Alarm 2 Rising Interrupt 0 = The junction temperature has not risen above TJAL2 since the last time this bit was read. 1 = The junction temperature has risen above TAJAL2 since the last time this bit was read.	SYSRST = 1	RC
4	0	TJAL1_R	Thermal Alarm 1 Rising Interrupt 0 = The junction temperature has not risen above TJAL1 since the last time this bit was read. 1 = The junction temperature has risen above TAJAL1 since the last time this bit was read.	SYSRST = 1	RC
3	0	nEN_R	nEN Rising Interrupt 0 = No nEN rising edges have occurred since the last time this bit was read. 1 = A nEN rising edge as occurred since the last time this bit was read.	SYSRST = 1	RC
2	0	nEN_F	nEN Falling Interrupt 0 = No nEN falling edges have occurred since the last time this bit was read. 1 = A nEN falling edge as occurred since the last time this bit was read.	SYSRST = 1	RC
1	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	RC
0	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	RC

8.1.3 INTM_GLBL

Register Name	INTM_GLBL
I2C Slave Address	function of ADDR OTP bit
Register Address	0x06
Reset Value (HEX)	0xFF
Reset Value (BIN)	0b11111111
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Interrupt Mask

Bit	Default	Bit Name	Description	Reset	Access Type
7	1	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W
6	1	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W
5	1	TJAL2_RM	Thermal Alarm 2 Rising Interrupt Mask 0 = Unmasked. If TJAL2_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to TJAL2_R.	SYSRST = 1	R/W
4	1	TJAL1_RM	Thermal Alarm 1 Rising Interrupt Mask 0 = Unmasked. If TJAL1_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to TJAL1_R.	SYSRST = 1	R/W
3	1	nEN_RM	nEN Rising Interrupt Mask 0 = Unmasked. If nEN_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to nEN_R.	SYSRST = 1	R/W
2	1	nEN_FM	nEN Falling Interrupt Mask 0 = Unmasked. If nEN_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to nEN_F.	SYSRST = 1	R/W
1	1	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W
0	1	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W

8.1.4 STAT_GLBL

Register Name	STAT_GLBL
I2C Slave Address	function of ADDR OTP bit
Register Address	0x05
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxx000000
Reset Condition	SYSRST = 1
Access Type	R
Register Type	Status

Bit	Default	Bit Name	Description	Reset
7	x	DIDM[1:0]	Device Identification Bits for Metal Options: 0b00 = MAX77680 0b01 = MAX7781 0b10 = Reserved for future use 0b11 = Reserved for future use	SYSRST = 1
6	x			SYSRST = 1
5	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1
4	0	TJAL2_S	Thermal Alarm 2 Status 0 = The junction temperature is less than TJA2 1 = The junction temperature is greater than TJAL2	SYSRST = 1
3	0	TJAL1_S	Thermal Alarm 1 Status 0 = The junction temperature is less than TJAL1 1 = The junction temperature is greater than TJAL1	SYSRST = 1
2	0	STAT_EN	Debounced Status for the nEN input. 0=nEN0 is not active (logic-high) 1=nEN0 is active (logic-low)	SYSRST = 1
1	0	STAT_PWR_HLD	PWR_HLD Input Debounced Status 0 = Logic-low 1 = Logic-high	SYSRST = 1
0	0	STAT_IRQ	Software Version of the nIRQ MOSFET gate drive. 0 = unmasked gate drive is logic-low 1 = unmasked gate drive is logic-high	SYSRST = 1

8.1.5 ERCFLAG

Register Name	ERCFLAG
I2C Slave Address	function of ADDR OTP bit
Register Address	0x04
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Condition	POR = 1
Access Type	RC
Register Type	Status

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	POR = 1	RC
6	0	PWR_HLD_RST	PWR_HLD Reset 0= A Reset has not occurred due to PWR_HLD2 deassertion since this last read of this register. 1= A Reset has occurred due to PWR_HLD2 deassertion since this last read of this register.	POR = 1	RC
5	0	SFT_CRST_F	Software Cold Reset Flag 0 = The software cold reset has not occurred since the last read of this register. 1 = The software cold reset has occurred since the last read of this register. This indicates that software has set SFT_RST = 0b01.	POR = 1	RC
4	0	SFT_OFF_F	Software Off Flag 0 = The SFT_OFF function has not occurred since the last read of this register. 1 = The SFT_OFF function has occurred since the last read of this register. This indicates that software has set SFT_RST = 0b10.	POR = 1	RC
3	0	MRST	Manual Reset Timer 0 = A Manual Reset has not occurred since this last read of this register. 1 = A Manual Reset has occurred since this last read of this register.	POR = 1	RC
2	0	SYSUVLO	SYS Domain Undervoltage Lockout 0 = The SYS domain undervoltage lockout has not occurred since this last read of this register. 1 = The SYS domain undervoltage lockout has occurred since the last read of this register. This indicates that the SYS domain voltage fell below VSYSUVLO (~2.4V)	POR = 1	RC
1	0	SYSOVLO	SYS Domain Overvoltage Lockout 0 = The SYS domain overvoltage lockout has not occurred since this last read of this register. 1 = The SYS domain overvoltage lockout has occurred since the last read of this register. This indicates that the SYS domain voltage rose below VSYSOVLO (~5.85V)	POR = 1	RC
0	0	TOVLD	Thermal Overload 0 = The thermal overload has not occurred since the last read of this register. 1 = The thermal overload has occurred since the list read of this register. This indicates that the junction temperature has exceeded 165C.	POR = 1	RC

8.1.6 CID

Register Name	CID
I2C Slave Address	function of ADDR OTP bit
Register Address	0x11
Reset Value (HEX)	OTP
Reset Value (BIN)	0b0xxxxxxx
Reset Condition	PORB
Access Type	R
Register Type	Data

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	PORB	R
6	x	CLKS[2:0]	Sampling Clock Frequency. This 3-bit configuration is for Maxim internal use only and controls a clock divider to set the internal sampling frequency of the global resources. 0b011 = 160Hz 0b100 = 80Hz 0b101 = 40Hz 0b110 = 20Hz 0b111 = 10Hz	PORB	R
5	x			PORB	R
4	x			PORB	R
3	x	CID[3:0]	Chip Identification Code. These bits track the OTP configuration. The value is register corresponds to a set of reset values in the register map.	PORB	R
2	x			PORB	R
1	x			PORB	R
0	x			PORB	R

8.2 Register Descriptions: SIMO Buck Boost

8.2.1 CNFG_SBB_TOP

Register Name	CNFG_SBB_TOP
I2C Slave Address	function of ADDR OTP bit
Register Address	0x28
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxxxxxxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	RESERVED	Reserved. Unutilized bit. Write to 0. Reads are don't care.	SYSRST = 1	R/W
6	x	MRT_OTP	Manual Reset Time Configuration 0 = the manual reset time (t_{MRST}) is typically 16s 1 = The manual reset time (t_{MRST}) is typically 8s Note that the default value of this bit controls the manual reset time. This bit can be written to its alternate value but does not change the manual reset time configuration. When writing to this register, it is recommended to leave this bit in its default configuration.	SYSRST = 1	R/W
5	x	SBIA_LPM_DEF	Default voltage of the SBIA_LPM bit 0 = SBIA_LPM defaults to 0 which gives the normal power mode 1 = SBIA_LPM defaults to 1 which gives the low power mode Note that the default value of this bit controls the default value of SBIA_LPM. This bit can be written to its alternate value but does not change the bias power mode. If software needs to change the bias power mode, it should program the SBIA_LPM bit directly. When writing to this register, it is recommended to leave this bit in its default configuration.	SYSRST = 1	R/W
4	x	DBNC_nEN_DEF	Default Value of the DBNC_nEN bit 0 = DBNC_nEN defaults to 0 which gives a 100us nEN debounce time 1 = DBNC_nEN defaults to 1 which gives a 30ms nEN debounce time Note that the default value of this bit controls the default value of DBNC_nEN. This bit can be written to its alternate value but does not change the nEN debounce time. If software needs to change the DBNC_nEN debounce time, it should program the DBNC_nEN bit directly. When writing to this register, it is recommended to leave this bit in its default configuration.	SYSRST = 1	R/W
3	x	RESERVED	Reserved. These bits are reserved. Write to 0x00.	SYSRST = 1	R/W
2	x			SYSRST = 1	R/W

1	x	DRV_SBB[1:0]	SIMO Buck-Boost (all channels) Drive Strength Trim. The ideal value of this register should be determined experimentally for each platform. The 0b01 setting is the best setting for a PCB layout that is comparable to Maxim's own EVKIT and represents a balance between efficiency and EMI. The faster setting can result in higher efficiency but generally requires a tighter EVKIT layout or shielding to avoid addition EMI. Slower settings allow for controlling EMI in non-ideal setting (i.e., contained layout, antenna adjacent to device, etc.). This setting is intended to be set once by the initialization code within a system. 0b00 = fastest transition time 0b01 = a little slower than 0b00 0b10 = a little slower than 0b01 0b11 = a little slower than 0b10	SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

8.2.2 CNFG_SBB0_A

Register Name	CNFG_SBB0_A
I2C Slave Address	function of ADDR OTP bit
Register Address	0x29
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxxxxxxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	IP_SBB0[1:0]	SIMO Buck-Boost Channel 1 Peak Current Limit 0b00 = 1.000A 0b01 = 0.866A 0b10 = 0.707A 0b11 = 0.500A	SYSRST = 1	R/W
6	x			SYSRST = 1	R/W
5	x	TV_SBB0[5:0]	SIMO Buck-Boost Channel 0 Target Output Voltage This 6-bit configuration is a linear transfer function that starts at 0.8V, ends at 2.375V, with 25mV increments. See the "TV_SBB0 Code Table" section in this document for a complete table of values.	SYSRST = 1	R/W
4	x			SYSRST = 1	R/W
3	x			SYSRST = 1	R/W
2	x			SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

8.2.3 TV_SBB0 Code Table

0x00=0b000000=0.800V	0x10=0b010000=1.200V	0x20=0b100000=1.600V	0x30=0b110000=2.000V
0x01=0b000001=0.825V	0x11=0b010001=1.225V	0x21=0b100001=1.625V	0x31=0b110001=2.025V
0x02=0b000010=0.850V	0x12=0b010010=1.250V	0x22=0b100010=1.650V	0x32=0b110010=2.050V
0x03=0b000011=0.875V	0x13=0b010011=1.275V	0x23=0b100011=1.675V	0x33=0b110011=2.075V
0x04=0b000100=0.900V	0x14=0b010100=1.300V	0x24=0b100100=1.700V	0x34=0b110100=2.100V
0x05=0b000101=0.925V	0x15=0b010101=1.325V	0x25=0b100101=1.725V	0x35=0b110101=2.125V
0x06=0b000110=0.950V	0x16=0b010110=1.350V	0x26=0b100110=1.750V	0x36=0b110110=2.150V
0x07=0b000111=0.975V	0x17=0b010111=1.375V	0x27=0b100111=1.775V	0x37=0b110111=2.175V
0x08=0b001000=1.000V	0x18=0b011000=1.400V	0x28=0b101000=1.800V	0x38=0b111000=2.200V
0x09=0b001001=1.025V	0x19=0b011001=1.425V	0x29=0b101001=1.825V	0x39=0b111001=2.225V
0x0A=0b001010=1.050V	0x1A=0b011010=1.450V	0x2A=0b101010=1.850V	0x3A=0b111010=2.250V
0x0B=0b001011=1.075V	0x1B=0b011011=1.475V	0x2B=0b101011=1.875V	0x3B=0b111011=2.275V
0x0C=0b001100=1.100V	0x1C=0b011100=1.500V	0x2C=0b101100=1.900V	0x3C=0b111100=2.300V
0x0D=0b001101=1.125V	0x1D=0b011101=1.525V	0x2D=0b101101=1.925V	0x3D=0b111101=2.325V
0x0E=0b001110=1.150V	0x1E=0b011110=1.550V	0x2E=0b101110=1.950V	0x3E=0b111110=2.350V
0x0F=0b001111=1.175V	0x1F=0b011111=1.575V	0x2F=0b101111=1.975V	0x3F=0b111111=2.375V

8.2.4 CNFG_SBB0_B

Register Name	CNFG_SBB0_B
I2C Slave Address	function of ADDR OTP bit
Register Address	0x2A
Reset Value (HEX)	OTP
Reset Value (BIN)	0b0000xxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
6	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
5	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
4	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
3	x	ADE_SBB0	SIMO Buck-Boost Channel 0 Active-Discharge Enable 0 = The active discharge function is disabled. When SBB0 is disabled, it's discharge rate is a function of the output capacitance and the external load. 1 = The active discharge function is enabled. When SBB0 is disabled, an internal resistor (R_{AD_SBB0}) is activated from SBB0 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB0} load.	SYSRST = 1	R/W
2	x	EN_SBB0[2:0]	Enable Control for SIMO Buck-Boost Channel 0. 0b000 = SBB0 powers-up and powers-down in FPS slot 0 0b001 = SBB0 powers-up and powers-down in FPS slot 1 0b010 = SBB0 powers-up and powers-down in FPS slot 2 0b011 = SBB0 powers-up and powers-down in FPS slot 3 0b100 = SBB0 is off irrespective of FPS 0b101 = same as 0b100 0b110 = SBB0 is on irrespective of FPS whenever the on/off controller is in its "On via Software" or "On via On/Off Controller" states. 0b111 = same as 0b110 Prior to enabling the SIMO, program the bias circuits to normal power mode (SBIA_LPM = 0). After the SIMO is enabled, the bias circuits can be programmed back to low power mode (SBIA_LPM = 1) to decrease quiescent current.	SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

8.2.5 CNFG_SBB1_A

Register Name	CNFG_SBB1_A
I2C Slave Address	function of ADDR OTP bit
Register Address	0x2B
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxxxxxxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	IP_SBB1[1:0]	SIMO Buck-Boost Channel 1 Peak Current Limit 0b00 = 1.000A 0b01 = 0.866A 0b10 = 0.707A 0b11 = 0.500A	SYSRST = 1	R/W
6	x			SYSRST = 1	R/W
5	x	TV_SBB1[5:0]	SIMO Buck-Boost Channel 1 Target Output Voltage This 6-bit configuration adjusts the MAX77680 from 0.8V to 1.5875V in 12.5mV increments with B0 = LSB and B5 = MSB. The MAX77681 adjustment range is from 2.4V to 2.55V in 50mV increments **but the LSB and MSB locations are not standard**. See the "MAX77681 TV_SBB1 Code Table" section in this document for a complete table of values.	SYSRST = 1	R/W
4	x			SYSRST = 1	R/W
3	x			SYSRST = 1	R/W
2	x			SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

8.2.6 MAX77680 TV_SBB1 Code Table

0x00=0b000000=0.8000V	0x10=0b010000=1.0000V	0x20=0b100000=1.2000V	0x30=0b110000=1.4000V
0x01=0b000001=0.8125V	0x11=0b010001=1.0125V	0x21=0b100001=1.2125V	0x31=0b110001=1.4125V
0x02=0b000010=0.8250V	0x12=0b010010=1.0250V	0x22=0b100010=1.2250V	0x32=0b110010=1.4250V
0x03=0b000011=0.8375V	0x13=0b010011=1.0375V	0x23=0b100011=1.2375V	0x33=0b110011=1.4375V
0x04=0b000100=0.8500V	0x14=0b010100=1.0500V	0x24=0b100100=1.2500V	0x34=0b110100=1.4500V
0x05=0b000101=0.8625V	0x15=0b010101=1.0625V	0x25=0b100101=1.2625V	0x35=0b110101=1.4625V
0x06=0b000110=0.8750V	0x16=0b010110=1.0750V	0x26=0b100110=1.2750V	0x36=0b110110=1.4750V
0x07=0b000111=0.8875V	0x17=0b010111=1.0875V	0x27=0b100111=1.2875V	0x37=0b110111=1.4875V
0x08=0b001000=0.9000V	0x18=0b011000=1.1000V	0x28=0b101000=1.3000V	0x38=0b111000=1.5000V
0x09=0b001001=0.9125V	0x19=0b011001=1.1125V	0x29=0b101001=1.3125V	0x39=0b111001=1.5125V
0x0A=0b001010=0.9250V	0x1A=0b011010=1.1250V	0x2A=0b101010=1.3250V	0x3A=0b111010=1.5250V
0x0B=0b001011=0.9375V	0x1B=0b011011=1.1375V	0x2B=0b101011=1.3375V	0x3B=0b111011=1.5375V
0x0C=0b001100=0.9500V	0x1C=0b011100=1.1500V	0x2C=0b101100=1.3500V	0x3C=0b111100=1.5500V
0x0D=0b001101=0.9625V	0x1D=0b011101=1.1625V	0x2D=0b101101=1.3625V	0x3D=0b111101=1.5625V
0x0E=0b001110=0.9750V	0x1E=0b011110=1.1750V	0x2E=0b101110=1.3750V	0x3E=0b111110=1.5750V
0x0F=0b001111=0.9875V	0x1F=0b011111=1.1875V	0x2F=0b101111=1.3875V	0x3F=0b111111=1.5875V

8.2.7 MAX77681 TV_SBB1 Code Table

B[5:2] / B[1:0]	0b0000	0b0001	0b0010	0b0011	0b0100	0b0101	0b0110	0b0111	0b1000	0b1001	0b1010	0b1011	0b1100	0b1101	0b1110	0b1111
0b00	2.40	2.45	2.50	2.55	2.60	2.65	2.70	2.75	2.80	2.85	2.90	2.95	3.00	3.05	3.10	3.15
0b01	3.20	3.25	3.30	3.35	3.40	3.45	3.50	3.55	3.60	3.65	3.70	3.75	3.80	3.85	3.90	3.95
0b10	4.00	4.05	4.10	4.15	4.20	4.25	4.30	4.35	4.40	4.45	4.50	4.55	4.60	4.65	4.70	4.75
0b11	4.80	4.85	4.90	4.95	5.00	5.05	5.10	5.15	5.20	5.25	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

The above transfer function is nonlinear. See Figure 1 and Figure 2 for code examples for managing the above transfer function.

```
def max77681_sbb1_code_to_voltage(self, code):
        lsb = 0.05
        base_0 = 2.40
        base_1 = 3.20
        base_2 = 4.00
        base_3 = 4.80

        code_1_0 = code & 0b11 # extract 2 lsb

        if code_1_0 == 0b00:
                voltage = base_0
        elif code_1_0 == 0b01:
                voltage = base_1
        elif code_1_0 == 0b10:
                voltage = base_2
        else:
                voltage = base_3
                code_5_2 = (code >> 2) & 0b1111 # extract bit 5 to 2
        voltage = voltage + code_5_2 * lsb
        return voltage
```

Figure 1. Python procedure to convert the MAX77681 SBB1 code to voltage

```
def max77681_sbb1_voltage_to_code(self, voltage):
        lsb = 0.05
        base_0 = 2.40
        base_1 = 3.20
        base_2 = 4.00
        base_3 = 4.80

        if voltage >= base_3:
                TV_SBB1_1_0 = 0b11
                TV_SBB1_5_2 = int(round((voltage-base_3)/lsb))
        elif voltage >= base_2:
                TV_SBB1_1_0 = 0b10
                TV_SBB1_5_2 = int(round((voltage-base_2)/lsb))
        elif voltage >= base_1:
                TV_SBB1_1_0 = 0b01
                TV_SBB1_5_2 = int(round((voltage-base_1)/lsb))
        else:
                TV_SBB1_1_0 = 0b00
                TV_SBB1_5_2 = int(round((voltage-base_0)/lsb))
        code = (TV_SBB1_5_2 << 2) + TV_SBB1_1_0
        return code
```

Figure 2. Python procedure to convert the MAX77681 SBB1 voltage to code

8.2.8 CNFG_SBB1_B

Register Name	CNFG_SBB1_B
I2C Slave Address	function of ADDR OTP bit
Register Address	0x2C
Reset Value (HEX)	OTP
Reset Value (BIN)	0b0000xxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
6	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
5	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
4	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
3	x	ADE_SBB1	SIMO Buck-Boost Channel 1 Active-Discharge Enable 0 = The active discharge function is disabled. When SBB1 is disabled, it's discharge rate is a function of the output capacitance and the external load. 1 = The active discharge function is enabled. When SBB1 is disabled, an internal resistor (R_{AD_SBB1}) is activated from SBB1 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB1} load.	SYSRST = 1	R/W
2	x	EN_SBB1[2:0]	Enable Control for SIMO Buck-Boost Channel 1. 0b000 = SBB1 powers-up and powers-down in FPS slot 0 0b001 = SBB1 powers-up and powers-down in FPS slot 1 0b010 = SBB1 powers-up and powers-down in FPS slot 2 0b011 = SBB1 powers-up and powers-down in FPS slot 3 0b100 = SBB1 is off irrespective of FPS 0b101 = same as 0b100 0b110 = SBB1 is on irrespective of FPS whenever the on/off controller is in its "On via Software" or "On via On/Off Controller" states. 0b111 = same as 0b110 Prior to enabling the SIMO, program the bias circuits to normal power mode (SBIA_LPM = 0). After the SIMO is enabled, the bias circuits can be programmed back to low power mode (SBIA_LPM = 1) to decrease quiescent current.	SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

8.2.9 CNFG_SBB2_A

Register Name	CNFG_SBB2_A
I2C Slave Address	function of ADDR OTP bit
Register Address	0x2D
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxxxxxxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	IP_SBB2[1:0]	SIMO Buck-Boost Channel 1 Peak Current Limit 0b00 = 1.000A 0b01 = 0.866A 0b10 = 0.707A 0b11 = 0.500A	SYSRST = 1	R/W
6	x			SYSRST = 1	R/W
5	x	TV_SBB2[5:0]	SIMO Buck-Boost Channel 2 Target Output Voltage This 6-bit configuration is a linear transfer function that starts at 0.8V, ends at 3.95V, with 50mV increments for the MAX77680. For the MAX77681, the transfer function starts ad 2.4V, ends at 3.95V, with 50mV increments. See the "TV_SBB2 Code Table" section in this document for a complete table of values.	SYSRST = 1	R/W
4	x			SYSRST = 1	R/W
3	x			SYSRST = 1	R/W
2	x			SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

8.2.10 MAX77680 TV_SBB2 Code Table

0x00=0b000000=0.80V	0x10=0b010000=1.60V	0x20=0b100000=2.40V	0x30=0b110000=3.20V
0x01=0b000001=0.85V	0x11=0b010001=1.65V	0x21=0b100001=2.45V	0x31=0b110001=3.25V
0x02=0b000010=0.90V	0x12=0b010010=1.70V	0x22=0b100010=2.50V	0x32=0b110010=3.30V
0x03=0b000011=0.95V	0x13=0b010011=1.75V	0x23=0b100011=2.55V	0x33=0b110011=3.35V
0x04=0b000100=1.00V	0x14=0b010100=1.80V	0x24=0b100100=2.60V	0x34=0b110100=3.40V
0x05=0b000101=1.05V	0x15=0b010101=1.85V	0x25=0b100101=2.65V	0x35=0b110101=3.45V
0x06=0b000110=1.10V	0x16=0b010110=1.90V	0x26=0b100110=2.70V	0x36=0b110110=3.50V
0x07=0b000111=1.15V	0x17=0b010111=1.95V	0x27=0b100111=2.75V	0x37=0b110111=3.55V
0x08=0b001000=1.20V	0x18=0b011000=2.00V	0x28=0b101000=2.80V	0x38=0b111000=3.60V
0x09=0b001001=1.25V	0x19=0b011001=2.05V	0x29=0b101001=2.85V	0x39=0b111001=3.65V
0x0A=0b001010=1.30V	0x1A=0b011010=2.10V	0x2A=0b101010=2.90V	0x3A=0b111010=3.70V
0x0B=0b001011=1.35V	0x1B=0b011011=2.15V	0x2B=0b101011=2.95V	0x3B=0b111011=3.75V
0x0C=0b001100=1.40V	0x1C=0b011100=2.20V	0x2C=0b101100=3.00V	0x3C=0b111100=3.80V
0x0D=0b001101=1.45V	0x1D=0b011101=2.25V	0x2D=0b101101=3.05V	0x3D=0b111101=3.85V
0x0E=0b001110=1.50V	0x1E=0b011110=2.30V	0x2E=0b101110=3.10V	0x3E=0b111110=3.90V
0x0F=0b001111=1.55V	0x1F=0b011111=2.35V	0x2F=0b101111=3.15V	0x3F=0b111111=3.95V

8.2.11 MAX77681 TV_SBB2 Code Table

0x00=0b000000=2.40V	0x10=0b010000=3.20V	0x20=0b100000=4.00V	0x30=0b110000=4.80V
0x01=0b000001=2.45V	0x11=0b010001=3.25V	0x21=0b100001=4.05V	0x31=0b110001=4.85V
0x02=0b000010=2.50V	0x12=0b010010=3.30V	0x22=0b100010=4.10V	0x32=0b110010=4.90V
0x03=0b000011=2.55V	0x13=0b010011=3.35V	0x23=0b100011=4.15V	0x33=0b110011=4.95V
0x04=0b000100=2.60V	0x14=0b010100=3.40V	0x24=0b100100=4.20V	0x34=0b110100=5.00V
0x05=0b000101=2.65V	0x15=0b010101=3.45V	0x25=0b100101=4.25V	0x35=0b110101=5.05V
0x06=0b000110=2.70V	0x16=0b010110=3.50V	0x26=0b100110=4.30V	0x36=0b110110=5.10V
0x07=0b000111=2.75V	0x17=0b010111=3.55V	0x27=0b100111=4.35V	0x37=0b110111=5.15V
0x08=0b001000=2.80V	0x18=0b011000=3.60V	0x28=0b101000=4.40V	0x38=0b111000=5.20V
0x09=0b001001=2.85V	0x19=0b011001=3.65V	0x29=0b101001=4.45V	0x39=0b111001=5.25V
0x0A=0b001010=2.90V	0x1A=0b011010=3.70V	0x2A=0b101010=4.50V	0x3A=0b111010=RSVD
0x0B=0b001011=2.95V	0x1B=0b011011=3.75V	0x2B=0b101011=4.55V	0x3B=0b111011=RSVD
0x0C=0b001100=3.00V	0x1C=0b011100=3.80V	0x2C=0b101100=4.60V	0x3C=0b111100=RSVD
0x0D=0b001101=3.05V	0x1D=0b011101=3.85V	0x2D=0b101101=4.65V	0x3D=0b111101=RSVD
0x0E=0b001110=3.10V	0x1E=0b011110=3.90V	0x2E=0b101110=4.70V	0x3E=0b111110=RSVD
0x0F=0b001111=3.15V	0x1F=0b011111=3.95V	0x2F=0b101111=4.75V	0x3F=0b111111=RSVD

8.2.12 CNFG_SBB2_B

Register Name	CNFG_SBB2_B
I2C Slave Address	function of ADDR OTP bit
Register Address	0x2E
Reset Value (HEX)	OTP
Reset Value (BIN)	0b0000xxxx
Reset Condition	SYSRST = 1
Access Type	R/W
Register Type	Configuration

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
6	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
5	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
4	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	SYSRST = 1	R/W
3	x	ADE_SBB2	SIMO Buck-Boost Channel 2 Active-Discharge Enable 0 = The active discharge function is disabled. When SBB2 is disabled, it's discharge rate is a function of the output capacitance and the external load. 1 = The active discharge function is enabled. When SBB2 is disabled, an internal resistor (R_{AD_SBB2}) is activated from SBB2 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB2} load.	SYSRST = 1	R/W
2	x	EN_SBB2[2:0]	Enable Control for SIMO Buck-Boost Channel 2. 0b000 = SBB2 powers-up and powers-down in FPS slot 0 0b001 = SBB2 powers-up and powers-down in FPS slot 1 0b010 = SBB2 powers-up and powers-down in FPS slot 2 0b011 = SBB2 powers-up and powers-down in FPS slot 3 0b100 = SBB2 is off irrespective of FPS 0b101 = same as 0b100 0b110 = SBB2 is on irrespective of FPS whenever the on/off controller is in its "On via Software" or "On via On/Off Controller" states. 0b111 = same as 0b110 Prior to enabling the SIMO, program the bias circuits to normal power mode (SBIA_LPM = 0). After the SIMO is enabled, the bias circuits can be programmed back to low power mode (SBIA_LPM = 1) to decrease quiescent current.	SYSRST = 1	R/W
1	x			SYSRST = 1	R/W
0	x			SYSRST = 1	R/W

9 Revision History

REV NUMBER	REV DATE	DESCRIPTION	PAGES CHANGED
0	9/17	Initial release	—