LM111JAN Voltage Comparator

Check for Samples: LM111JAN

FEATURES

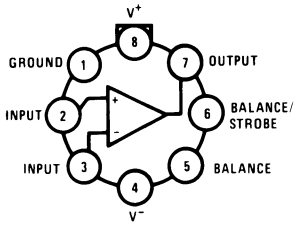
- **Operates from Single 5V Supply**
- **Input Current: 200 nA max. Over Temperature**
- **Offset Current: 20 nA max. Over Temperature**
- **Differential Input Voltage Range: ±30V**
- **Power Consumption: 135 mW at ±15V**
- **Power Supply Voltage, single 5V to ±15V**
- **Offset Voltage Null Capability**
- **Strobe Capability**

DESCRIPTION

The LM111 is a voltage comparator that has input currents nearly a thousand times lower than devices such as the LM106 or LM710. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. The output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

Connection Diagrams



Note: Pin 4 connected to case

Figure 1. Metal Can Package
Top View
See Package Number LMC0008C

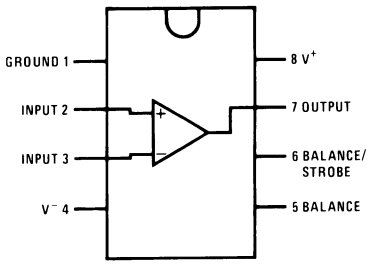


Figure 2. Dual-In-Line Package
Top View
See Package Number NAB0008A

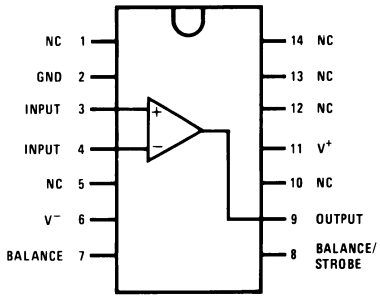


Figure 3. Dual-In-Line Package
Top View
See Package Number J0014A

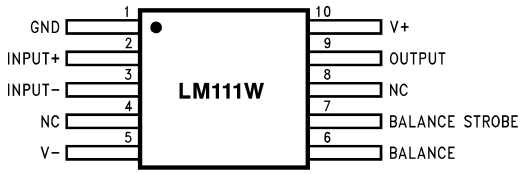
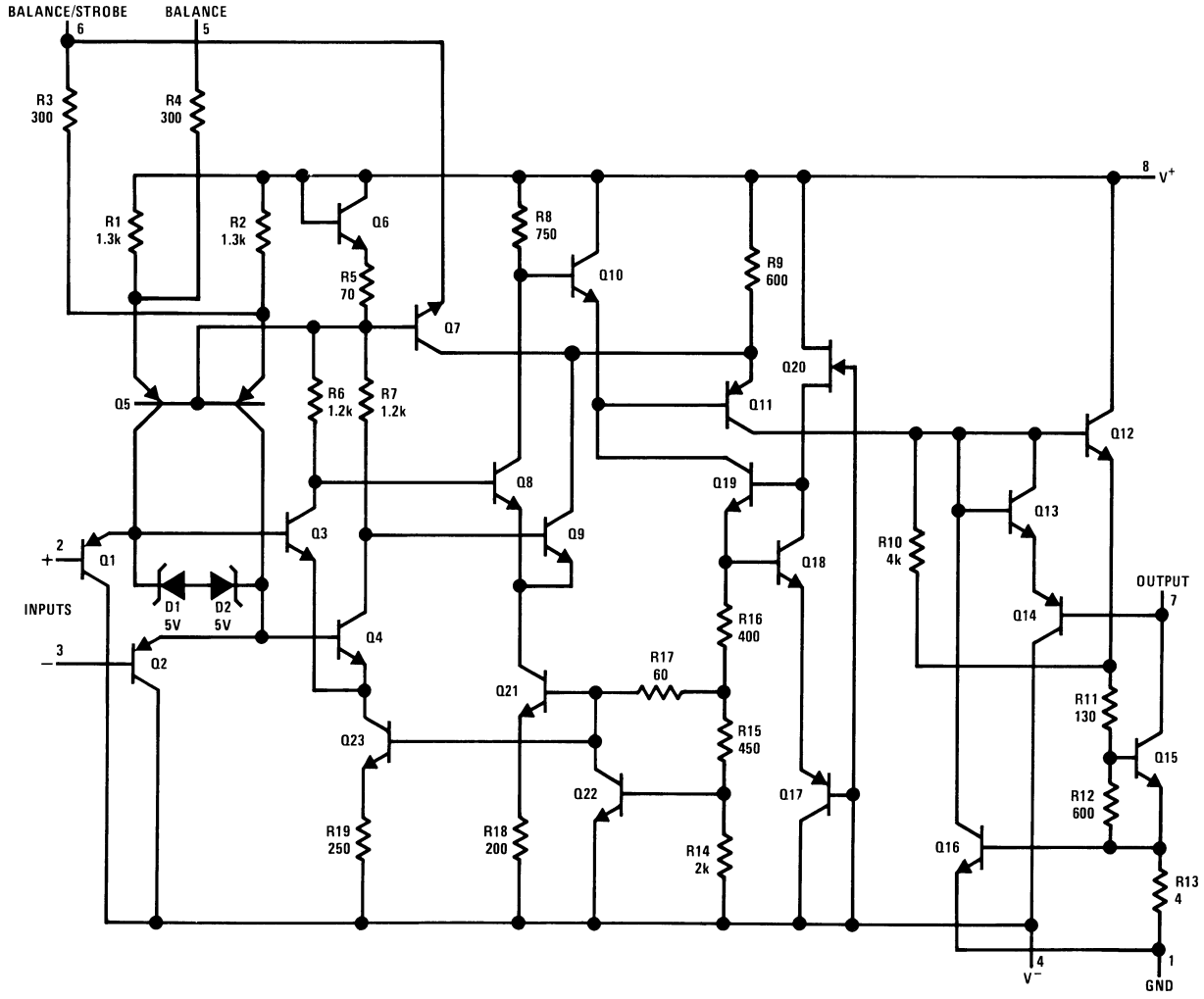


Figure 4. See Package Number NAD0010A, NAC0010A

Schematic Diagram



Note: Pin connections shown on schematic diagram are for LMC0008C package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Positive Supply Voltage			+30.0V
Negative Supply Voltage			-30.0V
Total Supply Voltage			36V
Output to Negative Supply Voltage			50V
GND to Negative Supply Voltage			30V
Differential Input Voltage			±30V
Sink Current			50mA
Input Voltage(2)			±15V
Power Dissipation(3)		8 LD CERDIP	400mW @ 25°C
		8 LD Metal Can	330mW @ 25°C
		10 LD CERPACK	330mW @ 25°C
		10 LD Ceramic SOIC	330mW @ 25°C
		14 LD CERDIP	400mW @ 25°C
Output Short Circuit Duration			10 seconds
Maximum Strobe Current			10mA
Operating Temperature Range			$-55°C \le T_A \le 125°C$
Thermal Resistance	θ_{JA}	8 LD CERDIP (Still Air @ 0.5W)	120°C/W
		8 LD CERDIP (500LF/Min Air flow @ 0.5W)	76°C/W
		8 LD Metal Can (Still Air @ 0.5W)	150°C/W
		8 LD Metal Can (500LF/Min Air flow @ 0.5W)	92°C/W
		10 Ceramic SOIC (Still Air @ 0.5W)	231°C/W
		10 Ceramic SOIC (500LF/Min Air flow @ 0.5W)	153°C/W
		10 CERPACK (Still Air @ 0.5W)	231°C/W
		10 CERPACK (500LF/Min Air flow @ 0.5W)	153°C/W
		14 LD CERDIP (Still Air @ 0.5W)	120°C/W
		14 LD CERDIP (500LF/Min Air flow @ 0.5W)	65°C/W
	θ_{JC}	8 LD CERDIP	35°C/W
		8 LD Metal Can Pkg	40°C/W
		10 LD Ceramic SOIC	60°C/W
		10 LD CERPACK	60°C/W
		14 LD CERDIP	35°C/W
Storage Temperature Range			$-65°C \le T_A \le 150°C$
Maximum Junction Temperature			175°C
Lead Temperature (Soldering, 60 seconds)			300°C
Voltage at Strobe Pin			V^+ -5V
Package Weight (Typical)		8 LD Metal Can	965mg
		8 LD CERDIP	1100mg
		10 LD CERPACK	250mg
		10 LD Ceramic SOIC	225mg
		14 LD CERDIP	TBD
ESD Rating(4)			300V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) This rating applies for ±15V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(4) Human body model, 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions

Supply Voltage	$V_{CC} = \pm 15V_{DC}$
Operating Temperature Range	$-55°C \le T_A \le 125°C$

Quality Conformance Inspection

Mil-Std-883, Method 5005 — Group A

Subgroup	Description	Temperature (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

LM111 JAN Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified.
DC: $V_{CC} = \pm 15V$, $V_{CM} = 0$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$V_I = 0V$, $R_S = 50\Omega$		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC} = 29.5V$, $-V_{CC} = -0.5V$, $V_I = 0V$, $V_{CM} = -14.5V$, $R_S = 50\Omega$		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC} = 2V$, $-V_{CC} = -28V$, $V_I = 0V$, $V_{CM} = +13V$, $R_S = 50\Omega$		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC} = +2.5V$, $-V_{CC} = -2.5V$, $V_I = 0V$, $R_S = 50\Omega$		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
V_{IO} R	Raised Input Offset Voltage	$V_I = 0V$, $R_S = 50\Omega$	See (1)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		$+V_{CC} = 29.5V$, $-V_{CC} = -0.5V$, $V_I = 0V$, $V_{CM} = -14.5V$, $R_S = 50\Omega$	See (1)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		$+V_{CC} = 2V$, $-V_{CC} = -28V$, $V_I = 0V$, $V_{CM} = +13V$, $R_S = 50\Omega$	See (1)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
I_{IO}	Input Offset Current	$V_I = 0V$, $R_S = 50K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC} = 29.5V$, $-V_{CC} = -0.5V$, $V_I = 0V$, $V_{CM} = -14.5V$, $R_S = 50K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC} = 2V$, $-V_{CC} = -28V$, $V_I = 0V$, $V_{CM} = +13V$, $R_S = 50K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3

(1) Subscript (R) indicates tests which are performed with input stage current raised by connecting BAL and BAL/STB terminals to $+V_{CC}$.

LM111 JAN Electrical Characteristics DC Parameters (continued)

The following conditions apply, unless otherwise specified.

DC: V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$I_{IO}R$	Raised Input Offset Current	V_I = 0V, R_S = 50KΩ	See (1)	-25	+25	nA	1, 2
				-50	+50	nA	3
$±I_{IB}$	Input Bias Current	V_I = 0V, R_S = 50KΩ		-100	0.1	nA	1, 2
				-150	0.1	nA	3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
V_OSt	Collector Output Voltage (Strobe)	$+V_I$ = Gnd, $-V_I$ = 15V, I_{St} = -3mA, R_S = 50Ω	See (2)	14		V	1, 2, 3
CMRR	Common Mode Rejection	-28V ≤ $-V_{CC}$ ≤ -0.5V, R_S=50Ω, 2V ≤ $+V_{CC}$ ≤ 29.5V, R_S = 50Ω, -14.5V ≤ V_{CM} ≤ 13V,R_S = 50Ω		80		dB	1, 2, 3
V_{OL}	Low Level Output Voltage	$+V_{CC}$ = 4.5V, $-V_{CC}$ = Gnd, I_O = 8mA, $±V_I$ = 0.5V, V_{ID} = -6mV	See (3)		0.4	V	1, 2, 3
		$+V_{CC}$ = 4.5V, $-V_{CC}$ = Gnd, I_O = 8mA, $±V_I$ = 3V, V_{ID} = -6mV	See (3)		0.4	V	1, 2, 3
		I_O = 50mA, ±VI = 13V, V_{ID} = -5mV	See (3)		1.5	V	1, 2, 3
		I_O = 50mA, ±VI = -14V, V_{ID} = -5mV	See (3)		1.5	V	1, 2, 3
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, V_O = 32V		-1.0	10	nA	1
				-1.0	500	nA	2
I_{IL}	Input Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, $+V_I$ = +12V, $-V_I$ = -17V		-5.0	500	nA	1, 2, 3
		$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, $+V_I$ = -17V, $-V_I$ = +12V		-5.0	500	nA	1, 2, 3
$+I_{CC}$	Power Supply Current				6.0	mA	1, 2
					7.0	mA	3
$-I_{CC}$	Power Supply Current			-5.0		mA	1, 2
				-6.0		mA	3
Δ V_{IO} / Δ T	Temperature Coefficient Input Offset Voltage	25°C ≤ T ≤ 125°C	See (4)	-25	25	uV/°C	2
		-55°C ≤ T ≤ 25°C	See (4)	-25	25	uV/°C	3
Δ I_{IO} / Δ T	Temperature Coefficient Input Offset Current	25°C ≤ T ≤ 125°C	See (4)	-100	100	pA/°C	2
		-55°C ≤ T ≤ 25°C	See (4)	-200	200	pA/°C	3
I_{OS}	Short Circuit Current	V_O = 5V, t ≤ 10mS, $-V_I$ = 0.1V, $+V_I$ = 0V			200	mA	1
					150	mA	2
					250	mA	3
$+V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω		5.0		mV	1
$-V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω			-5.0	mV	1
$±A_{VE}$	Voltage Gain (Emitter)	R_L = 600Ω	See (5)	10		V/mV	4
			See (5)	8.0		V/mV	5, 6

(2) I_{ST} = −2mA at −55°C
(3) V_{ID} is voltage difference between inputs.
(4) Calculated parameter.
(5) Datalog reading in K=V/mV.

LM111 JAN Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.

AC: V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
tR_{LHC}	Response Time (Collector Output)	V_{OD}(Overdrive) = -5mV, C_L = 50pF, V_I = -100mV			300	nS	7, 8B
					640	nS	8A
tR_{HLC}	Response Time (Collector Output)	V_{OD}(Overdrive) = 5mV, C_L = 50pF, V_I = 100mV			300	nS	7, 8B
					500	nS	8A

LM111 JAN Electrical Characteristics DC Drift Parameters

The following conditions apply, unless otherwise specified.

DC: V_{CC} = ±15V, V_{CM} = 0

Delta calculations performed on JANS devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_I = 0V, R_S = 50Ω		-0.5	0.5	mV	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-0.5	0.5	mV	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-0.5	0.5	mV	1
$\pm I_{IB}$	Input Bias Current	V_I = 0V, R_S = 50KΩ		-12.5	12.5	nA	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-12.5	12.5	nA	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-12.5	12.5	nA	1
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, V_O = 32V		-5.0	5.0	nA	1

LM111 Typical Performance Characteristics

Input Bias Current

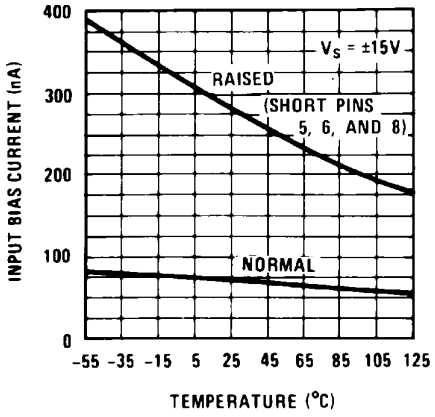


Figure 5.

Input Bias Current

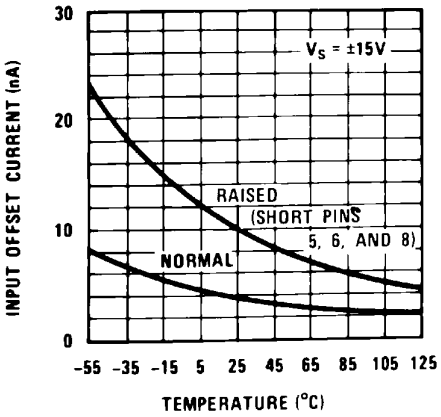


Figure 6.

Input Bias Current

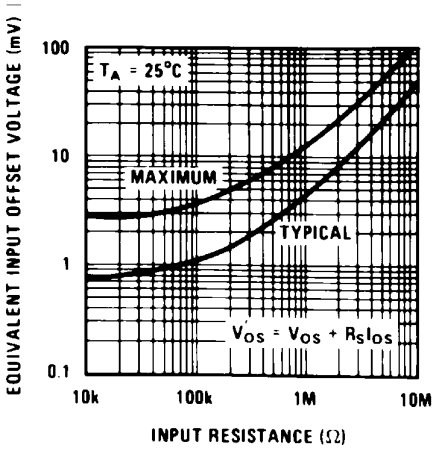


Figure 7.

Input Bias Current

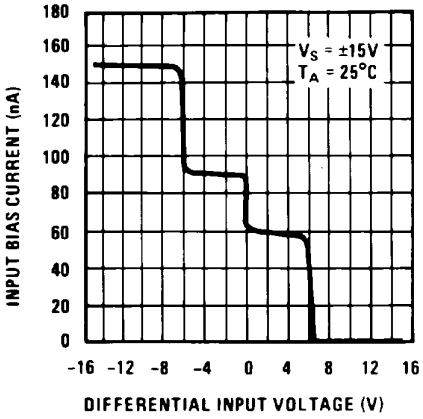


Figure 8.

Input Bias Current

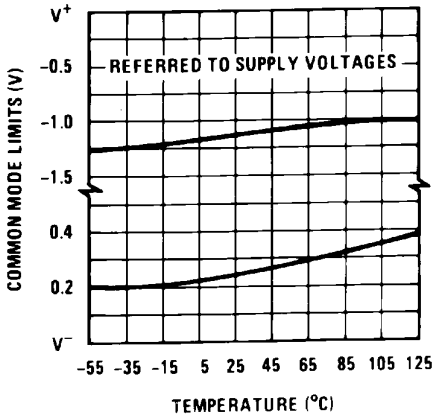


Figure 9.

Input Bias Current

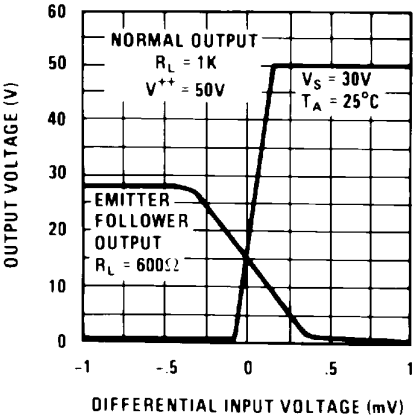


Figure 10.

LM111 Typical Performance Characteristics (continued)

Input Bias Current
Input Overdrives

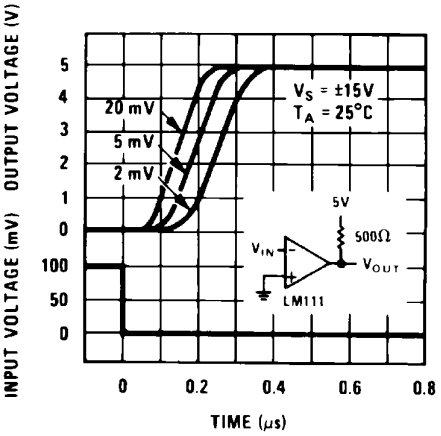


Figure 11.

Input Bias Current
Input Overdrives

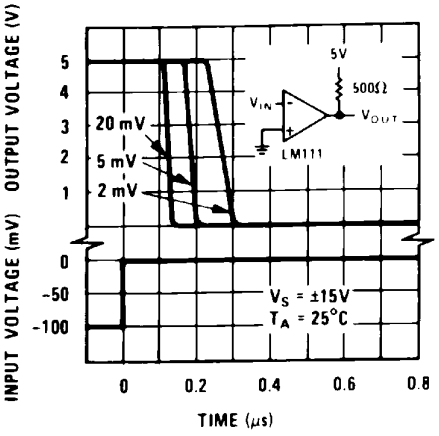


Figure 12.

Input Bias Current

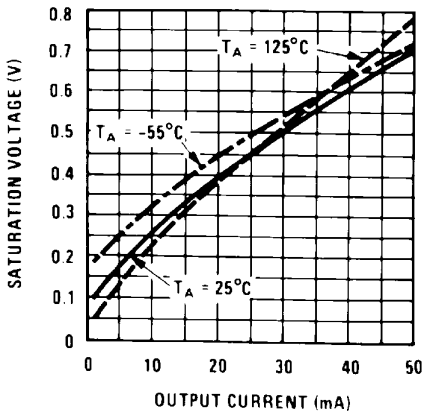


Figure 13.

Response Time for Various
Input Overdrives

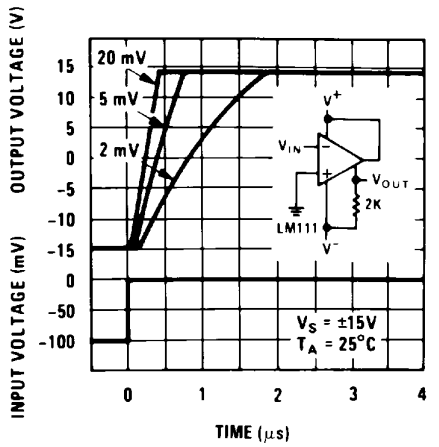


Figure 14.

Response Time for Various
Input Overdrives

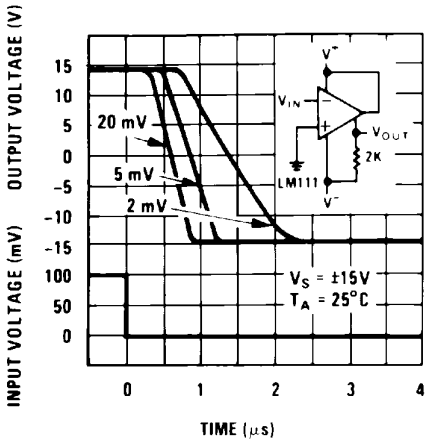


Figure 15.

Output Limiting Characteristics

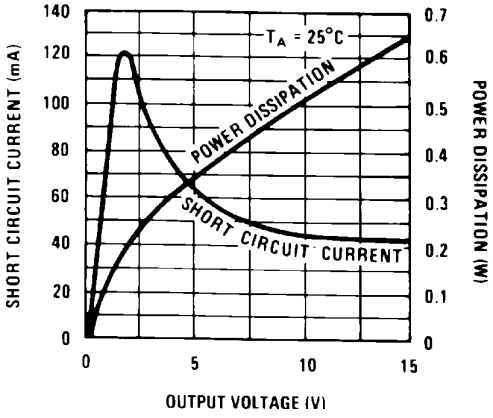


Figure 16.

LM111 Typical Performance Characteristics (continued)

Supply Current

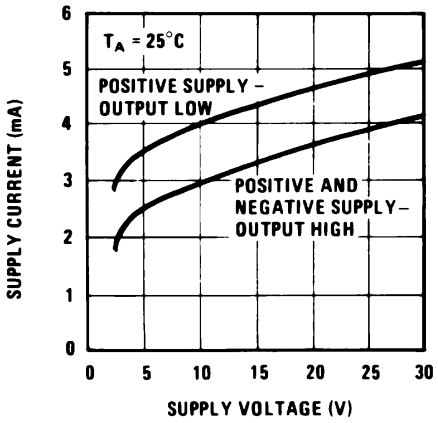


Figure 17.

Supply Current

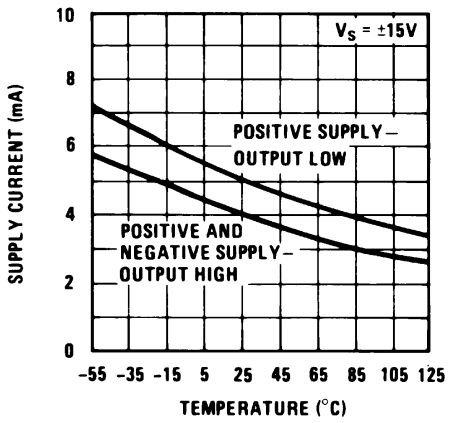


Figure 18.

Leakage Currents

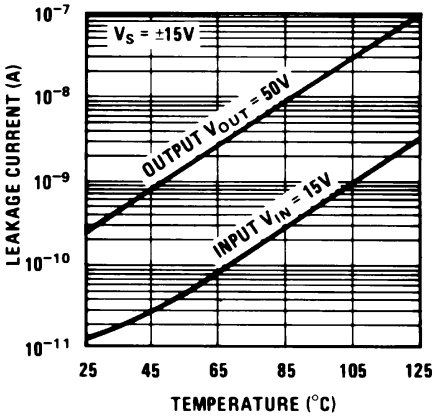


Figure 19.

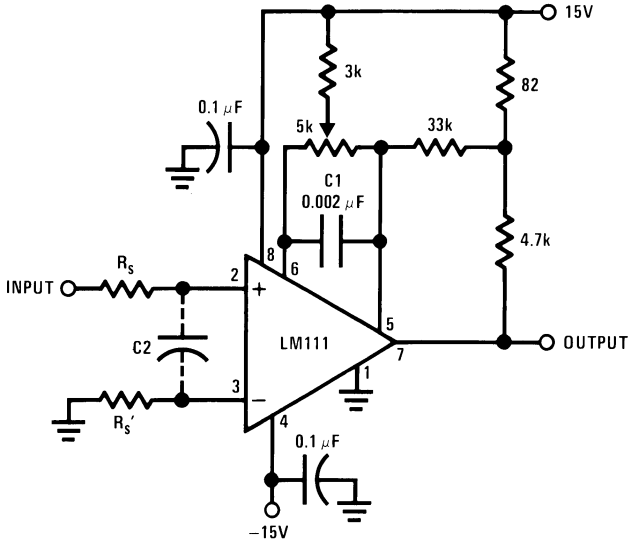
APPLICATION HINTS

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 µF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

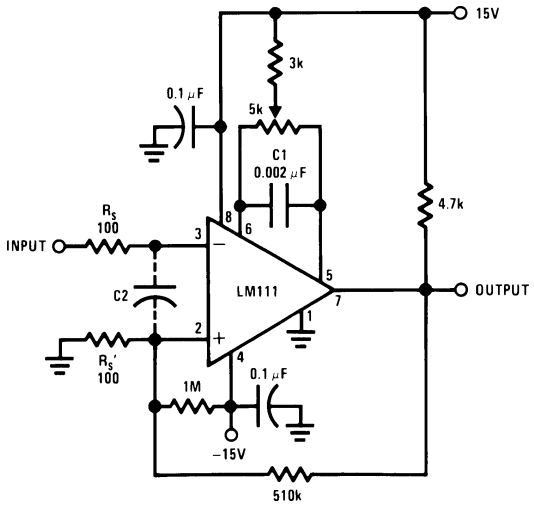
However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators such as the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 20 below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 µF capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in Figure 20.
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wire wound resistors are not suitable.
4. When comparator circuits use input resistors (e.g. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S=10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a ground plane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 µF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)
6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of Figure 21, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of Figure 22 could be used, but it is rather awkward. See the notes in paragraph 7 below.
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of Figure 20 is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.
8. These application notes apply specifically to the LM111 and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



Pin connections shown are for LM111H in the LMC0008C hermetic package

Figure 20. Improved Positive Feedback



Pin connections shown are for LM111H in the LMC0008C hermetic package

Figure 21. Conventional Positive Feedback

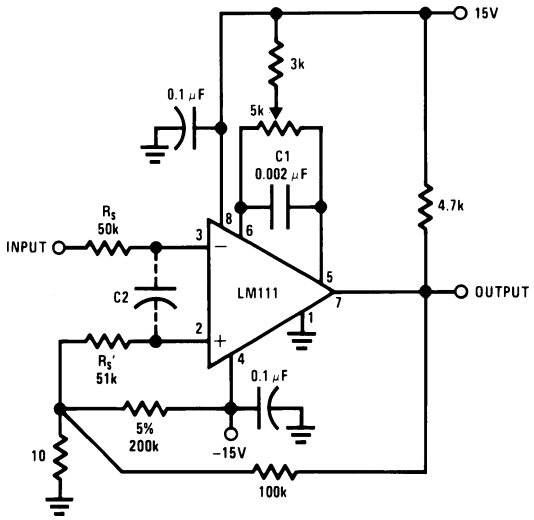


Figure 22. Positive Feedback with High Source Resistance

Typical Applications

Pin connections shown on schematic diagram and typical applications are for LMC0008C metal can package.

Offset Balancing

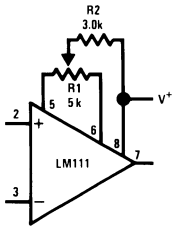
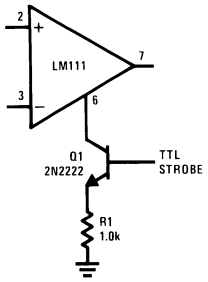


Figure 23.

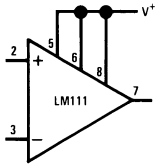
Strobing



Note: Do Not Ground Strobe Pin. Output is turned off when current is pulled from Strobe Pin.

Figure 24.

Increasing Input Stage Current



Note: Increases typical common mode slew from 7.0V/µs to 18V/µs.

Figure 25.

Detector for Magnetic Transducer

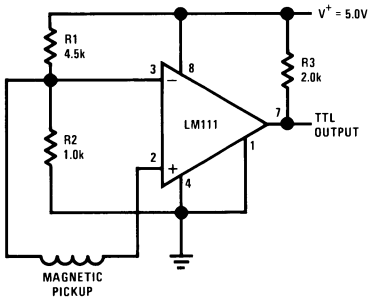


Figure 26.

Digital Transmission Isolator

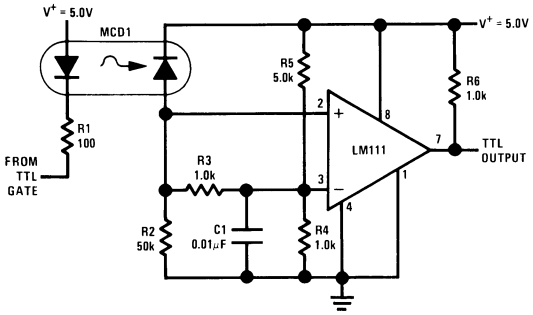
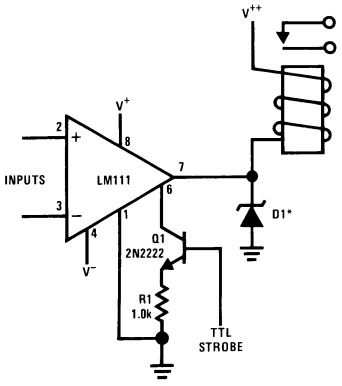


Figure 27.

Relay Driver with Strobe

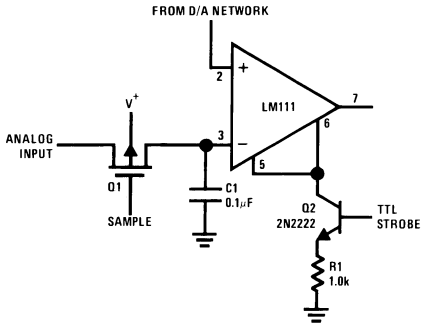


*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line.

Note: Do Not Ground Strobe Pin.

Figure 28.

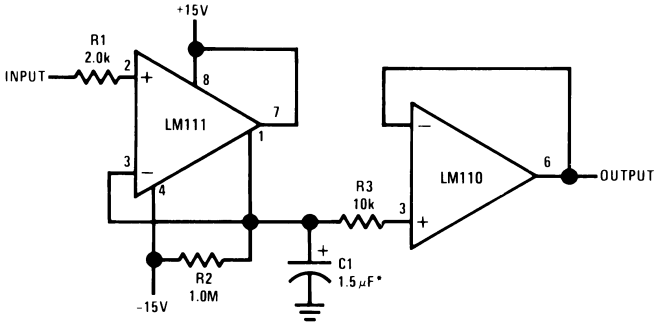
Strobing off Both Input and Output Stages



Note:Typical input current is 50 pA with inputs strobed off.

Figure 29.

Positive Peak Detector



*Solid tantalum

Figure 30.

Zero Crossing Detector Driving MOS Logic

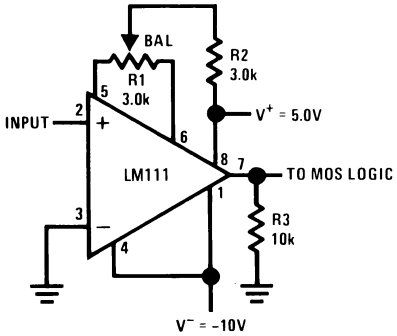


Figure 31.

Typical Applications

(Pin numbers refer to LMC0008C package)

Zero Crossing Detector Driving MOS Switch

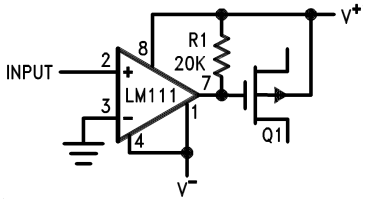
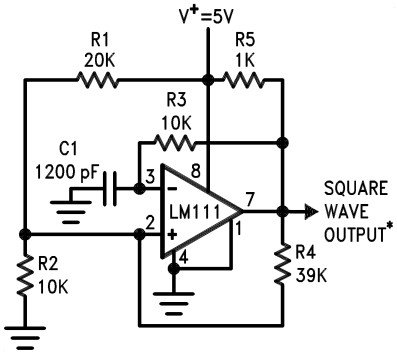


Figure 32.

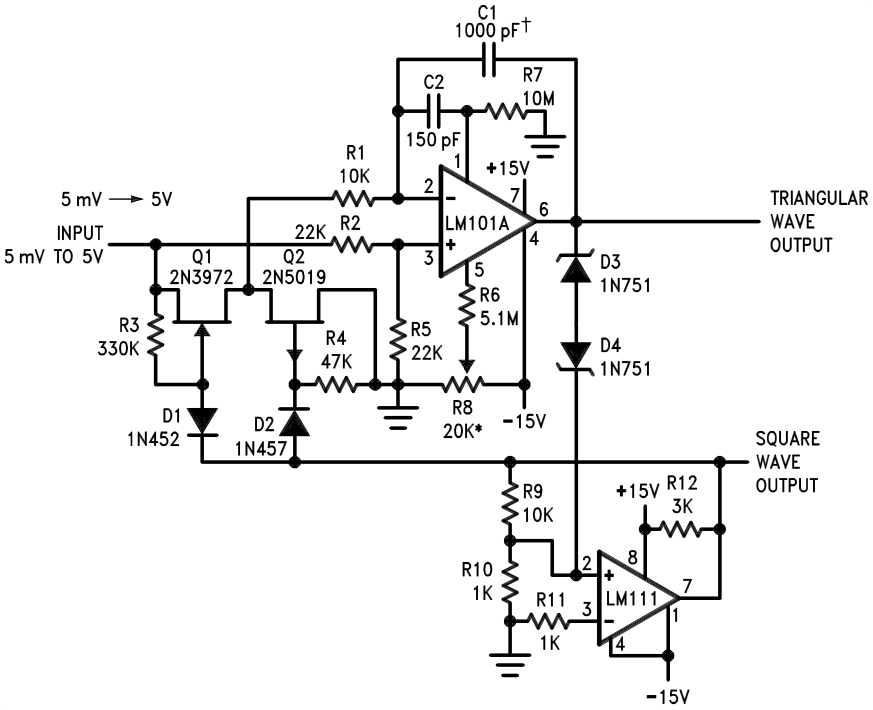
100 kHz Free Running Multivibrator



*TTL or DTL fanout of two

Figure 33.

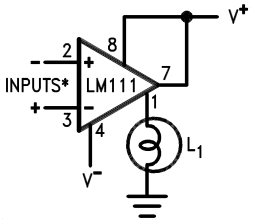
10 Hz to 10 kHz Voltage Controlled Oscillator



***Adjust for symmetrical square wave time when V_{IN} = 5 mV**
†Minimum capacitance 20 pF Maximum frequency 50 kHz

Figure 34.

Driving Ground-Referred Load



*Input polarity is reversed when using pin 1 as output.

Figure 35.

Using Clamp Diodes to Improve Response

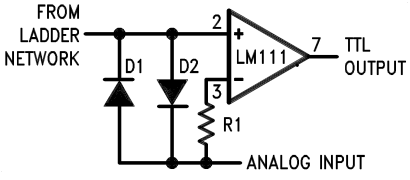
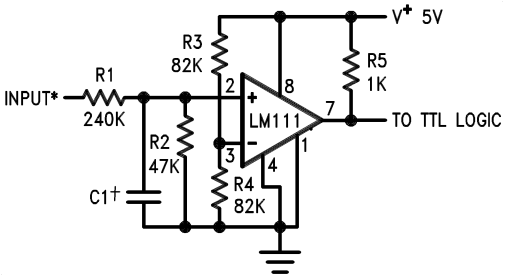


Figure 36.

TTL Interface with High Level Logic



***Values shown are for a 0 to 30V logic swing and a 15V threshold.**
†May be added to control speed and reduce susceptibility to noise spikes.

Figure 37.

Crystal Oscillator

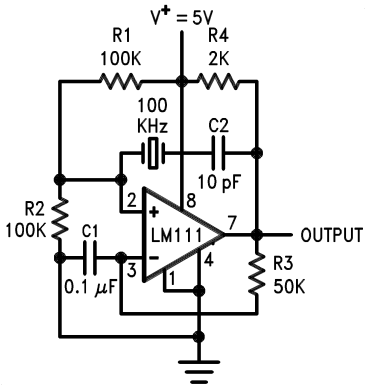


Figure 38.

Comparator and Solenoid Driver

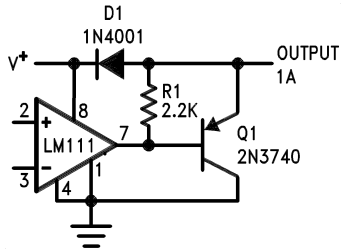
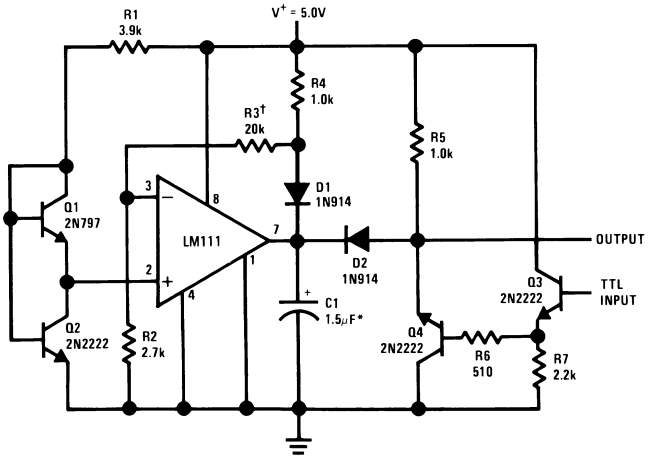


Figure 39.

Precision Squarer

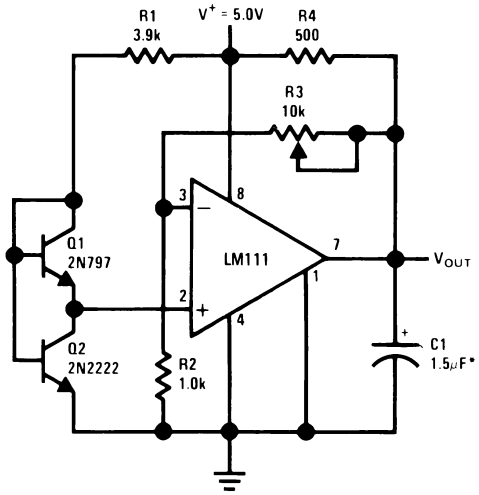


*Solid tantalum

†Adjust to set clamp level

Figure 40.

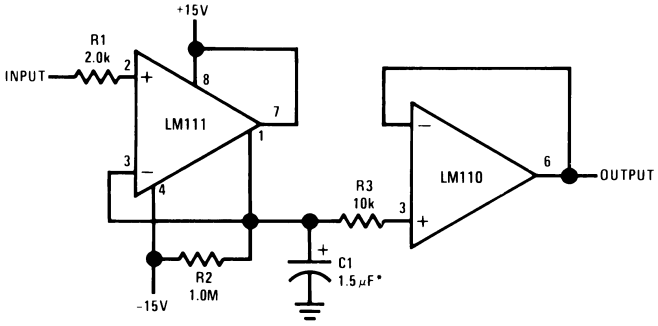
Low Voltage Adjustable Reference Supply



*Solid tantalum

Figure 41.

Positive Peak Detector



*Solid tantalum

Figure 42.

Zero Crossing Detector Driving MOS Logic

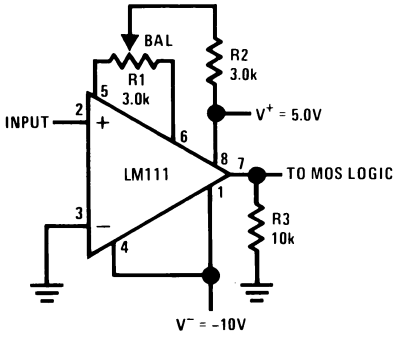
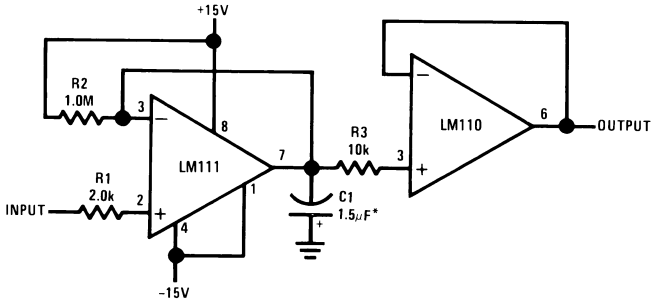


Figure 43.

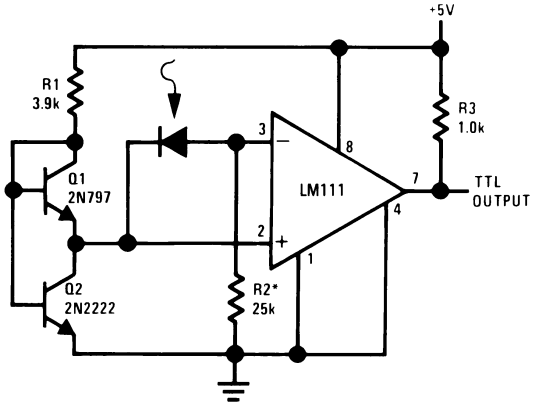
Negative Peak Detector



*Solid tantalum

Figure 44.

Precision Photodiode Comparator



*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

Figure 45.

Switching Power Amplifier

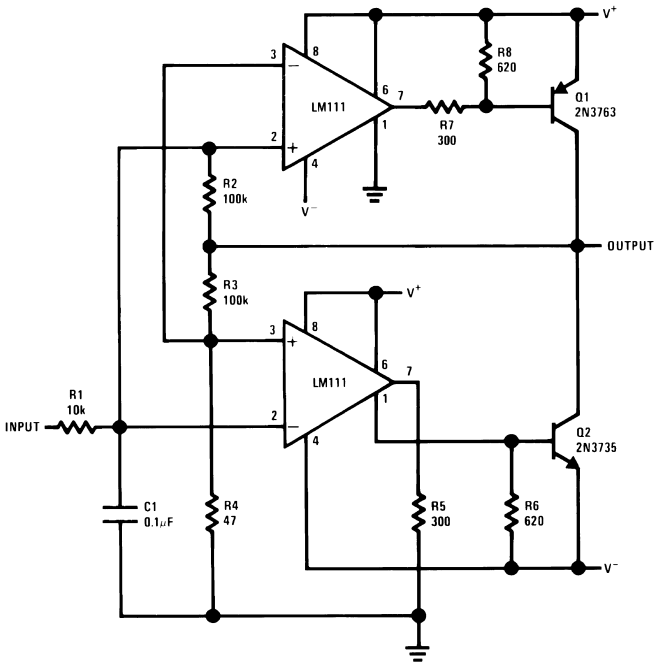


Figure 46.

Switching Power Amplifier

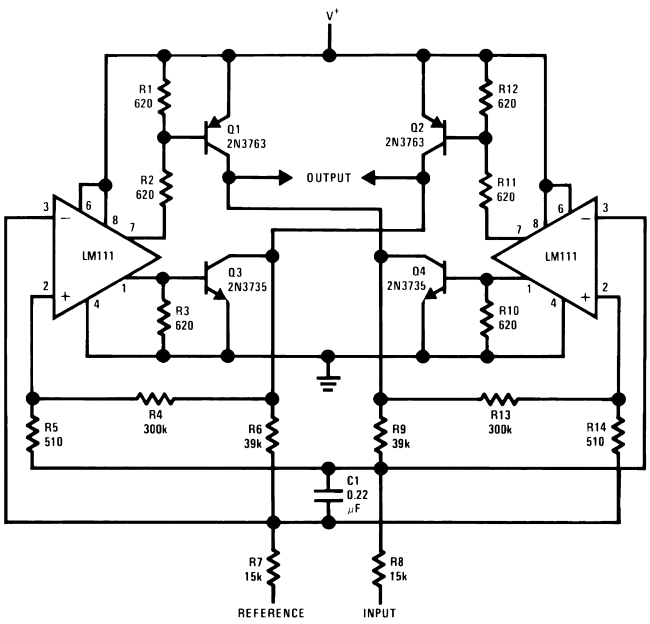


Figure 47.

REVISION HISTORY SECTION

Released	Revision	Section	Originator	Changes
05/09/05	A	New Release, Corporate format	L. Lytle	1 MDS data sheets converted into one Corp. data sheet format. MJLM111–X Rev 0D3 will be archived.
03/26/2013	B	All Sections		Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JL111BGA	ACTIVE	TO-99	LMC	8	20	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	JL111BGA JM38510/10304BGA Q ACO JM38510/10304BGA Q >T	Samples
JM38510/10304BGA	ACTIVE	TO-99	LMC	8	20	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	JL111BGA JM38510/10304BGA Q ACO JM38510/10304BGA Q >T	Samples
M38510/10304BGA	ACTIVE	TO-99	LMC	8	20	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	JL111BGA JM38510/10304BGA Q ACO JM38510/10304BGA Q >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

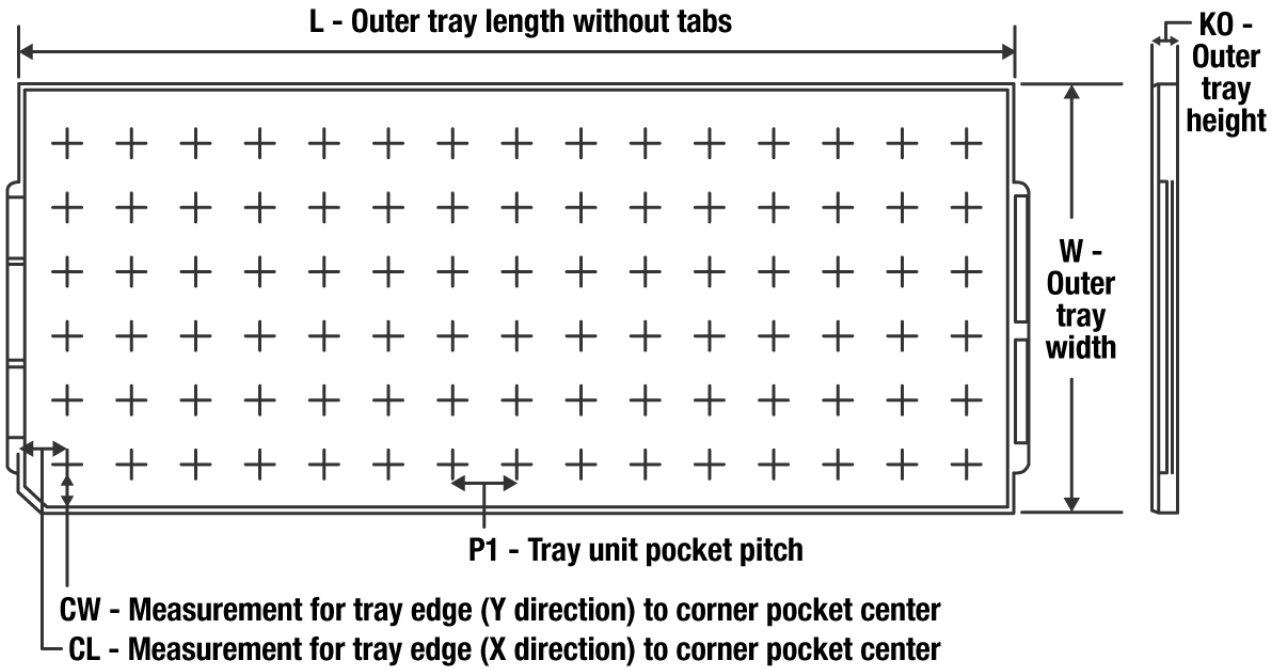
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY

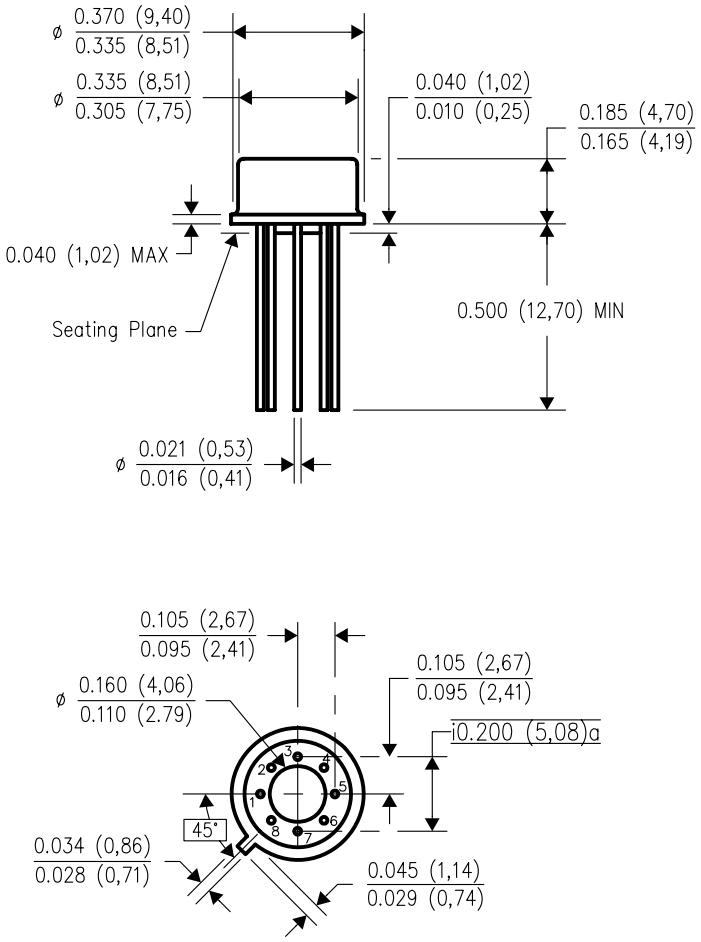


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
JL111BGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
JM38510/10304BGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54
M38510/10304BGA	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–002/TO–99.

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