PCN# 20211118000

No Availability of Spartan-6 FPGAs for:

MityDSP-L138(F) Modules

Date: November 18, 2021

To: Purchasing Agents & Design Engineers

Dear Customer,

This is an announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact the Hardware Manager Bill Halpin (bill.halpin@critiallink.com).

Sincerely,

Critical Link, LLC

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PCN Number: 20180402000

PCN Date: November 18, 2021

Title: No Availability of Spartan-6 FPGAs

Contact: Bill Halpin

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EOL Date: 12/21/2021

Overview

Changes to the MityDSP-L138F System on Modules are identified in the following sections.

1 Replace Spartan-6 FPGA with Artix-7 FPGA

1.1 Description of Change

Production for L138F variants using Xilinx Spartan-6 FPGAs will be discontinued as of January 1, 2022. Variants using the Spartan-6 FPGA will be replaced with variants instead using the Xilinx Artix-7 family of FPGAs.

1.2 Reason for Change

On November 5, 2021, Xilinx and its distributors advised Critical Link that the Spartan-6 family of FPGAs would no longer be available for purchase. The availability issue is due to the inability of the chip foundry that owns the required 46 nm fabrication process to meet the market demand. Critical Link has been advised to treat the Spartan-6 product essentially as if it had been declared obsolete and to design it out of any existing product.

In order to minimize impact on customers using the MityDSP-L138F, Critical Link has designed an updated variant of the module that will provide for an Artix-7 replacement of the Spartan-6 FPGA. The variant provides the same mechanical footprint and wherever possible maintains a common electrical interface with the goal to minimize impact to customer carrier card designs. Updated variants will leverage the XC7A15T-2CGS324 and the XC7A50T-2CSG324 Artix-7 devices, which should serve as suitable replacements for the XC6SLX16-2CSG324 and XC6SLX45-2CSG324 Spartan-6 devices, respectively.

See Table 2 Products Affected for a detailed list of suggested variant migration.

1.3 Anticipated Impact on Form, Fit, Function (positive / negative)

Mechanically, the Artix-7 variant board perimeter size, shape, and mounting interface will not change. Any change in weight should be negligible. It is not expected that there will be significant change to the performance of the Artix-7 based module for shock, vibration, or performance over temperature.

Electrically, the new variants have been designed to preserve as much of the current edge connector interface as possible with a goal to being fully compatible with existing carrier cards. No modifications to any pins were made except those connecting directly to the Spartan-6 device. Table 1 shows a comparison of the edge connector interface between the Spartan-6 based SOM and the Artix-7 based SOM. In a similar way as the original Spartan-6 design, the VCCO and IO pins from 2 banks (banks 15 and 35) from the Artix-7 were routed to the DDR edge

connector. As indicated in the table, the grouping of all but 4 of the IO pins was preserved as compared to the Spartan-7 variants. In addition, the FPGA_SUSPEND signal on pin 90 was made a no-connect as the Artix-7 does not support the SUSPEND operation.

Table 1 Changes to DDR Interface Connector

Pin	Signal	S6 Bank	A7 Bank	Pin	Signal	S6 Bank	A7 Bank
1	+3.3 V in			2	+3.3 V in		
3	+3.3 V in			4	+3.3 V in		
5	+3.3 V in			6	+3.3 V in		
7	GND			8	GND		
9	GND			10	GND		
11	RESET_IN#			12	EXT_BOOT#		
13	SATA_TX_P			14	GP0_7		
15	SATA_TX_N			16	GP0_10		
17	SATA_RX_P			18	GP0_11		
19	SATA_RX_N			20	GP0_15		
21	USB0_ID			22	GP0_6		
23	USB1_D_N			24	GP0_14		
25	USB1_D_P			26	GP0_12		
27	USB0_VBUS			28	GP0_5		
29	USB0_D_N			30	GP0_13		
31	USB0_D_P			32	GP0_1		
33	USB0_DRVVBUS			34	GP0_4		
35	3V RTC Battery			36	GP0_3		
37	+3.3 V in			38	+3.3 V in		
39	+3.3 V in			40	+3.3 V in		
41	GND			42	GND		
43	SPI1_MISO			44	GP0_2		
45	SPI1_MOSI			46	GP0_0		
47	SPI1_ENA			48	GP0_8		
49[1]	SPI1_CLK			50	GP0_9		
51	SPI1_SCS1			52	MMCSD0_DAT7		
53	Reserved			54	MMCSD0_DAT6		
55[2]	I2C0_SCL			56	MMCSD0_DAT5		
57[2]	I2C0_SDA			58	MMCSD0_DAT4		
59	UART2_TXD / I2C1_SDA			60	MMCSD0_DAT3		
61	UART2_RXD / I2C1_SCL			62	MMCSD0_DAT2		
63	GND			64	GND		
65	UART1_TXD			66	MMCSD0_DAT1		
67	UART1_RXD			68	MMCSD0_DAT0		
69	MDIO_CLK			70	MMCSD0_CMD		
71	MDIO_DAT			72	MMCSD0_CLK		
73	MII_RXCLK			74	MII_TXCLK		
75	MII_RXDV			76	MII_TXD3		
77	MII_RXD0			78	MII_TXD2		
79	MII_RXD1			80	MII_TXD1		
81	MII_RXD2			82	MII_TXD0		
83	MII_RXD3			84	MII_TXEN		

Pin	Signal	S6 Bank	A7 Bank	Pin	Signal	S6 Bank	A7 Bank
85	GND			86	GND		
87	MII_CRS			88	MII_COL		
89	MII_RXER			90	FPGA_SUSPEND – No Connect on Artix-7 Variant		
91	B1 _47_P	1	15	92	B1 _48_P	1	15
93	B1_ 47_N	1	15	94	B1_ 48_N	1	15
95	B1 _45_P	1	15	96	B1 _46_P	1	15
97	B1_ 45_N	1	15	98	B1_ 46_N	1	15
99	B1_43_P	1	15	100	B1 _44_P	1	15
101	B1_43_N	1	15	102	B1_ 44_N	1	15
103	B1_41_P	1	15	104	B1 _42_P	1	15
105	B1_41_N	1	15	106	B1_ 42_N	1	15
107	GND			108	GND		
109	B1_39_P	1	15	110	B1 _40_P	1	15
111	B1_39_N	1	15	112	B1_ 40_N	1	15
113	B1_37_P	1	15	114	B1 _38_P	1	15
115	B1_37_N	1	15	116	B1_ 38_N	1	15
117	B1_35_P	1	15	118	B1 _36_P	1	15
119	B1_35_N	1	15	120	B1_ 36_N	1	15
121	B1_33_P	1	15	122	B1 _34_P	1	15
123	B1_33_N	1	15	124	B1_ 34_N	1	15
125	B1_31_P	1	15	126	B1 _32_P	1	15
127	B1_31_N	1	15	128	B1_ 32_N	1	15
129	GND			130	GND		
131	B1_29_P	1	15	132	B1 _30_P	1	15
133	B1_29_N	1	15	134	B1_ 30_N	1	15
135	B1_27_P	1	15	136	B1 _28_P	1	15
137	B1_27_N	1	15	138	B1_ 28_N	1	15
139	B1_25_P	1	15	140	B1 _26_P	1	15
141	B1_25_N	1	15	142	B1_ 26_N	1	15
143	B1_23_P (bank grouping change)	1	35	144	B0 _24_P	0	35
145	B1_23_N (bank grouping change)	1	35	146	B0_ 24_N	0	35
147	B1_21_P (bank grouping change)	1	35	148	B0 _22_P	0	35
149	B1_21_N (bank grouping change)	1	35	150	B0_ 22_N	0	35
151	GND			152	GND		
153	B0_19_P	0	35	154[3]	B0 _20_P	0	35
155	B0_19_N	0	35	156[3]	B0_ 20_N	0	35
157	B0_17_P	0	35	158[3]	B0 _18_P	0	35
159	B0_17_N	0	35	160[3]	B0_ 18_N	0	35
161	B0_15_P	0	35	162[3]	B0 _16_P	0	35
163	B0_15_N	0	35	164[3]	B0_ 16_N	0	35
165	B0_13_P	0	35	166	B0 _14_P	0	35
167	B0_13_N	0	35	168	B0_ 14_N	0	35
169	B0_11_P	0	35	170[3]	B0 _12_P	0	35
171	B0_11_N	0	35	172[3]	B0_ 12_N	0	35
173	GND			174	GND		
175	B0_9_P	0	35	176	B0 _10_P	0	35
177	B0_9_N	0	35	178	B0_ 10_N	0	35
179	B0_7_P	0	35	180	B0 _8_P	0	35

Pin	Signal	S6 Bank	A7 Bank	Pin	Signal	S6 Bank	A7 Bank
181	B0_7_N	0	35	182	B0_ 8_N	0	35
183	B0_5_P	0	35	184	B0 _6_P	0	35
185	B0_5_N	0	35	186	B0_ 6_N	0	35
187	B0_3_P	0	35	188	B0 _4_P	0	35
189	B0_3_N	0	35	190	B0_ 4_N	0	35
191	B0_1_P	0	35	192	B0 _2_P	0	35
193	B0_1_N	0	35	194	B0_ 2_N	0	35
195	GND			196	GND		
197	VCCO	1	15	198	VCCO	0	35
199	VCCO	1	15	200	VCCO	0	35

In general, the 7 series FPGA fabric should be expected to meet or exceed the performance of the Spartan-6 FPGA fabric, but the parts are architecturally different. The following sections outline topics that should be considered when migrating from a Spartan-6 variant to the Artix-7 design.

1.3.1 **New FPGA Firmware / Bitstream Required**

While the loading interface supported by uBoot and the Linux kernel drivers will be the same, the physical FPGA bitstream files for a Spartan-6 are not valid for an Artix-7. Application FPGA projects will need to be migrated from the Xilinx ISE toolset to the Xilinx Vivado toolset and targeted for the correct Artix-7 device. While most HDL code (Verilog or VHDL) should port with little complication, IP leveraging the ISE Core Generator will need to be re-configured using the Vivado IP Wizard tools. In addition, the Xilinx timing constraints should be migrated to the synopsis design constrains language (SDC) supported by the Vivado framework.

The Artix-7 fabric is an improvement over the Spartan-6, and it is expected that all existing Spartan-6 designs should be able to meet timing constraints when targeting Artix-7. Artix-7 logic density options have been selected to match the existing Spartan-6 16 and 45 KLE options. One area that is notable is that the Artix-7 Block Ram (BRAM) primitives are organized as 36 Kbit structures instead of 18 Kbit structures. Designs using large numbers of small BRAM blocks may require additional attention in this area.

1.3.2 **Power Consumption and Supply Considerations**

The Artix-7 variant +3.3V input power requirements and overall consumption is expected to be consistent with the equivalent Spartan-6 based variant. It is not anticipated that a change to the carrier board power supply for the MItyDSP-L138F SOM will be required. Customers are advised to leverage the Xilinx Power Estimation (XPE) tools for both Spartan-6 and Artix-7 designs to understand any power impacts to their specific designs.

The Artix-7 specifications require that HR VCCO voltages not exceed VCCAUX by more than 2.625V for more than 800 ms (at 85 C). If carrier boards assert 3.3V external bank VCCO voltages at approximately the same time as the module main +3.3V input, this should not be an issue, as the onboard supplies for VCCAUX will be enabled < 100 ms after the +3.3V supply rail is present.

1.3.3 **Mixed LVDS and 3.3V IO Not Supported**

The Spartan-6 device family Select IO supported the LVDS_33 IO standard, which allowed for placing LVDS inputs and/or LVDS outputs on a Bank configured to operate with a 3.3V VCCO setting. The 7-series FPGA fabric from Xilinx does not support the LVDS_33 standard. Users with carrier card designs that leverage LVDS standards on

Banks using 3.3V IO should consult Xilinx Answer Record 43989 to assess impact and for guidance on design migration (the Artix-7 IO banks are all High Range (HR) Banks).

1.3.4 **FPGA Clocking**

The Artix-7 Bank clock pins have been routed to the same locations on the DDR edge connector as on the Spartan-7 based SOM variants. However, the IO clocking structure for the Artix-7 and Spartan-6 is different. Of the 4 clock IO pins on the Artix-7, 2 are defined as Single Region Clock Capable IOs (SRCC) and 2 are defined Multi-Region Clock Capable IOs (MRCC). In general, both the SRCC and MRCC clock IO pins are able to reach most necessary clocking resources within the Artix-7 fabric, but there may be situations where a clock needs to be connected to an MRCC pin to support a given design. Users are encouraged to refer to Xilinx's User Guide 472, 7 Series FPGA Clocking Resources for additional information.

1.3.5 **Artix-7 does not support the SUSPEND capability**

The Artix-7 FPGA does not support the SUSPEND function provided by the Spartan-6 FPGA. Critical Link is unaware of any carrier board design that uses this feature. Customers with a carrier board design that uses the FPGA SUSPEND feature should contact Critical Link as well as their local Xilinx FAE for guidance on migrating to the Artix-7 architecture.

1.3.6 **IO pair lengths will be slightly different from Spartan-6 Variant**

While both the Spartan-6 and Artix-7 variants of the SOM use matched lengths for the P and N pairs of IO, the trace lengths between pairs on the board are not matched. FPGA designers may need to account for slight skew length mismatch in high-speed applications. Normally, this can be accounted for in the FPGA design for both transmit and receive applications using appropriate design constraints and/or IOB delay or PLL phase adjustment circuitry. Contact Critical Link for support and details of trace length data.

1.3.7 **Addition of Artix-7 XADC support**

The Artix-7 FPGA has been configured to include a precision 1.25 volt reference on the XADC circuit. While the main XADC analog input connections are not connected to the DDR connector (they are grounded), users may leverage the multifunction IO pins on Bank 15 and 35 that include the ADxN/P inputs if desired. In addition, the XADC circuit may be used to monitor die temperature as well as core and bank IO voltages on the Artix-7 device via FPGA fabric. See Xilinx User Guide 480, 7-Series XADC for more information.

1.4 Anticipated Impact on Quality or Reliability (positive / negative)

There is no impact to Quality or Reliability.

2 Products Affected

Details regarding the full revision history can be located in the MityDSP-L138 Revision History section on the Critical Link support site.
https://support.criticallink.com/redmine/projects/arm9-platforms/wiki/Module_Product_Change_Notifications

Table 2 Products Affected

Model Number	Starting PCA	Suggested Replacement Model	Suggested Replacement PCA
L138-FI-336-RL	80-001110RL	L138-FM-336-RL	80-001538RL
L138-FI-325-RC	80-001108RC	L138-FM-336-RL	80-001538RL
L138-FG-326-RC	80-001114RC	L138-FJ-326-RC	80-001539RC
L138-FG-325-RC	80-001105RC	L138-FJ-326-RC	80-001539RC
L138-DI-325-RI	80-001112RI	L138-DM-336-RI	80-001541RI
L138-DG-325-RI	80-001115RI	L138-DJ-325-RI	80-001540RI
L138-DI-336-RI	80-001368RI	L138-DM-336-RI	80-001541RI
Others	Contact Critical Link	Contact Critical Link	Contact Critical Link

3 Document Revision History

Date	Version	Change Description
18-November-2021	1.0	Initial Version