Au53x5_x4_x2 Family of Parts:
Quad Frequency Translations and Jitter Clean Up Synthesizer

General Description

The Au53x5, Au53x4 and Au53x2 are a family of programmable Quad Fractional Frequency translation based jitter attenuating clock synthesizer parts with flexible input to output frequency translation options. It supports up to 4 input clocks that are common for all the 4 fractional translations and provides 10 (Au5315/25), 4 (Au5314/24) or 2 (Au5312/22) clock outputs. The clock outputs can be derived from the 4 PLLs in a highly flexible manner.

They are fully programmable with the I2C/SPI interface or an on chip, two time programmable, non-volatile memory for factory pre-programmed devices.

Using advanced design technology, they provide excellent integrated jitter performance as well as low frequency offset noise performance while working reliably in the ambient temperature range from -40 °C to 85 °C. The chip has best-in-class transient performance features in terms of clock switching transients and repeatable input to output delays.

Nomenclature:

Au5315/25: 4 input, 10 output, 64-QFN 9 mm x 9 mm
Au5314/24: 4 input, 4 output, 44-QFN 7 mm x 7 mm
Au5312/22: 4 input, 2 output, 44-QFN 7 mm x 7 mm
Au531x : VDDIN = VDD = VDDIO = 2.5V/3.3V
Au532xBC1:VDDIN =3.3V,VDD = 1.8V/2.5V/3.3V, VDDIO = 1.8V
Au532xBC2:VDDIN =3.3V,VDD = 1.8V/2.5V/3.3V, VDDIO = 3.3V

Applications:

- Carrier Ethernet,
- OTN Equipment,
- Microwave Backhaul,
- Gigabit Ethernet,
- Wireless Infrastructure,
- Network Line Cards,
- Small Cells,
- Data Center/Storage,
- SONET/SDH,
- Test / Instrumentation,
- Broadcast Video

Features

- Flexible quad PLL frequency translation from a common input: 4 fractional output domains from single input
- Fully Integrated Fractional N PLLs with integrated VCO and programmable loop filter (1 mHz to 4 kHz)
- Wide frequency support
  - Differential Output from 8 KHz to 2.1 GHz
  - Single Ended Output from 8 KHz to 250 MHz
  - Support for 1 Hz frequency on one output
  - Differential Input from 8 KHz to 2.1 GHz
  - Single Ended Input from 8 KHz to 250 MHz
  - Multiple Crystals / XO / TCXO / OCXO support
- LVPECL, CML, HCSL, LVDS and LVCMOS Outputs
- 150 fs typical rms integrated jitter performance
- Synchronized, holdover or free run operation modes
- Meets G.8262 EEC Option 1,2(Sync E)
- Hitless input clock switching: Auto or manual
  - Sub 50 ps phase build out mode transients
  - Phase Propagation with programmable slopes
  - Frequency ramp for plesiochronous clocks with programmable slopes
  - Robust and fast cycle slip and frequency step detection for input frequency steps (Clean frequency tracking for large frequency steps)
- Excellent Close-in Phase noise performance with no external discrete VCXOs or passive external filters
- Digitally Controlled Oscillator mode: to 0.005 ppb
- Programmable Output Delay Control
- Programmable Frequency Ramp Slopes for Switching Pleisochronous Clocks
- Indicators: Lock Loss, Clock Loss, Frequency Drift
- Repeatable Input to Output delays for each power up of chip
  - Zero Delay Buffer mode also possible on any one PLL
  - Output wake up sync with an independent clock also possible

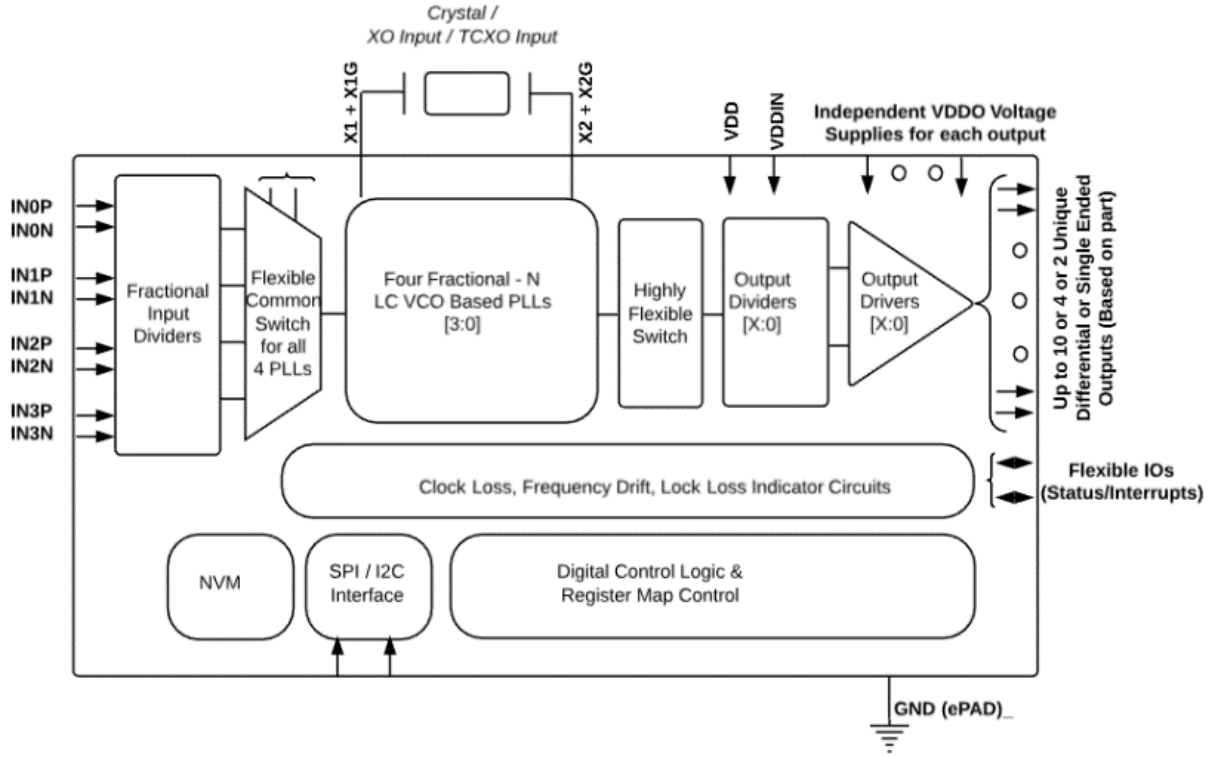

Figure 1 Functional Overview

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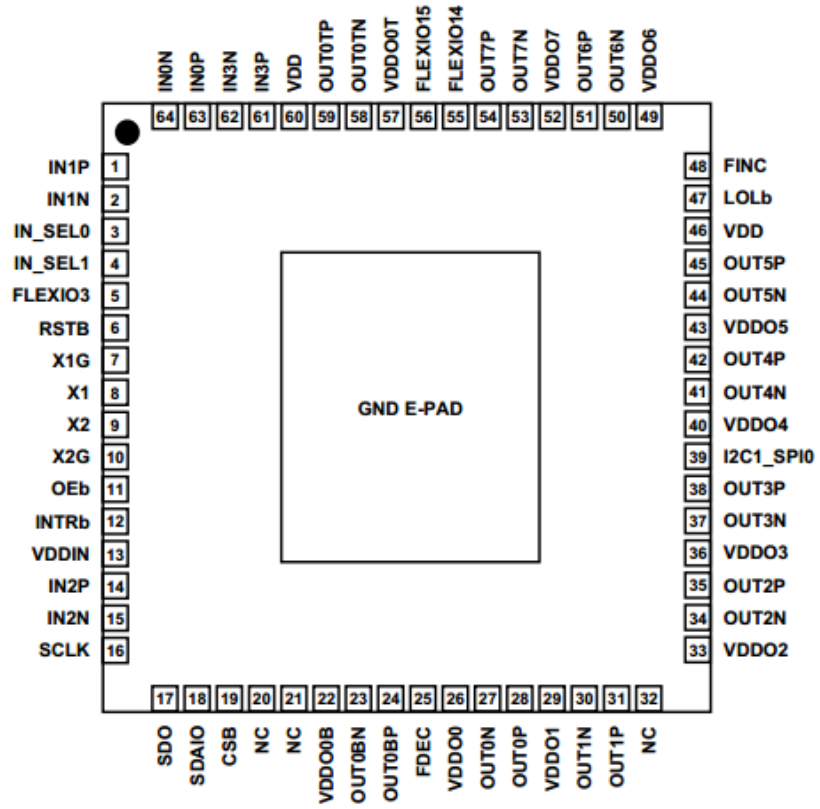


Figure 2 Au5315 & Au5325 Top View

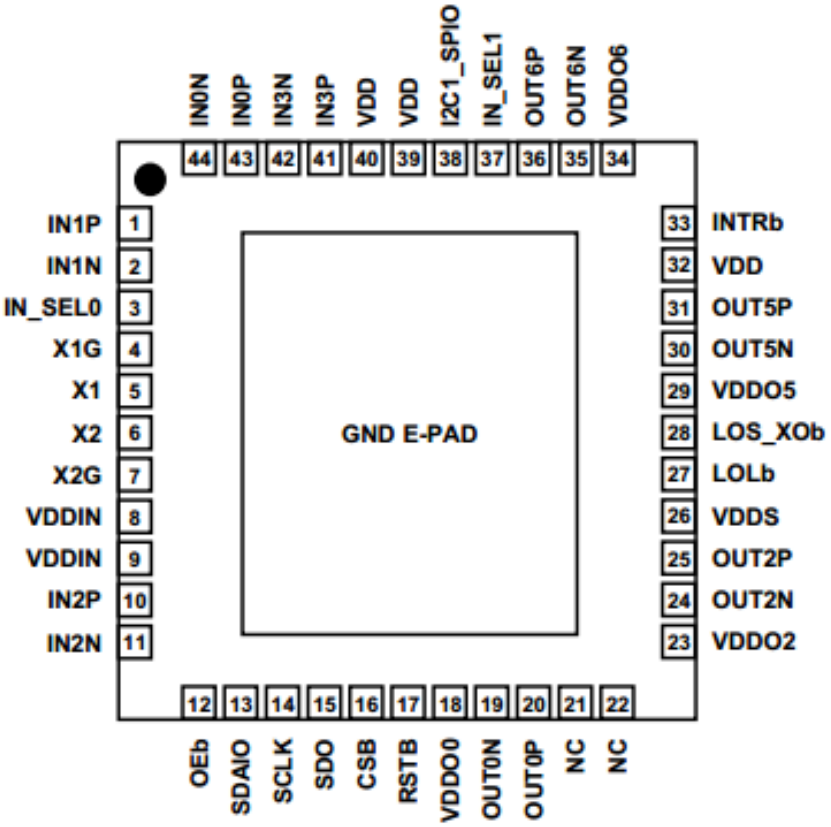


Figure 3 Au5314 & Au5324 Top View

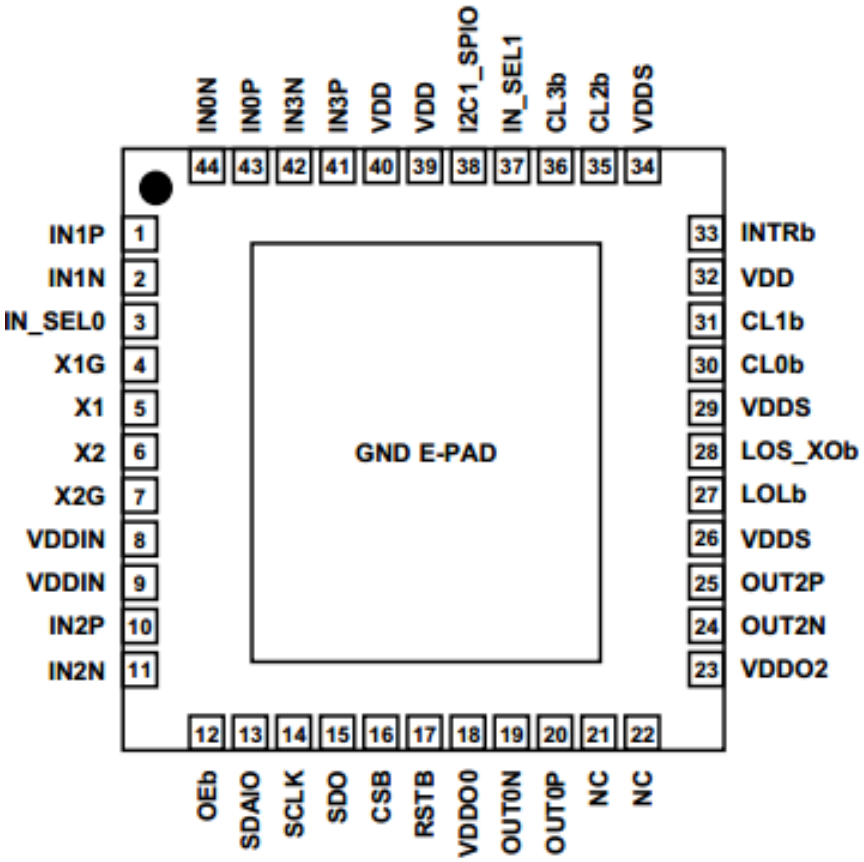


Figure 4 Au5312 & Au5322 Top View

Table 1 Pin Description

Pin Name	I/O Type	Pin			Function	Comments
		Au53x5	Au53x4	Au53x2		
IN0P	Input	63	43	43	True input for IN0 differential pair. Input for LVCMOS IN0 input. Need series external capacitor for differential input.	IN0 / IN1 / IN2 / IN3 inputs can be used for output clock synchronization. An active clock and three spare clocks are chosen such that the same choice holds for all PLLs.
IN0N	Input	64	44	44	Complement input for IN0 differential pair. Ground with capacitor for LVCMOS IN0 input. Need series external capacitor for differential input.	
IN1P	Input	1	1	1	True input for IN1 differential pair. Input for LVCMOS IN1 input. Need series external capacitor for differential input.	
IN1N	Input	2	2	2	Complement input for IN1 differential pair. Ground with capacitor for LVCMOS IN1 input. Need series external capacitor for differential input.	

Pin Name	I/O Type	Pin			Function	Comments
		Au53x5	Au53x4	Au53x2		
IN2P	Input	14	10	10	True input for IN2 differential pair. Input for LVCMOS IN2 input. Need series external capacitor for differential input.	
IN2N	Input	15	11	11	Complement input for IN2 differential pair. Ground with capacitor for LVCMOS IN2 input. Need series external capacitor for differential input.	
IN3P	Input	61	41	41	True input for IN3 differential pair. Input for LVCMOS IN3 input. Need series external capacitor for differential input.	
IN3N	Input	62	42	42	Complement input for IN3 differential pair. Ground with capacitor for LVCMOS IN3 input. Need series external capacitor for differential input.	
GND	Power	EPAD	EPAD	EPAD	Electrical and Package Ground	Exposed Ground on the bottom E-PAD
OUT0P	Output	28	20	20	Output 0 True Output or Output 0 LVCMOS.	LVPECL, LVDS, HCSL, CML and LVCMOS support.
OUT0N	Output	27	19	19	Output 0 Complement Output or Output 0 LVCMOS.	
OUT1P	Output	31	-	-	Output 1 True Output or Output 1 LVCMOS.	
OUT1N	Output	30	-	-	Output 1 Complement Output or Output 1 LVCMOS.	
OUT2P	Output	35	25	25	Output 2 True Output or Output 2 LVCMOS.	
OUT2N	Output	34	24	24	Output 2 Complement Output or Output 2 LVCMOS.	
OUT3P	Output	38	-	-	Output 3 True Output or Output 3 LVCMOS.	
OUT3N	Output	37	-	-	Output 3 Complement Output or Output 3 LVCMOS.	
OUT4P	Output	42	-	-	Output 4 True Output or Output 4 LVCMOS.	
OUT4N	Output	41	-	-	Output 4 Complement Output or Output 4 LVCMOS.	
OUT5P	Output	45	31	-	Output 5 True Output or Output 5 LVCMOS.	
OUT5N	Output	44	30	-	Output 5 Complement Output or Output 5 LVCMOS.	
OUT6P	Output	51	36	-	Output 6 True Output or Output 6 LVCMOS.	

Pin Name	I/O Type	Pin			Function	Comments
		Au53x5	Au53x4	Au53x2		
OUT6N	Output	50	35	-	Output 6 Complement Output or Output 6 LVCMOS.	
OUT7P	Output	54	-	-	Output 7 True Output or Output 7 LVCMOS.	
OUT7N	Output	53	-	-	Output 7 Complement Output or Output 7 LVCMOS.	
OUT0BP	Output	24	-	-	Output 0B True Output or Output 0B LVCMOS.	
OUT0BN	Output	23	-	-	Output 0B Complement Output or Output 0B LVCMOS.	
OUT0TP	Output	59	-	-	Output 0T True Output or Output 0T LVCMOS.	
OUT0TN	Output	58	-	-	Output 0T Complement Output or Output 0T LVCMOS.	
VDDIN	Power	13	8,9	8,9	Power Supply Voltage pin	Decoupling capacitor close to supply pin required.
VDD	Power	46,60	32,39, 40	32,39, 40	Power Supply Voltage pin	Multiple Supply Pins, Decoupling capacitor close to each supply pin required.
VDDS	Power	-	26	26,29, 34	Following Status signals are referred to VDDS: Au53x4: (LOLb, LOS_XOb) Au53x2: (LOLb, LOS_XOb, CL0b, CL1b, CL2b, CL3b)	
IN_SEL0	Input	3	3	3	Input Clock Selection for Manual selection of active clock. Can be left floating or pulled down to GND if not used.	
IN_SEL1	Input	4	37	37		
FLEXIO3	Output	5	-	-	Flexible Status GPIO. Can be left floating or pulled down to GND if not used.	
RSTB	Input	6	17	17	Active low reset internally pulled up to VDDIO; Pull Up Resistor to VDDIO of fixed value (25 KΩ). Can be left floating or pulled up to VDDIO if not used.	Active low signal performs a complete reset of the part
OEb	Input	11	12	12	Used to disable (when 1) all the output clocks. Can be left floating or pulled down to GND if not used.	
INTRb	Output	12	33	33	Active low indicator of programmable sticky notifies. Can be left floating if not used.	

Pin Name	I/O Type	Pin			Function	Comments
		Au53x5	Au53x4	Au53x2		
SCLK	Input	16	14	14	I2C Serial Interface Clock or SPI Clock Input. Pull Up Resistor to VDDIO of fixed value (25 KΩ).	
SDO	Output	17	15	15	Serial Data Output (SPI Interface). In I2C mode this is the A1 address pin (see I2C section).	
SDAIO	Input / Output	18	13	13	I2C Serial Interface Data (SDA) / SPI Input data (SDI).	
CSB	Input	19	16	16	Chip Select for the SPI Interface. In I2C mode this is the A0 address pin (see I2C section).	
FDEC	Input/Output	25	-	-	DCO Decrement. Can be left floating or pulled down to GND if not used.	
I2C1_SPI0	Input	39	38	38	Choose between SPI(0) and I2C(1) interface being used.	
LOLb	Output	47	27	27	Loss of Lock Indicator (NOR value of all PLLs' LOL active high indicators comes out on the LOLb pin). Can be left floating if not used.	
LOS_XOb	Output	-	28	28	XO Loss of Lock Indicator. Can be left floating if not used.	
CL0b	Output	-	-	30	Clock Loss Indicators. Can be left floating if not used.	
CL1b	Output	-	-	31		
CL2b	Output	-	-	35		
CL3b	Output	-	-	36		
FINC	Input/Output	48	-	-	DCO Increment. Can be left floating or pulled down to GND if not used.	
FLEXIO14	Input/Output	55	-	-	Flexible Outputs can be used for programmable status monitoring (Refer AN53001 for more information). Can be left floating or pulled down to GND if not used.	
FLEXIO15	Input/Output	56	-	-		
{X1, X1G}	Input/Output	8,7	5,4	5,4	Crystal X1 Pin and accompanying ground pin	{X1G, X2G} land on a floating island on the PCB
{X2, X2G}	Input/Output	9,10	6,7	6,7	Crystal X2 Pin and accompanying ground pin	
VDDO0	Power	26	18	18	Output Power Supply for Bank 0 outputs	Decoupling capacitor close to each supply pin required.
VDDO1	Power	29	-	-	Output Power Supply for Bank 1 outputs	

Pin Name	I/O Type	Pin			Function	Comments
		Au53x5	Au53x4	Au53x2		
VDDO2	Power	33	23	23	Output Power Supply for Bank 2 outputs	
VDDO3	Power	36	-	-	Output Power Supply for Bank 3 outputs	
VDDO4	Power	40	-	-	Output Power Supply for Bank 4 outputs	
VDDO5	Power	43	29	-	Output Power Supply for Bank 5 outputs	
VDDO6	Power	49	34	-	Output Power Supply for Bank 6 outputs	
VDDO7	Power	52	-	-	Output Power Supply for Bank 7 outputs	
VDDO0T	Power	57	-	-	Output Power Supply for Bank 8 outputs	
VDDO0B	Power	22	-	-	Output Power Supply for Bank 9 outputs	
NC	No Connect	20,21, 32	21,22	21,22	No connect. This pin is not connected to the die.	

Notes:

1. VDDIO is the voltage used for all the status GPIOs and the serial interface. The default voltage for VDDIO can be chosen as either VDDIN or VDD through the programmable GUI (Enabled only on selected GUI variants).
   Configure VDDIO as VDD and VDDIN using 0x23[7] on Page0 as per below table:

Variant	Default VDDIO Power Up	VDDIO=VDD	VDDIO=VDDIN
Au531x	VDDIN	0x23[7]=1, Page0	0x23[7]=0, Page0
Au532xBC1	VDD	0x23[7]=0, Page0 (Default)	Not Supported
Au532xBC2	VDDIN	Not Supported	0x23[7]=1, Page0 (Default)

2. All digital input/output GPIOs (FLEXIOs) have an on-chip 25 kΩ pull down resistor to ePAD ground (unless mentioned otherwise)and can be left unconnected if not used.
3. The I2C1_SPI0 pad has a an on-chip 25 kΩ pull up resistor to indicate default mode of communication as I2C unless this pin is pulled down on the board to indicate the SPI mode.
4. In I2C mode, the serial data and clock have an on-chip 25 kΩ pull up resistor to VDDIO.
5. The RSTB pin has an on-chip 25 kΩ pull up resistor to VDDIO. Writing 0xFE[0] to 1 with delay additon of 10ms has the same effect as the pulling RSTB pin to GND for chip reset.
6. SDO and CSB pins are used to set the I2C default address as 0x69 when floating since SDO and CSB has 25k pull down and pull up to GND and VDDIN respectively. Otherwise the I2C address can be changed as 11010{SDO},{CSB} by forcing the SDO and CSB externally to VDDIN or GND accordingly.
   - The chip can be reset from the register map by writing address 0xFE as 0x01 using the current I2C address.
   - To disable reset from register map by writing 0xFE register as 0x00, Address needs to be 0b11010{SDO}{CSB}, 5 MSB address bits are 11010, LSB 2 bits are the state of SDO and CSB pins. If these pins are floating, use 0x69 as the address. At all other times default slave address chosen for the part can be used.

2 Electrical Characteristics

Table 2 Absolute Maximum Ratings

Description	Conditions	Symbol	Min	Typ	Max	Units
Core supply voltage, Analog Input		V_{DDIN}	-0.5		+3.63	V
Core supply voltage, PLL		V_{DD}	-0.5		+3.63	
Output bank supply voltage		V_{DDO}	-0.5		+3.63	V
Input voltage, All Inputs	Relative to GND	V_{IN}	-0.5		+3.63	V
XO Inputs[3]	Relative to GND	V_{XO}	-0.5		+1.4	V
I2C Bus input voltage	SCLK, SDAT pins	V_{INI2C}	-0.5		+3.63	V
SPI Bus input voltage		V_{INSPI}	-0.5		+3.63	V
Storage temperature	Non-functional, Non-Condensing	T_S	-55		+150	°C
Programming Temperature		T_{PROG}	+25		+85	°C
Maximum Junction Temperature in Operation		T_{JCT}			+125	°C
Programming Voltage (for Programming the OTP Fuse Memory).		V_{PROG}	2.375	2.5	2.625	V
ESD (human body model)	JESD22A-114	ESD_{HBM}			2000	V
Latchup	JEDEC JESD78D	LU			100	mA

Notes:

1. Exceeding maximum ratings may shorten the useful life of the device.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.
3. Refer to AN53012 for the additonal information on the absolute minimum and maximum voltage on XO Inputs before and after the chip power up.

Table 3 Operating Temperatures and Thermal Characteristics

Description	Conditions	Symbol	Min	Typ	Max	Units
Ambient temperature		TA	–40	–	+85	°C
Junction temperature		TJ			+125	°C
Au5315 / Au5325: 64-QFN package						
Thermal Resistance Junction to Ambient	Still Air	θ_{JA}		25.5		°C/W
	Air Flow 1m/s			20.8		°C/W
	Air Flow 2m/s			19.6		°C/W
Thermal Resistance Junction to Case		θ_{JC}		8.70		°C/W
Thermal Resistance Junction to Board		θ_{JB}		7.07		°C/W
Thermal Resistance Junction to Top Center		ψ_{JT}		0.2		°C/W
Au5314 / Au5324, Au5312 / Au5322: 44-QFN package						
Thermal Resistance Junction to Ambient	Still Air	θ_{JA}		25.1		°C/W
	Air Flow 1m/s			20.6		°C/W
	Air Flow 2m/s			19.4		°C/W
Thermal Resistance Junction to Case		θ_{JC}		9.4		°C/W

Description	Conditions	Symbol	Min	Typ	Max	Units
Thermal Resistance Junction to Board		θ_{JB}		4.42		°C/W
Thermal Resistance Junction to Top Center		ψ_{JT}		0.2		°C/W

Table 4 DC Electrical Characteristics

Description	Conditions	Symbol	Min	Typ	Max	Units
Au5315 / Au5314 / Au5312						
Supply voltage, Analog Input Pathways and XTAL Pathways	2.5 V range: ± 5%	V_{DDIN}[1]	2.375	2.50	2.625	V
	3.3 V range: ±10%		2.97	3.3	3.63	V
Supply voltage, PLL	2.5 V range: ±5 %	V_{DD}	2.375	2.50	2.625	V
	3.3 V range: ±10%		2.97	3.3	3.63	V
Au5325 / Au5324 / Au5322						
Supply voltage, Analog Input Pathways and XTAL Pathways	3.3 V range: ±10%	V_{DDIN}	2.97	3.3	3.63	V
Supply voltage, PLL	1.8 V range: ±5%	V_{DD}	1.71	1.80	1.89	V
	2.5 V range: ±5 %		2.375	2.50	2.625	V
	3.3 V range: ±10%		2.97	3.3	3.63	V
All Variants						
Supply Voltage, Output Drivers	1.8 V range: ±5%	V_{DDO}	1.71	1.80	1.89	V
	2.5 V range: ±5%		2.375	2.50	2.625	V
	3.3 V range: ±10%		2.97	3.3	3.63	V
Programmable Status Supply for selected IOs	1.8 V range: ±5%	V_{DDS}	1.71	1.80	1.89	V
	2.5 V range: ±5%		2.375	2.50	2.625	V
	3.3 V range: ±10%		2.97	3.3	3.63	V
Au5315 / Au5314 / Au5312 (VDDIN = VDD = 3.3 V)						
Total Power Dissipation (2.5V LVDS Outputs @ 156.25M)	4 PLLs, 10 Outputs (4 Independent Fractional Translations)	Pd		1550	1860	mW
	1 PLL, 2 Outputs			365	438	mW
Au5315 / Au5314 (VDDIN = VDD = 2.5 V)						
Total Power Dissipation (2.5V LVDS Outputs @ 156.25M)	4 PLLs, 10 Outputs (4 Independent Fractional Translations)	Pd		1280	1536	mW
	1 PLL, 2 Outputs			300	360	mW
Au5325 / Au5324 (VDDIN = 3.3 V, VDD = 1.8 V)						
Total Power Dissipation (2.5V LVDS Outputs @ 156.25M)	4 PLLs, 10 Outputs (4 Independent Fractional Translations)	Pd		1054	1265	mW
	1 PLL, 2 Outputs			250	300	mW
All Variants						
Supply Current, VDDIN	All Four Inputs assumed to be enabled	I_{DDIN}[1]		18	21.6	mA
Supply Current, VDD	All Four PLLs and All 10 Outputs enabled (Maximum current mode)	I_{DD}		340	408	mA
Power supply current, VDDO	LVPECL, output pair terminated 50 Ω to V_{TT} (VDDO – 2 V).	I_{DDO}[2,3,4,5,6]		40	48	mA

Description	Conditions	Symbol	Min	Typ	Max	Units
	LVPECL2, output pair terminated 50 Ω to V_{TT} (VDDO – 2 V) or 0 V without common mode current.			28	36	mA
Power supply current, VDDO	CML, output pair terminated 50 Ω to VDDO	I_{DDO}[2,3,4,5,6,7]		20	24	mA
Power supply current, VDDO	HCSL, output pair with HCSL termination	I_{DDO}[2,3,4,5,6,7]		27	36	mA
Power supply current, VDDO	LVDS, output pair terminated with an AC or DC Coupled diff 100 Ω	I_{DDO}[2,3,4,5,6,7]		16	19.2	mA
Power supply current, VDDO	LVDS Boost, output pair terminated with an AC or DC Coupled diff 100 Ω	I_{DDO}[2,3,4,5,6,7]		20	24	mA
Power supply current, VDDO	LVCMOS, 250 MHz, 2.5 V output, 5-pF load	I_{DDO}[2,3,4,5,6,7]		15	18	mA

Notes:

1. VDD and VDDIN are independent supplies that are expected to be at the same voltage level (either 3.3 V or 2.5 V) for Au531x parts. For Au532x parts VDDIN = 3.3 V and VDD = 1.8V/2.5V/3.3V is the recommended supply combination. Additional current consumption of 3 mA for a third overtone crystal instead of a fundamental mode crystal.
2. LVPECL and LVDS Boost standards are supported for VDDO = {2.5 V, 3.3 V}. LVPECL2, HCSL, CML and LVDS standards are supported for VDDO = {1.8 V, 2.5 V, 3.3 V}.
3. LVPECL mode provides 6mA of common mode current on each output. LVPECL2 mode does not provide this common mode current.
4. A 50 Ω Termination resistor with a DC bias of VDDO – 2 V for LVPECL standards is supported for VDDO = {2.5 V, 3.3 V}.
5. IDDOx Output driver supply current specified for one output driver in the table. This includes current in each of the output module that includes output dividers, drivers and clock distributions.
6. The LVDS Boost Mode and the LVDS Mode can be used for AC Coupled output terminations. LVDS Boost provides an LVPECL like swing with an AC Coupled 100 Ω Differential termination.
7. Refer to Output Termination Information in the data sheet for the descipription of the various terminations that are supported. For efuse programming in Au532x parts, VDD alongwith VDDIN can be set to 2.5 V and has no reliability concerns.

Table 5 Input Clock Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Standard Input Buffer with Differential or Single-Ended — AC-coupled (IN0/IN0, IN1/IN1, IN2/IN2, IN3/IN3)						
Input Frequency Range	Differential	f_{IN}	0.008	—	2100	MHz
	All Single-ended signals (including LVCMOS)		0.008	—	250	MHz
Voltage Swing (Differential Amplitude Peak or Single Ended Peak to Peak for the differential signal) [1]	AC-coupled f_{IN} < 400 MHz	V_{IN}	100	—		mV
	400 MHz < AC-coupled f_{IN} < 750 MHz		225	—		mV
	750 MHz < AC-coupled fIN < 2100 MHz		350	—		mV
Single Ended AC Coupled Inputs (Single Ended Peak to Peak Input) [1][4]	AC-Coupled f_{IN} < 250 MHz		500	_	3600	mV
Slew Rate [2,3]		SR	400	—	—	V/µs
Duty Cycle		DC	40	—	60	%
Input Capacitance		C_{IN}	—	0.3	—	pF
Input Resistance	AC Coupled SE	R_{IN}	—	15	—	kΩ
	Differential		—	10	—	kΩ
Pulsed CMOS Input Buffer — DC-coupled (IN0, IN1, IN2, IN3) [3]						
Input Frequency		$f_{IN\_PULSED\_CMOS}$	0.008	—	250	MHz
Input Voltage		V_{IL}	–0.2	—	0.4	V

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
		V_{IH}	0.8	—	—	V
Slew Rate [2,3]		SR	400	—	—	V/µs
Duty Cycle		DC	40	—	60	%
Minimum Pulse Width	Pulse Input	PW	1.6	—	—	ns
Input Resistance		R_{IN}	—	30	—	kΩ
Reference Clock (Applied to X1), Can be external XO, TCXO or OCXO						
Reference Clock Frequency	Range for best jitter	F_{IN_REF}	48	-	160	MHz
	Overall supported range		37.5	-	160	MHz
Input Voltage Swing	Single Ended peak to peak	V_{IN_SE}	365	-	2000	mVpp_se
	Differential peak to peak	V_{IN_DIFF}	365	-	2500	mVpp_diff
Slew rate		SR	400	-	-	V/us
Duty Cycle		DC	40	-	60	%

Notes:

1. AC Coupled input assumed with series capacitance for differential inputs or single ended AC Coupled inputs. Swing requirement at device pins.
2. Resistor termination for differential input followed by series capacitors for each of true and complement differential input connecting to the device pins.
3. LVCMOS single ended is direct coupled on the true input. Connect complement input to ground with a 100nF capacitor.
4. Single Ended AC coupled Input Swing requirement (Single Ended Peak to Peak Input) [1][4] is for optimal noise performance.

Table 6 Serial and Clock Input

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Voltage		V_{IL}	—	—	0.3 x V_{DDIO}[1]	V
		V_{IH}	0.7 x V_{DDIO}[1]	—	—	V
Input Capacitance		C_{IN}	—	1	—	pF
Input Resistance		R_{IN}	—	25	—	kΩ
Minimum Pulse Width	FINC, FDEC	PW	100	—	—	ns
Update Rate	FINC, FDEC	F_{UR}	—	—	1	µs

Notes:

1. VDDIO is the voltage used for all the status GPIOs and the serial interface. The default voltage for VDDIO can be chosen as either VDDIN or VDD with a hard coded eFuse based selection.

Table 7 Output Serial and Status Pin

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
All VDDIO based GPIOs						
Output Voltage	I_{OH} = -2 mA	V_{OH}	V_{DDIO} x 0.75	—	—	V
	I_{OL} = 2 mA	V_{OL}	—	—	V_{DDIO} x 0.25	V
All VDD based GPIOs						
Output Voltage	I_{OH} = -2 mA	V_{OH}	V_{DDS} x 0.75	—	—	V
	I_{OL} = 2 mA	V_{OL}	—	—	V_{DDS} x 0.25	V

Notes:

1. VDDIO is the voltage used for all the status GPIOs and the serial interface. The default voltage for VDDIO can be chosen as either VDDIN or VDD with a hard coded eFuse based selection.

Table 8 Output Clock Characteristics

Description	Conditions	Symbol	Min	Typ	Max	Units
Differential output frequency	LVPECL, CML, LVDS outputs	$F_{OUT,DIFF}$ [1]	1		2100M	Hz
Differential output frequency	HCSL outputs	$F_{OUT,DIFFH}$ [1]	1		700 M	Hz
Single ended output frequency	LVCMOS outputs	$F_{OUN,SE}$ [1]	1		250 M	Hz
PLL loop bandwidth	Programmable	F_{BW}	0.001		4000	Hz

Description	Conditions	Symbol	Min	Typ	Max	Units
Jitter peaking	Meets SONET Jitter Peaking requirements in closed loop	J_{PEAK}			0.1	dB
Time delay before the Historical average for output Frequency is considered.	Programmable in register map	H_{DELAY} [2,3]	0.035	0.5	35	s
Length of time for which the Average of the frequency is considered	Programmable in register map	H_{AVG} [2,3]	0.07	1	70	s
Power Supply to I2C or SPI interface ready	No I2C transaction valid till 10ms after all power supplies are ramped to 90% of final value.	T_{START}			10	ms
With Speed-Up mode enabled	Speed-up mode is programmable. This is a Typical number. Actual wake up time depends on fast lock and normal BW settings	T_{LOCK} [4]		300		ms
DCO Mode Frequency Step Resolution	Frequency Increment or Decrement resolution. This is controlled through the register map.	$F_{RES,DCO}$ [5]		0.005		ppb
Resolution for output delay	Programmable per output clock with this resolution for a total delay of ±7.5 ns	T_{RES} [6]		35		ps
Maximum Phase Hit	Default Hitless Switching Mode (no phase propagation)	T_{MAX} [7]	-50		50	ps
Uncertainty in Input to Output Delay	Maximum variation in the static delay from input to output clock between repeated power ups of the chip	ΔT_{DELAY}	-175		175	ps
Pull Range		ω_P		500		ppm
POR to Serial Interface Ready		T_{RDY}			15	ms
Input to Output Delay in ZDB mode (matched pathways on external feedback, IN0 input, IN3 feedback)		T_{ZDELAY} [8]		100		ps
Temperature Variation of delay in ZDB mode		$T_{ZDELAY,TMP}$ [8]			1	ps/C
One free run PLL clock on fuse locked parts	Using a special mode for fuse locked parts to generate one free run output from one PLL	$T_{START,Special}$			10	ms

Notes:

1. 1 Hz Output Available only on output OUT0B (OUT0BP, OUT0BN). Range supported is 8 kHz to 2100 MHz for all the other outputs.
2. Hitless Switching enables PLL to switch between input clocks when the current clock is lost,
    a. Clock Loss can be defined as 2 / 4 / 8 / 16 consecutive missing pulses.
    b. Priority list for the input clocks can be set in the register map independently for each PLL.
    c. Output is truly hitless (no phase transient and 0 ppb relative error in frequency) for exactly same frequency input clocks that are switched.
    d. Hitless switching support is both revertive and non-revertive
        i. Revertive / Non-revertive Support: Assume Clock Input 0 is lost and switch is made to Clock Input 1. Then, PLL reverts to Clock Input 0 when it becomes valid again in Revertive mode. It does not switch back to Clock Input 0 even when it becomes valid again in the non-Revertive mode.
3. PLL enters holdover mode when the active input clock and all spare clocks in the clock priority list for hitless switching are lost,
    a. Clock Loss can be defined as 2 / 4 / 8 / 16 consecutive missing pulses

   b. Programmable Clock Loss settings ensure Gapped Clocks can be supported by choosing higher number of missing pulses as the trigger for clock being invalid
   c. Entering hold over mode is supported with the frequency frozen at a historical average determined from the H_{DELAY} and H_{AVG} settings.
4. For low PLL Loop Bandwidths, wake up time can be very large unless the speed up feature is used. The speed up feature provides the user options to use a completely independent loop bandwidth for the wake up transitioning to the regular bandwidth after frequency and phase are locked.
   a. Fast Lock Bandwidth needs to be less than 100 times smaller than the input clock frequency (divided input at PLL phase detector) for stable and bounded (in time) lock trajectory of the PLL
5. The 0.005 ppb specification is for the smallest frequency step resolution available. Larger frequency step resolutions up to 100 ppm can be used also. The frequency resolution for the DCO mode frequency step is independently programmable for each DCO step.
6. All output clocks from one specific PLL are phase aligned. Relative delay adjustment is then possible on each clock individually as defined by the T_{RES} parameter.
7. This test is for 2 inputs at 8M that are switched to get a 622.08M output.
8. Both input and feedback at 8 MHz with the delays exactly matched and same slew for both for the chip.

Table 9 Fault Monitoring Indicators

Description	Conditions	Symbol	Min	Typ	Max	Units
Clock Loss Indicator Thresholds	Clock Loss Indicators can be set on any of the four inputs. Loss of 2 / 4 / 8 / 16 consecutive pulses can be used to indicate a clock loss. Programmable in the register map.	CL_X [1,4]	2	4	16	Pulses
Fine Frequency Drift Indicator Thresholds: Step Size	Frequency drift threshold is programmable in the range with the step size resolution specified. Frequency drift hysteresis is programmable in the range with the step size resolution specified.	FD_X [2,3,4]		±2		ppm
Fine Frequency Drift Indicator Thresholds: Hysteresis Range			±2		±500	ppm
Fine Frequency Drift Indicator Thresholds: Range			±2		±500	ppm
Coarse Frequency Drift Indicator Thresholds	Coarse Drift Indicators programmable from {Up to ±1600 ppm in steps of ± 100 ppm}		±100		±1600	ppm
Lock Loss Indicator Threshold	Lock Loss Indicator threshold is programmable in the range specified from the following choices for setting and clearing LL: {±0.2, ±0.4} ppm, {±2, ±4} ppm, {±20, ±40} ppm, {±200, ±400} ppm, {±2000, ±4000} ppm	LL	±0.2		±4000	ppm

Notes:

1. Clock Loss Indicators are used for:
   a. Hitless Switching Triggers
   b. Update in Status Registers in the register map
2. Frequency Drift Indicators can use any one of the four inputs or the Crystal / Reference input as the golden reference with respect to which FDx for all other clocks can be recorded in the Status Registers. FDx thresholds for each clock input for each clock can be set independently.
3. Coarse and Fine Frequency Drift indicators can be concurrently enabled. This enables the user to detect fast drifting frequencies since detecting fine drifts will take longer measurements.
4. Clock loss and Lock loss indicators are available as alerts on flexible IO pins as described in the functional description section of the data sheet.
5. Clock Loss can be combined with either of the frequency drift monitors (coarse and fine) to trigger the hitless switching event in the PLLs. The trigger for a hitless switching event in the PLL can therefore be either the Clock Loss event or either of Clock Loss or Frequency Drift.

Table 10 Crystal Requirements

Description	Conditions	Symbol	Min	Typ	Max	Units
High Fundamental Frequency Crystal Reference (HFF)						
Crystal Frequency	Can be supported with a fundamental crystal of 100-160 MHz range.	$XTAL_{IN}$	100		160	MHz
C0 cap for crystal		$XTAL_{C0}$			2	pF
CL cap for crystal	Small range around CL only	$XTAL_{CL}$		5		pF
ESR for crystal	ESR defined at frequency of oscillation	$XTAL_{ESR}$			40	Ω
Rm1 for crystal		$XTAL_{Rm1}$			20	Ω
Power delivered to crystal	Drive Level to the crystal	$XTAL_{PWR}$		100		µW
Third Overtone Crystal Reference (OT3)						
Crystal Frequency	Can be supported with an OT3 crystal of 100-160 MHz range.	$XTAL_{IN}$	100		160	MHz
C0 cap for crystal		$XTAL_{C0}$			2	pF
CL cap for crystal	Small range around CL only	$XTAL_{CL}$		5		pF
ESR for crystal	ESR defined at frequency of oscillation	$XTAL_{ESR}$[1]			80	Ω
Rm3 for crystal		$XTAL_{Rm3}$			40	Ω
Power delivered to crystal	Drive Level to the crystal	$XTAL_{PWR}$		100		µW
Low Frequency Fundamental Crystal (LFF)						
Crystal Frequency	Can be supported with a fundamental crystal > 37.5 MHz range. For Best Performance use an LFF crystal > 48 MHz	$XTAL_{IN}$	48		54	MHz
C0 cap for crystal		$XTAL_{C0}$			2	pF
CL cap for crystal	Small range around CL only	$XTAL_{CL}$		8		pF
ESR for crystal	ESR defined at frequency of oscillation	$XTAL_{ESR}$ [1]			60	Ω
Rm1 for crystal		$XTAL_{Rm1}$			40	Ω
Power delivered to crystal	Drive Level to the crystal	$XTAL_{PWR}$		100		µW

Notes:

1. ESR relates to the motional resistance Rm with the relationship $ESR = Rm\ (1 + C0/CL)^2$

Table 11 Output RMS Jitter in Frequency Translation Modes

Description	Conditions	Symbol	Min	Typ	Max	Units
RMS Jitter for 12 kHz – 20 MHz Integration Bandwidth F_{IN} = 38.88 MHz, PLL BW = 100 Hz, Single PLL Profile	F_{OUT} = 622.08 MHz	RMS_{JIT} [1,2]		140		fs rms
	F_{OUT} = 156.25 MHz			150		fs rms

Notes:

1. For best noise performance in jitter attenuation mode, use lowest usable loop bandwidth for the PLL.
2. Does not include noise from the input clocks to the PLL

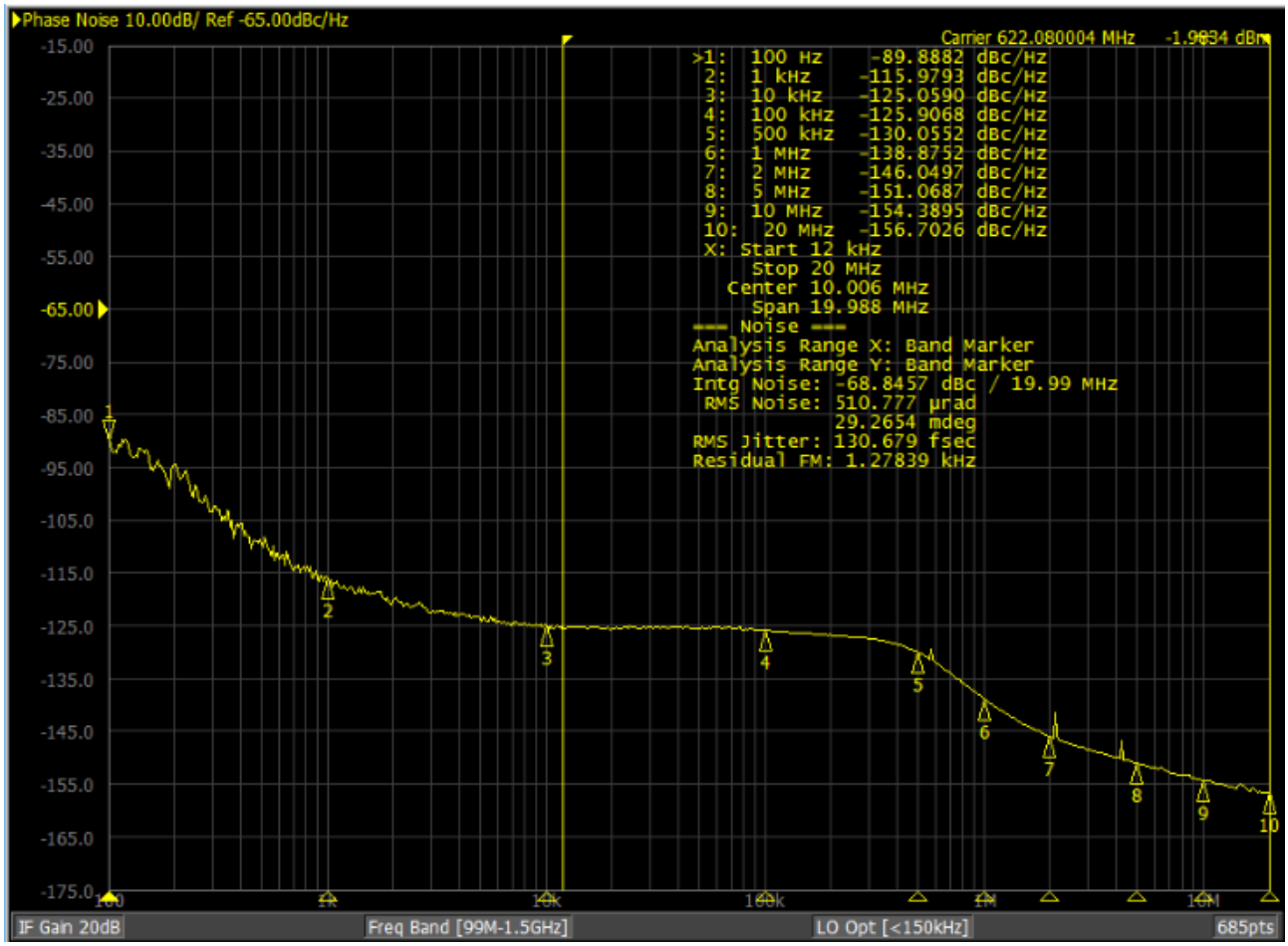


Figure 5 Representative Phase Noise Measurement

Note: F_{OUT} = 622.08 MHz, F_{IN} = 38.88 MHz, BW = 100 Hz, F_{REF} = 54 M XO

Table 12 Close In Offset Phase Noise

Description	Conditions	Symbol	Min	Typ	Max	Units
Phase Noise Skirt F_{OUT} = 122.88 MHz, PLL BW = 100 Hz	Offset Frequency = 100 Hz	PN[1]		-113		dBc/Hz
	Offset Frequency = 1 kHz			-130		
	Offset Frequency = 10 kHz			-138		

Notes:

1. This is the noise contribution of the chip only without including the input and reference self contributions

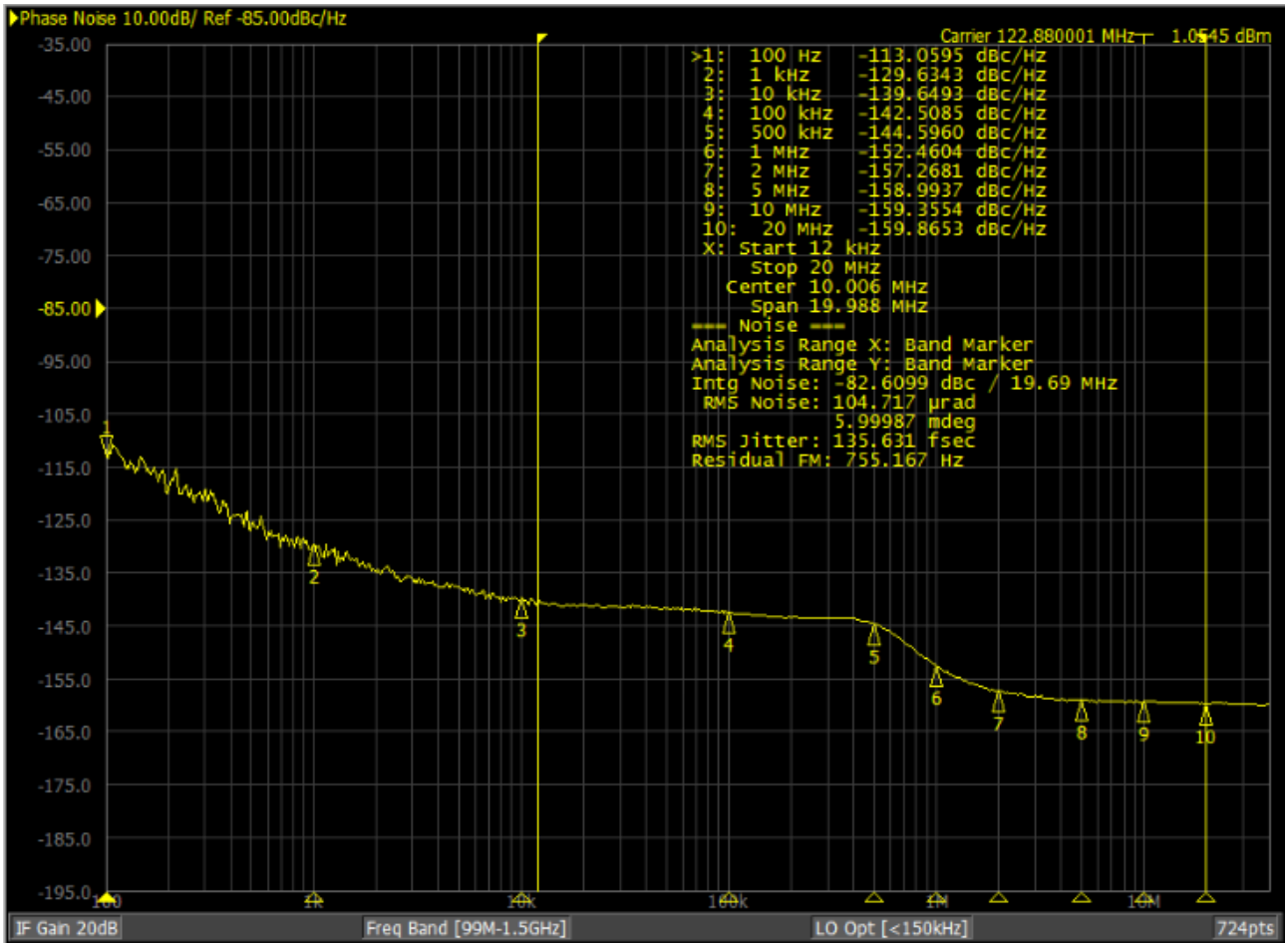


Figure 6 Representative Close In Phase Noise Measurement

Note: F_{OUT} = 122.88M, BW = 100 Hz, F_{REF} and F_{IN} are provided from R&S SMA100 equipment to ensure a low close in phase noise for the reference and input to illustrate the chip contribution to close in phase noise.

Table 13 Power Supply Rejection

Description	Conditions	Symbol	Min	Typ	Max	Units
F_{OUT} = 156.25 MHz, F_{SPUR} = 100 kHz, BW = 100 Hz PSRR on VDD Supply	Au531x, VDD = 3.3 V	$PSRR_{VDD}$		-96		dBc
	Au531x, VDD = 2.5 V			-90		
	Au532x, VDD = 1.8 V			-75		
F_{OUT} = 156.25 MHz, F_{SPUR} = 100 kHz, BW = 100 Hz PSRR on VDDIN Supply	Au531x, VDD = 3.3 V	$PSRR_{VDDIN}$		-100		dBc
	Au531x, VDD = 2.5 V			-100		
	Au532x, VDD = 3.3 V			-100		
F_{OUT} = 156.25 MHz, F_{SPUR} = 100 kHz, BW = 100 Hz PSRR on VDDO Supply	All variants, VDDO = 3.3 V	$PSRR_{VDDO}$		-80		dBc

Notes:
1. The PSRR is measured with a 50 mVpp sinusoid in series with the supply and checking the spurious level relative to the carrier on the output in terms of phase disturbance impact.
2. Output PSRR measured with LVDS standard which (along with the LVDS boost) are the recommended standards for AC Coupled terminations

Table 14 Adjacent Output Cross Talk

Description	Conditions	Symbol	Min	Typ	Max	Units
156.25 M and 155.52 M on adjacent outputs	Au5315 / Au5325	X_{TALK}		-75		dBc
	Au5314 / Au5324			-80		

Notes:
1. Measured across adjacent outputs- All adjacent outputs are covered and the typical value for the worst case output to output coupling is reported.
2. The adjacent output pairs are chosen at 155.52 MHz and 156.25 MHz frequencies.

3. This cross talk between outputs is mainly package dependent therefore terminated outputs are used for reporting these numbers ensuring that there is signal current in the bond wires.

Table 15 Output Clock Specifications

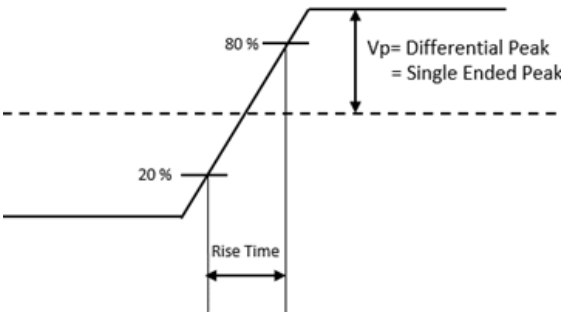
Descriptions	Conditions	Symbol	Min	Typ	Max	Units
DC Electrical Specifications - LVCMOS output (Complementary Out of Phase Outputs or One CMOS Output per Output Driver)						
Output High Voltage	4 mA load, VDD = 3.3 V	V_{OH}	VDDO-0.3		-	V
Output High Voltage	4 mA load, VDD = 1.8 V and 2.5 V	V_{OH}	VDDO-0.4		-	V
Output Low Voltage	4 mA load	V_{OL}			0.3	V
DC Electrical Specifications - LVCMOS output (In Phase Outputs)						
Output High Voltage	4 mA load, VDD = 3.3 V	V_{OH}	VDDO-0.35		-	V
Output High Voltage	4 mA load, VDD = 2.5 V	V_{OH}	VDDO-0.45		-	V
Output High Voltage	4 mA load, VDD = 1.8 V	V_{OH}	VDDO-0.5		-	V
DC Electrical Specifications – LVDS Outputs (VDDO = 1.8 V, 2.5 V or 3.3 V range)						
Output Common-Mode Voltage	VDDO = 2.5 V or 3.3 V range	V_{OCM}	1.125	1.2	1.375	V
Change in VOCM between complementary output states		ΔV_{OCM}			50	mV
Output Leakage Current	Output Off, VOUT = 0.75 V to 1.75 V	I_{OZ}	-20		20	µA
DC Electrical Specifications - LVPECL Outputs (VDDO = 2.5-V or 3.3-V range)						
Output High Voltage	Rterm = 50 Ω to VTT(VDDO – 2.0 V)	V_{OH}	VDDO-1.165		VDDO-0.800	V
Output Low Voltage	Rterm = 50 Ω to VTT(VDDO – 2.0 V), w/o common mode current	V_{OL}	VDDO-2.0		VDDO-1.45	
AC Electrical Specifications - HCSL Outputs (VDD = 1.8 V, 2.5 V or 3.3 V range)						
Output High Voltage Max	Measurement on single-ended signal	V_{MAX}			1150	mV
Output Low Voltage Min	Measurement on single-ended signal	V_{MIN}	-300			mV
Differential Voltage	Measurement taken from differential waveform	VP	300			mV
Absolute Crossing point voltage	Measurement taken from single ended waveform	V_{CROSS}	250		600	mV
Variation of VCROSS over all rising clock edges	Measurement taken from single ended waveform	$V_{CROSSDELTA}$			140	mV
DC Electrical Specifications - CML Outputs (VDDO = 1.8 V, 2.5 V or 3.3 V range)						
Output High Voltage	Rterm = 50 Ω to VDDO	V_{OH}	VDDO-0.085	VDDO-0.01	VDDO	V
Output Low Voltage	Rterm = 50 Ω to VDDO	V_{OL}	VDDO-0.6	VDDO-0.4	VDDO-0.3	V
AC Electrical Specifications LVCMOS Output Load: 10 pF < 100 MHz, 7.5 pF < 150 MHz, 5 pF > 150 MHz > 200 MHz						
Output Frequency		f_{OUT}	8k		250M	Hz
Output Duty cycle	Measured at 1/2 VDDO, loaded, fOUT < 100 MHz	t_{DC}	45		55	%
Output Duty cycle	Measured at 1/2 VDDO, loaded, fOUT > 100 MHz	t_{DC}	40		60	%
Rise/Fall time	VDDO = 1.8 V, 20-80%, Highest Drive setting	t_{RFCMOS}			2	ns
Rise/Fall time	VDDO = 2.5 V, 20-80%, Highest Drive setting	t_{RFCMOS}			1.5	ns
Rise/Fall time	VDDO=3.3 V, 20-80%, Highest Drive setting	t_{RFCMOS}			1.2	ns

Descriptions	Conditions	Symbol	Min	Typ	Max	Units
AC Electrical Specifications (LVPECL, LVDS, CML)						
Clock Output Frequency		f_{OUT}	8k		2100M	Hz
PECL Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for PECL outputs.	t_{RF}			350	ps
CML Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for CML outputs	t_{RF}			350	ps
LVDS Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for LVDS outputs.	t_{RF}			350	ps
Output Duty Cycle	Measured at differential 50% level, 156.25 MHz	t_{ODC}	45	50	55	%
LVDS Output differential peak	Measured at 156.25M Output	VP	300	350	454	mV
Boosted LVDS Output differential peak	Measured at 156.25M Output	VP	500	700	950	mV
LVPECL Output Differential peak	Measured at 156.25M Output	VP	450	750	900	mV
CML Output Differential Peak	Measured at 156.25M Output	VP	250		600	mV

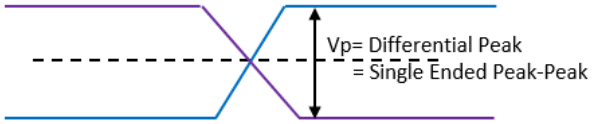
Notes:

Convention for Wave Forms

Differential Signal = OUTP - OUTN



Single Ended Signals {OUTP,OUTN}



3 Functional Description

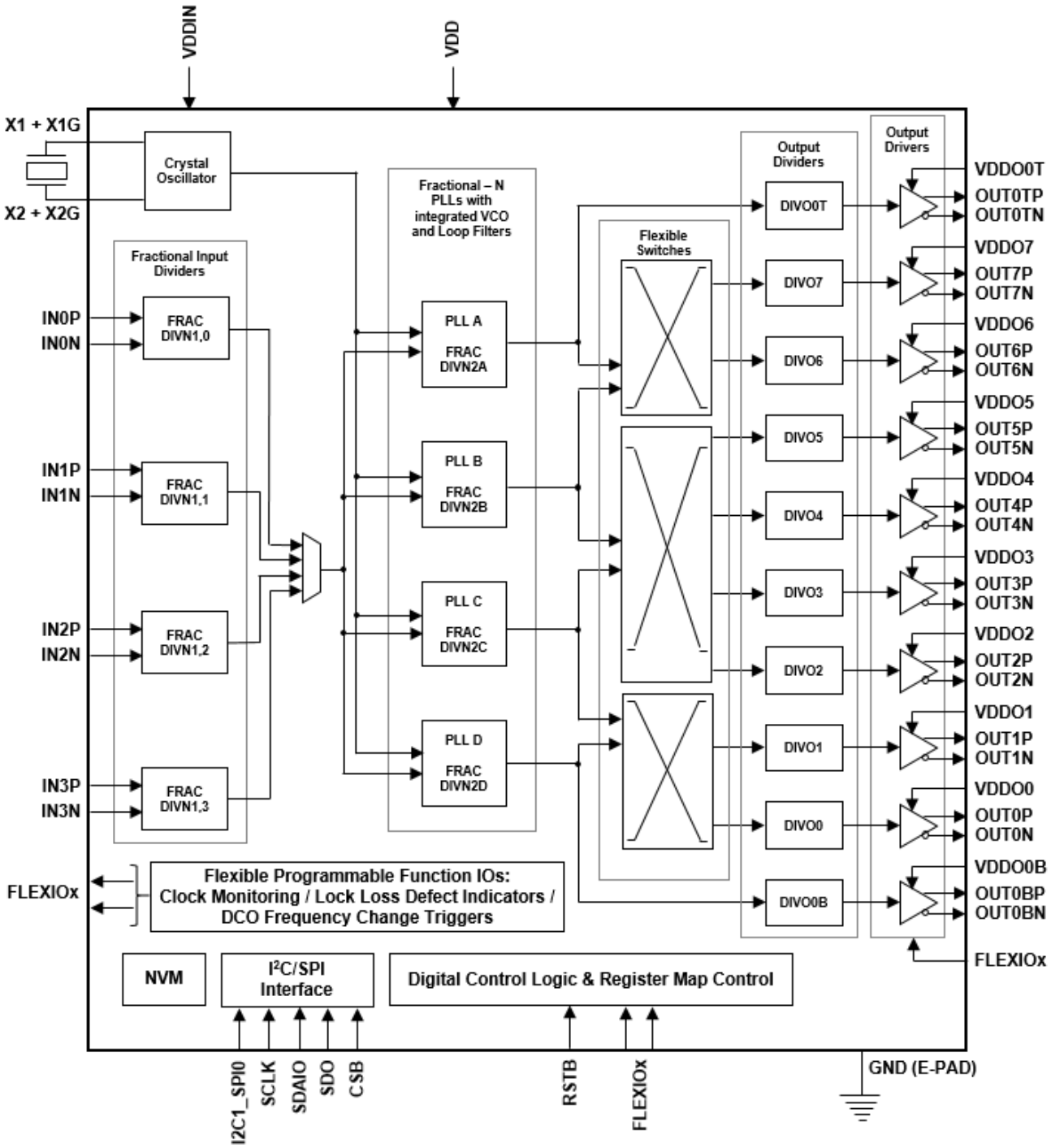


Figure 7 Au5315 & Au5325 Overall Architecture

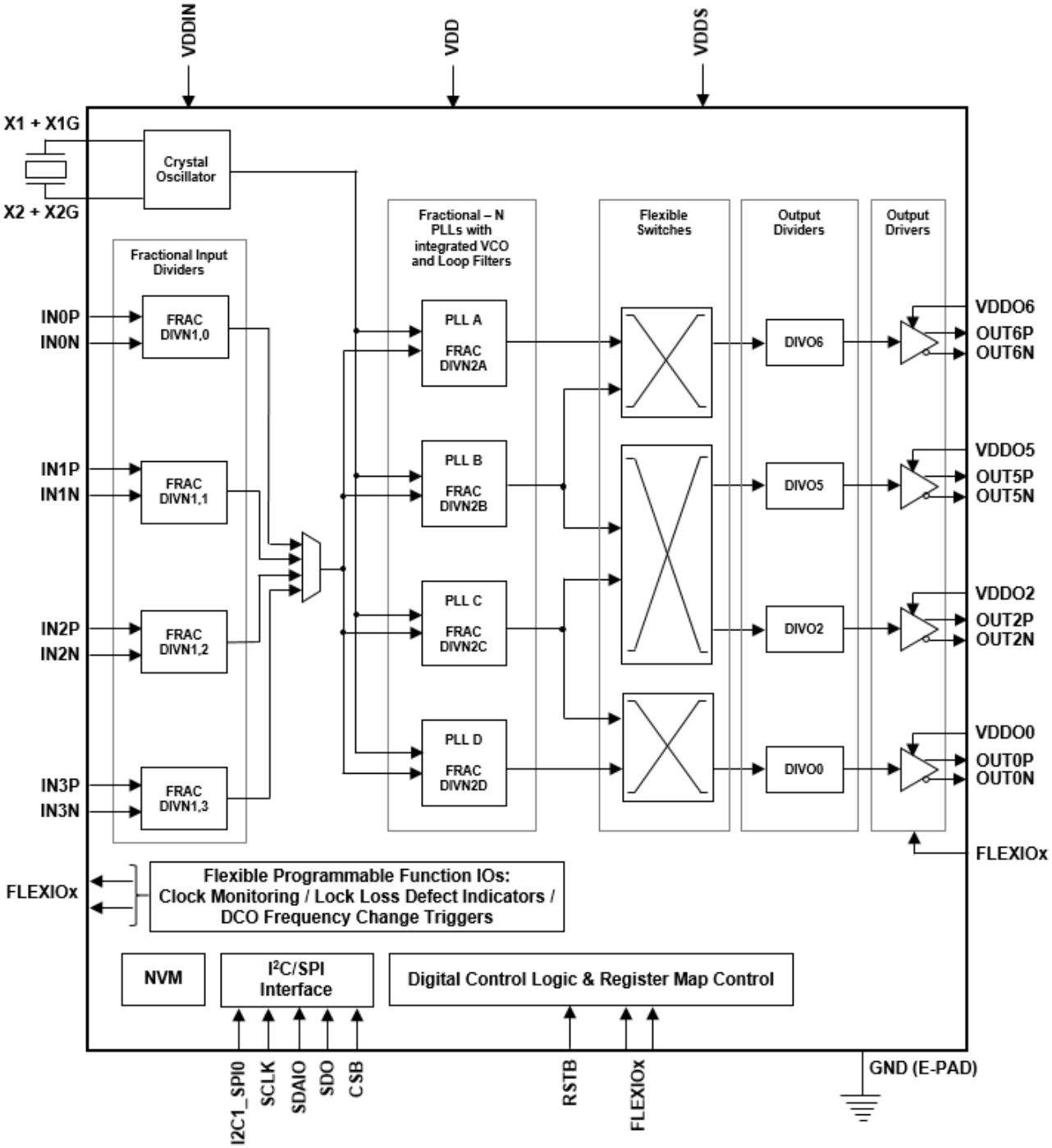


Figure 8 Au5314 & Au5324 Overall Architecture

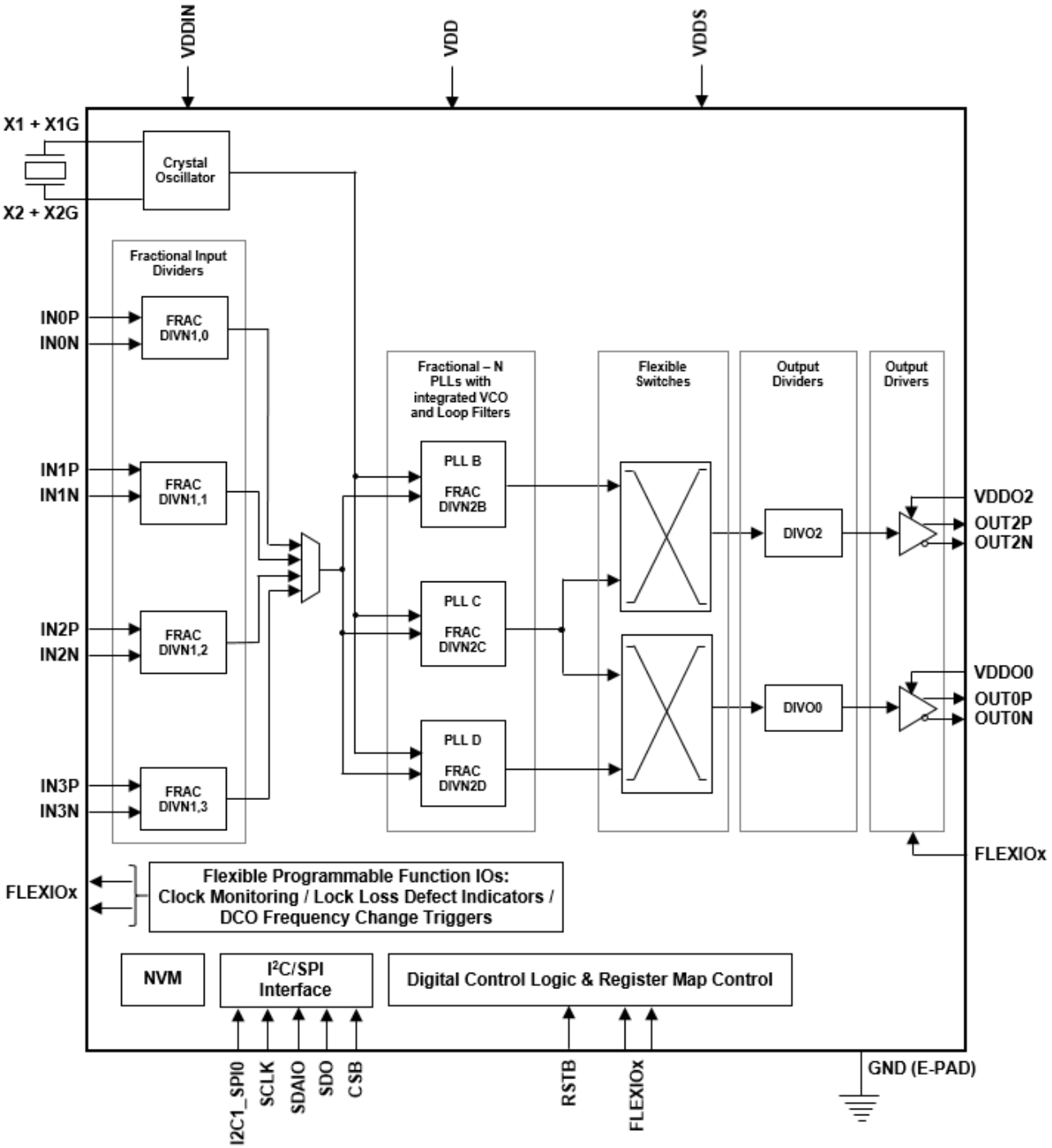


Figure 9 Au5312 & Au5322 Overall Architecture

Au53x5, Au53x4 and Au53x2 are a family of jitter attenuating frequency translation devices that offers four PLLs for 4 frequency translation pathways from the same input. The four clock inputs map to all of the four PLLs such that clock priority is the same across the 4 PLLs. This creates an arrangement that provides up to 4 fractional translations from one input at any given time. The output high frequency voltage controlled oscillators (VCOs) associated with each PLL are mapped to the 10 outputs (Au53x5) or 4 outputs (Au53x4) or 2 outputs (Au53x2) in a very flexible fashion. This offers a very flexible frequency translation arrangement with independent control of each PLL in terms of jitter attenuation, bandwidth control and input clock selection with redundancy.

The hierarchy of the clocks, nomenclature of the various frequency dividers as well as the clock translation pathways available on the chip are shown in Figure 10, Figure 11 and Figure 12.

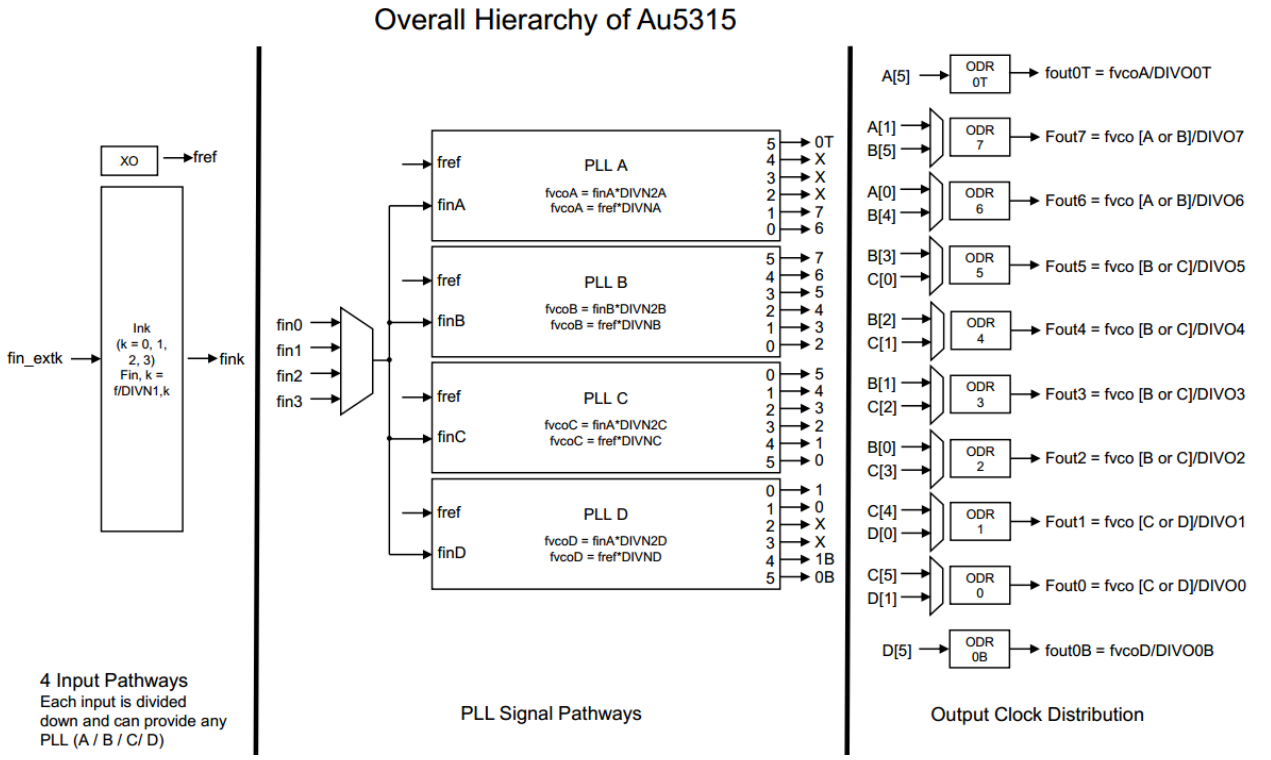


Figure 10 Au5315 & Au5325 Overall Hierarchy of Clocks

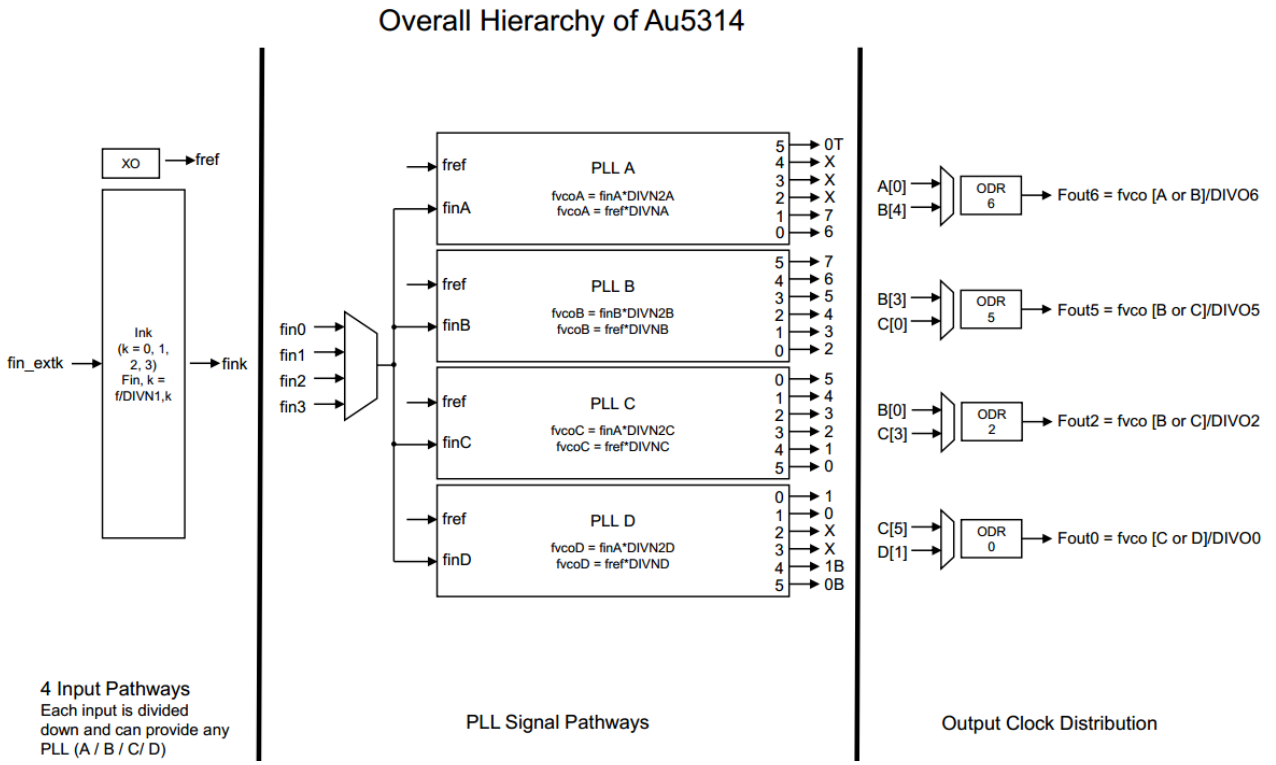


Figure 11 Au5314 & Au5324 Overall Hierarchy of Clocks

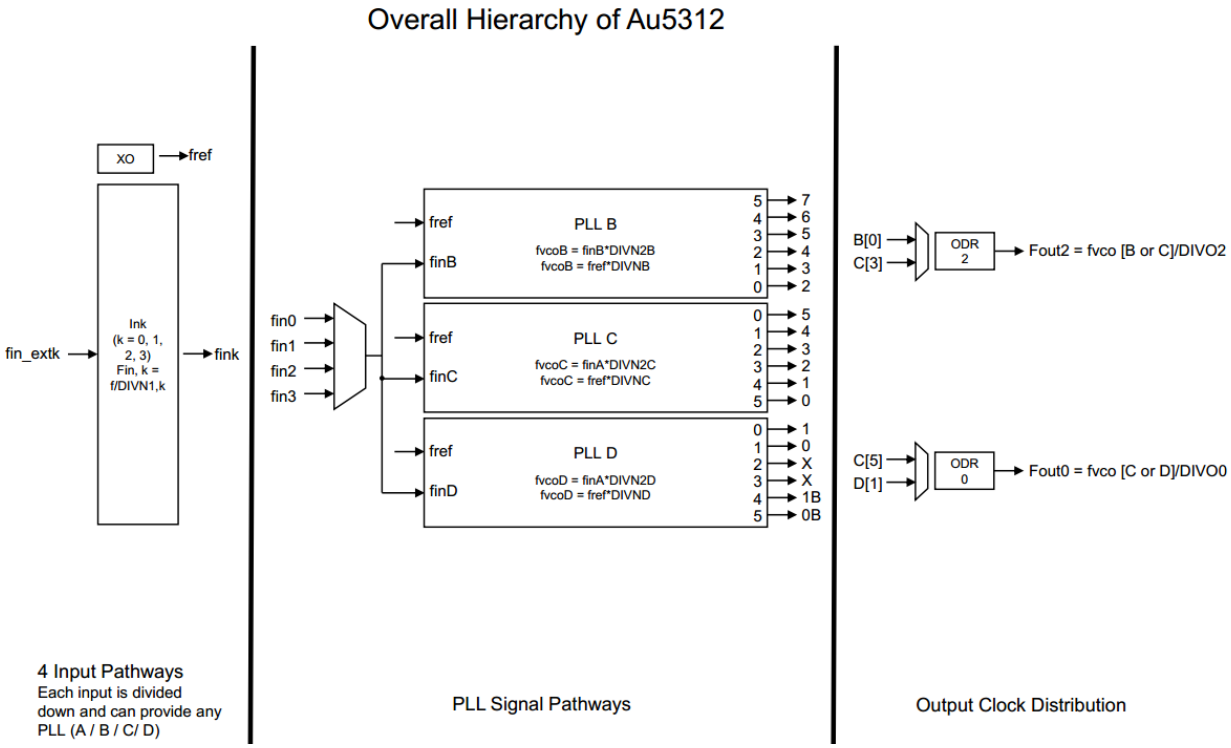


Figure 12 Au5312 & Au5322 Overall Hierarchy of Clocks

The four input clocks with frequencies fin_extk translate to PLL input clocks fink following division by the respective input dividers with fractional or integer frequency division ratios DIVN1k where the index k ϵ {0, 1, 2, 3}. See Figure 10, Figure 11 and Figure 12. All of the PLLs choose one of the four divided input clocks fink as its active input clock and set the priority for up to three spare clocks from the remaining three input clocks if required for hitless switching to a redundant input.

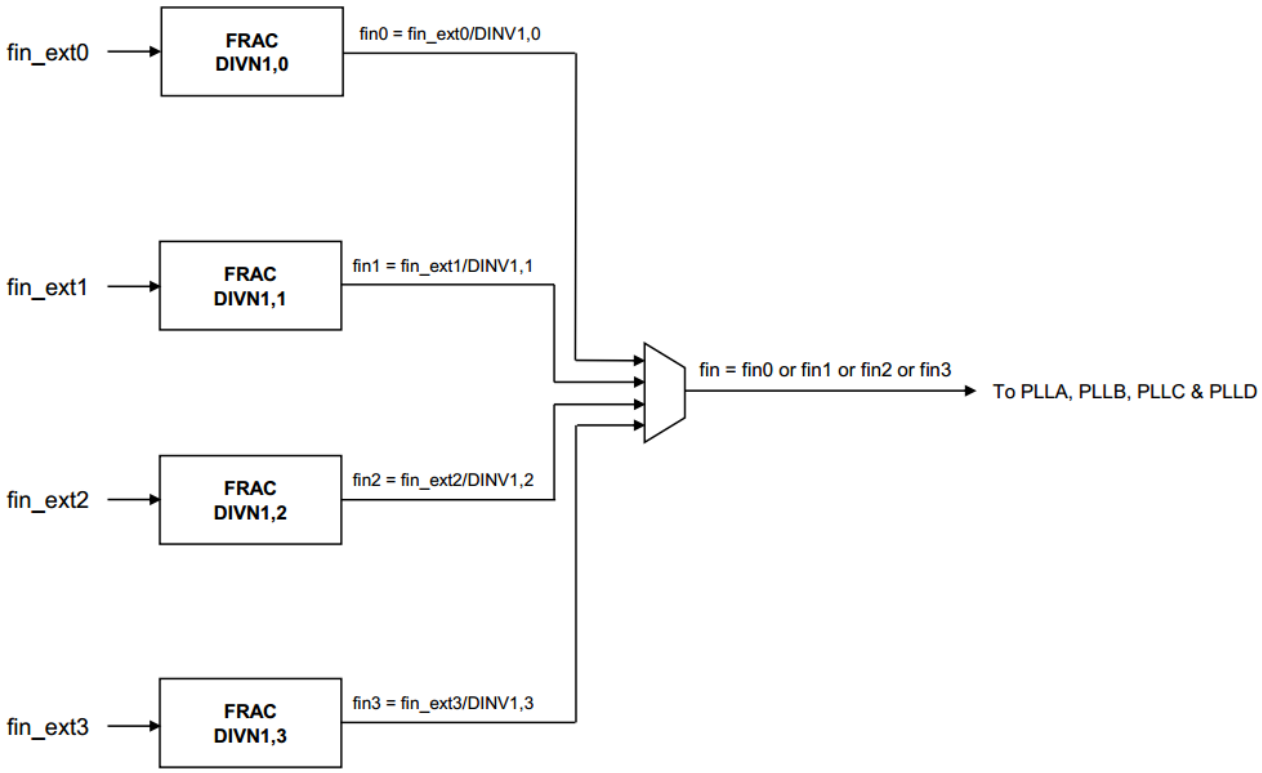


Figure 13 Input Clock Distribution

The crystal oscillator reference input (called fref) is also routed to each PLL. A TCXO or OCXO based input reference clock can also be used directly in place of the crystal oscillator. Each PLLx (x ϵ {A, B, C, D}) has a high frequency VCO whose frequency is determined in the free run mode by fref with the relation fVCOx = DIVNx*fref. In the frequency translation synchronized mode, the VCO frequency is corrected from its free run frequency to satisfy the relation fVCOx = DIVN2x*finx where finx is chosen from one of fink input clocks per the desired input clock priority for PLLx. Nominally the fractional dividers DIVNx and DIVN2x are chosen such that the relation DIVNx*fref = DIVN2x*fin,x = fVCOx is satisfied. See Figure 14.

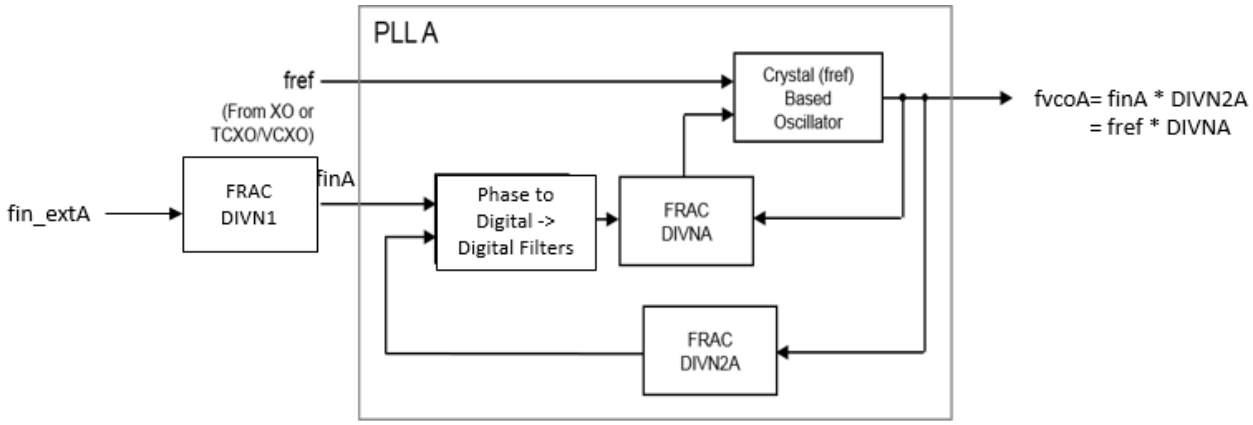


Figure 14 PLL Dividers

Each of the Output Drivers (ODRj, j ϵ {0, 1, 2, 3, 4, 5, 6, 7, 0T, 0B}) then chooses an appropriate VCO frequency and divides it using their respective integer divider DIVOj to get the output frequency foutj.

See Figure 15, Figure 16 and Figure 17.

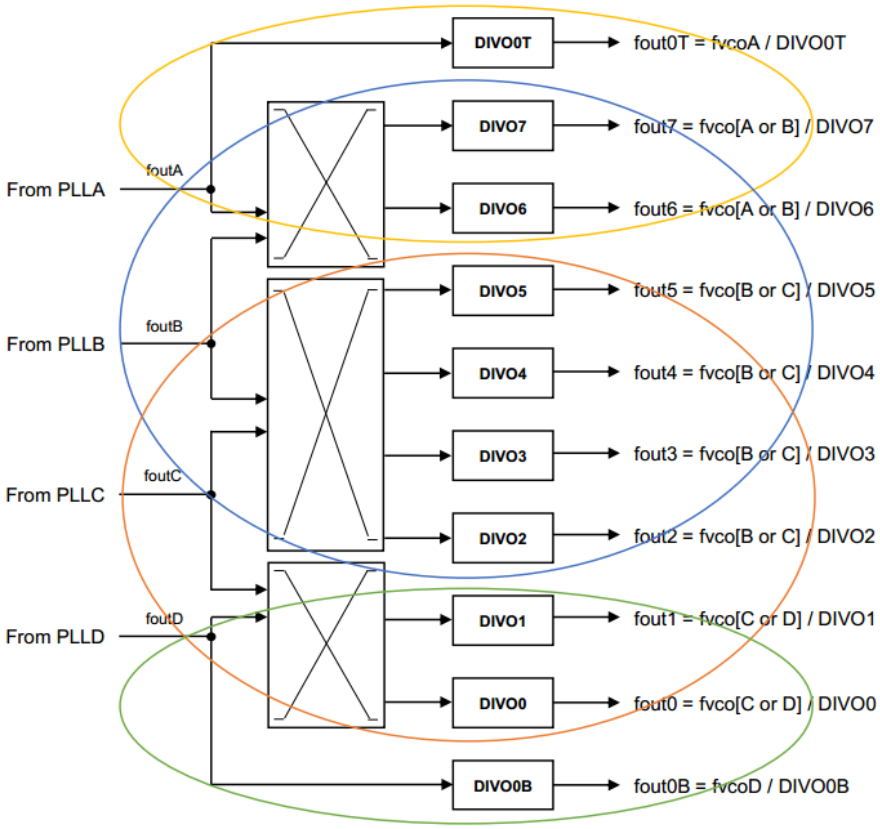


Figure 15 Au5315 & Au5325 Output Clock Distribution

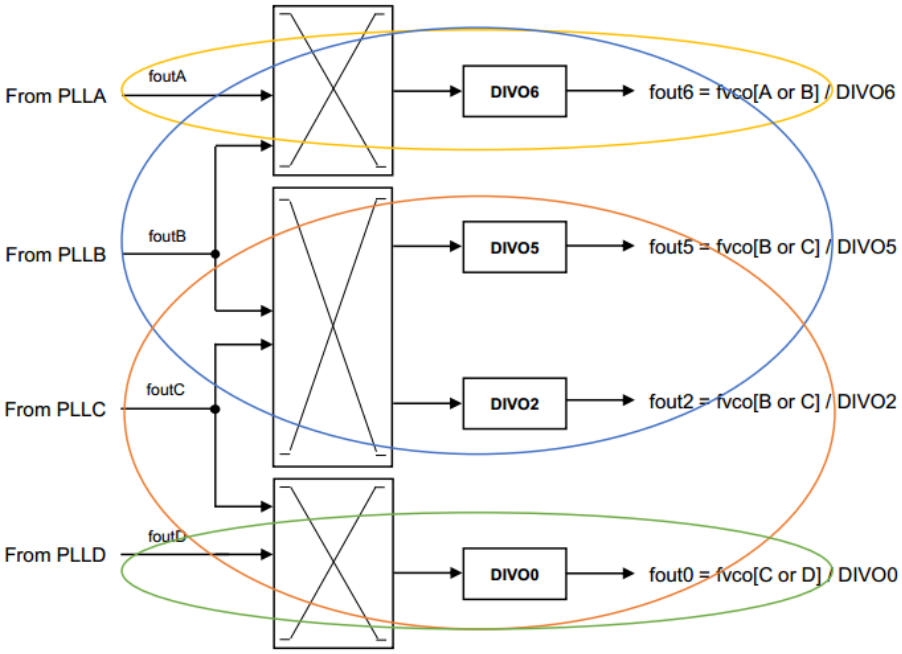


Figure 16 Au5314 & Au5324 Output Clock Distribution

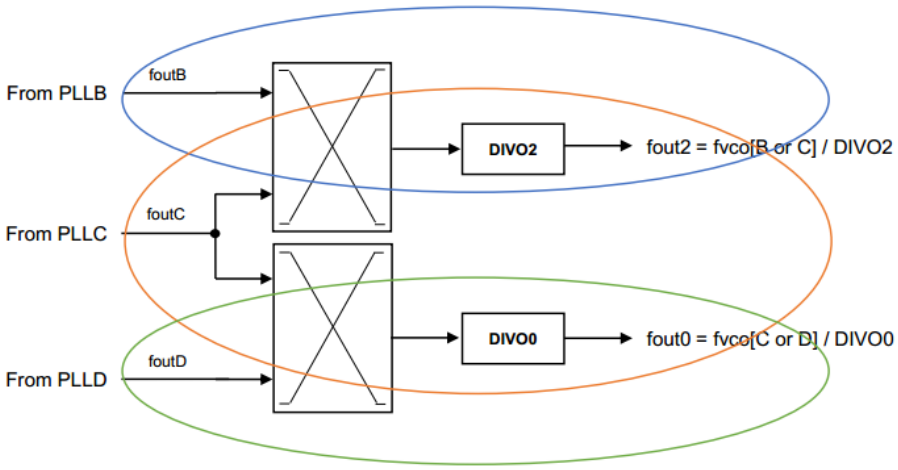


Figure 17 Au5312 & Au5322 Output Clock Distribution

The choice of the fractional dividers {DIVN1k, DIVNx, DIVN2x, DIVOj} as well as the placement of foutj frequencies at various outputs is facilitated by associated software tools.

The digital architecture of the chip is partitioned into a master digital controller and seven slave controllers. The master controller and each of the seven controllers has an associated volatile programmable interface (PIF). The overall PIF structure is a register map that is divided into several pages according to function. Each controller (master and slaves) has an associated unique Page number. Each Page has an independent 8 bit addressable PIF memory. In all the pages, the last address, FF, holds the current page number and is reserved for changing the page. The current page to be communicated with can be set by writing the page number in hexadecimal form {0x00, 0x01, 0x02, 0x03, 0x0A, 0x0B, 0x0C, 0x0D} corresponding to pages {0, 1, 2, 3, A, B, C, D} in the address FF on any page. Table 16 shows a summary of the PIF contents residing on each page.

Table 16 PIF Description

Page	Contents	Summary of contents
0	Master	All Generic Information related to the chip Chip Configuration details Control for the master sequencer FSM Crystal Reference Related Information Fuse Pointer for each of the remaining pages
1	ClkMon Slave	Clock Loss related function Frequency Drift related function
2	Input Slave	Input 3 / 2 / 1 / 0 related information (Input type, DIVN1 divider configuration)
3	Output Slave	Flexible Outputs 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0 (ODR Standards, DIVO, Programmable delay configurations for each)
		Fixed Outputs 0T / 0B (ODR Standards, DIVO, Programmable delay configurations for each)
A	PLL A Slave	All PLL related functionality
B	PLL B Slave	All PLL related functionality
C	PLL C Slave	All PLL related functionality
D	PLL D Slave	All PLL related functionality

4 Master and Slaves: Architecture Description and Programming Procedures

The Master controller is the first system to autonomously wake up on the application of power to the chip due to on-chip power on reset circuitry. All generic system information resides in the Master controller memory and it proceeds to wake up the Slaves as required based on this information. The relative wake up sequences of the Master and the various Slaves are described in more detail later in this section after a description of the memory structures. A complete power up of the chip is also emulated with the release of an active low hard reset (RSTB) from pin while selective Master and Slave sub-system resets are enacted from software using the serial interface (I2C/SPI).

The Master memory structure is shown in Figure 18. It contains a one-time programmable non-volatile memory (NVM) that stores the settings for the chip associated with the master controller. The master controller also contains a volatile PIF bank (NVMCopy) that has an exact copy of the NVM at every chip power up. This NVMCopy is the memory that is addressable using the serial interface (I2C/SPI) on Page 0 and can be overwritten from the I2C/SPI interface. The “Chip Settings” is the memory space that is not addressable from the I2C/SPI control and is the actual control for the chip. The NVM contains a two bit “Lock Pattern” that can be set to “10” or “01” to ‘lock’ the chip configuration once the final configuration is determined and wake up of the entire chip is desired in this configuration. Additionally, there is a bit in the NVM that is an active low indicator of a manual wake up. This bit set to “1” along with the ‘lock’ for the configuration leads to an autonomous wake up of the chip using the ‘locked’ configuration. Any number of different configurations can alternatively be tried at all times using only the volatile NVMCopy PIF section. This is useful for evaluations as well as allowing real time programming of the chip in various configurations with complete flexibility. The Master Controller finite state machine (FSM) described later in this section controls the device behavior in accordance with the configuration in this memory structure and as per the wake up mode.

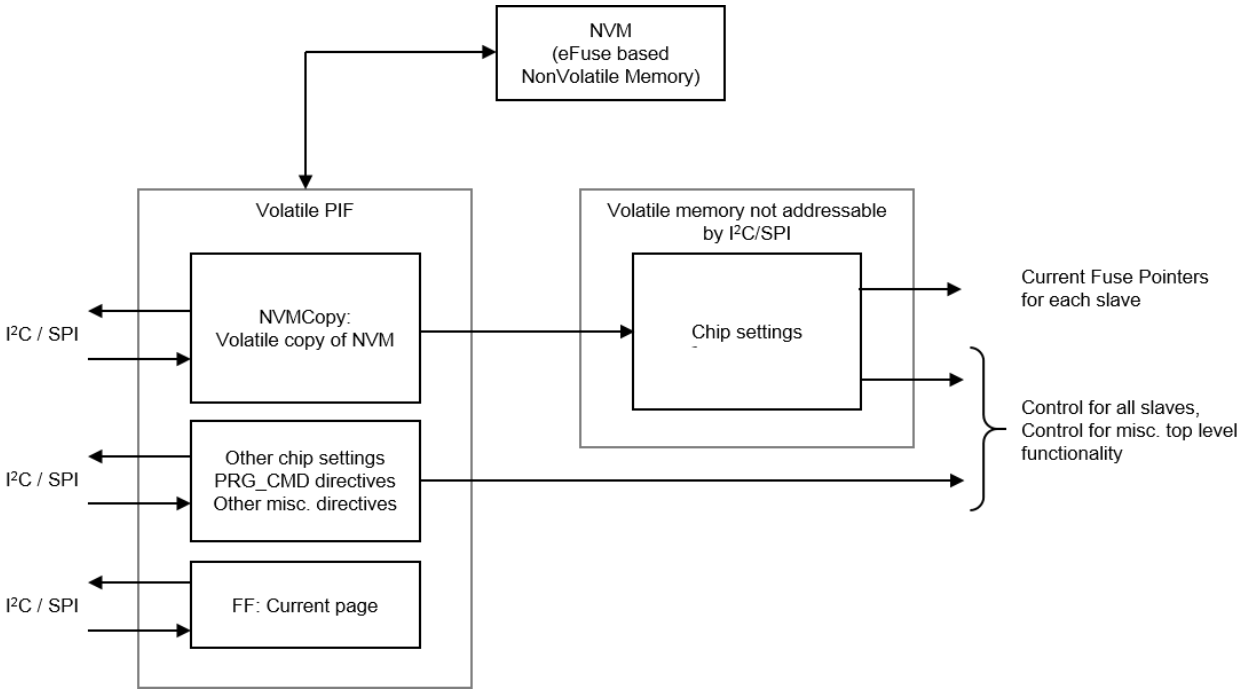


Figure 18 Master Memory Structure

The memory structure for each slave is shown in Figure 19 and is similar in construction to the master controller memory structure with some minor differences. The NVMCopy volatile PIF for the slave is addressable by the serial interface with the unique Page number associated with the slave. The “Slave Settings” is the memory space that is not addressable from the I2C/SPI control and is the actual control for the slave. Each Slave has a two time programmable NVM by virtue of two copies of the NVM memory. This makes the slave settings two time programmable with the fuse pointer from the master controller determining which of the two NVM banks is used.

The presence of two NVM banks is transparent to the slave controller since the current pointer which determines which of the two NVM banks is used is set by the master controller independently.

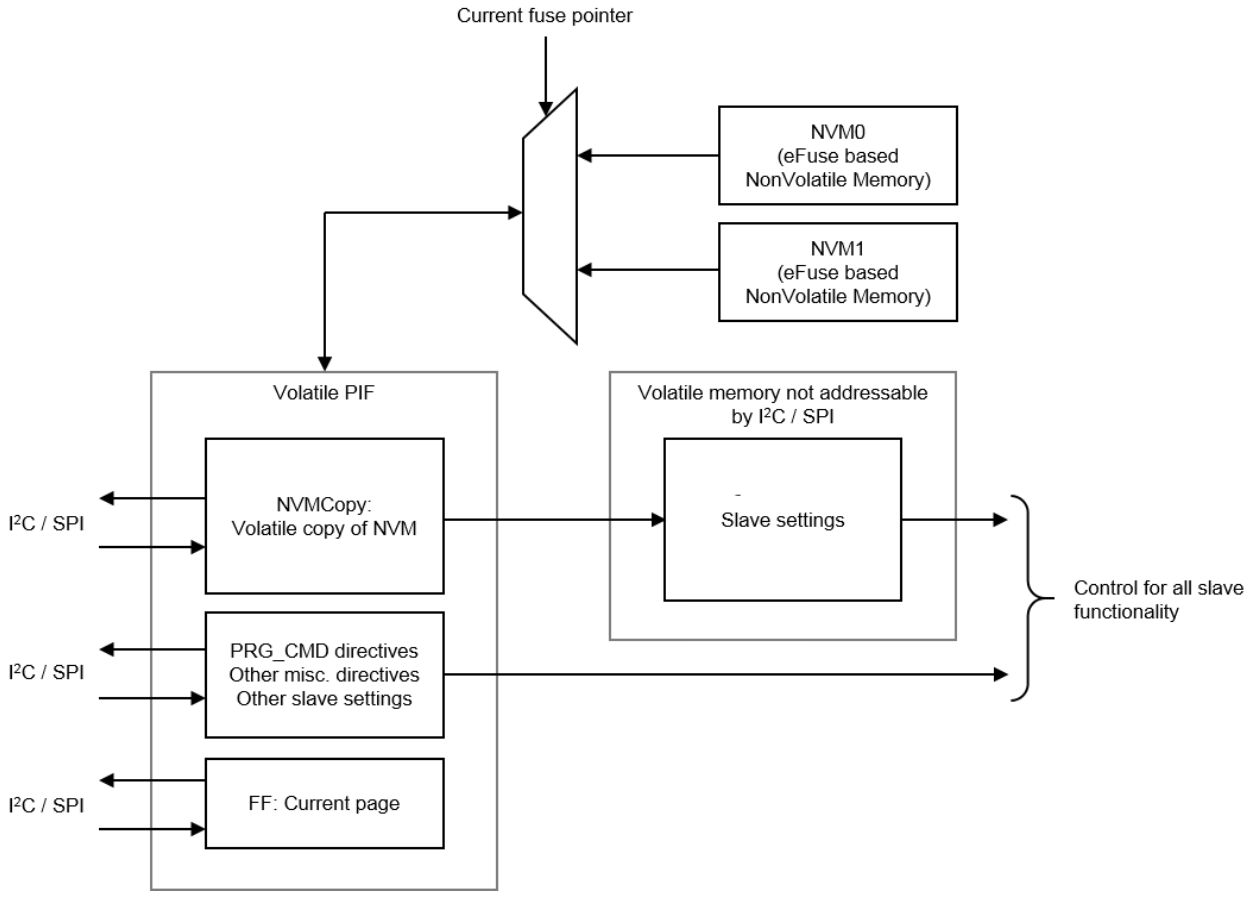


Figure 19 Slave Memory Structure

The Master Wake-Up Finite State Machine (FSM) is shown in more detail in Figure 20. At every power up of the device (or release from hard reset), the power-on-reset circuitry resets all systems and then autonomously releases only the master controller from reset. The NVM contents are copied to the NVMCopy volatile space on Page 0 which is in turn copied to the “Chip Settings”. The master controller now decides if the chip configuration is locked and it is an autonomous wake up of the entire chip or if a manual wake up is desired through the PIF based on the contents in the “Chip Settings”.

In case a “Lock” is detected and an autonomous wake up is desired, the Master controller proceeds to enable the Crystal oscillator and associated fref pathways followed by the Slave systems in a pre-determined sequence. This finally leads the chip to the “Active State” with all desired outputs available as a result of all slave systems released from reset by the master controller. This is according to the requested settings that are programmed in the Master and the Slave NVM banks.

For the case where the final chip settings are not frozen hence the “Lock” pattern is not exercised, the master controller FSM reaches the Program Command Wait State (PRG_CMD). The desired chip settings can be written in the NVMCopy on Page 0 using the serial interface and desired slave sub-systems can be enabled. Several PRG_CMD state directives are available that are exercisable only in this state. Using these directives, the desired settings written in NVMCopy can now be copied to “Chip Settings” followed by issuing the directive for the FSM to proceed to the “Active” state where each slave can now be manually written with the desired settings and in turn asked to proceed to its “Active” state.

A similar “Lock” pattern is available in the NVM bank of each slave. The currently used NVM bank for a slave (as determined by the current pointer from the master controller) can be locked for the autonomous wake up of each slave. The slave wake-up FSM is shown in Figure 21 and it similarly has a PRG_CMD state with associated directives. On Proceed to Active state directive on the slave, the slave controller wakes up the various blocks in its sub-system with the correct pre-determined sequence.

The NVM bank for the master and each slave can be programmed with a PRG_CMD directive in that state to lock a configuration / setting specific to the respective sub-system.

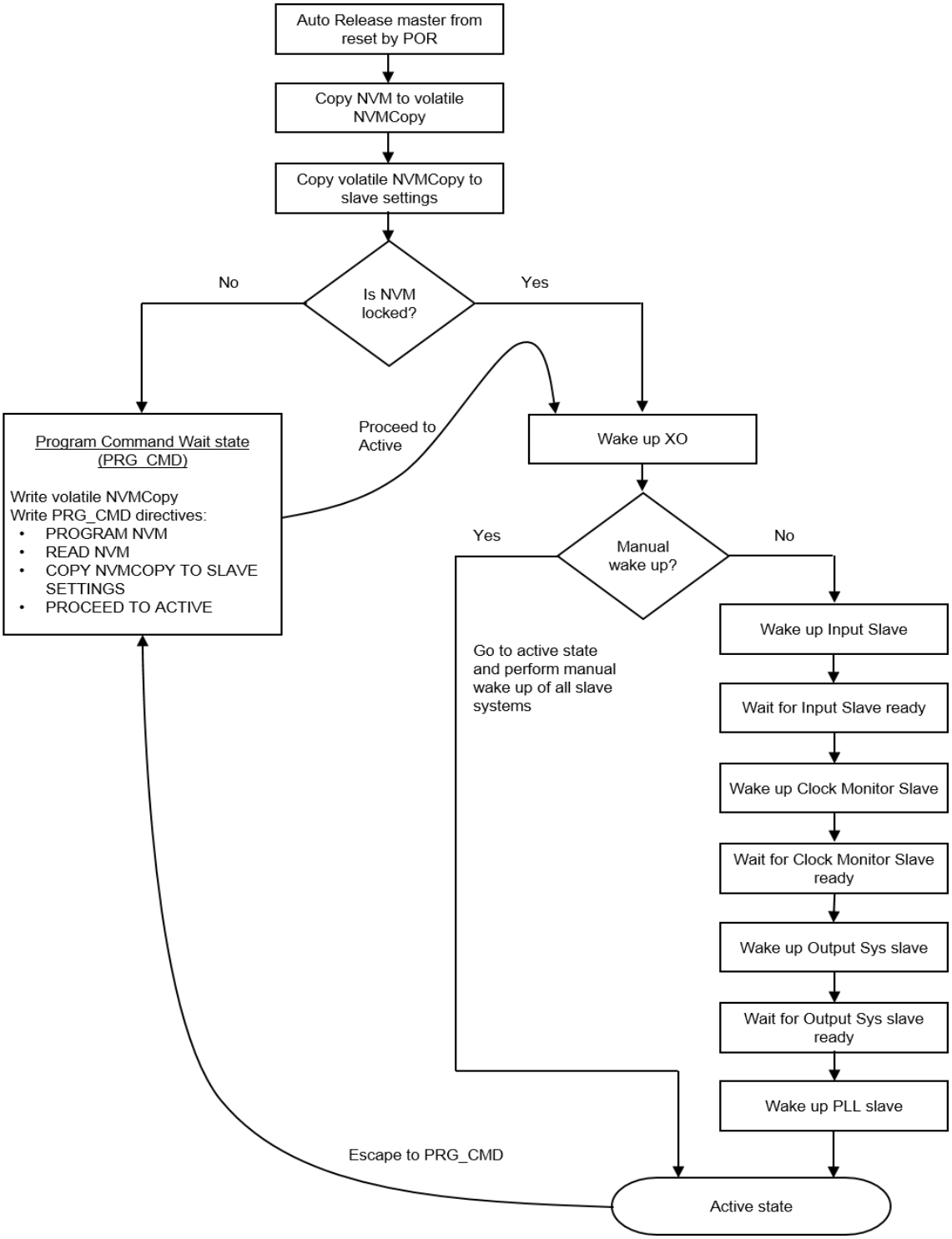


Figure 20 Master Wake-up Finite State Machine

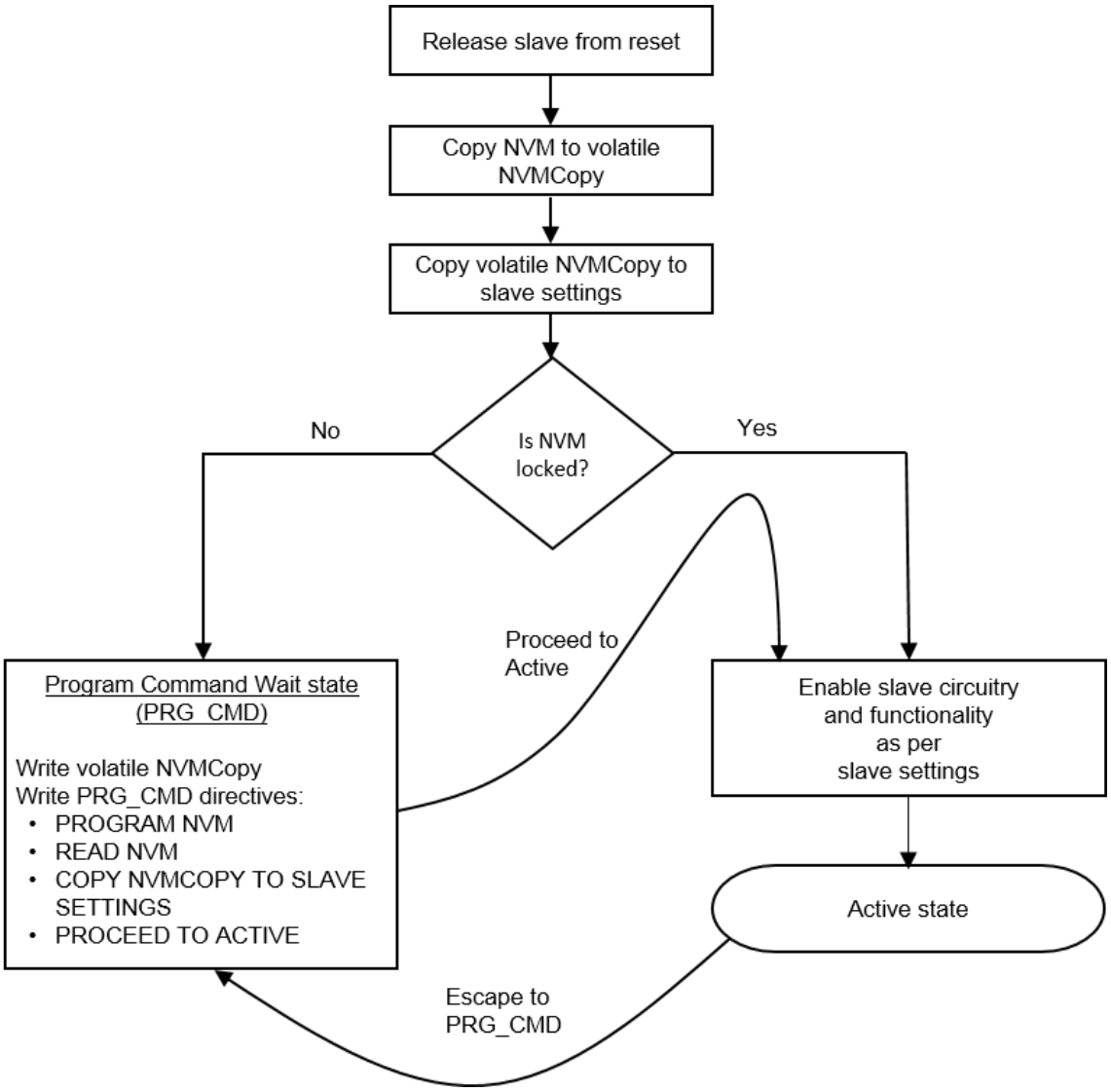


Figure 21 Slave Wake-up Finite State Machine

Each FSM (Master and Slaves) allows an escape sequence to go back to PRG_CMD state from its Active State. This can be used to selectively change the settings for that particular sub-system. Such an escape to the PRG_CMD state in the master FSM can be used for example to change current NVM pointers for any of the slaves.

Note that the NVM for the master controller and current NVM for all slaves should be locked after writing desired settings for a completely autonomous wake up of the entire chip. The NVM pointer can then be changed for any slave independently if alternate settings are desired for that slave. In that case, the new NVM is unlocked and can be written with new settings and locked. For evaluations of the chip as well as cases where flexible on-the-fly programmable settings are desired, the chip can be used without engaging the NVM banks at all by using the NVMCopy space for the master and each slave in conjunction with the PRG_CMD directives. It is also possible to lock some of the slaves (to not re-write their settings for each wake up) while use programmable settings for other slaves.

This provides complete flexibility in terms of programming and using the chip in all scenarios.

5 Input Slave Description

Four independent clock inputs are available on the chip that can be routed to any PLL with complete flexibility. Both single ended and AC coupled differential clock inputs are possible. The input clock receiver settings (to receive a single ended or differential clock) as well as the input clock divider settings are configurable on Page 2 that is assigned to the Input Slave. It is possible to bypass the input clock divider and use the input clock directly as an input to the PLL.

6 Clock Monitor Slave Description

Various fault monitoring indicators are available on the chip. The Clock Loss and the Frequency Drift indicators are configurable with the Clock Monitor Slave that is accessible on Page 1. The specifications of these fault monitors are indicated in the specifications section of the data sheet.

Defect monitoring on any of the clock monitors can be accessed using multiple techniques. The current status of the defect is available as an Active High defect that can be read from the PIF. The “status” is a current indicator of the defect that is high only during the defect (for example during the time that a Clock Loss event is on-going). Additionally, a sticky indicator of the defect called “Notify” can be enabled in the PIF. In this case, the concerned “notify” bit is high the first time the respective defect occurs and stays high till cleared.

There are multiple FLEXIOs (Flexible IOs) available in the system that can be programmed to monitor individual “notify” signals or a combination of them (as an OR logic). The choice of which fault defect is monitored as an output on the FLEXIO pin is flexible and can be programmed. Additionally there are selected GPIOs that are hard coded for the information for the clock defects.

6.1 Fault Monitoring

The Au53xx parts provide an elaborate arrangement of fault monitoring indicators. There are 4 categories of clock monitoring that are necessary for the chip namely: Clock Loss Monitor (CL), Frequency Drift Monitor (FD), Lock Loss Monitor (LL) and XO Clock Loss Monitor (CL_XO).

Clock Loss (CL) monitors loss of input clocks defined as a pre-determined number of consecutive edges missing.

Frequency Drift (FD) monitors frequency drift of a particular clock against a pre-determined Golden Reference.

Lock Loss (LL) monitors the loss of lock in any PLL by monitoring the difference in frequency between the feedback and input clocks.

XO Clock Loss (CL_XO) monitors the loss of the XO reference that is generated from either an external oscillator (XO / TCXO / OCXO) or using the on chip XO amplifier that can work with a crystal blank on the PCB.

Each of these categories monitors the health of a particular clock for a certain failure type as illustrated in the name of the clock monitoring category.

For each clock failure observed by the clock monitor block there are two types of indicators provided to the user using the register map:

1. Live Failure Bit: There is a bit to indicate the live status of a particular failure. [Status]
2. Sticky Failure Bit: For each live failure bit there is a corresponding sticky bit that is set the first time that corresponding failure is encountered and stays set even if the failure has gone away. Only when the user clears the bit does it clear. [Notify]

The status of these can be either read from the register map or from the pins as a dynamic alarm monitoring arrangement. Additionally, sticky notify registers are available which have sticky status read back from the register map for the various defects. These can be selectively chosen to create an INTRB de-assertion on the INTRB pin as well.

An important point to note is that all of the fault monitoring indicators mentioned above that work with respect to the input clock work on the divided input clock post the DIVN1,k dividers (refer to the data sheet for the respective Au53xx part). This implies that the fault monitoring indicators use the frequency fin*k* that is input to the PLL (*k* ϵ {0, 1, 2, 3}) post the DIVN1,*k* divider translation rather than the external frequencies fin_ext*k* (*k* ϵ {0, 1, 2, 3}).

6.1.1 Clock Loss Monitors

Each of the 4 inputs (IN0, IN1, IN2, IN3) are monitored for Clock Loss in terms of missing edges to indicate a loss of input signal. The number of edges used to indicate a clock loss (or recovery from a clock loss) is programmable in the Au53xx GUI interface allowing for flexibility in choosing these thresholds. In addition there is a programmable “Wait Time” all of which are to be interpreted as follows:

Assertion of Clock Loss-

We declare a CL if “Trigger Edge” number of consecutive edges are missing. The “Trigger Edge” parameter is programmable in the chip GUI.

De-Assertion of Clock Loss-

We declare a ~CL if the clock is back and has less than “Clear Edge” consecutive edges missing. The “Clear Edge” parameter is programmable in the chip GUI.

Wait Time: After the clock is established to have returned, it is ensured that no CL error as defined by the de-assertion threshold occurs for “Val Time” seconds. This valid wait time is programmable using the chip GUI using the “Val Time” parameter which is programmable from the following options: {2 m, 100 m, 200 m, 1} sec. The use of the this valid wait time ensures that sporadic edges in the input clock (such as ones caused by noise on floating nodes or intermittent unstable clock edges) does not de-assert clock loss and it is established over a user determined period of time that the input clock is available and stable.

6.1.2 Frequency Drift Monitors

Any one of the 4 input clocks or the XO clock can be used as the Golden Clock for calculating the frequency drifts of the other 4 clocks. The Golden Clock can be chosen in the GUI and is used as the “0 ppm” Reference Clock for all monitoring.

Fine Frequency Drift has a step size of ±2 ppm.

Fine Frequency Drift has a range of ±2 to ±510 ppm and an independent threshold is programmable for “Set” (for setting the FD monitor) and for “Clear” (for clearing the FD monitor).

Fine Frequency Drift has an implicit hysteresis with resolution of ±2 ppm since the same range is available for the FD assertion and de-assertion. Use of hysteresis prevents unwanted oscillation of the FD monitor output at the decision threshold and is recommended for robust operation. The value of the FD threshold hysteresis is implicit in the choice of the set and clear thresholds.

The Fine Frequency Drift monitors provide precise information for input clock frequency drift. However, since the resolution of the measurement determines time for the measurement- an alternate faster measurement mechanism for drift is needed. This is Coarse Frequency Drift which has coarser measurement but is fast. It is available for cases where the drift is very fast in the input frequency and is programmable from options as shown below.

Coarse Frequency Drift has a step size of ±100 ppm.

Coarse Frequency Drift has a range of ±100 to ±1600 ppm and an independent threshold is programmable for “Set” (for setting the FD monitor) and for “Clear” (for clearing the FD monitor).

Coarse Frequency Drift has an implicit hysteresis with resolution of ±100 ppm since the same range is available for the FD assertion and de-assertion. Use of hysteresis prevents unwanted oscillation of the FD monitor output at the decision threshold and is recommended for robust operation. The value of the FD threshold hysteresis is implicit in the choice of the set and clear thresholds.

Important Note regarding the above monitors with respect to clock switch in the PLL:

Normally the CL monitor is used for ascertaining a clock is lost for the PLL to switch to a secondary reference or proceed to Holdover. However, the Fine and/or Coarse FD monitors can also be used in addition to the CL monitor to cause a PLL switch. This implements an "OR" logic for the FD Monitors to be used in addition to the CL monitors for triggering a PLL input clock switch or entry to Holdover. This is programmable as an option in the GUI.

6.1.3 Lock Loss Monitors

Lock loss is programmable for each PLL with lock loss triggered if the frequency of the input reference to the PLL phase detection arrangement and the feedback clock to same PLL are different as per the programmed assertion and de-assertion thresholds.

The Set threshold for asserting the LL monitor is programmable from {±0.2, ±0.4, ±2, ±4, ±20, ±40, ±200, ±400, ±2000, ±4000} ppm while the Clear threshold for de-asserting the LL monitor is programmable from {±0.2, ±0.4, ±2, ±200} ppm. A pre-determined level of hysteresis is implicit by choosing appropriately the set and clear thresholds for the LL monitor.

Additionally from the point of view of LL de-assertion, there is a delay from the point in time that lower than the specified ppm value is achieved to the point where the actual LL is de-asserted to the user such that LL never asserts during this delay period. The choice of this delay is with a timer that ensures that the delay is in line with the BW of the PLL loop. It is fully programmable from the GUI and is useful to ensure complete settling of the PLL without un-necessary toggling before LL de-assertion.

6.1.4 XO Clock Loss Monitors

The XO Clock Loss Monitor asserts the XO Clock Loss Alarm when the external reference input to the X1 pin (XO or TCXO or OCXO) or the internal XO clock generated with the crystal blank is not available.

7 Output Slave Description

The Output Slave accessible on Page 3 is used to configure the output divider (DIVO) and output standard for each output individually. The output load and terminations for each differential output standard are shown in the Output Terminations section of the data sheet. The LVDS and LVDS Boosted modes are recommended for AC coupled termination loads with the termination at the far end. Additionally, an internal termination mode for differential outputs is available where the resistive terminations are internally provided and a differential output is available that can be AC coupled to a clock receiver. The differential clock output pins are shared for LVCMOS outputs as well. LVCMOS outputs can be either enabled on both outputs individually or on any one of the two differential outputs {OUTjP, OUTjN}. The LVCMOS outputs can be used in-phase or out-of-phase on {OUTjP, OUTjN} in case both outputs are chosen. Out of phase LVCMOS toggling on the complementary outputs is recommended for best spur performance.

8 PLL Slave Description

All settings with respect to each PLLx slave (*x* ϵ {A, B, C, D}) are accessible on the respective Page {A, B, C, D}. The PLL architecture is shown in Figure 22. There are three distinct modes of operation of the PLL: free run mode, synchronized mode and holdover mode. The frequency of the high frequency VCO in the PLL is determined by the specific mode of operation. The VCO frequency is then divided down to get the output frequency on the ODR as described with relation to the overall hierarchy of clocks described earlier.

The PLL in the free run mode can be described as a crystal based oscillator where the output frequency is determined by the relation fVCOx = DIVNx*fref. This is the mode of operation before the loop is locked to the selected input clock or the mode of operation for the case none of the input clocks is available. After locking to the chosen input clock, the PLL enters the synchronized mode of operation where the output is now locked to the input frequency with the relation fVCOx = DIVN2x*finx. The PLL Loop that synchronizes (locks) the output to the input clock has a programmable loop bandwidth between 1 mHz to 4 KHz and is not affected by static or dynamic drifts in the crystal oscillator based fref frequency. In case the input clock is lost, the PLL locks to the highest priority spare clock available. If all specified input clocks are lost, the PLL remembers the correction based on historical average of the input clock as specified to enter the Holdover mode of operation.

In synchronized mode, the PLL is also able to lock to a Gapped Input clock with some edges missing producing a smooth output clock without any gaps with the requested frequency translation from input to output. Frequency translation ratios in this case should be specified with respect to the average input frequency of the gapped clock rather than the faster instantaneous frequency.

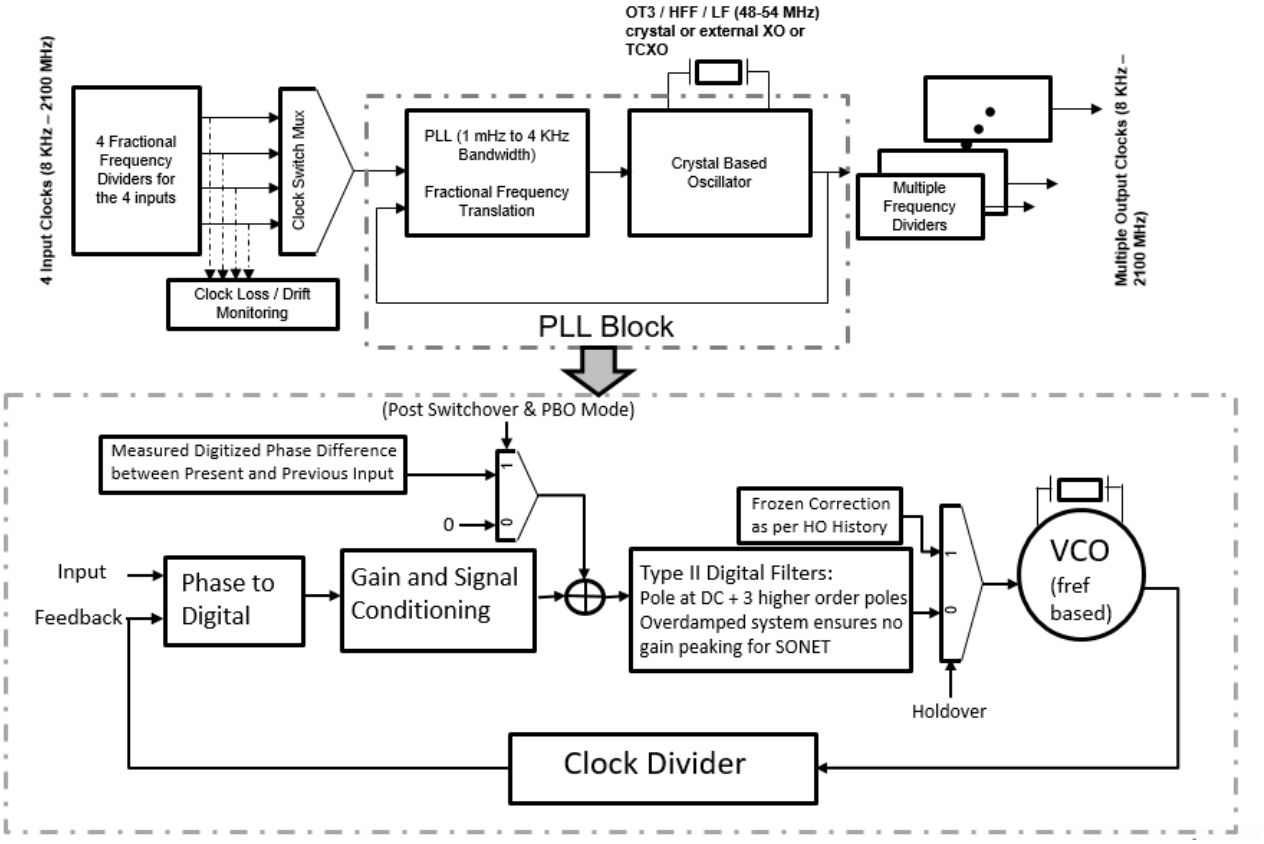


Figure 22 PLL Architecture

9 PLL Input Selection: Manual and Hitless Switching

All PLL Slaves share the same clock priority in terms of the four input clocks. This is programmed in to the Clock Monitor slave memory. The PLL Slave then looks at Clock Loss status from the Clock Monitor slave to lock to the highest priority available clock to lock. Three spare clocks with an order of priority can be specified in case the highest priority active clock is not available. Additionally, a forced manual selection of the active clock with no spares is possible. Less than three spares can also be specified making the clock priority arrangement completely flexible in terms of choosing the input clock for operation.

Phase Build Out Mode of hitless switching ensures that phase transients are not propagated to the output (the phase difference between redundant input clocks is absorbed by the PLL) and desired MTIE characteristics are seen in the output clock. This is the default mode of hitless switching for the PLL. The transition of input clock for a PLL from one clock to another is hitless in nature (with maximum phase hit limited to be less than 50 ps) for the case of the switched input clocks being same in frequency. Hitless switch is also supported for the switched clocks being fractionally related such that the same frequency can be obtained for both clocks at the input of the PLL using the input clock dividers (DIVN1k).

For redundant input clocks to the PLL that are not exactly the same frequency (plesichronous clocks), the frequency ramp feature can be enabled that ramps the output frequency of the PLL at a slope that is programmable to one of the following 4 settings: {0.2, 2, 20, 40000} ppm/s. For redundant input clocks to the PLL that are exactly the same frequency, the frequency ramp feature should not be enabled.

An alternate mode of hitless switching is the Phase Propagation mode where the phase difference between redundant input clocks is not absorbed by the PLL but is rather propagated to the output. The phase difference that is propagated to the output can either be allowed to propagate as per the PLL bandwidth or can be limited to a phase propagation slope that is programmable to one of the following 3 settings: {10, 40, 160} us/s.

Zero Delay Buffer mode is available on any of the 4 PLLs by routing the output clock back to the IN3 input. This ensures minimum delay between the input and output. It can be used for one of the four PLLs at any time.

10 Zero Delay Mode

A zero delay mode is available and can be configured for any one of the PLLs in the chip. This provides the option to close the feedback loop of the PLL on the PCB and therefore bypasses the internal feedback dividers cancelling therefore the delays introduced by internal dividers and clock distribution pathways. The IN3 input pins are used as the external feedback and any of the outputs from the PLL which is being set up in zero delay mode should be routed to the IN3 differential inputs. It is recommended to use IN0 as the input clock when using IN3 as the external feedback clock in the zero delay mode. The terminations used for IN3 would depend on the driver type chosen- the preferred option is to use an LVDS or LVDS boost output ac coupled into a differential 100 Ω termination at the IN3 input side.

The diagram below shows the configuration recommended as an example. In this example the PLLA is set up in zero delay mode with OUT0T routed in to IN3 for the ZDB feedback.

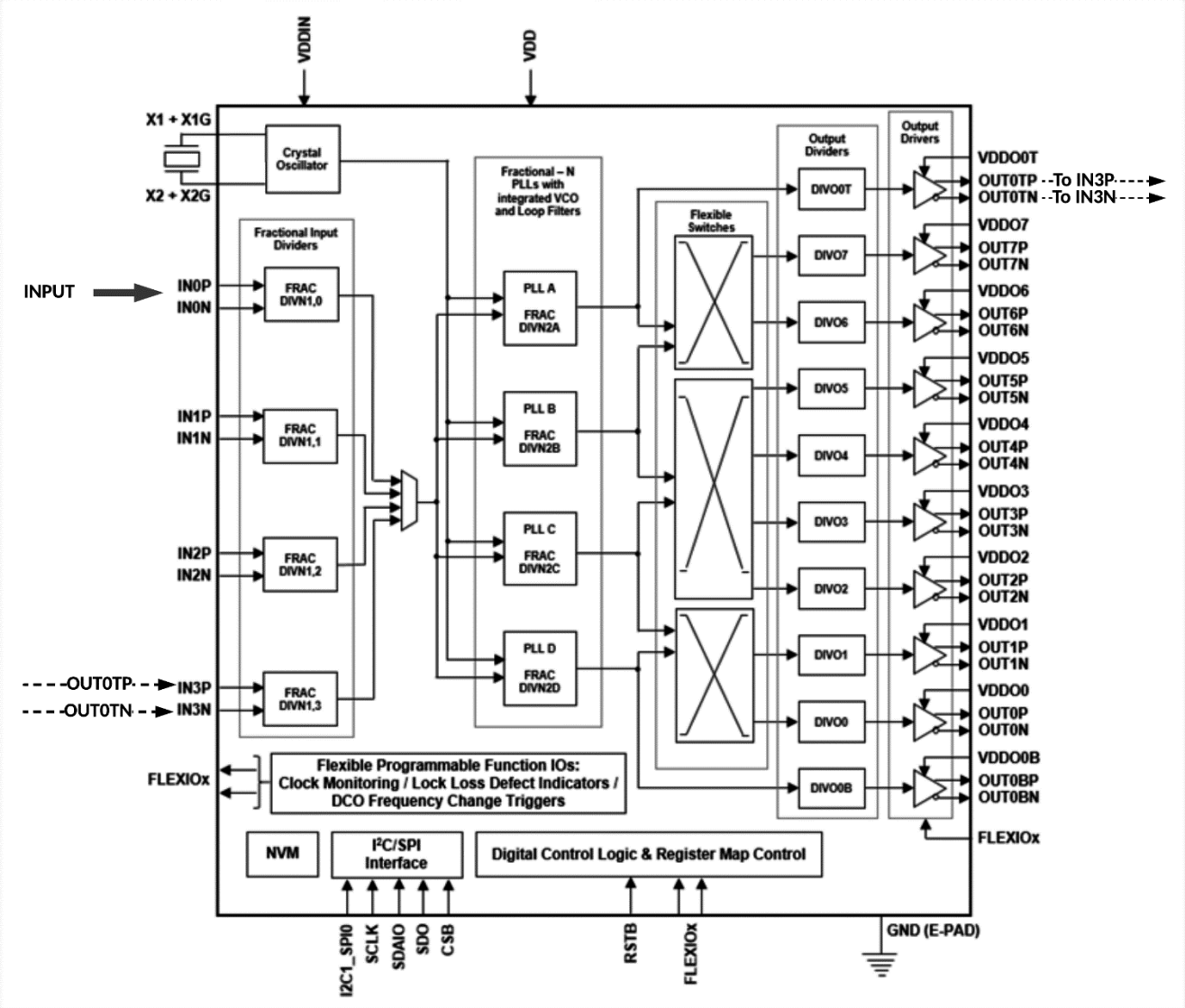


Figure 23 Zero Delay Mode Set Up: PLLA in ZDB mode with OUT0T routed in to IN3 for the ZDB feedback

11 PLL Bandwidth Control

Each PLL Slave independently chooses the Bandwidth for jitter attenuation from 1 mHz to 4 KHz. This is the bandwidth that is normally used for steady state operation. However, an independent choice for a fast bandwidth is also available that can be used for speeding up the initial lock. After the PLL lock is achieved and the system is in the synchronized mode, the bandwidth is automatically transitioned to the steady state jitter attenuation bandwidth. This feature avoids the abnormally large wake up times that may be needed for very low PLL bandwidths. For stability considerations of the PLL, the fast lock bandwidth or regular bandwidth for the PLL should be no larger than 1/100th of the input frequency at the input of the PLL (post the DIVN1k dividers).

12 PLL Crystal Clock Reference

An external crystal can be connected between the {X1, X2} pins on the die to work with the internal crystal oscillator circuitry to produce the fref clock for the system. Alternatively, a TCXO based external clock source can be directly connected on the X1 pin. The requirements for the crystal is captured in Table 10 and that of the external clock source is presented in Table 5. It is recommended to place the crystal on a floating metal island on the PCB that is provided the ground connection by the chip with the X1G and X2G pins. This metal island should not be connected to the PCB ground to prevent extraneous fref related currents to distribute on the board.

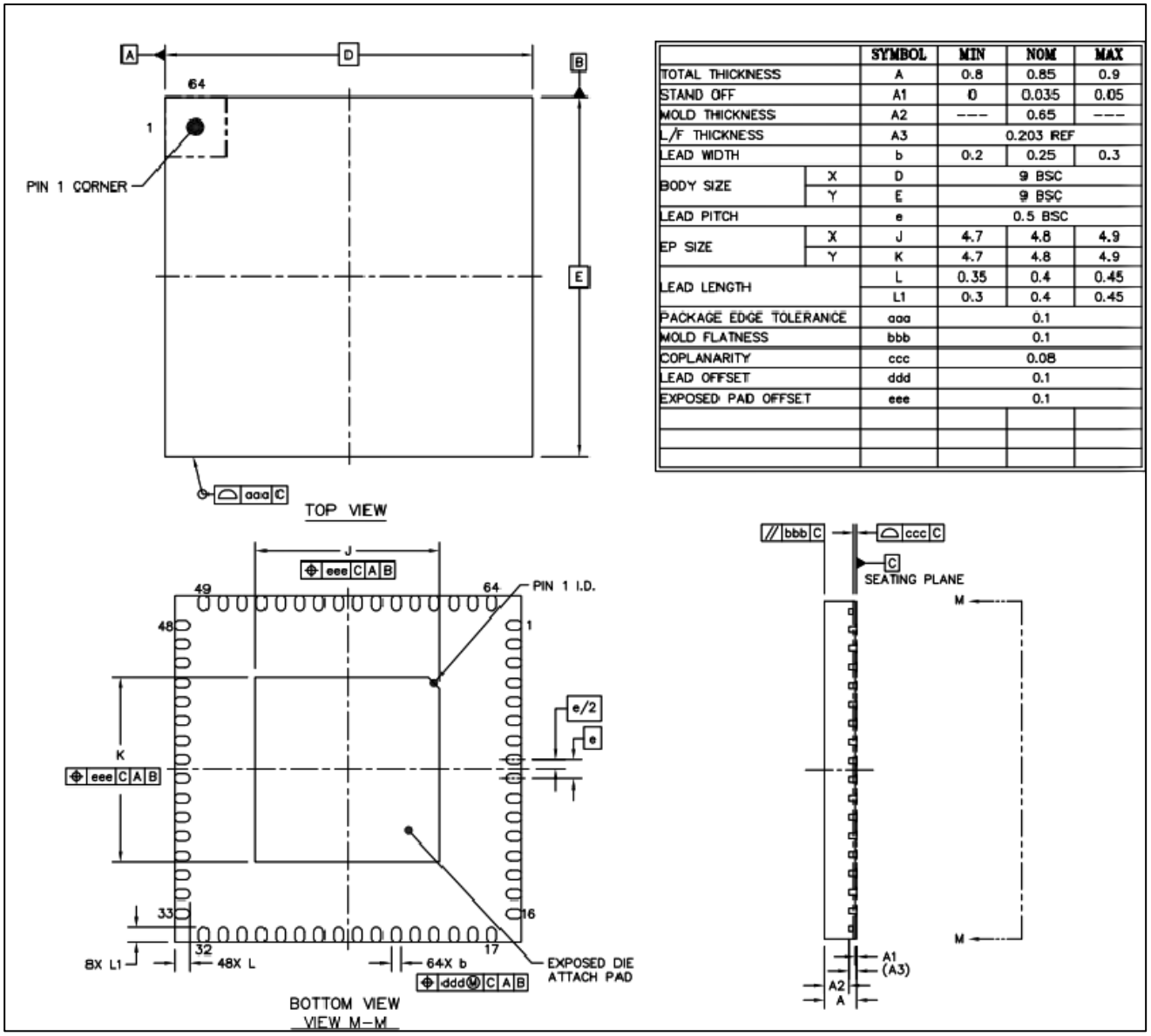
13 PLL Lock Loss Defect Monitoring

PLL Lock Loss is another fault monitor whose specifications are available in the Electrical Characteristics section of this data sheet. Various programmable thresholds are available that can be used to detect lock loss in the PLL. Lock loss is indicated by the programmable drift between the frequency of the input clock for the PLL and the divided VCO clock. Similar to the faults monitored by the Clock Monitor Slave, this defect can be tracked with status, notify and on the FLEXIOs. This defect monitoring is described in detail in the section on “Clock Monitor Slave Description”.

14 PLL DCO Mode operation

The Digitally Controlled Oscillator (DCO) mode of operation is used for changing the output frequency of a PLL using software control on the serial interface or pin control. A pre-defined change in frequency is programmed in the PIF of the respective PLL. After that an increase (FINC) or decrease (FDEC) command can be given on the PIF of the same PLL to make the change in output frequency effective. Alternatively, appropriate GPIOs are chosen for the trigger of the DCO function. A low to high transition (as an edge detect) is used for the trigger of the DCO increment or decrement. Any relative change in frequency from as fine as 5 ppt to as coarse as 100 ppm is available with the DCO mode. DCO mode is available in both free run and synchronized modes of operation.

15 Package Information

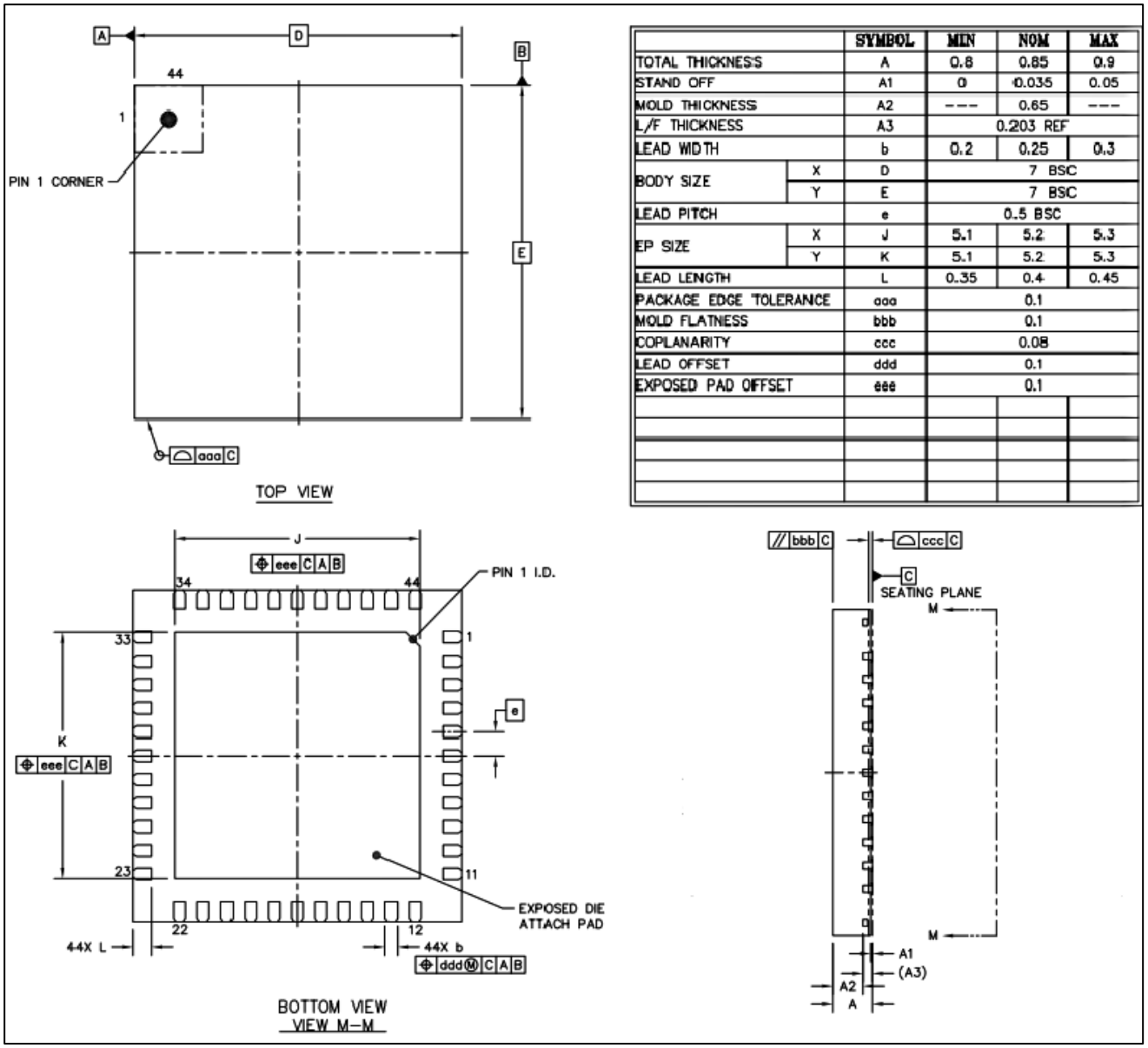


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	4.7	4.8	4.9
	Y	K	4.7	4.8	4.9
LEAD LENGTH		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 24 Au53x5: 64-QFN Package Dimensions

Notes:

1. Coplanarity applies to LEADS, CORNER LEADS and DIE ATTACH PAD
2. Total Thickness does not include SAW BURR



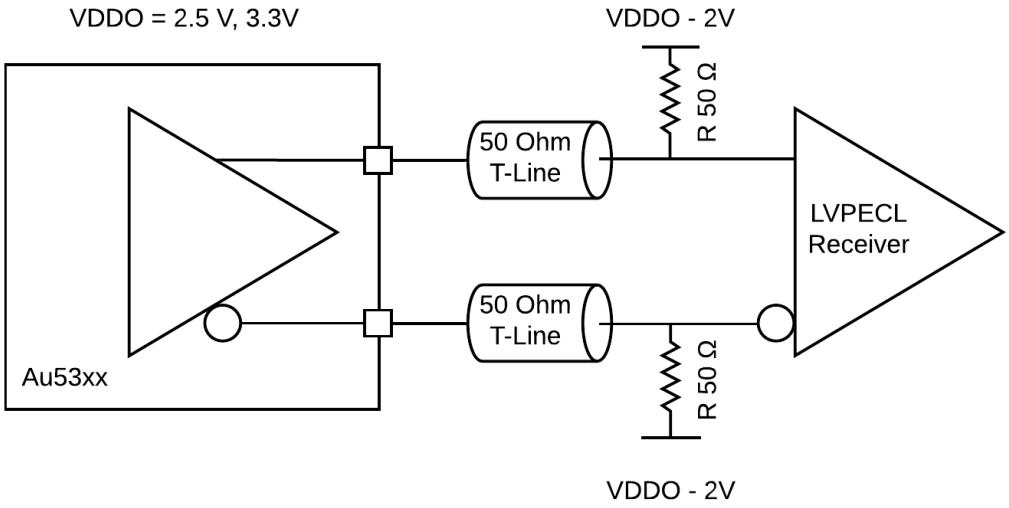
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.1	5.2	5.3
	Y	K	5.1	5.2	5.3
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 25 Au53x4 and Au53x2: 44-QFN Package Dimensions

Notes:

1. Coplanarity applies to LEADS, CORNER LEADS and DIE ATTACH PAD
2. Total Thickness does not include SAW BURR

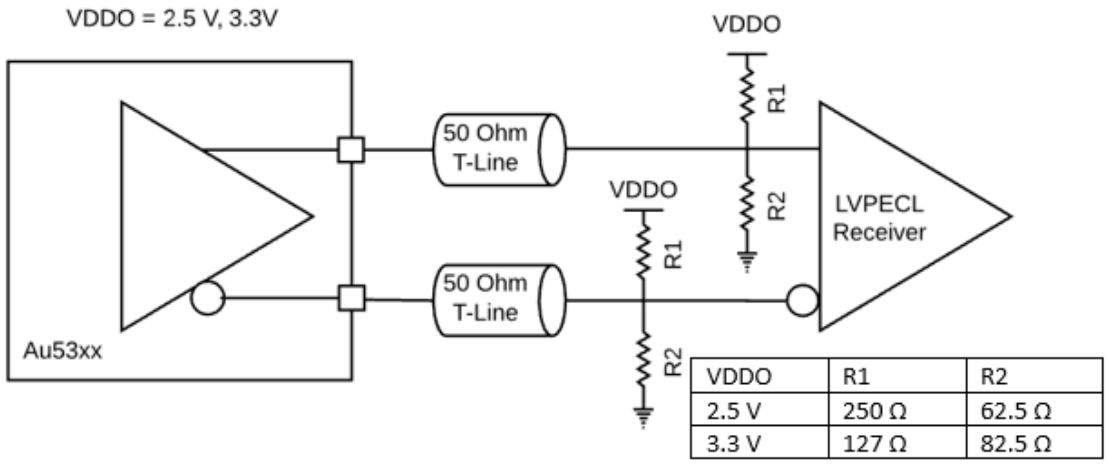
16 Output Termination Information



Traditional DC Coupled LVPECL Receiver: **Use LVPECL Standard for the Au53xx Output Driver**

Spec	Conditions	Min	Typical	Max
Output Differential Peak	Measured at 156.25M Output	450 mV	750 mV	

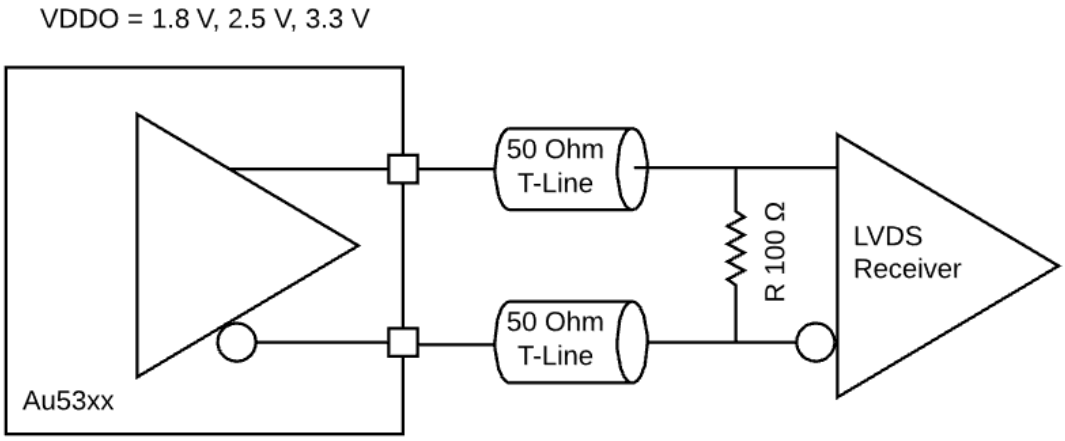
Figure 26 LVPECL DC Termination to VDDO – 2V



Alternate DC Coupled LVPECL Receiver: **Use LVPECL Standard for the Au53xx Output Driver**

Spec	Conditions	Min	Typical	Max
Output Differential Peak	Measured at 156.25M Output	450 mV	750 mV	

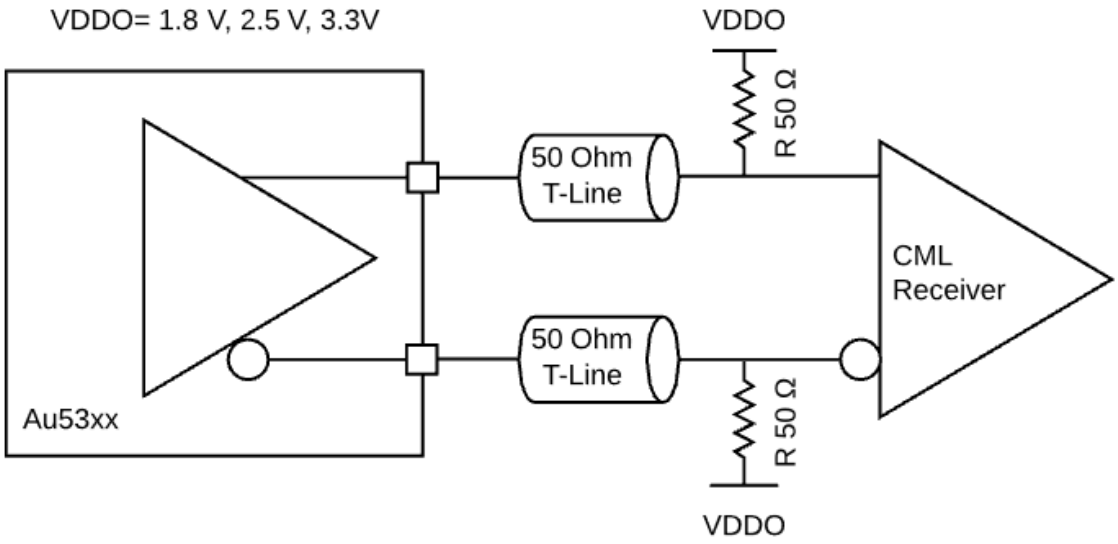
Figure 27 LVPECL Alternate DC Termination: Thevenin Equivalent



Traditional DC Coupled LVDS Receiver: **Use LVDS Standard for the Au53xx Output Driver**

Spec	Conditions	Min	Typical	Max
Output Differential Peak	Measured at 156.25M Output	247 mV	350 mV	474 mV

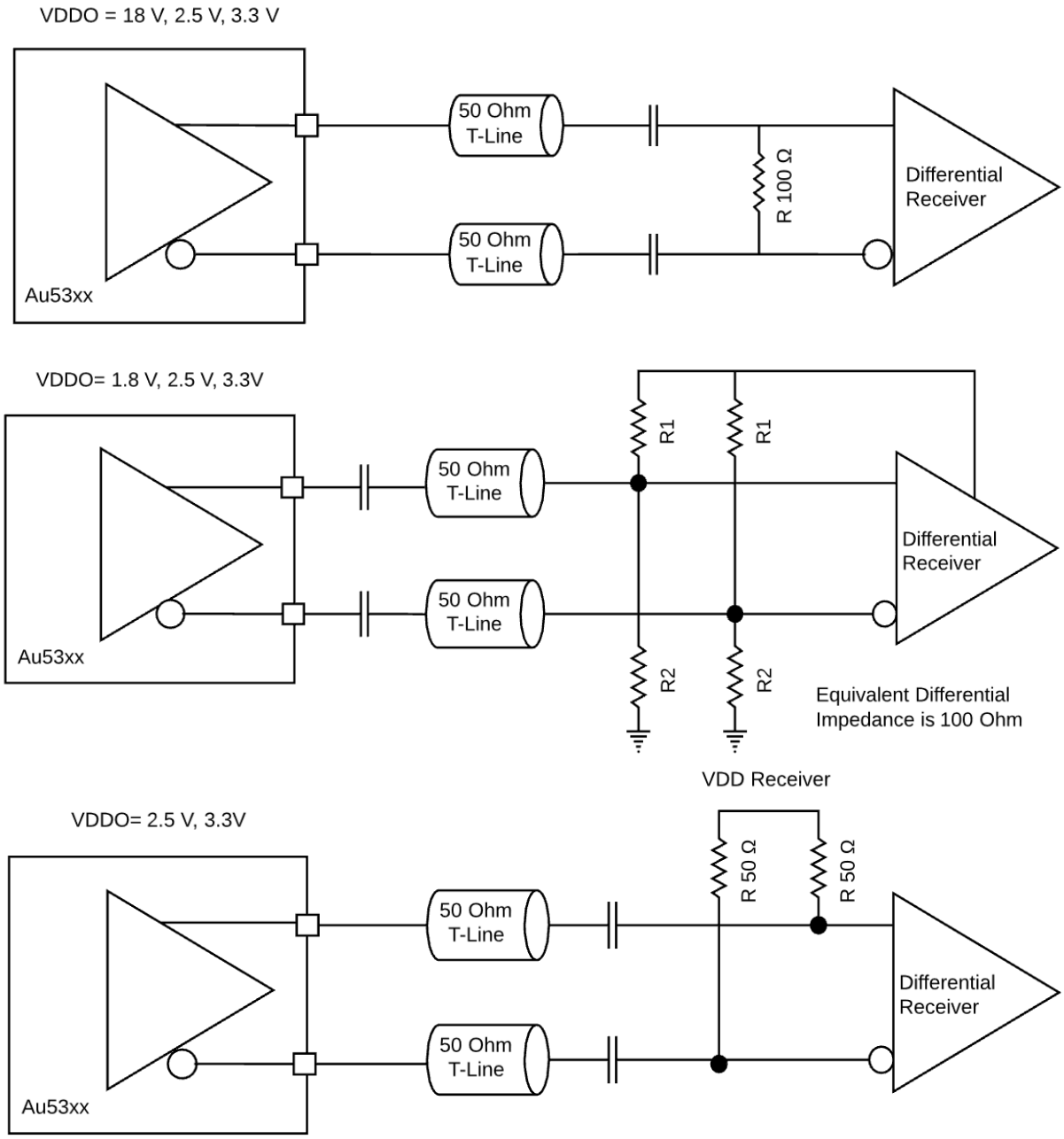
Figure 28 DC Coupled LVDS Termination



Traditional DC Coupled CML Receiver: **Use CML Standard for the Au53xx Output Driver**

Spec	Conditions	Min	Typical	Max
Output Differential Peak	Measured at 156.25M Output	250 mV	350 mV	600 mV

Figure 29 DC Coupled CML



AC Coupled Receiver side termination Option1: Use LVDS Standard for the Au53xx Output Driver

LVDS Standard works for VDDO= 1.8 V/2.5 V/3.3 V

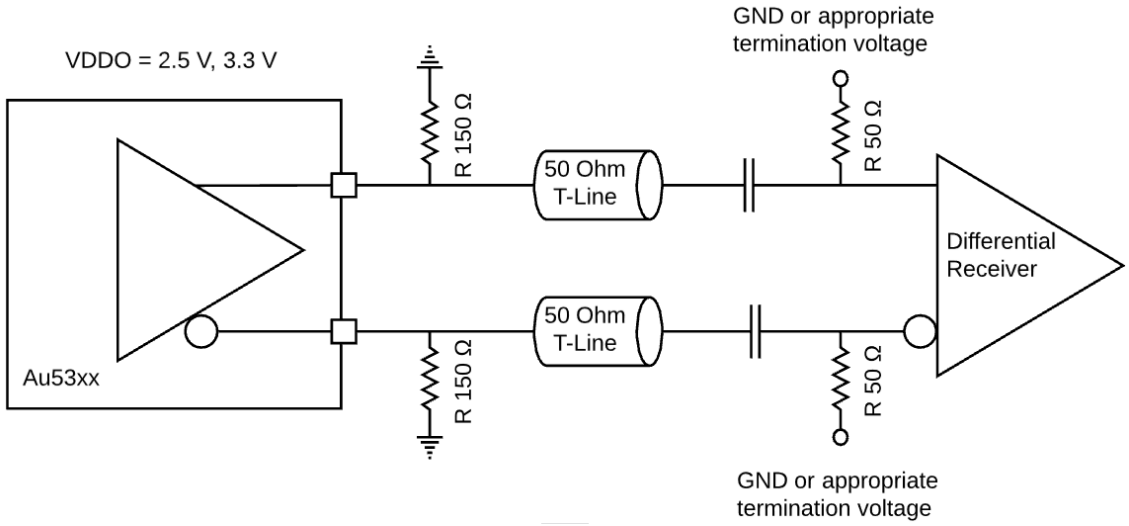
Spec	Conditions	Min	Typical	Max
Output Differential Peak	Measured at 156.25M Output	247 mV	350 mV	474 mV

AC Coupled Receiver side termination Option2: Use LVDS Boost Standard for the Au53xx Output Driver

LVDS Boost Standard works for VDDO = 2.5 V/3.3 V

Spec	Conditions	Min	Typical	Max
Output Differential Peak	Measured at 156.25M Output	500 mV	700 mV	

Figure 30 AC Coupled Receiver side resistive Termination options



AC Coupled with termination on Chip side: **Use LVPECL2 Standard for the Au53xx Output Driver**

Spec	Conditions	Min	Typical	Max
Output Differential Peak	Measured at 156.25M Output	335 mV	525 mV	

Figure 31 Alternate AC Coupled LVPECL with DC coupled resistors on Chip side

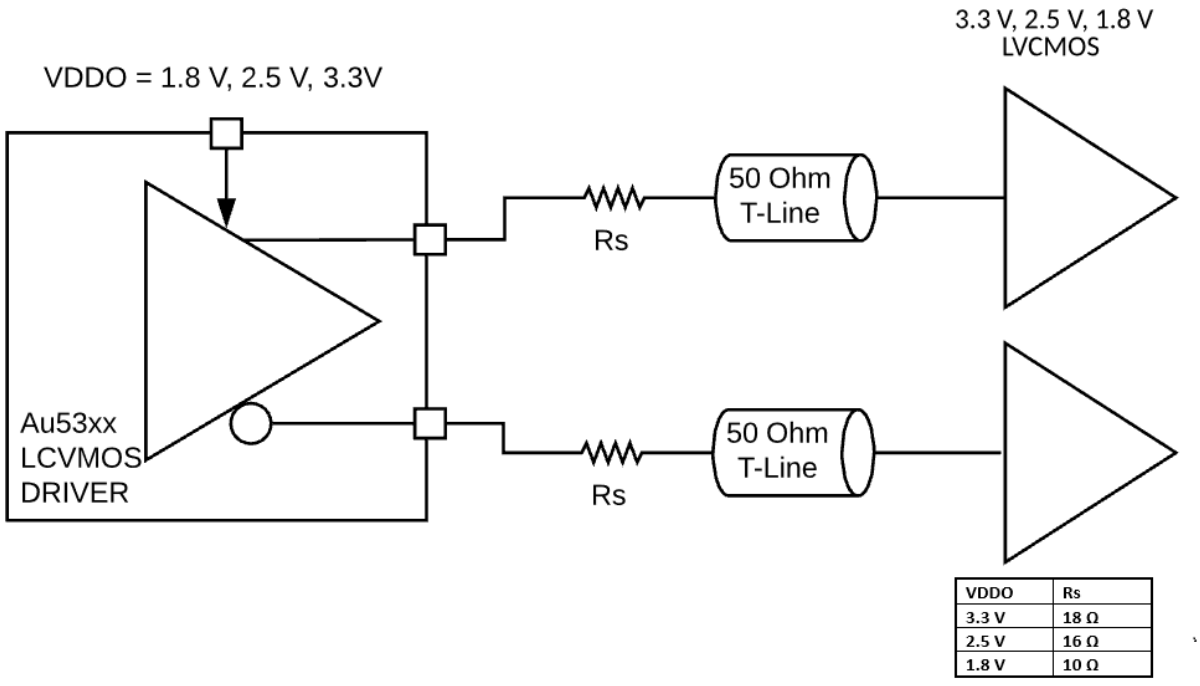


Figure 32 DC Coupled LVCMOS

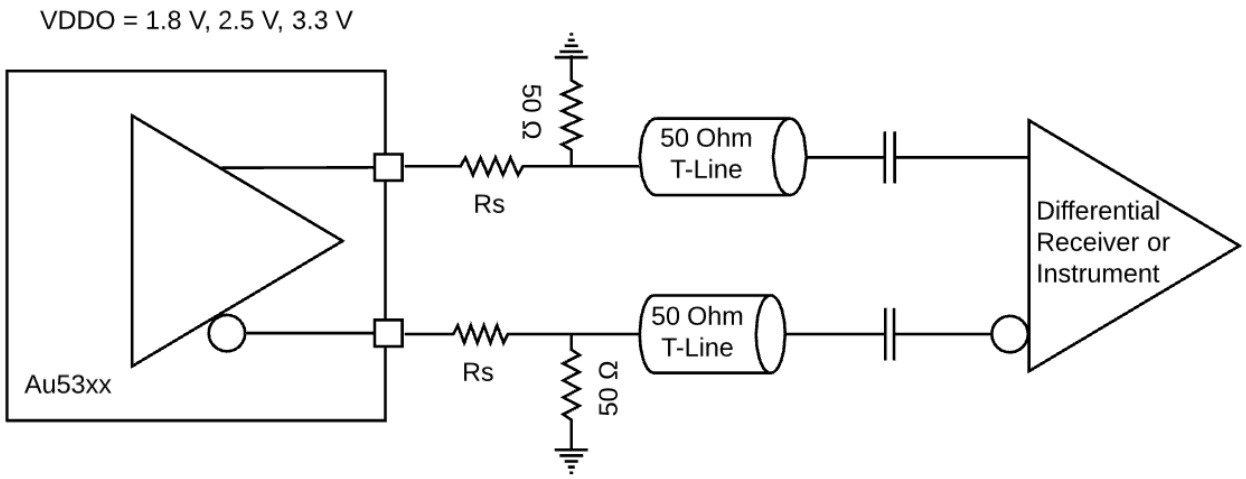


Figure 33 HCSL AC Coupled Termination. Source Terminated 50 Ohm

Note: Rs is sometimes used for limiting overshoot - Can be 0 Ohm

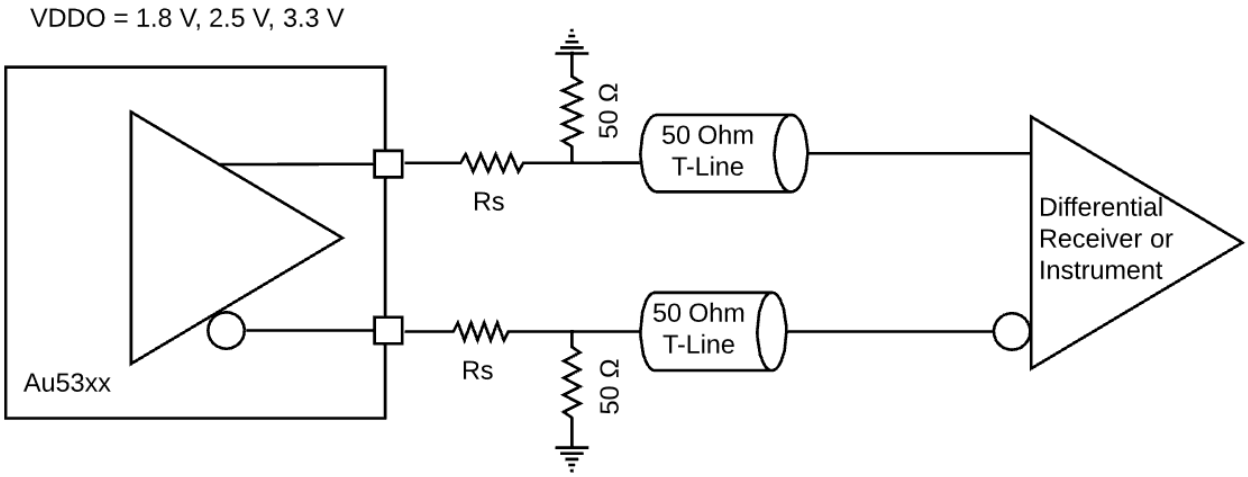


Figure 34 HCSL DC Coupled Termination. Source Terminated 50 Ohm

Note: Rs is sometimes used for limiting overshoot - Can be 0 Ohm

17 Input Termination Information

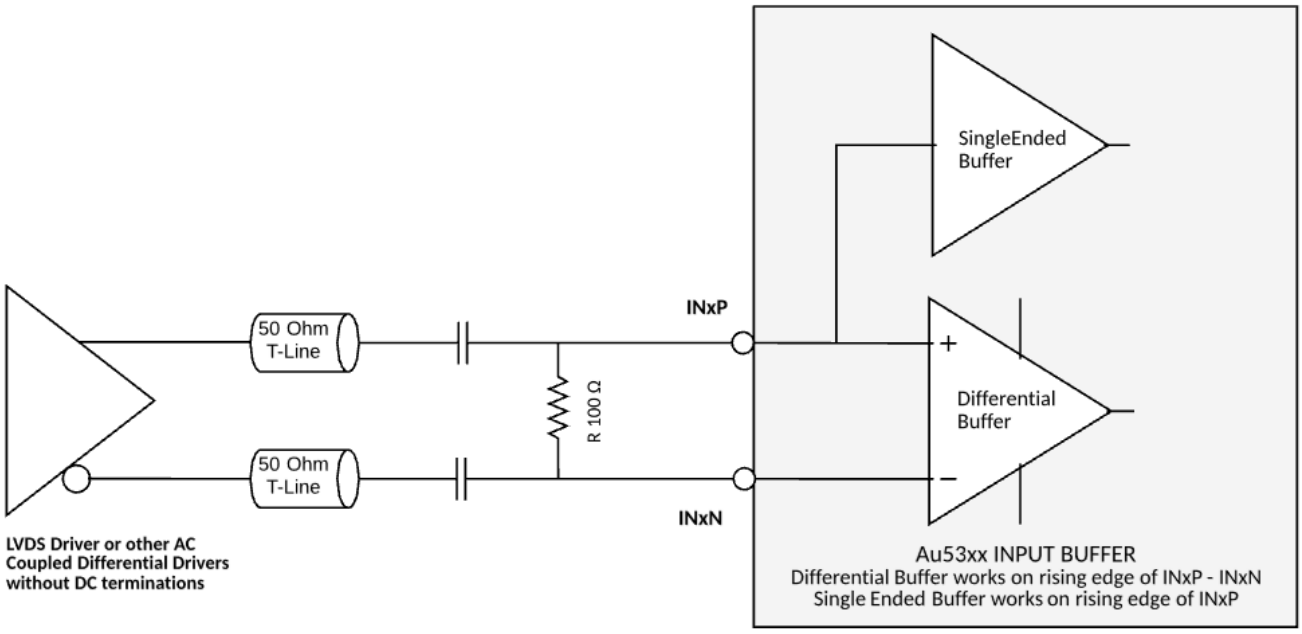


Figure 35 AC Coupled Differential LVDS Input / Other AC Coupled Driver without DC Terminations

Note: Uses Differential Buffer Pathway

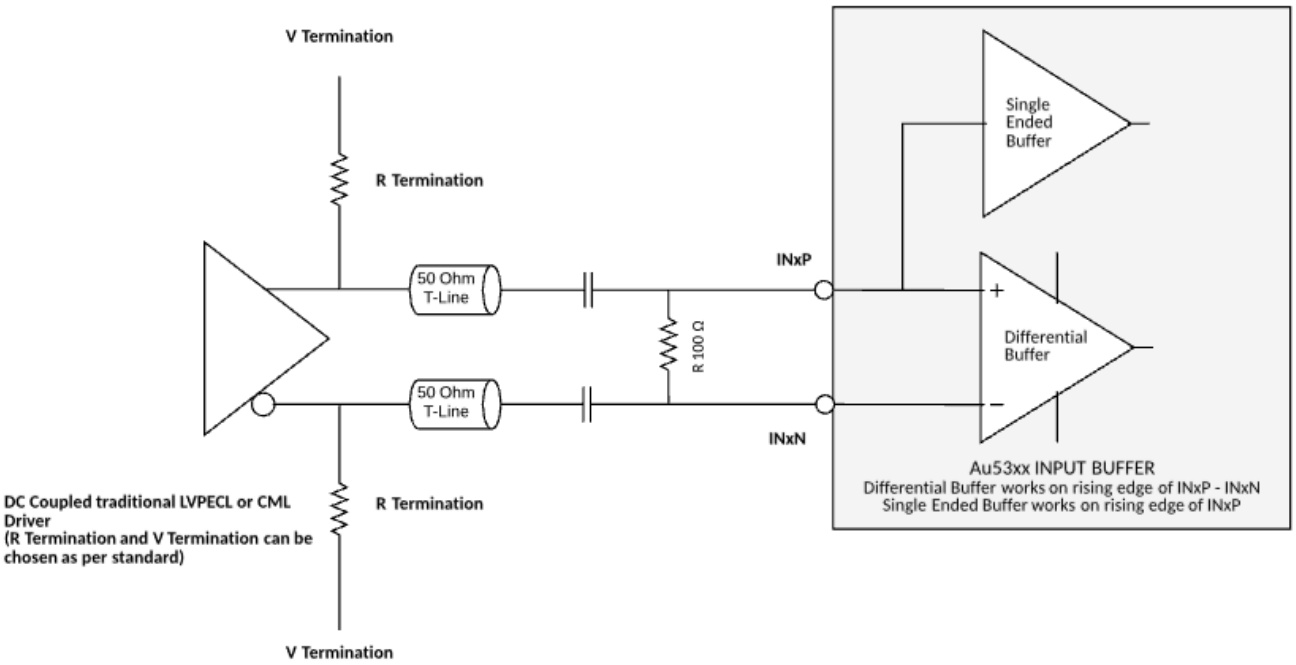
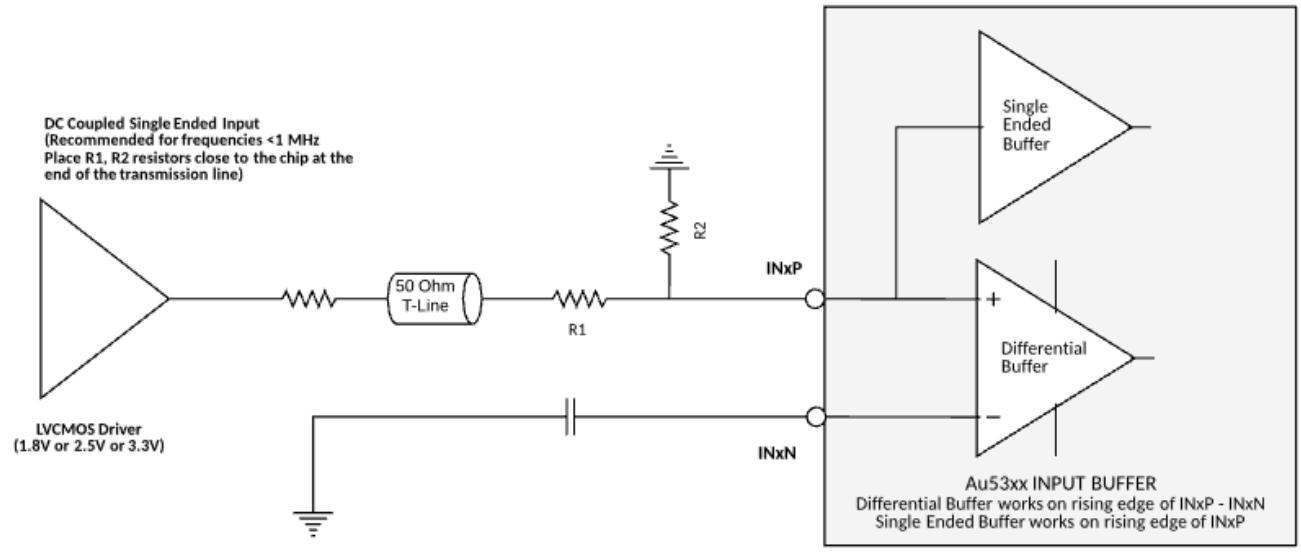


Figure 36 AC Coupled Differential LVPECL or CML

Note: Resistor and Voltage termination is as per the standard. Uses Differential Buffer Pathway. Please refer to the termination requirements of the driver.



Drive Supply	R1 (Ohms)	R2 (Ohms)
1.8 V	140	665
2.5 V	325	475
3.3 V	445	365

Figure 37 DC Coupled Single Ended Driver

Note: Uses Single Ended Buffer Pathway in DC Coupled Mode. Recommended for non-standard duty cycle applications. Please refer above table for the recommended resistor values for frequencies < 1 MHz.

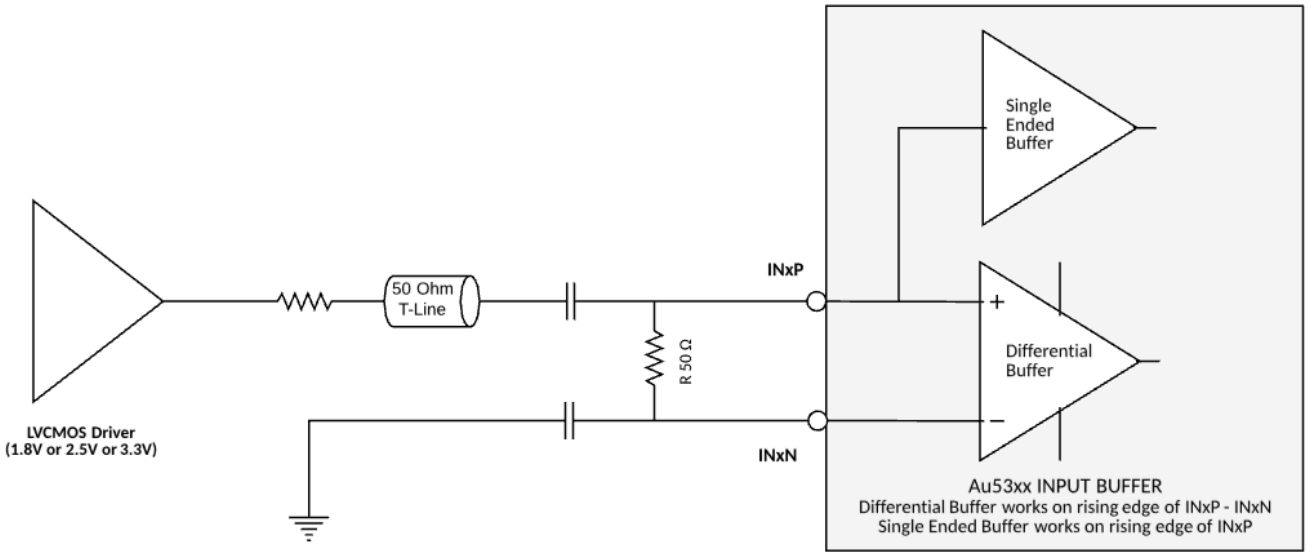


Figure 38 AC Coupled Single Ended Driver with 50 Ohm Termination on receiver (chip) side

Note: Uses Single Ended Buffer pathway in AC coupled mode.

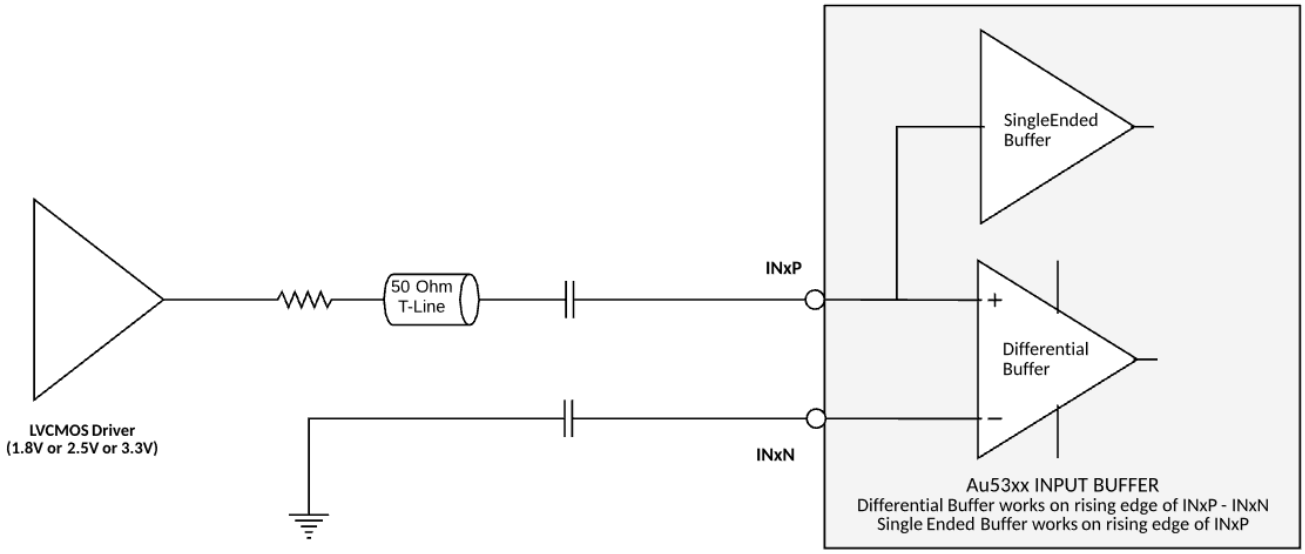


Figure 39 AC Coupled Single Ended LVCMOS input without 50 Ohm Termination

Note: Uses Single Ended Buffer pathway in AC Coupled Mode. The LVCMOS driver in this case needs to ensure source termination to match to the transmission line.

18 Crystal Pathway Connectivity Options

The CMOS XO/TCXO output and the termination components should be placed as close as possible to the X1/X2 pins

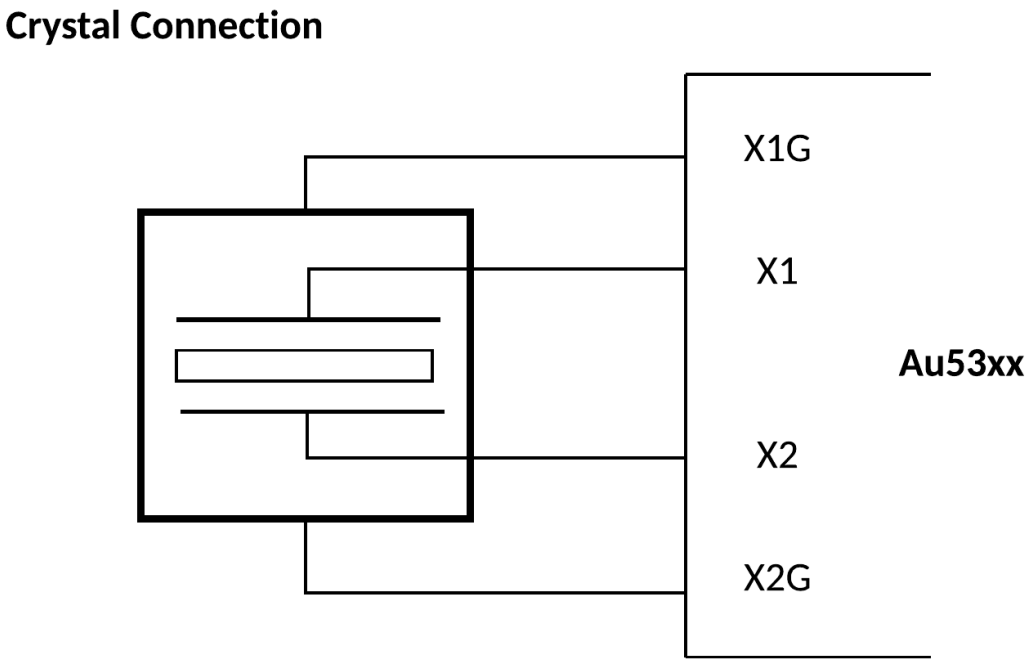
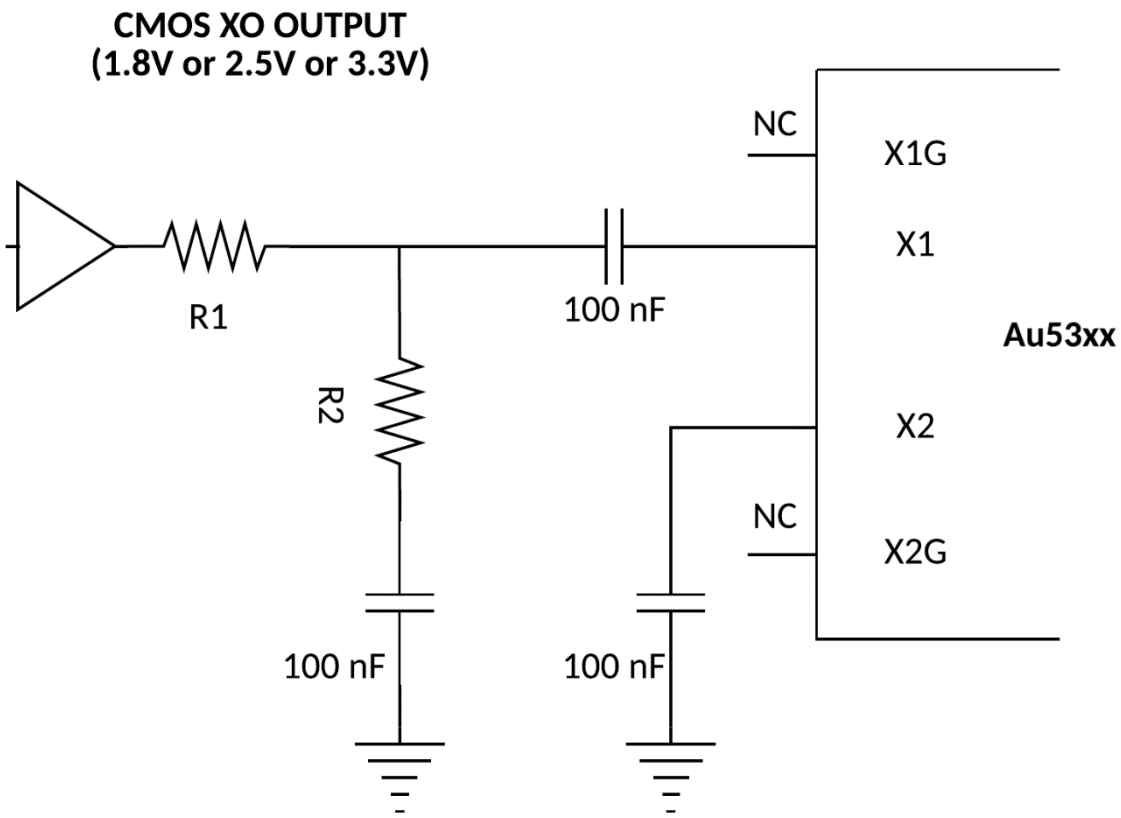


Figure 40 Crystal Connection



CMOS XO Driver Supply	R1 (Ohms)	R2 (Ohms)
1.8 V	0	DNP
2.5 V	274	732
3.3 V	453	549

Figure 41 CMOS XO Connection

Differential XO/Clock

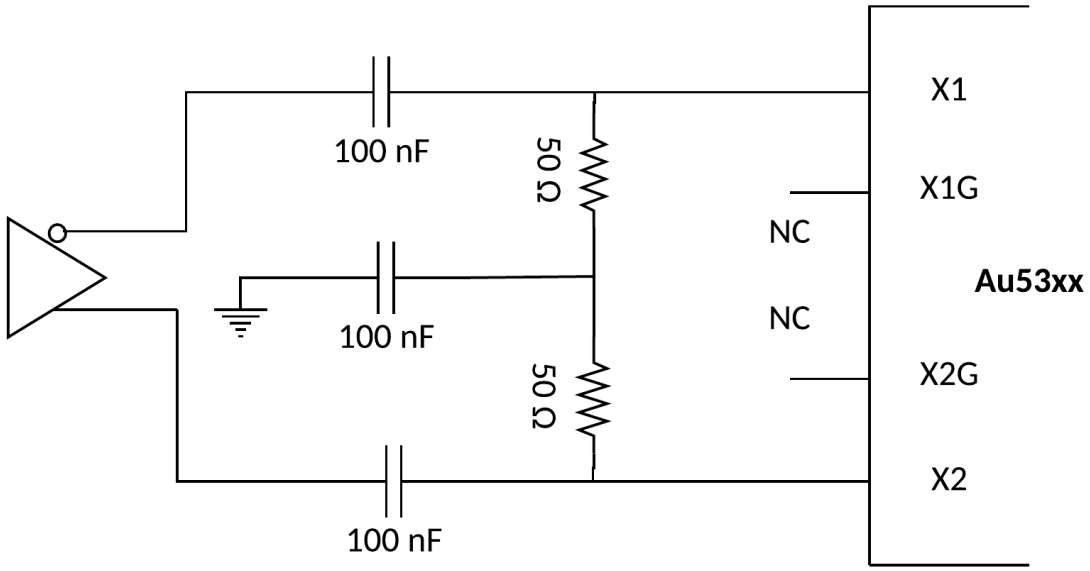


Figure 42 Differential XO Connection

19 Ordering Information

Table 17 Ordering Information for Au5315

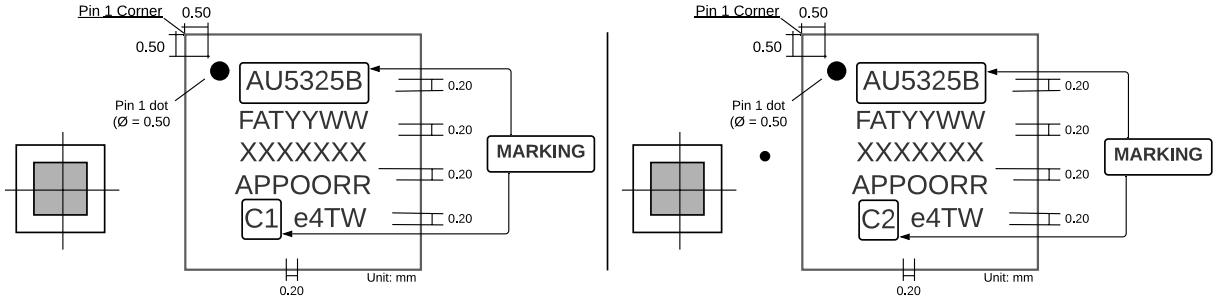
Ordering Part Number (OPN)	Marking	No. of Input/ Output Clocks	Output Clock Frequency Range (MHz)	Supported Frequency Synthesis modes	VDDIN , VDD, VDDIO	Package	Temp Range
Au5315							
Au5315AC0-QMR[1,2]	AU5315A	4/10	8 KHz-2.1 GHz	Integer and Fractional	3.3 , 2.5	64-QFN 9x9 mm	–40 to 85 °C
Au5315AC0-QMT[1,2]	AU5315A	4/10	8 KHz-2.1 GHz	Integer and Fractional	3.3 , 2.5	64-QFN 9x9 mm	–40 to 85 °C
Au53x5C0-EVB		—	—	—	—	Evaluation Board	—

Notes:
1. Add an R at the end of the OPN to denote tape and reel ordering option. Add a T at the end of the OPN to denote tray ordering option.
2. Custom and factory preprogrammed devices are available. Ordering part numbers are assigned by Aura Semiconductor, please contact local sales to request the unique part number. Custom part number format is “Au53xxACxQM” where “x” is a unique numerical sequence representing the preprogrammed configuration.

Table 18 Ordering Information for Au5325

Ordering Part Number (OPN)	Marking	No. of Input/ Output Clocks	Output Clock Frequency Range (MHz)	Supported Frequency Synthesis modes	VDDIN , VDD, VDDIO	Package	Temp Range
Au5325							
Au5325AC1-QMR[1,2]	Au5325A	4/10	8 KHz-2.1 GHz	Integer and Fractional	3.3,1.8/2.5/3.3,3.3	64-QFN 9x9 mm	–40 to 85 °C
Au5325AC1-QMT[1,2]	Au5325A	4/10	8 KHz-2.1 GHz	Integer and Fractional	3.3,1.8/2.5/3.3,3.3	64-QFN 9x9 mm	–40 to 85 °C
Au5325BC1-QMR[1,2]	Au5325BC1[4]	4/10	8 KHz-2.1 GHz	Integer and Fractional	3.3,1.8/2.5/3.3,1.8	64-QFN 9x9 mm	–40 to 85 °C
Au5325BC1-QMT[1,2]	Au5325BC1[4]	4/10	8 KHz-2.1 GHz	Integer and Fractional	3.3,1.8/2.5/3.3,1.8	64-QFN 9x9 mm	–40 to 85 °C
Au5325BC2-QMR[1,2]	Au5325BC2[4]	4/10	8 KHz-2.1 GHz	Integer and Fractional	3.3,1.8/2.5/3.3,3.3	64-QFN 9x9 mm	–40 to 85 °C
Au5325BC2-QMT[1,2]	Au5325BC2[4]	4/10	8 KHz-2.1 GHz	Integer and Fractional	3.3,1.8/2.5/3.3,3.3	64-QFN 9x9 mm	–40 to 85 °C
Au53x5C1-EVB		—	—	—	—	Evaluation Board	—

Notes:
1. Add an R at the end of the OPN to denote tape and reel ordering option. Add a T at the end of the OPN to denote tray ordering option.
2. Custom and factory pre- programmed devices are available. Ordering part numbers are assigned by Aura Semiconductor, please contact local sales to request the unique part number. Custom part number format is “Au53xxACxQM” where “x” is a unique numerical sequence representing the pre-programmed configuration.
3. BC1 and BC2 version has superior PSRR and spur performance compared to AC1 and is recommended for new designs.
4. Please refer to 5th row of the Die Marking to differentiate between Au5325BC1 and Au5325BC2. Au5325BC1 starts with C1 in the 5th row and Au5325BC2 starts with C2 in the 5th row.



20 Revision History

Table 19 Revision History

Version	Date	Description	Author
0.1	1st June 2021	Au53x5, Au53x4 and Au53x2 Short Data Sheet First Draft Created	Aurasemi

21 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

22 Contact Information

For more information visit www.aurasemi.com

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