Document Number:KV30FKV31FPB
Rev 1, 3/2014

KV30F and KV31F Family Product Brief

Supports 120/100MHz devices with 64 KB to 512 KB Embedded Flash

Contents

1 KV30F/KV31F Family Introduction

KV30 and KV31 MCU families are members of the Kinetis V series and provide a high-performance solution for 3-phase BLDC, PMSM and ACIM motor control. Built upon the ARM® Cortex®-M4 core operating at 100/120 MHz with DSP and floating-point unit, features include dual 16-bit analog-to-digital converters with 835 nS conversion time in 12-bit mode, multiple motor-control timers, programmable-delay block, 64 KB to 512 KB of flash memory, and an external bus interface. KV3x MCUs are offered in 100LQFP, 64LQFP, 48LQFP[1] and 32QFN packages. All Kinetis V series MCUs are supported by a comprehensive enablement suite from Freescale and third-party resources, including reference designs, software libraries, and motor configuration tools.

For further information on other Freescale Kinetis Microcontrollers, go to **www.freescale.com/kinetis**.

2 Block Diagram

The following figure shows a superset block diagram of the device. Other devices within the family have a subset of the features.

1. This package offering is subject to removal.

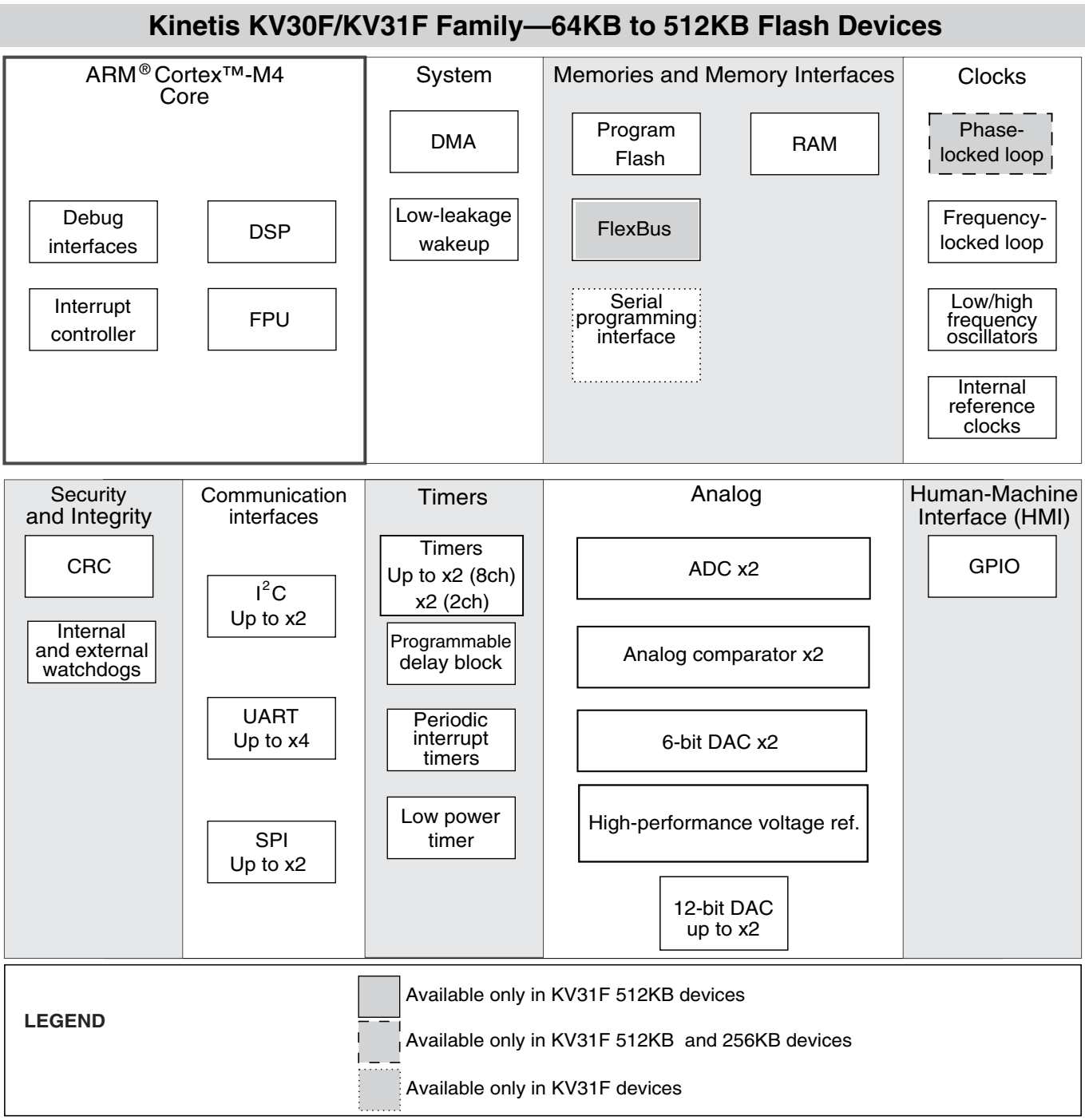

Figure 1. KV30F/KV31F block digram

3 Features

3.1 KV30F/KV31F High-Level Feature Comparison

Table 1. KV30F/KV31—120 MHz / 100 MHz devices (64K to 512K)

Family	KV31			KV30	
Flash Memory	**512KB**	**256KB**	**128KB**	**128KB**	**64KB**
CPU Frequency	120MHz	120MHz	100MHz	100MHz	100MHz
FlexBus	√	—	—	—	—
DMA	16-ch	16-ch	4-ch	4-ch	4-ch
PLL	√	√	—	—	—
FlexTimers	2x8ch; 2x2ch	1x8ch; 2x2ch	1x8ch; 2x2ch	1x6ch; 2x2ch	1x6ch; 2x2ch
DAC	2x 12-bit	1 x12-bit	1x 12-bit	1x 12-bit	1x 12-bit
Total UARTs	4	4	4	2	2
I^2C	2	2	2	1	1
EzPort Serial Programming Interface	√	√	√	—	—
DSPI	2	2	2	1	1
100LQFP	√	√	√	—	—
64LQFP	√	√	√	√	√
48LQFP	—	—	—	√	√
32QFN	—	—	—	√	√

3.2 KV30F/KV31F 64 KB to 512 KB Common Features

Table 2. KV30F/KV31F—64 KB to 512 KB Common Features

Core/System Modules			Timers Modules	
CPU / Frequency	Cortex-M4		Motor Control/General purpose/PWM	up to 2x 8-ch
DMA	up to 16-ch		Quad decoder/General purpose/PWM	2x 2-ch
Floating Point Unit	Single Precision		FTM External Clock	2
Debug	JTAG, SWD		Low Power Timer	1
Trace	TPIU, FPB, DWT, ITM		PDB	Yes
Memory and Memory Interface			PIT	4-ch
Flash Memory	up to 512 KB			
Total SRAM	up to 96 KB			

Table continues on the next page...

Table 2. KV30F/KV31F—64 KB to 512 KB Common Features (continued)

Core/System Modules			Timers Modules	
Clock Modules			**Communication Interfaces**	
MCG	Yes (FLL)		Total UART	Up to 4
Internal Oscilators	32kHz / 4MHz / 48MHz		DSPI	Up to 2
OSC	32-40kHz / 3-32MHz		I^2C	Up to 2
Security and Integrity			**Human Machine Interface**	
Software Watchdog	Yes		GPIO (w/interrupts)	up to 70
Hardware Watchdog	Yes		NMI	Yes
CRC	Yes		**Operating Characteristics**	
Analog Modules			Voltage Range	1.71-3.6V
ADC	2x 16-bit ADC sampling at 1.2 MSPS in 12-bit mode		Temperature Range	-40-105ºC
12-bit DAC	up to 2			
Analog Comparators	2			
High-precision internal voltage	1			

3.3 KV30F/KV31F—64 KB to 512 KB of flash feature differences per package

Table 3. KV30F/KV31F differences

Feature	100LQFP (LL)	64LQFP (LH)	48LQFP[1] (LF)	32QFN (FM)
Memory Interface (Only in 512K Flash devices)				
External Bus Interface (FlexBus) (Addr/Data/CS)	21/16/5[2]	18/16/2[2]	—	—
Non-Muxed External Bus Interface (Flexbus) (Addr/Data/CS)	21/16/5[2]	—	—	—
Analog Modules				
High-performance voltage reference	Yes	Yes	Yes	No
ADC0 (SE:single-ended, DP:differential pair)	23chSE + 4chDP	20chSE + 2chDP	19chSE + 3chDP	13chSE + 2chDP
ADC1 (SE:single-ended, DP:differential pair)	20chSE + 3chDP	13chSE + 2chDP[3]	7chSE + 3chDP	5chSE + 2chDP
Total ADC DP inputs	4ch	2ch[4]	3ch	2ch
Total ADC SE inputs	38ch	29ch	20ch	13ch
Analog Comparators Inputs (CMP0 / CMP1)	6 / 4	6 / 4	3 / 4	2 / 3
Communication Interfaces				
Total UARTs	4	4[5]	2	2
DSPI chip selects per module (DSPI0 / DSPI1)	6 / 4	5 / 2	5 / 0	4 / 0
I^2C	2	2[6]	1	1

Table continues on the next page...

Table 3. KV30F/KV31F differences (continued)

Feature	100LQFP (LL)	64LQFP (LH)	48LQFP[1] (LF)	32QFN (FM)
Human Machine Interface				
GPIO (with interrupts)	70	46	35	26

1. This package offering is subject to removal.
2. Only in 512KB Flash devices.
3. KV30F has 16chSE + 4chDP.
4. KV30F has 4ch.
5. With the exception of the KV30F that has 2.
6. With the exception of the KV30F that has 1.

3.4 Orderable part numbers

The following table summarizes the part numbers of the devices covered by this document. See the Part identification section for details on the part number format.

Table 4. KV31F / KV30F - 64KB to 512KB orderable part numbers summary

Part number	CPU frequency	Pin count	Package	Flash	RAM	GPIOs	Flex timers
MKV31F512VLL12	120 MHz	100	LQFP	512KB	96KB	70	2x8ch; 2x2ch
MKV31F512VLH12	120 MHz	64	LQFP	512KB	96KB	46	2x8ch; 2x2ch
MKV31F256VLL12	120 MHz	100	LQFP	256KB	48KB	70	1x8ch; 2x2ch
MKV31F256VLH12	120 MHz	64	LQFP	256KB	48KB	46	1x8ch; 2x2ch
MKV31F128VLL10	100 MHz	100	LQFP	128KB	24KB	70	1x8ch; 2x2ch
MKV31F128VLH10	100 MHz	64	LQFP	128KB	24KB	46	1x8ch; 2x2ch
MKV30F128VLH10	100 MHz	64	LQFP	128KB	16KB	46	1x6ch; 2x2ch
MKV30F128VLF10[1]	100 MHz	48	LQFP	128KB	16KB	35	1x6ch; 2x2ch
MKV30F128VFM10	100 MHz	32	QFN	128KB	16KB	26	1x6ch; 2x2ch
MKV30F64VLH10	100 MHz	64	LQFP	64KB	16KB	46	1x6ch; 2x2ch
MKV30F64VLF10[1]	100 MHz	48	LQFP	64KB	16KB	35	1x6ch; 2x2ch
MKV30F64VFM10	100 MHz	32	QFN	64KB	16KB	26	1x6ch; 2x2ch

1. This package offering is subject to removal

3.5 Module-by-module feature list

The following sections describe the high-level module features for the family's superset device. See the previous section for differences among the subset devices.

3.5.1 Core modules

3.5.1.1 ARM® Cortex®-M4 Core

- Supports up to 120 MHz frequency with 1.25DMIPS/MHz
- ARM® Core based on the ARMv7 Architecture & Thumb®-2 ISA
- Microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments
- Harvard bus architecture
- 3-stage pipeline with branch speculation
- Integrated bus matrix
- Integrated Digital Signal Processor (DSP)
- Configurable nested vectored interrupt controller (NVIC)
- Advanced configurable debug component
- Single Precision Floating Point Unit (SPFPU)

3.5.1.2 Nested Vectored Interrupt Controller (NVIC)

- Close coupling with Cortex-M4 core's Harvard architecture enables low latency interrupt handling
- Up to 120 interrupt sources
- Includes a single non-maskable interrupt
- 16 levels of priority, with each interrupt source dynamically configurable
- Supports nesting of interrupts when higher priority interrupts are activated
- Relocatable vector table

3.5.1.3 Wake-up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low power modes
- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to very-deep-sleep
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a non-masked interrupt is detected
- Contains no programmer’s model visible state and is therefore invisible to end users of the device other than through the benefits of reduced power consumption while sleeping

3.5.1.4 Debug Controller

- Serial Wire Debug (SWD) provides an external serial-wire bidirectional debug interface
- Debug Watchpoint and Trace (DWT) with the following functionality:
  - four comparators configurable as a hardware watchpoint, a PC sampler event trigger, or a data address sampler event trigger
  - several counters or a data match event trigger for performance profiling
  - configurable to emit PC samples at defined intervals or to emit interrupt event information
- Instrumentation Trace Macrocell (ITM) with the following functionality:
  - Software trace - writes directly to ITM stimulus registers can cause packets to be emitted
  - Hardware trace - packets generated by DWT are emitted by ITM
  - Time stamping - emitted relative to packets
- Test Port Interface Unit (TPIU) acts as a bridge between ITM and an off-chip Trace Port Analyzer
- Flash Patch and Breakpoints (FPB) implements hardware breakpoints and patches code and data from code space to system space

3.5.2 System modules

3.5.2.1 Power Management Control Unit (PMC)

- Separate digital (regulated) and analog (referenced to digital) supply outputs
- Programmable power saving modes
- No output supply decoupling capacitors required
- Available wake-up from power saving modes via RTC and external inputs
- Integrated Power-on Reset (POR)
- Integrated Low Voltage Detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Buffered bandgap reference voltage output
- Factory programmed trim for bandgap and LVD
- 1 kHz Low Power Oscillator (LPO)

3.5.2.2 DMA Channel Multiplexer (DMA MUX)

- Up to 16 independently selectable DMA channel routers
- 4 periodic trigger sources available
- Each channel router can be assigned to 1 of 63 possible peripheral DMA sources

3.5.2.3 DMA Controller

- Up to 16 fully programmable channels with 32-byte transfer control descriptors
- Data movement via dual-address transfers for 8-, 16-, 32-, 128-, and 256-bit data values
- Programmable source, destination addresses, transfer size, support for enhanced address modes
- Support for major and minor nested counters with one request and one interrupt per channel
- Support for channel-to-channel linking and scatter/gather for continuous transfers with fixed priority and round-robin channel arbitration

3.5.2.4 System Clocks

- Frequency-locked loop (FLL)
  - Digitally-controlled oscillator (DCO)
  - DCO frequency range is programmable
  - Option to program DCO frequency for a 32,768 Hz external reference clock source
  - Internal or external reference clock can be used to control the FLL
  - 0.2% resolution using 32 kHz internal reference clock
- Phase-locked loop (PLL)
  - Voltage-controlled oscillator (VCO)
  - External reference clock is used to control the PLL
  - Modulo VCO frequency divider Phase/Frequency detector
  - Integrated loop filter
- Internal reference clock generator
  - Slow clock with nine trim bits for accuracy
  - Fast clock with four trim bits
  - Can be used to control the FLL
  - Either the slow or the fast clock can be selected as the clock source for the MCU
  - Can be used as a clock source for other on-chip peripherals
- External clock from the Crystal Oscillator (XOSC)
  - Can be used to control the FLL and/or the PLL
  - Can be selected as the clock source for the MCU
- External clock monitor with reset request capability
- Lock detector with interrupt request capability for use with the PLL
- Auto Trim Machine (ATM) for trimming both the slow and fast internal reference clocks
- Multiple clock source options available for most peripherals

3.5.3 Memories and Memory Interfaces

3.5.3.1 On-Chip Memory

- Security circuitry to prevent unauthorized access to RAM and flash contents

3.5.3.2 External Bus Interface (FlexBus)

- Six independent, user-programmable chip-select signals that can interface with external SRAM, PROM, EPROM, EEPROM, flash, and other peripherals
- Supports up to 2 GB addressable space
- 8-, 16- and 32-bit port sizes with configuration for multiplexed or non-multiplexed address and data buses
- Byte-, word-, longword-, and 16-byte line-sized transfers
- Programmable address-setup time with respect to the assertion of chip select
- Programmable address-hold time with respect to the negation of chip select and transfer direction

3.5.3.3 Serial Programming Interface (EzPort)

- Same serial interface as, and subset of, the command set used by industry-standard SPI flash memories
- Ability to read, erase, and program flash memory
- Reset command to boot the system after flash programming

3.5.4 Security and Integrity

3.5.4.1 Cyclic Redundancy Check (CRC)

- Hardware CRC generator circuit using 16/32-bit shift register
- User Configurable 16/32 bit CRC
- Programmable Generator Polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Programmable initial seed value
- High-speed CRC calculation
- Optional feature to transpose input data and CRC result via transpose register, required on applications where bytes are in lsb format

3.5.4.2 Watchdog Timer (WDOG)

- Independent, configurable clock source input
- Write-once control bits with unlock sequence
- Programmable timeout period
- Ability to test watchdog timer and reset
- Windowed refresh option
- Robust refresh mechanism
- Cumulative count of watchdog resets between power-on resets
- Configurable interrupt on timeout

3.5.4.3 External Watchdog Monitor (EWM)

- Independent 1 kHz LPO clock source
- Output signal to gate an external circuit which is controlled by CPU service or external input

3.5.5 Analog

3.5.5.1 16-bit Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with up to 16-bit resolution
- Output modes:
  - Differential 16-bit, 13-bit, 11-bit, and 9-bit modes, in two's complement 16-bit sign-extended format
  - Single-ended 16-bit, 12-bit, 10-bit, and 8-bit modes, in right-justified unsigned format
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Conversion complete and hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in low power modes for lower noise operation
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable asynchronous hardware conversion trigger with hardware channel select
- Automatic compare with interrupt for various programmable values
- Temperature sensor
- Hardware average function
- Selectable voltage reference
- Self-calibration mode

3.5.5.2 High-Speed Analog Comparator (CMP)

- 6-bit DAC programmable reference generator output
- Up to eight selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Comparator output supports:
  - Sampled
  - Windowed (ideal for certain PWM zero-crossing-detection applications
  - Digitally filtered using external sample signal or scaled peripheral clock
- Two performance modes:
  - Shorter propagation delay at the expense of higher power
  - Low power, with longer propagation delay
- Operational in all MCU power modes

3.5.5.3 12-Bit Digital-to-Analog Converter (DAC)

- 12-bit resolution
- Guaranteed 6-sigma monotocity over input word
- High- and low-speed conversions
  - 1 µs conversion rate for high speed, 2 µs for low speed
- Power-down mode
- Choice of asynchronous or synchronous updates
- Automatic mode allows the DAC to generate its own output waveforms including square, triangle, and sawtooth

- Automatic mode allows programmable period, update rate, and range
- DMA support with configurable watermark level

3.5.5.4 Voltage Reference (VREF)

- Programmable trim register with 0.5mV steps, automatically loaded with room temp value upon reset
- Programmable mode selection:
  - Off
  - Bandgap out (or stabilization delay)
  - Low-power buffer mode
  - Tight-regulation buffer mode
- 1.2V output at room temperature
- Dedicated output pin

3.5.6 Timers

3.5.6.1 Programmable Delay Block (PDB)

- Up to 15 trigger input sources and software trigger source
- Up to eight configurable PDB channels for ADC hardware trigger
  - One PDB channel is associated with one ADC.
  - One trigger output for ADC hardware trigger and up to eight pre-trigger outputs for ADC trigger select per PDB channel
  - Trigger outputs can be enabled or disabled independently.
  - One 16-bit delay register per pre-trigger output
  - Optional bypass of the delay registers of the pre-trigger outputs
  - Operation in One-Shot or Continuous modes
  - Optional back-to-back mode operation, which enables the ADC conversions complete to trigger the next PDB channel
  - One programmable delay interrupt
  - One sequence error interrupt
  - One channel flag and one sequence error flag per pre-trigger
  - DMA support
- Up to eight DAC interval triggers
  - One interval trigger output per DAC
  - One 16-bit delay interval register per DAC trigger output
  - Optional bypass the delay interval trigger registers
  - Optional external triggers
- Up to eight pulse outputs (pulse-out's)
  - Pulse-out's can be enabled or disabled independently.
  - Programmable pulse width

3.5.6.2 FlexTimers (FTM)

- Selectale FTM source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes

- Operation of FTM channels as pairs with equal outputs, pairs with complimentary outputs, or independent channels with independent outputs
- Deadtime insertion is available for each complementary pair
- Generation of hardware triggers
- Software control of PWM outputs
- Up to 4 fault inputs for global fault control
- Configurable channel polarity
- Programmable interrupt on input capture, reference compare, overflowed counter, or detected fault condition
- Quadrature decoder with input filters, relative position counting, and interrupt on position count or capture of position count on external event
- DMA support for FTM events
- Global time base mode shares single time base across multiple FTM instances

3.5.6.3 Programmable Interrupt Timers (PITs)

- Up to 4 general purpose interrupt timers
- Up to 4 interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by system clock frequency
- DMA support

3.5.6.4 Low Power Timer

- Operation as timer or pulse counter
- Selectable clock for prescaler/glitch filter
  - 1 kHz internal LPO
  - External low power crystal oscillator
  - Internal reference clock (not available in low leakage power modes)
  - Secondary external reference clock (for example, 32 kHz crystal)
- Configurable glitch filter or prescaler
- Interrupt generated on timer compare
- Hardware trigger generated on timer compare

3.5.7 Communication interfaces

3.5.7.1 Serial Peripheral Interface (SPI)

- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Programmable 8-bit or 16-bit data transmission length
- Receive data buffer hardware match feature
- 64-bit FIFO mode for high speed transfers of large amounts of data
- Support for both transmit and receive by DMA

3.5.7.2 Inter-Integrated Circuit (I^2C)

- Compatible with I^2C bus standard and *SMBus Specification Version 2* features
- Up to 100 kbps with maximum bus loading
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt or DMA driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low power mode

3.5.7.3 UART

- Support for ISO 7816 protocol for interfacing with smartcards
- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Parameterizable buffer support for one dataword for each transmit and receive
- Independent FIFO structure for transmit and receive
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Address match feature in receiver to reduce address mark wakeup ISR overhead
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking
- 1/16 bit-time noise detection

3.5.7.4 LPUART

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Two receiver wake-up methods:
  - Idle line wake-up
  - Address mark wake-up
- Address match feature in receiver to reduce address mark wake-up ISR overhead
- Interrupt or DMA driven operation

- Receiver framing error detection
- Hardware parity generation and checking
- Configurable oversampling ratio to support from 1/4 to 1/32 bit-time noise detection
- Operation in low-power modes

3.5.8 Human-machine interface

3.5.8.1 General Purpose Input/Output (GPIO)

- Progammable glitch filter and interrupt with selectable polarity on select input pins
- Hysteresis and configurable pull up/down device on all input pins
- Configurable slew rate on all output pins
- Configurable drive strength on select output pins
- Independent pin value register to read logic level on digital pin

4 Part identification

4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

4.2 Format

Part numbers for this device have the following format:

Q KV## A FFF R T PP CC N

4.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KV##	Kinetis V Series	• KV3x: Cortex-M4 based MCU
A	Key attribute	• D = Cortex-M4 w/ DSP • F = Cortex-M4 w/ DSP and FPU
FFF	Program flash memory size	• 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB

Table continues on the next page...

Part identification

Field	Description	Values
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • LF = 48 LQFP[1] (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 XFBGA (8 mm x 8 mm) • DC = 121 XFBGA (8 mm x 8 mm x 0.5 mm)
CC	Maximum CPU frequency (MHz)	• 10 = 100 MHz • 12 = 120 MHz
N	Packaging type	• R = Tape and reel

1. This package offering is subject to removal.

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number KV30FKV31FPB
Revision 1, 3/2014