

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

- Internal Look-Ahead Circuitry for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) DIPs

description

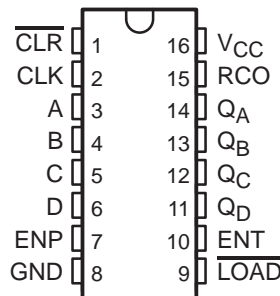
These synchronous, presettable, 4-bit decade and binary counters feature an internal carry look-ahead circuitry for application in high-speed counting designs. The SN54ALS162B is a 4-bit decade counter. The 'ALS161B, 'ALS163B, 'AS161, and 'AS163 devices are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; they can be preset to any number between 0 and 9 or 15. Because presetting is synchronous, setting up a low level at the load (LOAD) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

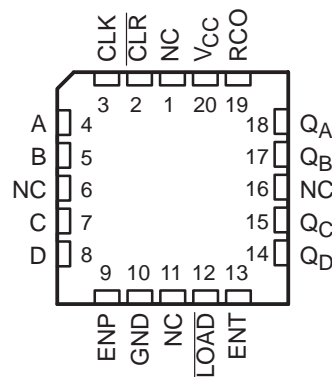
The clear function for the 'ALS161B and 'AS161 devices is asynchronous. A low level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, LOAD, or enable inputs. The clear function for the SN54ALS162B, 'ALS163B, and 'AS163 devices is synchronous, and a low level at CLR sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{\text{CLR}}$ to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP and ENT inputs and a ripple-carry (RCO) output are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled,

SN54ALS161B, SN54ALS162B, SN54ALS163B,
SN54AS161, SN54AS163 . . . J PACKAGE
SN74ALS161B, SN74AS161,
SN74AS163 . . . D OR N PACKAGE
SN74ALS163B . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54ALS161B, SN54ALS162B, SN54ALS163B,
SN54AS161, SN54AS163 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

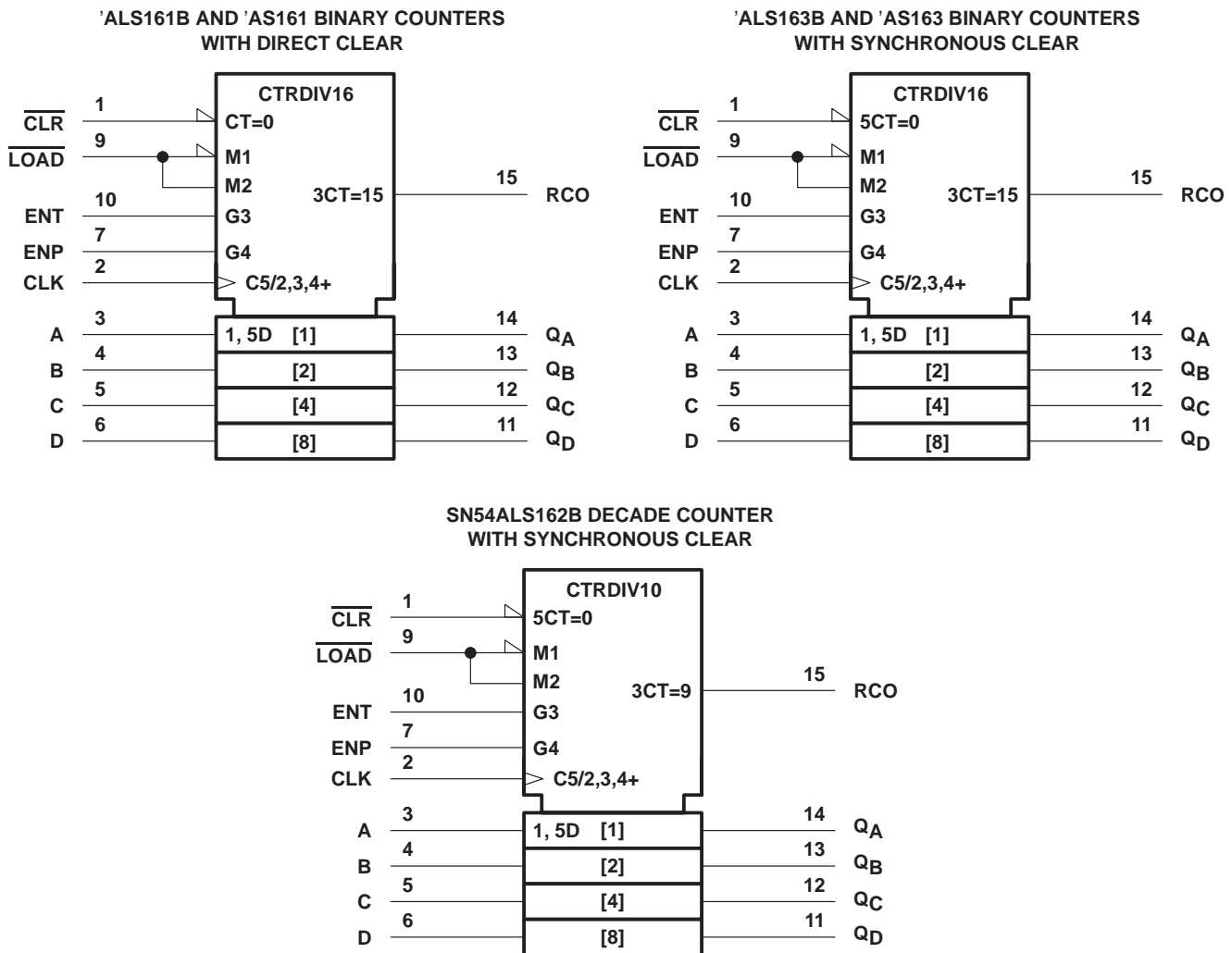
description (continued)

produces a high-level pulse while the count is maximum (9 or 15, with Q_A high). The high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or \overline{LOAD}) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, and SN54AS163 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS161B, SN74ALS163B, SN74AS161, and SN74AS163 are characterized for operation from 0°C to 70°C .

logic symbols†



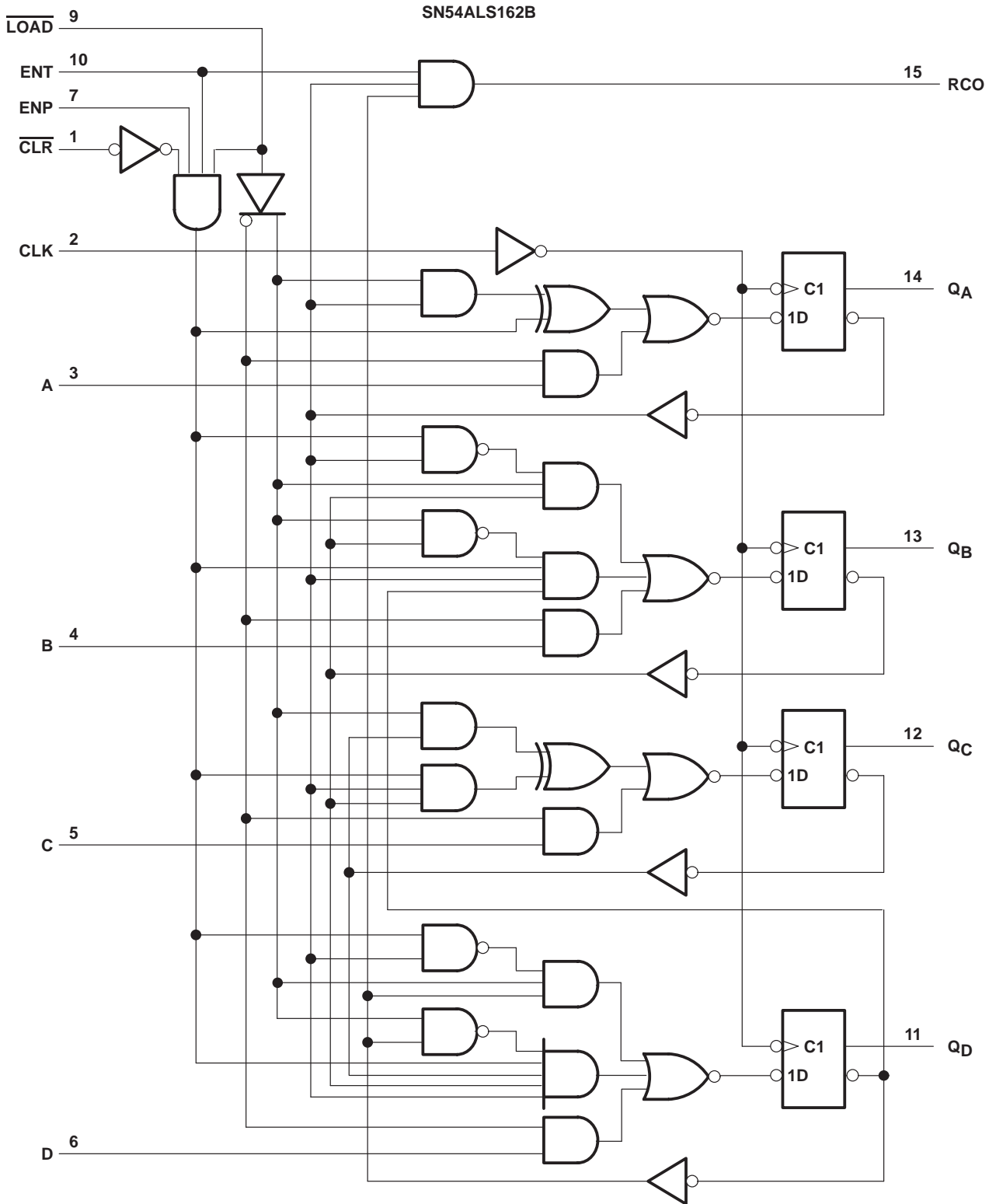
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, and N packages.



SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

logic diagram (positive logic)



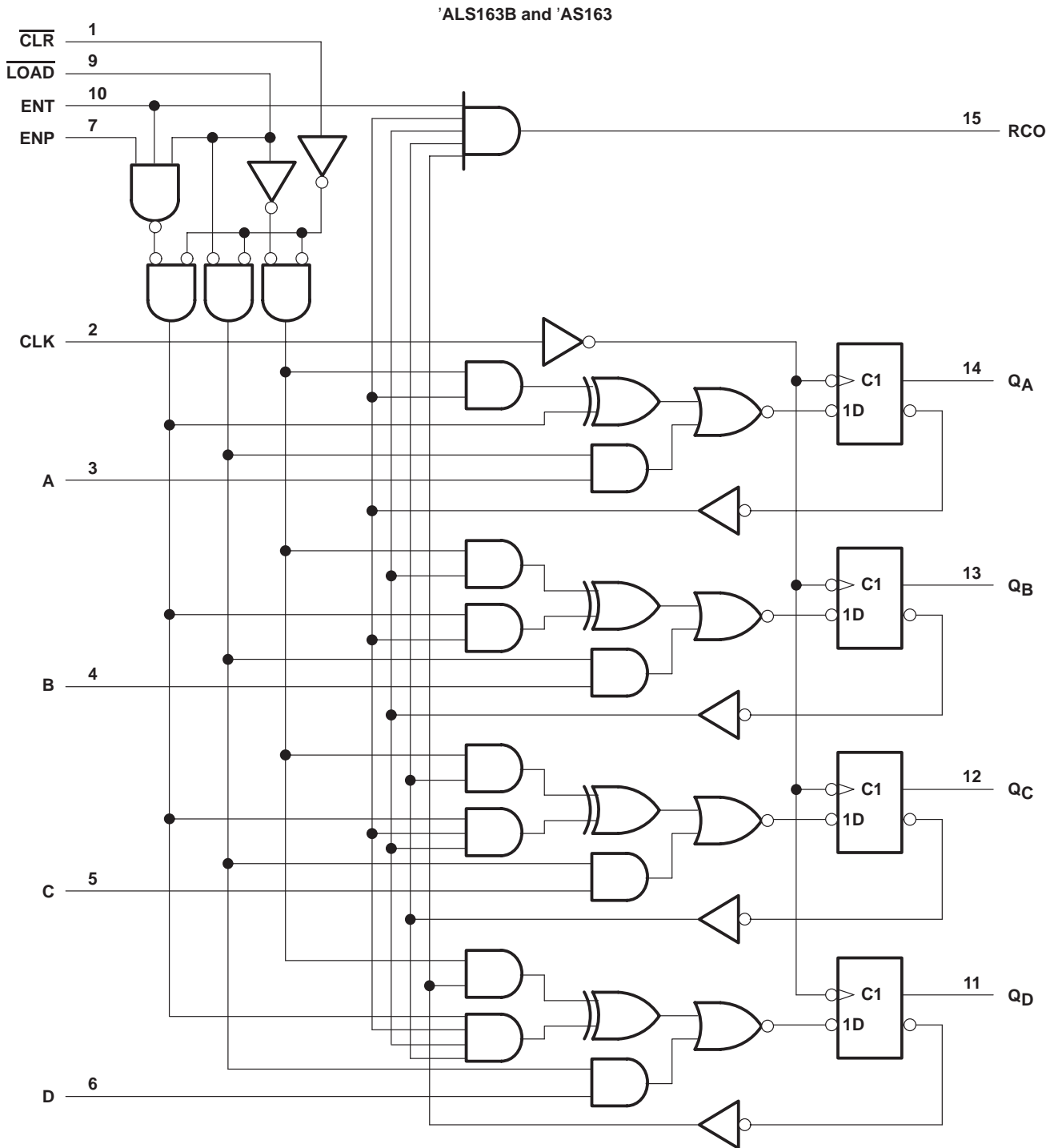
Pin numbers shown are for the J package.



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and N packages.
 'ALS161B and 'AS161 synchronous binary counters are similar; however, $\overline{\text{CLR}}$ is asynchronous.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

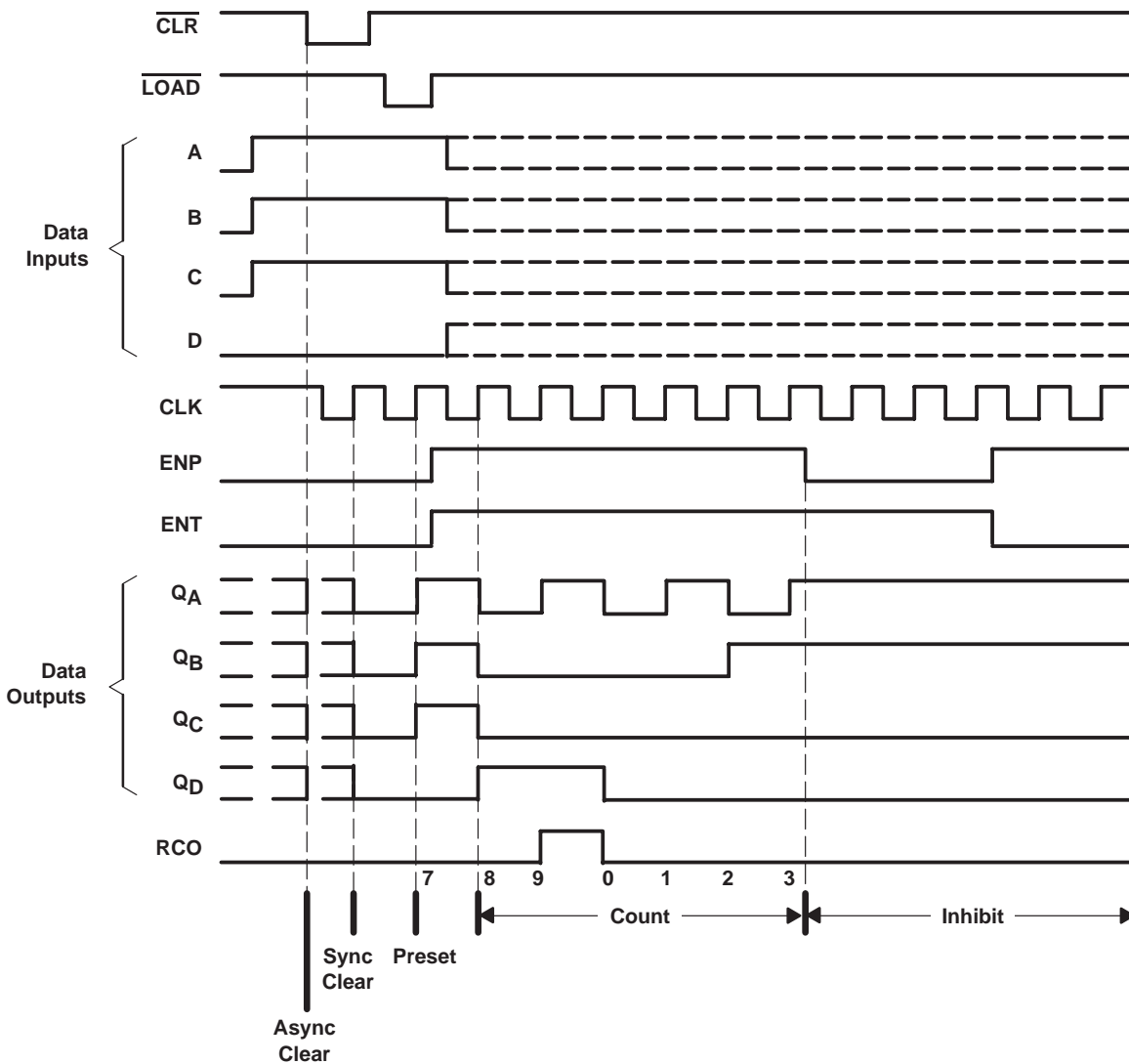
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typical clear, preset, count, and inhibit sequences

SN54ALS162B

The following sequence is illustrated below:

1. Clear outputs to zero (SN54ALS162B is synchronous)
2. Preset to BCD 7
3. Count to 8, 9, 0, 1, 2, and 3
4. Inhibit



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

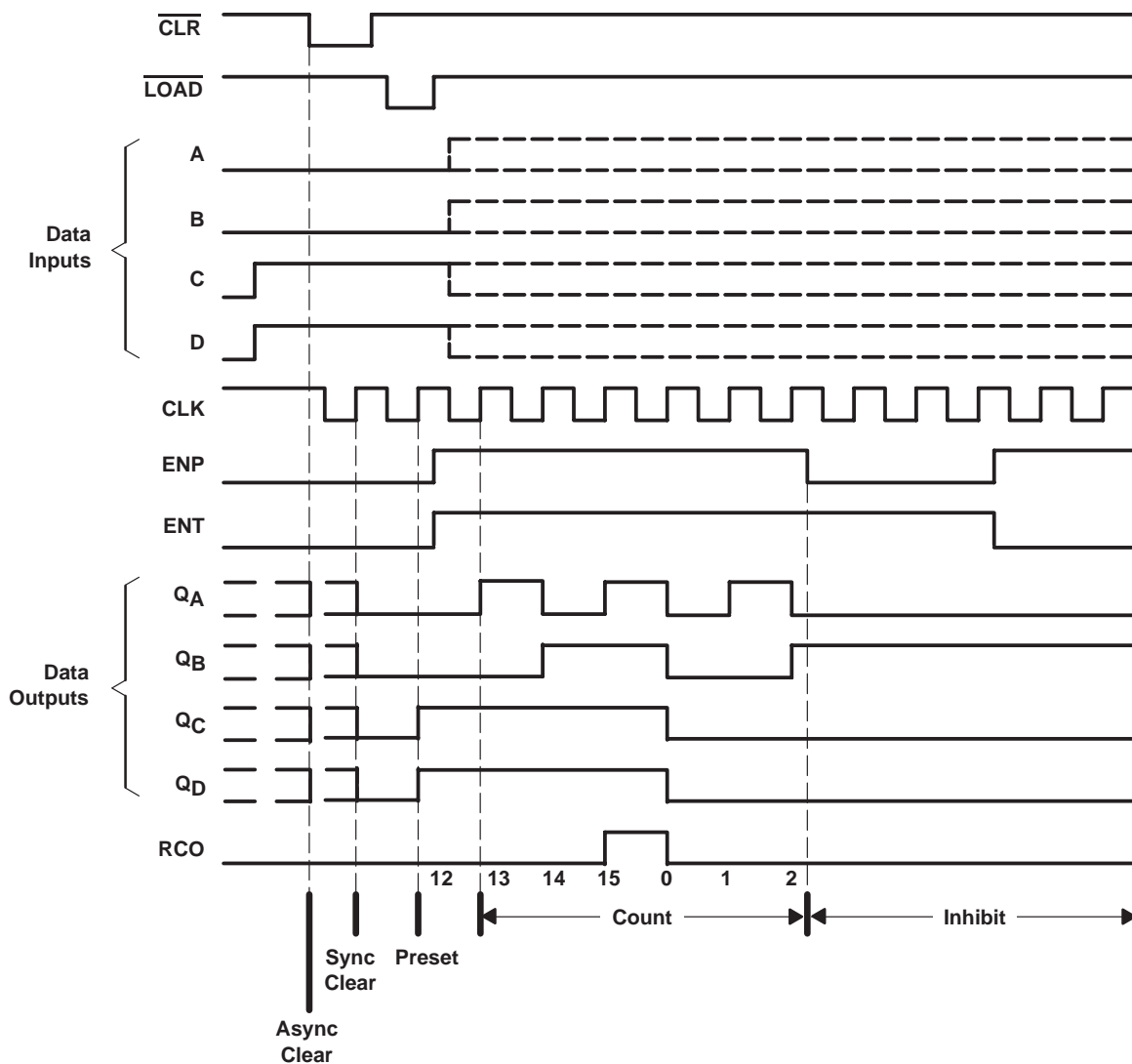
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typical clear, preset, count, and inhibit sequences

'ALS161B, 'AS161, 'ALS163B, and 'AS163

The following sequence is illustrated below:

1. Clear outputs to zero ('ALS161B and 'AS161 are asynchronous; 'ALS163B and 'AS163 are synchronous.)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I | –0.5 V to 7 V |
| Package thermal impedance, θ_{JA} (see Note 1): D package | 73°C/W |
| DB package | 82°C/W |
| N package | 67°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

| | | SN54ALS161B SN54ALS162B SN54ALS163B | | | SN74ALS161B SN74ALS163B | | | UNIT |
|----------|--------------------------------|---|-----|------|----------------------------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| I_{OH} | High-level output current | | | –0.4 | | | –0.4 | mA |
| I_{OL} | Low-level output current | | | 4 | | | 8 | mA |
| T_A | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54ALS161B SN54ALS162B SN54ALS163B | | | SN74ALS161B SN74ALS163B | | | UNIT | |
|--------------|---|---|-----------------|------|----------------------------|------|------|------|---|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V_{IK} | $V_{CC} = 4.5$ V, $I_I = -18$ mA | | | –1.5 | | | –1.5 | V | |
| V_{OH} | $V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -0.4$ mA | $V_{CC} - 2$ | | | $V_{CC} - 2$ | | | V | |
| V_{OL} | $V_{CC} = 4.5$ V | | $I_{OL} = 4$ mA | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL} = 8$ mA | | | | 0.35 | 0.5 | |
| I_I | $V_{CC} = 5.5$ V, $V_I = 7$ V | | | 0.1 | | | 0.1 | mA | |
| I_{IH} | $V_{CC} = 5.5$ V, $V_I = 2.7$ V | | | 20 | | | 20 | µA | |
| I_{IL} | $V_{CC} = 5.5$ V, $V_I = 0.4$ V | | | –0.2 | | | –0.2 | mA | |
| I_{O}^{\S} | $V_{CC} = 5.5$ V, $V_O = 2.25$ V | –20 | | –112 | –30 | | –112 | mA | |
| I_{CC} | $V_{CC} = 5.5$ V | | 12 | 21 | | 12 | 21 | mA | |

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

timing requirements over recommended operating conditions (unless otherwise noted) (see Figure 1)

| | | | SN54ALS161B SN54ALS162B SN54ALS163B | | SN74ALS161B SN74ALS163B | | UNIT | |
|-------------|--|-------------------------------|---|-----|----------------------------|-----|------|--|
| | | | MIN | MAX | MIN | MAX | | |
| f_{clock} | Clock frequency | | 22 | | 40 | | MHz | |
| t_w | Pulse duration | \overline{CLR} high or low | 20 | | 12.5 | | ns | |
| | | 'ALS161B \overline{CLR} low | 20 | | 15 | | | |
| t_{su} | Setup time, before CLK \uparrow | A, B, C, D | 50 | | 15 | | ns | |
| | | \overline{LOAD} | 20 | | 15 | | | |
| | | 'ALS161B | ENP, ENT | 25 | | 15 | | |
| | | SN54ALS162B, 'ALS163B | | 20 | | 15 | | |
| | | 'ALS161B | \overline{CLR} inactive | 10 | | 10 | | |
| | | SN54ALS162B, 'ALS163B | \overline{CLR} low | 20 | | 15 | | |
| | | \overline{CLR} high | 20 | | 10 | | | |
| t_h | Hold time, all synchronous inputs after CLK \uparrow | | 0 | | 0 | | ns | |

switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ALS161B | | SN74ALS161B | | UNIT |
|-----------|------------------|-------------|-------------|-----|-------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| f_{max} | | | 22 | | 40 | | MHz |
| t_{PLH} | CLK | RCO | 5 | 34 | 5 | 20 | ns |
| t_{PHL} | | | 5 | 27 | 5 | 20 | |
| t_{PLH} | CLK | Any Q | 4 | 19 | 4 | 15 | ns |
| t_{PHL} | | | 6 | 25 | 6 | 20 | |
| t_{PLH} | ENT | RCO | 3 | 18 | 3 | 13 | ns |
| t_{PHL} | | | 3 | 17 | 3 | 13 | |
| t_{PHL} | \overline{CLR} | Any Q | 8 | 27 | 8 | 24 | ns |
| | | RCO | 11 | 32 | 11 | 23 | |

switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ALS162B SN54ALS163B | | SN74ALS163B | | UNIT |
|-----------|--------------|-------------|----------------------------|-----|-------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| f_{max} | | | 22 | | 40 | | MHz |
| t_{PLH} | CLK | RCO | 5 | 25 | 5 | 20 | ns |
| t_{PHL} | | | 5 | 25 | 5 | 20 | |
| t_{PLH} | CLK | Any Q | 4 | 18 | 4 | 15 | ns |
| t_{PHL} | | | 6 | 25 | 6 | 20 | |
| t_{PLH} | ENT | RCO | 3 | 16 | 3 | 13 | ns |
| t_{PHL} | | | 3 | 16 | 3 | 13 | |



**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

recommended operating conditions

| | | SN54AS161 SN54AS163 | | | SN74AS161 SN74AS163 | | | UNIT |
|-----------------|--------------------------------|------------------------|-----|-----|------------------------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} | High-level output current | | | -2 | | | -2 | mA |
| I _{OL} | Low-level output current | | | 20 | | | 20 | mA |
| T _A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54AS161 SN54AS163 | | | SN74AS161 SN74AS163 | | | UNIT |
|------------------|------------|-----------------------------------|-------------------------|------------------------|------|------|------------------------|------|------|------|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V _{IK} | | V _{CC} = 4.5 V, | I _I = -18 mA | | | -1.2 | | | -1.2 | V |
| V _{OH} | | V _{CC} = 4.5 V to 5.5 V, | I _{OH} = -2 mA | V _{CC} - 2 | | | V _{CC} - 2 | | | V |
| V _{OL} | | V _{CC} = 4.5 V, | I _{OL} = 20 mA | 0.25 | 0.5 | | 0.25 | 0.5 | | V |
| I _I | LOAD | V _{CC} = 5.5 V, | V _I = 7 V | | | 0.3 | | | 0.3 | mA |
| | ENT | | | | | 0.2 | | 0.2 | | |
| | All others | | | | | 0.1 | | 0.1 | | |
| I _{IH} | LOAD | V _{CC} = 5.5 V, | V _I = 2.7 V | | | 60 | | | 60 | μA |
| | ENT | | | | | 40 | | 40 | | |
| | All others | | | | | 20 | | 20 | | |
| I _{IL} | LOAD | V _{CC} = 5.5 V, | V _I = 0.4 V | | | -1.5 | | | -1.5 | mA |
| | ENT | | | | | -1 | | -1 | | |
| | All others | | | | | -0.5 | | -0.5 | | |
| I _O ‡ | | V _{CC} = 5.5 V, | V _O = 2.25 V | -30 | | -112 | -30 | | -112 | mA |
| I _{CC} | | V _{CC} = 5.5 V | | 35 | 53 | | 35 | 53 | | mA |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

**SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS**

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

timing requirements over recommended operating conditions (see Figure 1)

| | | SN54AS161 SN54AS163 | | SN74AS161 SN74AS163 | | UNIT |
|--------------------|--|-------------------------------------|---|------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | 65 | | 75 | | MHz |
| t_w | Pulse duration | $\overline{\text{CLR}}$ high or low | | 7.7 | 6.7 | ns |
| | | 'AS161 | $\overline{\text{CLR}}$ low | 10 | 8 | |
| t_{su} | Setup time, before CLK \uparrow | A, B, C, D | | 10 | 8 | ns |
| | | $\overline{\text{LOAD}}$ | | 10 | 8 | |
| | | ENP, ENT | | 10 | 8 | |
| | | 'AS161 | $\overline{\text{CLR}}$ inactive | 10 | 8 | |
| | | 'AS163 | $\overline{\text{CLR}}$ low | 14 | 12 | |
| | | | $\overline{\text{CLR}}$ high (inactive) | 10 | 9 | |
| t_h | Hold time, all synchronous inputs after CLK \uparrow | 2 | | 0 | | ns |

switching characteristics over recommended operating conditions (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54AS161 | | SN74AS161 | | UNIT |
|------------------|-------------------------|--|-----------|------|-----------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| f_{max} | | | 65* | | 75 | | MHz |
| t_{PLH} | CLK | RCO (with $\overline{\text{LOAD}}$ high) | 1 | 8.5 | 1 | 8 | ns |
| | | RCO (with $\overline{\text{LOAD}}$ low) | 3 | 17.5 | 3 | 16.5 | |
| t_{PHL} | CLK | RCO | 2 | 14 | 2 | 12.5 | ns |
| t_{PLH} | CLK | Any Q | 1 | 7.5 | 1 | 7 | ns |
| t_{PHL} | | | 2 | 14 | 2 | 13 | |
| t_{PLH} | ENT | RCO | 1.5 | 10 | 1.5 | 9 | ns |
| t_{PHL} | | | 1 | 9.5 | 1 | 8.5 | |
| t_{PHL} | $\overline{\text{CLR}}$ | Any Q | 2 | 14 | 2 | 13 | ns |
| | | RCO | 2 | 14 | 2 | 12.5 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating conditions (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54AS163 | | SN74AS163 | | UNIT |
|------------------|-----------------|--|-----------|------|-----------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| f_{max} | | | 65* | | 75 | | MHz |
| t_{PLH} | CLK | RCO (with $\overline{\text{LOAD}}$ high) | 1 | 8.5 | 1 | 8 | ns |
| | | RCO (with $\overline{\text{LOAD}}$ low) | 3 | 17.5 | 3 | 16.5 | |
| t_{PHL} | CLK | RCO | 2 | 14 | 2 | 12.5 | ns |
| t_{PLH} | CLK | Any Q | 1 | 7.5 | 1 | 7 | ns |
| t_{PHL} | | | 2 | 14 | 2 | 13 | |
| t_{PLH} | ENT | RCO | 1.5 | 10 | 1.5 | 9 | ns |
| t_{PHL} | | | 1 | 9.5 | 1 | 8.5 | |

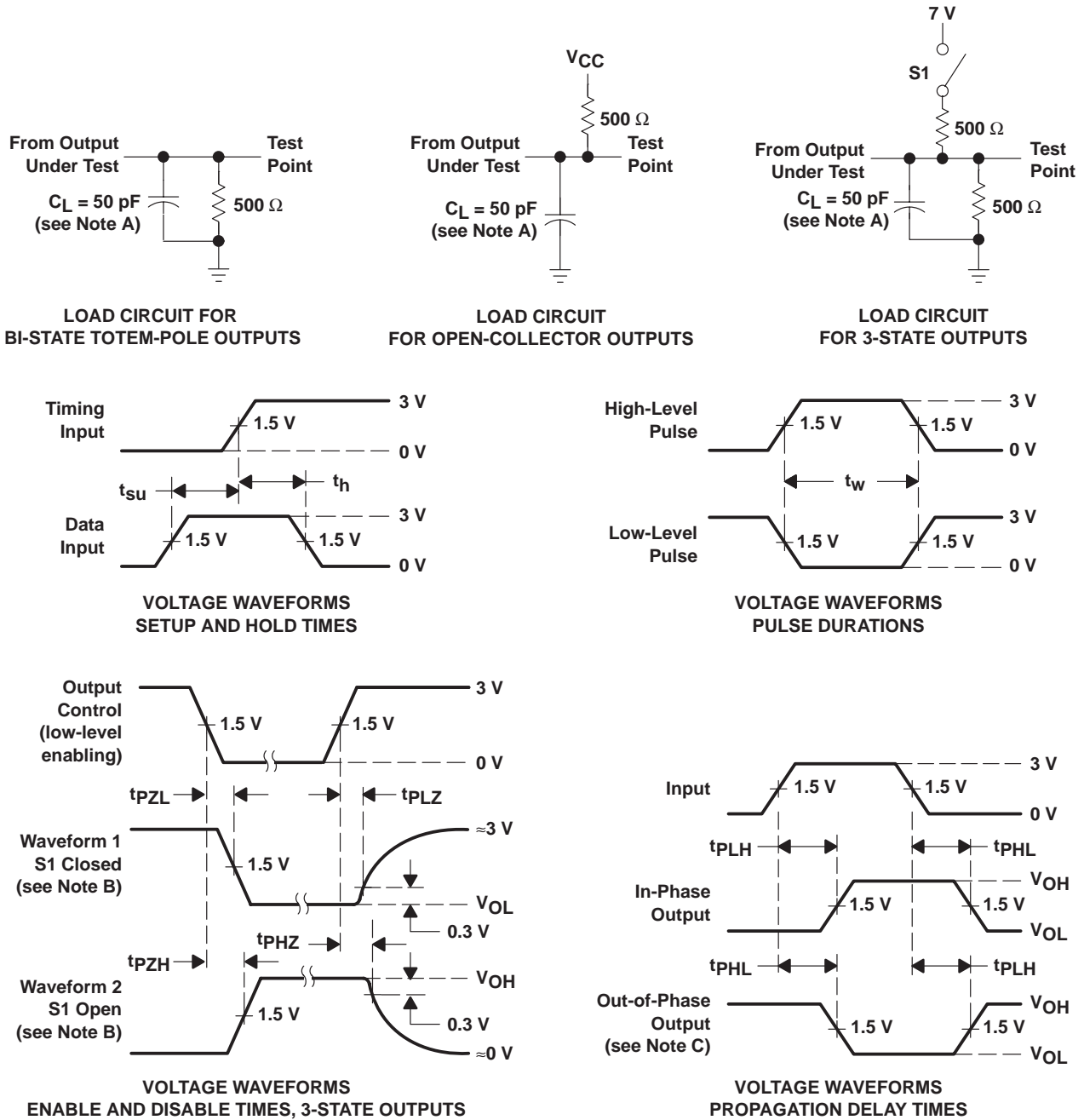
* On products compliant to MIL-PRF-38535, this parameter is not production tested.



SN54ALS161B, SN54ALS162B, SN54ALS163B, SN54AS161, SN54AS163
 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

PARAMETER MEASUREMENT INFORMATION
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

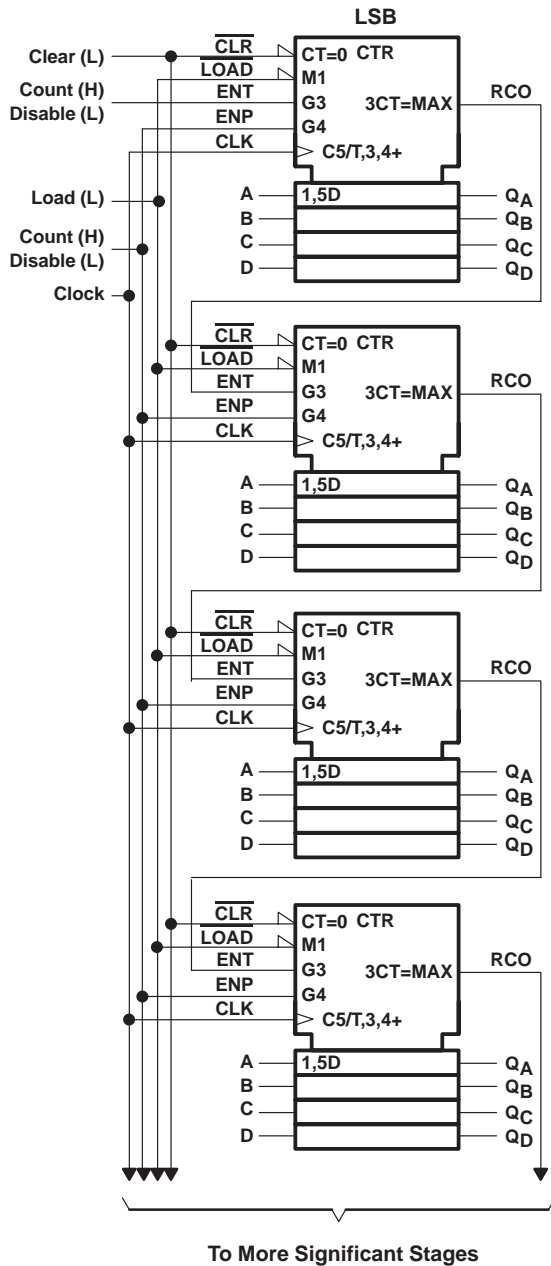
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 SN74ALS161B, SN74ALS163B, SN74AS161, SN74AS163
 SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SDAS276A – DECEMBER 1994 – REVISED JULY 2000

APPLICATION INFORMATION

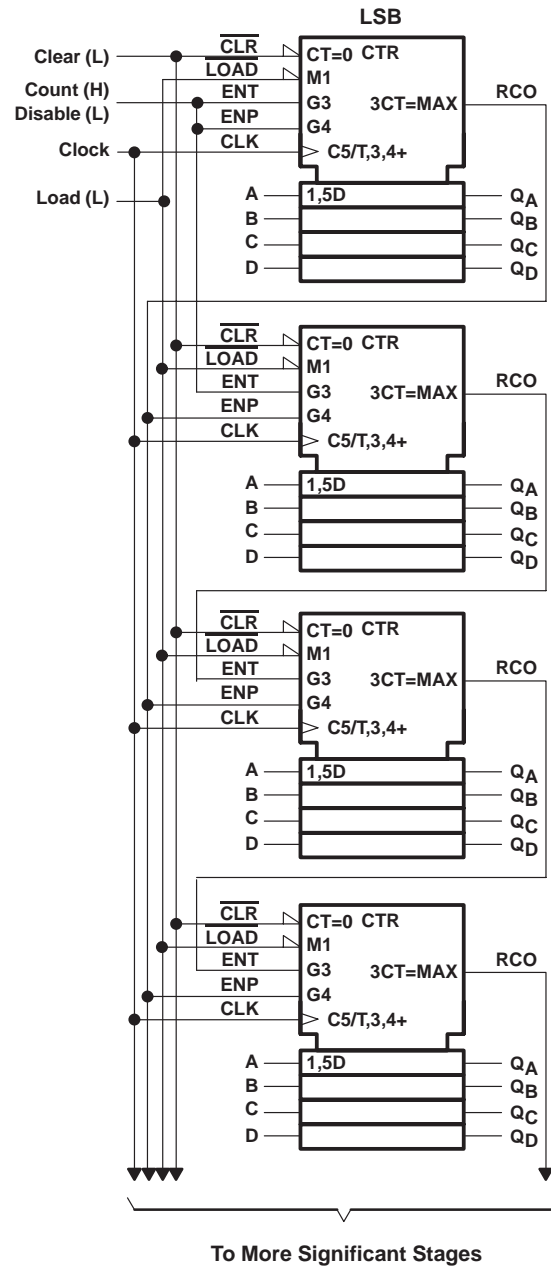
n-bit synchronous counters

This application demonstrates how the ripple-mode carry circuit (see Figure 2) and the carry look-ahead circuit (see Figure 3) can be used to implement a high-speed n-bit counter. The SN54ALS162B counts in BCD. The 'ALS161B, 'AS161, 'ALS163B, and 'AS163 devices count in binary. When additional stages are added, the f_{max} decreases in Figure 2, but remains unchanged in Figure 3.



$$f_{max} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENT to RCO } t_{PLH}) (N - 2) + (\text{ENT } t_{su})$$

Figure 2. Ripple-Mode Carry Circuit



$$f_{max} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENP } t_{su})$$

Figure 3. Carry Look-Ahead Circuit

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|---------------------------------|-------------------------|
| 83022012A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 83022012A SNJ54ALS 161BFK | Samples |
| 8302201EA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8302201EA SNJ54ALS161BJ | Samples |
| 8302201FA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8302201FA SNJ54ALS161BW | Samples |
| 83022022A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 83022022A SNJ54ALS 163BFK | Samples |
| 8302202EA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8302202EA SNJ54ALS163BJ | Samples |
| JM38510/38001B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 38001B2A | Samples |
| JM38510/38001BEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 38001BEA | Samples |
| JM38510/38002B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 38002B2A | Samples |
| JM38510/38002BEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 38002BEA | Samples |
| M38510/38001B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 38001B2A | Samples |
| M38510/38001BEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 38001BEA | Samples |
| M38510/38002B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 38002B2A | Samples |
| M38510/38002BEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 38002BEA | Samples |
| SN54ALS161BJ | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54ALS161BJ | Samples |
| SN54ALS163BJ | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54ALS163BJ | Samples |
| SN74ALS161BD | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS161B | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|---------------------------------|-------------------------|
| SN74ALS161BDR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS161B | Samples |
| SN74ALS161BN | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS161BN | Samples |
| SN74ALS161BNSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS161B | Samples |
| SN74ALS163BD | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS163B | Samples |
| SN74ALS163BDR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS163B | Samples |
| SN74ALS163BN | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74ALS163BN | Samples |
| SN74ALS163BNSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS163B | Samples |
| SN74AS161N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS161N | Samples |
| SN74AS161NSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS161 | Samples |
| SN74AS163D | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS163 | Samples |
| SN74AS163N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74AS163N | Samples |
| SNJ54ALS161BFK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 83022012A SNJ54ALS 161BFK | Samples |
| SNJ54ALS161BJ | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8302201EA SNJ54ALS161BJ | Samples |
| SNJ54ALS161BW | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8302201FA SNJ54ALS161BW | Samples |
| SNJ54ALS163BFK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 83022022A SNJ54ALS 163BFK | Samples |
| SNJ54ALS163BJ | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8302202EA SNJ54ALS163BJ | Samples |
| SNJ54AS161J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54AS161J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS161B, SN54ALS163B, SN54AS161, SN74ALS161B, SN74ALS163B, SN74AS161 :

● Catalog : [SN74ALS161B](#), [SN74ALS163B](#), [SN74AS161](#)

● Military : [SN54ALS161B](#), [SN54ALS163B](#), [SN54AS161](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS161BDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74ALS161BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ALS163BDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74ALS163BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AS161NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS161BDR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74ALS161BNSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74ALS163BDR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74ALS163BNSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AS161NSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 83022012A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| 8302201FA | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| 83022022A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| JM38510/38001B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| JM38510/38002B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| M38510/38001B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| M38510/38002B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SN74ALS161BD | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74ALS161BN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS161BN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS163BD | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74ALS163BN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS163BN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS161N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS161N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS163D | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74AS163N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS163N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54ALS161BFBK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54ALS161BW | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| SNJ54ALS163BFBK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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