3A, 34V Input PWM/VFM Step Down DC/DC Converter with PLL Synchronization for Automotive Applications

NO.EC-299-200624

OUTLINE

The R1270S is CMOS-based Step-down DC/DC converter with internal N-channel high side Tr. The ON resistance of the built-in high-side transistor is 0.10Ω and the R1270S can provide the maximum 3A output current. Each of the ICs consists of an oscillator, a PWM control circuit, a voltage reference unit, an error amplifier, a phase compensation circuit, a slope compensation circuit, a soft-start circuit, protection circuits, an internal voltage regulator, and a switch for bootstrap circuit. The ICs can make up a step-down DC/DC converter with adding an inductor, resistors, a diode, and capacitors externally. The R1270S is current mode operating type DC/DC converters without an external current sense resistor, and realizes fast response and high efficiency. As an output capacitor, a ceramic type capacitor is usable. The internal oscillator frequency is adjustable over a range of 300kHz to 2400kHz by an external resistor, and also can be synchronized externally by PLL. The phase compensation is adjustable by using external resistor and capacitor. Thereby optimizations for the inductor and the capacitor can be done. To improve performance under light load conditions, the R1270S can select automatically between two modes: the VFM mode when the inductor current is discontinuous and the PWM mode when the inductor current is continuous. The ripple voltage at VFM mode is 40mV (Typ.). As for protection, the R1270S has a current limit function to control an inductor peak current every cycle, a fold-back function to reduce the oscillator frequency under the short circuit, a thermal shutdown function, an under voltage lockout (UVLO) function, and an over voltage lockout (OVLO) function. Furthermore, the R1270S can include a latch protection function to cut off the output when the output current reaches the set current limit for a certain time. That is, the R1270S supports two types of the presence (R1270S001A) or the absence (R1270S001B) of the latch protection function. The current limit, which is fixed at 4.5A (Typ.), is adjustable by an external resistor. The soft start time is fixed at 0.4ms (Typ.) internally, but is adjustable by an external resistor. And, the R1270S has the FLG pin to monitor the overvoltage of the FB pin voltage and the 6V rated pin. When detecting an abnormal voltage, the R1270S outputs a flag. The R1270S is available in HSOP-18 package.

FEATURES

- Operating Voltage (Maximum Rating) ····· 3.6V to 34V (36V)
- Consumption Current ····· Typ. 18μA (V_{IN} = 12V)
- Stand-by Current ····· Typ. 0μA (V_{IN} = 34V, CE=0V)
- Output Voltage ····· Externally-adjustable at 0.8V or more
  (Max. step down ratio 160ns × fosc)
- Feedback Voltage and Tolerance ····· 0.8V±1.0%

- Output Current ····· 3A[1]
- Operating Frequency ····· 300kHz to 2.4MHz settable by external resistor
- Minimum Off Time ····· Typ. 120ns
- Maximum Duty ····· Min. 93% (fosc = 300kHz), Min. 67% (fosc = 2400kHz)
- UVLO Function Detection Voltage ····· Typ. 2.6V
- OVLO Function Detection Voltage ····· Min. 38V
- Soft-start Time ····· Internal soft-start time (Typ. 0.4ms), as a lower limit, Externally-adjustable by using capacitor
- High-side Switch Current Limit ····· Typ. 4.5A, as a upper limit, Externally-adjustable by using resistor
- Thermal Shutdown Function ····· Typ. 160°C
- CE Threshold Voltage ····· Typ. 1.0V
- Latch Protection Delay Time ····· Typ. 2ms (R1270S001A)
- Fold-back Protection ····· Fold-back for oscillation frequency
- Packages ····· HSOP-18

APPLICATIONS

- Power source for car accessories including car audio equipment, car navigation system, and ETC system.
- Power source for control units including EV inverter and charge control.

SELECTION GUIDE

The latch type protection function is user-selectable.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1270S001∗-E2-#E	HSOP-18	1,000 pcs	Yes	Yes

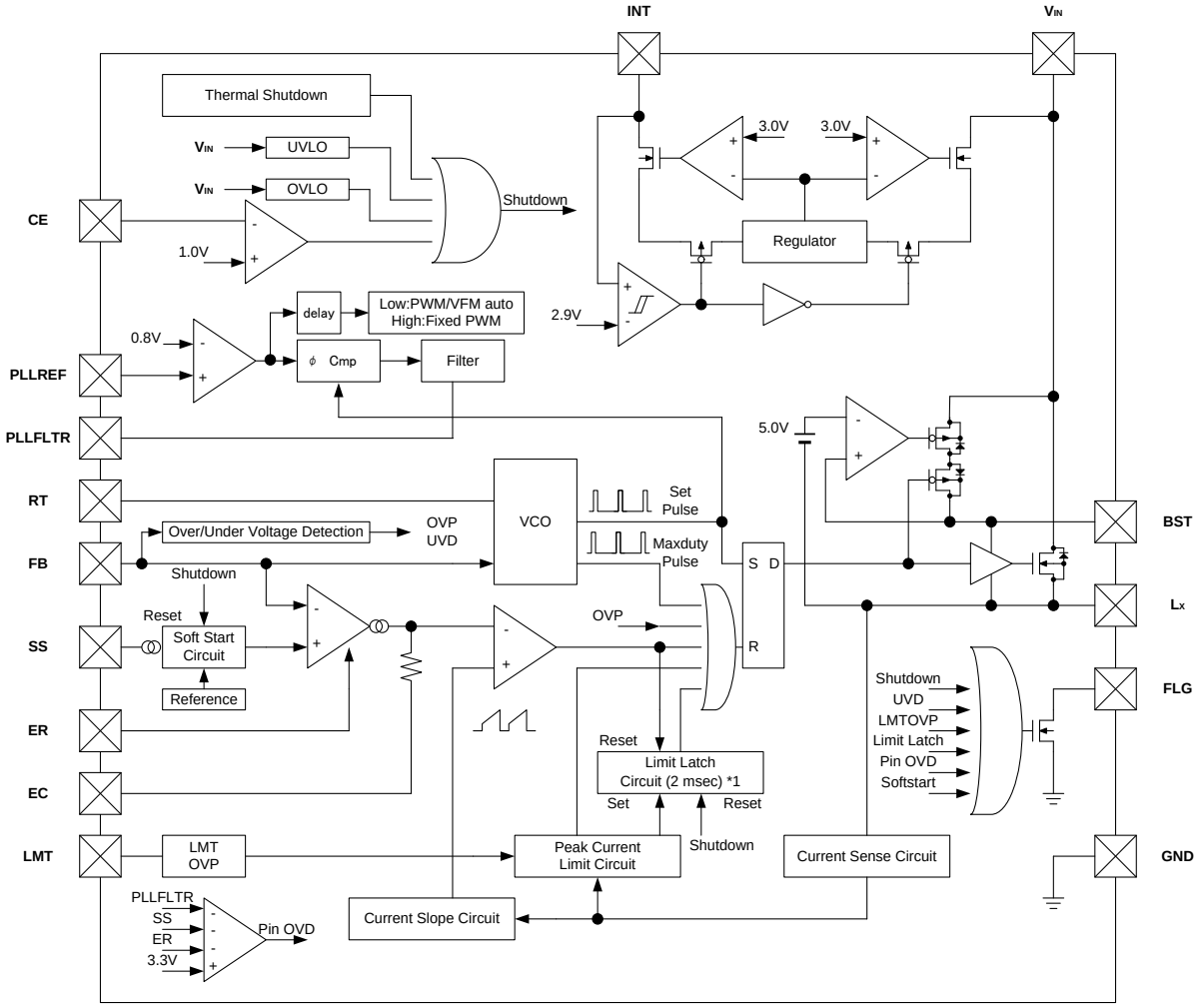
∗: Select the presence or absence of the latch type protection function.
A: with Latch type protection function
B: without Latch type protection function

#: Select the quality class.

	Operating Temperature Range	Test Temp.
A	−40°C to 125°C	25°C, High
K	−40°C to 125°C	Low, 25°C, High

[1] The output current depends on external components and conditions.

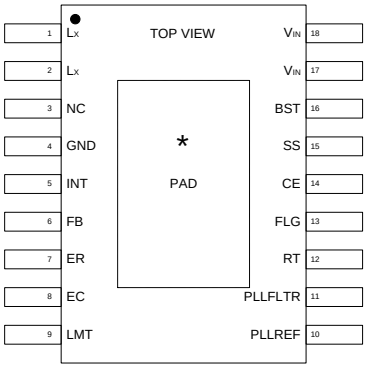
BLOCK DIAGRAMS



*1 R1270S001A equips the limit latch circuit.

R1270S001A/B Block Diagram

PIN DESCRIPTIONS



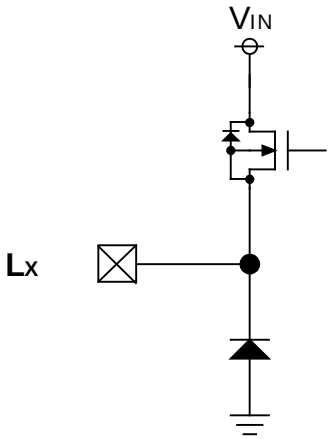
R1270S (HSOP-18) Pin Configuration

R1270S Pin Description

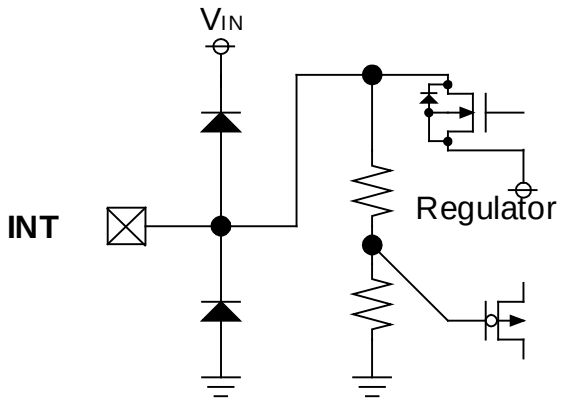
Pin No.	Symbol	Description
1, 2	L_X	Lx Switching Pin
3	NC	No connection
4	GND	Ground Pin
5	INT	Internal Bias Pin
6	FB	Feedback Pin
7	ER	Phase Compensation Pin for External Resistor
8	EC	Phase Compensation Pin for External Capacitor
9	LMT	Current Limit adjustment Pin
10	PLLREF	PLL Synchronization Pin
11	PLLFLTR	PLL Filter Pin
12	RT	Oscillation adjustment Pin
13	FLG	Flag Output Pin
14	CE	Chip Enable Pin (Active “H”)
15	SS	Soft-start Pin
16	BST	Bootstrap Pin
17, 18	VIN	Power Supply Pin

* The tab on the bottom of the package must be electrically connected to GND (substrate level) when mounted on the board.

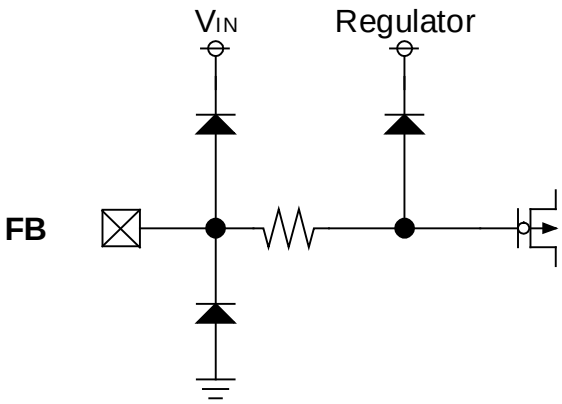
Internal Equivalent Circuit for Each Pin



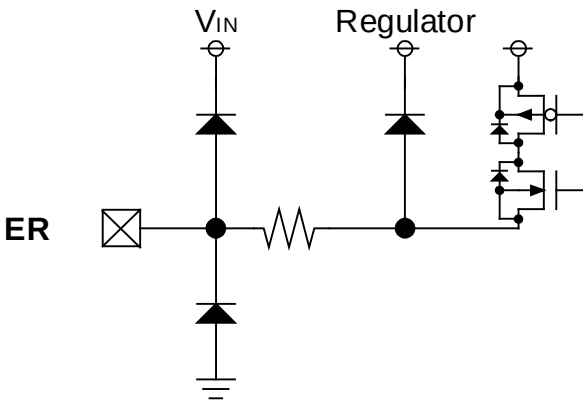
<Lx Pin>



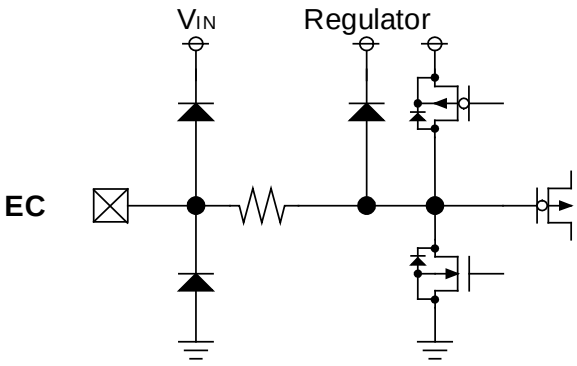
<INT Pin>



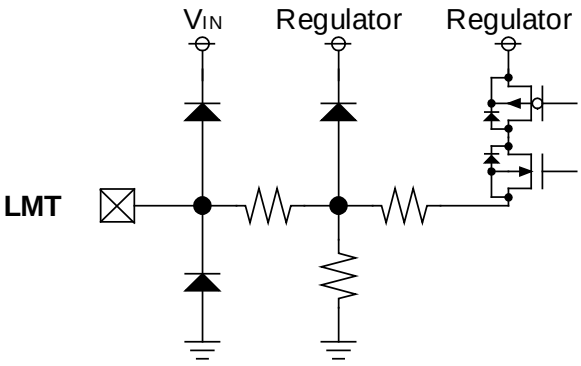
<FB Pin>



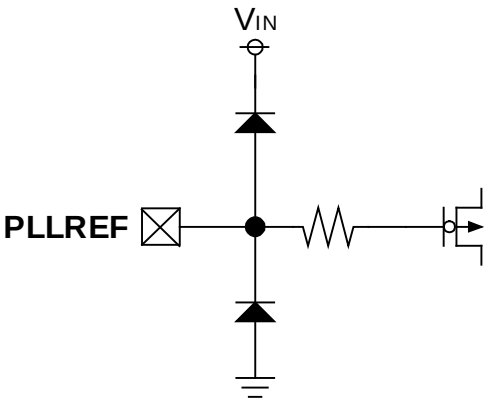
<ER Pin >



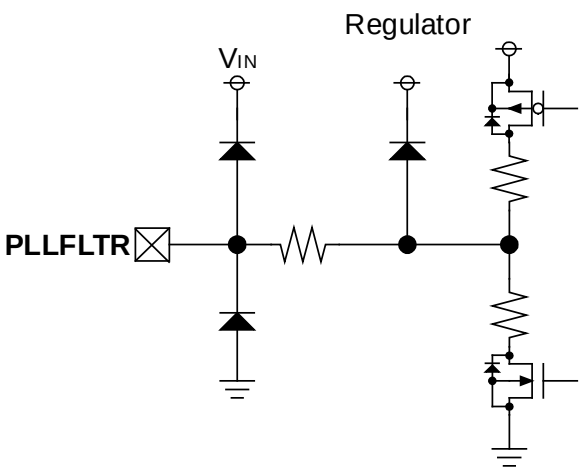
<EC Pin>



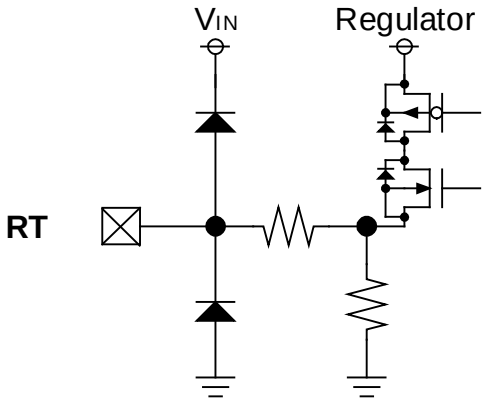
<LMT Pin>



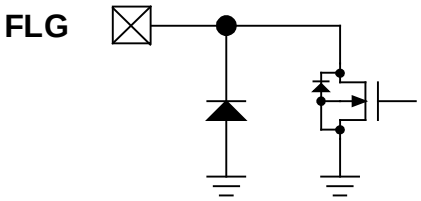
<PLLREF Pin>



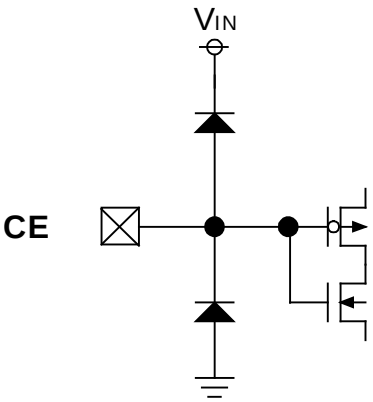
<PLLFLTR Pin>



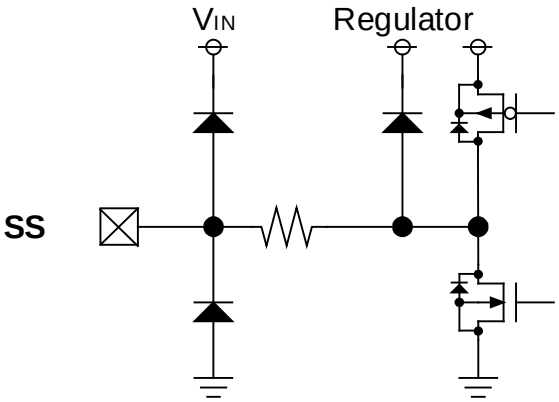
<RT Pin>



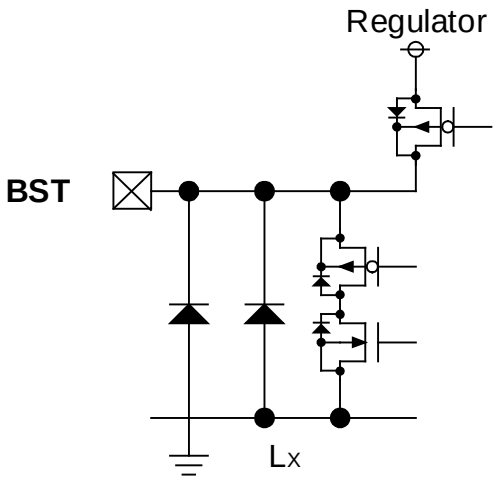
<FLG Pin>



<CE Pin>



<SS Pin>



<BST Pin>

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	−0.3 to 36	V
V_{BST}	BST Pin Voltage(1)	V_{LX}−0.3 to V_{LX}+6	V
V_{LX}	L_X Pin Voltage	−0.3 to 36	V
V_{CE}	CE Pin Input Voltage	−0.3 to 36	V
V_{INT}	INT Pin Voltage	−0.3 to 36	V
V_{SS}	Soft-start Pin Voltage	−0.3 to 6	V
V_{ER}	ER Pin Voltage	−0.3 to 6	V
V_{EC}	EC Pin Voltage	−0.3 to 6	V
V_{FB}	Feedback Pin Voltage	−0.3 to 6	V
V_{FLG}	Flag Pin Voltage(1)	−0.3 to 24	V
V_{PLLREF}	External Oscillation Synchronization Pin Voltage	−0.3 to 36	V
$V_{PLLFLTR}$	PLL Filter Pin Voltage	−0.3 to 6	V
V_{RT}	Oscillation adjustment Pin Voltage	−0.3 to 6	V
V_{LMT}	Current Limit adjustment Pin Voltage	−0.3 to 6	V
P_D	Power Dissipation(2) (HSOP-18, JEDEC STD.51)	3900	mW
Tj	Junction Temperature	−40 to 150	°C
Tstg	Storage Temperature Range	−55 to 150	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	3.6 to 34	V
Ta	Operating Temperature Range	−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) The pin voltage except V_{BST} and V_{FLG} must be prevented from exceeding V_{IN} +0.3V.
(2) Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, Ta = 25°C, unless otherwise specified.
The specifications surrounded by [ ] are guaranteed by design engineering at -40°C ≤ Ta ≤ 125°C.

R1270S001A/B-AE **(Ta = 25°C)**

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
I_{IN1}	V_{IN} Consumption current 1	V_{IN} = 34 V, V_{INT} = Open, V_{PLLREF} = 34 V, V_{FB} = 1.5 V	[0.7]	1	[1.3]	mA
I_{IN2}	V_{IN} Consumption current 2	V_{IN} = 34 V, V_{INT} = Open, V_{PLLREF} = 0, V_{FB} = 0.84 V	[13]	18	[30]	µA
V_{UVLO2}	UVLO Released Voltage	V_{IN} Rising	[2.5]	2.6	[2.7]	V
V_{UVLO1}	UVLO Detect Voltage	V_{IN} Falling	[V_{UVLO2} −0.16]	V_{UVLO2} −0.15	[V_{UVLO2} −0.11]	V
V_{OVLO2}	OVLO Released Voltage	V_{IN} Falling	[34]			V
V_{OVLO1}	OVLO Detect Voltage	V_{IN} Rising		38		V
V_{FB}	V_{FB} Voltage Tolerance	Ta = 25°C	0.792	0.800	0.808	V
		−40°C ≤ Ta ≤ 125°C	[0.784]		[0.816]	V
V_{VFM}	FB High Detection at VFM mode				[0.831]	V
fosc0	Oscillation Frequency 0	RT = Open	[270]	300	[330]	kHz
fosc1	Oscillation Frequency 1	RT = 62 kΩ	[900]	1010	[1120]	kHz
fosc2	Oscillation Frequency 2	RT = GND	[2160]	2400	[2640]	kHz
toff	Minimum Off Time			120		ns
D_{MAX0}	Maximum Duty Cycle 0	RT = Open	[93]			%
D_{MAX0}	Maximum Duty Cycle 1	RT = 62 kΩ	[83]			%
D_{MAX2}	Maximum Duty Cycle 2	RT = GND	[67]			%
f_{SYNC}	Oscillation Synchronized Frequency	f_{PLLREF} = 1000 kHz	[fosc/2]		[foscx2]	kHz
tss1	Soft-start Time 1	SS = Open, V_{FB} = 0.72 V	[0.3]		[0.55]	ms
tss2	Soft-start Time 2	C_{SS} = 0.01 µF, V_{FB} = 0.72 V	[3.1]		[4.5]	ms
Itss	Soft-start charge current	SS = 0 V	[1.7]	2.0	[2.35]	µA
tdelay	Delay Time for Latch Protection	for R1270S001A	[1.4]	2	[2.8]	ms
R_{LXH}	Lx High Side Switch ON Resistance	V_{BST}−V_{LX} = 4.5V, I_{LX} = 0.1A		0.1	[0.15]	Ω
I_{LXHOFF}	Lx High Side Switch Leakage Current			0	[20]	µA
$I_{LIMLXH1}$	Lx High Side Switch Limited Current 1	LMT = 220 kΩ、DC Current	[3.0]	3.5	[4.3]	A
$I_{LIMLXH2}$	Lx High Side Switch Limited Current 2	LMT = 39 kΩ、DC Current	[1.25]	1.6	[2.4]	A

V_{IN} = 12 V, Ta = 25°C, unless otherwise specified.
The specifications surrounded by [ ] are guaranteed by design engineering at -40°C ≤ Ta ≤ 125°C.

R1270S001A/B-AE (Continued) **(Ta = 25°C)**

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{CEH}	CE “H” Input Voltage		[1.15]			V
V_{CEL}	CE “L” Input Voltage				[0.85]	V
I_{CEH}	CE “H” Input Current		[−1.0]	0	[1.0]	µA
I_{CEL}	CE “L” Input Current		[−1.0]	0	[1.0]	µA
I_{FBH}	FB “H” Input Current	V_{FB} = 1.5 V	[−0.1]	0	[0.1]	µA
I_{FBL}	FB “L” Input Current	V_{FB} = 0 V	[−0.1]	0	[0.1]	µA
V_{PLLH}	PLLREF “H” Input Voltage		[0.95]			V
V_{PLLL}	PLLREF “L” Input Voltage				[0.67]	V
I_{PLLH}	PLLREF“H” Input Current		[−1.0]	0	[1.0]	µA
I_{PLLL}	PLLREF“L” Input Current		[−1.0]	0	[1.0]	µA
T_{TSD}	Thermal Shutdown Detect Temperature			160		°C
T_{TSR}	Thermal Shutdown Release Temperature			130		°C
Istandby	Standby Current	V_{IN} = 34 V, V_{CE} = 0 V		0	[20]	µA
V_{FLGL}	FLAG ”L” Voltage	V_{IN} = 2.0 V, I_{FLG} = 1 mA			[0.25]	V
I_{FLGOFF}	FLAG ”Off” Current	V_{FLG} = 6.0 V		0.0	[0.1]	µA
V_{OVP}	FB Pin OVP Detect Voltage		[0.91]	0.98	[1.04]	V
V_{UVD}	FB Pin UVD Detect Voltage		[0.59]	0.64	[0.69]	V
V_{FLB}	Fold Back Detect Voltage		[0.59]		[0.69]	V
V_{POVD}	6V-rated Pin OVP Detect Voltage	V_{ER}, $V_{PLLFLTR}$, V_{SS}		4.0		V
V_{VOS0}	INT Pin Operation Voltage		[2.75]		[3.1]	V
V_{VOS1}	INT Pin Disable Voltage		[2.68]		[2.8]	V

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

V_{IN} = 12 V, unless otherwise specified.

R1270S001A/B-KE **(−40°C ≤ Ta ≤ 125°C)**

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
I_{IN1}	V_{IN} Consumption current 1	V_{IN} = 34 V, V_{INT} = Open, V_{PLLREF} = 34 V, V_{FB} = 1.5 V	0.7	1	1.3	mA
I_{IN2}	V_{IN} Consumption current 2	V_{IN} = 34 V, V_{INT} = Open, V_{PLLREF} = 0, V_{FB} = 0.84 V	13	18	30	µA
V_{UVLO2}	UVLO Released Voltage	V_{IN} Rising	2.5	2.6	2.7	V
V_{UVLO1}	UVLO Detect Voltage	V_{IN} Falling	V_{UVLO2} −0.16	V_{UVLO2} −0.15	V_{UVLO2} −0.11	V
V_{OVLO2}	OVLO Released Voltage	V_{IN} Falling	34			V
V_{OVLO1}	OVLO Detect Voltage	V_{IN} Rising		38		V
V_{FB}	V_{FB} Voltage Tolerance	Ta = 25°C	0.792	0.800	0.808	V
		−40°C ≤ Ta ≤ 125°C	0.784		0.816	V
V_{VFM}	FB High Detection at VFM mode				0.831	V
fosc0	Oscillation Frequency 0	RT = Open	270	300	330	kHz
fosc1	Oscillation Frequency 1	RT = 62 kΩ	900	1010	1120	kHz
fosc2	Oscillation Frequency 2	RT = GND	2160	2400	2640	kHz
toff	Minimum Off Time			120		ns
D_{MAX0}	Maximum Duty Cycle 0	RT = Open	93			%
D_{MAX0}	Maximum Duty Cycle 1	RT = 62 kΩ	83			%
D_{MAX2}	Maximum Duty Cycle 2	RT = GND	67			%
f_{SYNC}	Oscillation Synchronized Frequency	f_{PLLREF} = 1000 kHz	fosc/2		foscx2	kHz
tss1	Soft-start Time 1	SS = Open, V_{FB} = 0.72 V	0.3		0.55	ms
tss2	Soft-start Time 2	C_{SS} = 0.01 µF, V_{FB} = 0.72 V	3.1		4.5	ms
Itss	Soft-start charge current	SS = 0 V	1.7	2.0	2.35	µA
tdelay	Delay Time for Latch Protection	for R1270S001A	1.4	2	2.8	ms
R_{LXH}	Lx High Side Switch ON Resistance	V_{BST}−V_{LX} = 4.5V, I_{LX} = 0.1A		0.1	0.15	Ω
I_{LXHOFF}	Lx High Side Switch Leakage Current			0	20	µA
$I_{LIMLXH1}$	Lx High Side Switch Limited Current 1	LMT = 220 kΩ、DC Current	3.0	3.5	4.3	A
$I_{LIMLXH2}$	Lx High Side Switch Limited Current 2	LMT = 39 kΩ、DC Current	1.25	1.6	2.4	A

V_{IN} = 12 V, unless otherwise specified.

R1270S001A/B-KE (Continued) **(−40°C ≤ Ta ≤ 125°C)**

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{CEH}	CE “H” Input Voltage		1.15			V
V_{CEL}	CE “L” Input Voltage				0.85	V
I_{CEH}	CE “H” Input Current		−1.0	0	1.0	µA
I_{CEL}	CE “L” Input Current		−1.0	0	1.0	µA
I_{FBH}	FB “H” Input Current	V_{FB} = 1.5 V	−0.1	0	0.1	µA
I_{FBL}	FB “L” Input Current	V_{FB} = 0 V	−0.1	0	0.1	µA
V_{PLLH}	PLLREF “H” Input Voltage		0.95			V
V_{PLLL}	PLLREF “L” Input Voltage				0.67	V
I_{PLLH}	PLLREF“H” Input Current		−1.0	0	1.0	µA
I_{PLLL}	PLLREF“L” Input Current		−1.0	0	1.0	µA
T_{TSD}	Thermal Shutdown Detect Temperature			160		°C
T_{TSR}	Thermal Shutdown Release Temperature			130		°C
Istandby	Standby Current	V_{IN} = 34 V, V_{CE} = 0 V		0	20	µA
V_{FLGL}	FLAG ”L” Voltage	V_{IN} = 2.0 V, I_{FLG} = 1 mA			0.25	V
I_{FLGOFF}	FLAG ”Off” Current	V_{FLG} = 6.0 V		0.0	0.1	µA
V_{OVP}	FB Pin OVP Detect Voltage		0.91	0.98	1.04	V
V_{UVD}	FB Pin UVD Detect Voltage		0.59	0.64	0.69	V
V_{FLB}	Fold Back Detect Voltage		0.59		0.69	V
V_{POVD}	6V-rated Pin OVP Detect Voltage	V_{ER}, $V_{PLLFLTR}$, V_{SS}		4.0		V
V_{VOS0}	INT Pin Operation Voltage		2.75		3.1	V
V_{VOS1}	INT Pin Disable Voltage		2.68		2.8	V

THEORY OF OPERATION

OVLO (Over Voltage Lock Out) Function

When the input voltage to V_{IN} pin is higher than OVLO detection voltage, the inside circuit becomes standby to prevent malfunction. If the voltage on the V_{IN} pin becomes lower than the OVLO release voltage, R1270S will restart and the soft-start function will begin. Also, the OVLO protection has a function to prevent the possibility of the malfunction and destruction to the IC. Since the OVLO detection voltage is set higher than the absolute maximum rating for V_{IN} pin, the function itself is not guaranteed.

OVP (Over Voltage Protection) Function for FB Pin

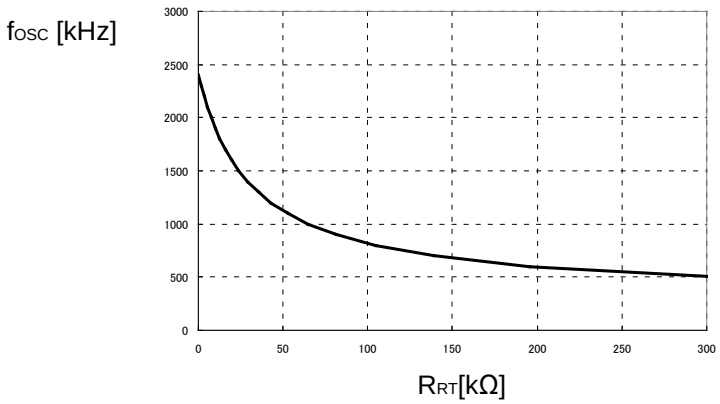
When the FB pin voltage becomes higher than the OVP detection voltage, the OVP function stops the switching of Lx pin without stopping the function of the internal circuit. When the FB pin voltage becomes lower than the OVP detect voltage, the Lx pin switching returns to normal control. If aberrant conditions around the FB pin circuit occur, the overvoltage of the output voltage may not be decreased because the R1270S indirectly monitors the output voltage via FB pin.

Setup for Oscillation Frequency

By using R_{RT} between the RT pin and GND, the R1270S can control the oscillation frequency in the range of 300 kHz to 2400 kHz. For example, by using 62 kΩ as R_{RT}, the frequency will be set about 1000 kHz.

When setting the frequency at either 300 kHz or 2400 kHz, the frequency depends on whether the RT pin is set to "Open" or "GND", without using RRT. That is, the frequency is set at 300 kHz when the RT pin is “Open”, and is set at 2400 kHz when it is “GND”.

The Electrical Characteristics guarantees the oscillation frequency under the conditions stated below for f_{OCS0}, f_{OCS1} and f_{OCS2}.



R_{RT} [kΩ] = 1 / (1 / (((1 / fosc [kHz] x 1000000 −125) / 292 x 25) − 25) − 1 / 250)

R1270S001A/B Oscillation Frequency Setting Resistor (R_{RT}) vs. Oscillation Frequency (fosc)

Synchronization of Oscillation Frequency

The R1270S can synchronize to an external clock, which is input from the PLLREF pin, with using phase-locked loop. The PWM fixed mode is set during synchronization. The detection threshold of the external clock is 0.8 V (Typ.) and the pulse of 100 ns or more are required.

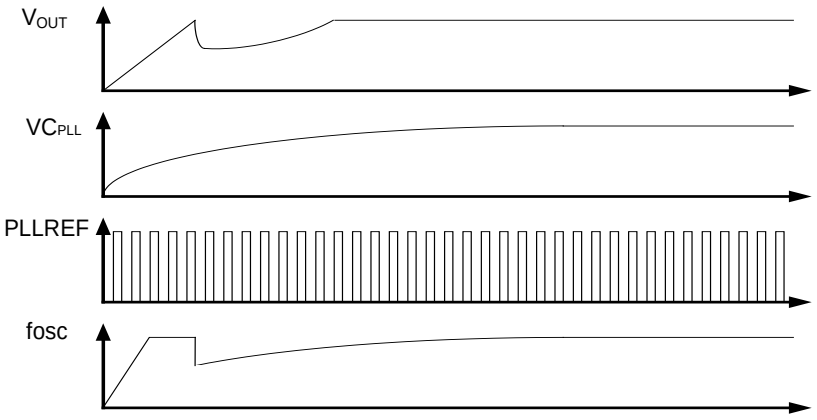
The phase compensation filter is required to stabilize the phase-locked loop. The frequency fluctuation, which is changed from the set frequency to the synchronized frequency, can be achieved smoothly by the constant of this filter. Place 10 kΩ resistor and 220 pF capacitor in series between PLLFTR pin and GND.

The oscillation frequency which could be synchronized is 0.5 to 2 times of that stated in the “Setup of Oscillation Frequency”. However the guaranteed oscillation frequency is 270 kHz at the minimum, and 2640 kHz at the maximum. Until the soft-start sequence is over, the R1270S operates at set oscillation frequency and after the soft-start sequence is over the oscillation frequency is synchronized to the external clock.

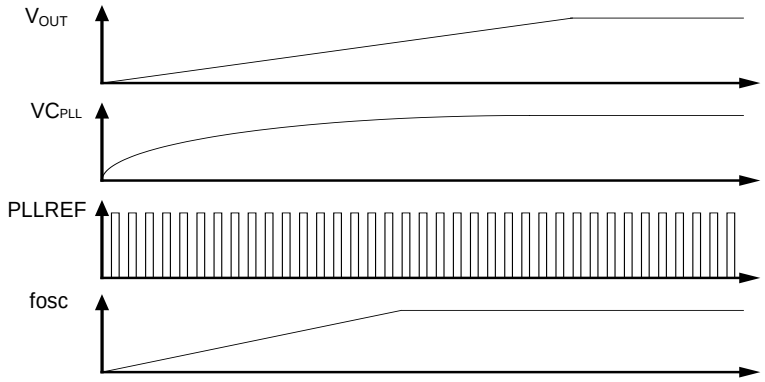
The phase compensation filter is charged with limited impedance, and the filter must be charged when synchronization starts. The time required for the phase compensation filter to be charged is as bellow.

$POLE_{PLL}$: $1/(C_{PLL}*(R_{PLL}+260k))$
95% charged : $3/POLE_{PLL}$[sec]
98% charged : $4/POLE_{PLL}$[sec]

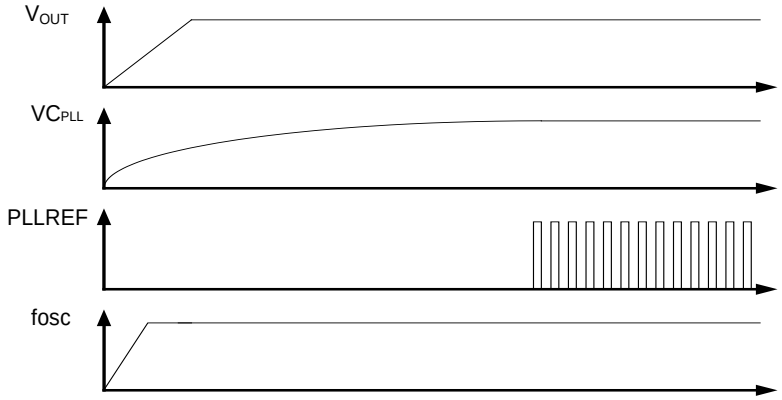
Adjust the soft-start time or the timing of the external clock input as $POLE_{PLL}$. The following shows the timing chart of self oscillation and external clock input.



R1270S001A/B PLL Filter Start-up Sequence
Phase Compensation Filter Charging Time > Soft-Start Time



R1270S001A/B PLL Filter Start-up Sequence
Phase Compensation Filter Charging Time < Soft-Start Time



R1270S001A/B PLL Filter Start-up Sequence
Phase Compensation Filter Charging Time < Synchronous Start Time with Eternal Clock

VFM/PWM Alternative Mode and PWM Fixed Mode

By applying either the voltage of 0.95 V or more or the external clock to the PLLREF pin, the R1270S operates in PWM fixed mode (Pulse-skip at light load). By applying the voltage of 0.67 V or less to the PLLREF pin, the R1270S operates in VFM/PWM alternative mode.

INT Pin Voltage

By applying the voltage of 3.1 V (Typ.) or more to the INT pin via the V_{OUT} pin, the R1270S generates 3 V internal power supply from V_{OUT}. Thereby the R1270S can improve the efficiency of the IC in VFM mode. When I_{IN_VFM} is as the 3 V internal current supply, the approximate expression for IC's consumption current: I_{IN} is V_{OUT} / V_{IN} × I_{IN_VFM}. That is, the consumption current will decrease as V_{OUT}/V_{IN} becomes smaller. But, when the INT pin voltage is lower than 3.1 V, the consumption current will not be reduced since the internal voltage supply becomes V_{IN}. Therefore, this architecture is aimed for applications which the V_{OUT} is 3.3 V or more. If the V_{OUT} is lower than 3.3 V, set the INT pin OPEN (No C_{INT} necessary).

Minimum ON Time

The minimum ON time is 160ns that is determined by the current sense circuit.

The R1270S adopts a resistor free current control mode. By using R_{ON} (Nch driver ON resistor) as a substitute for sense resistor, the R1270S senses I_{LX} (inductor current) according to $V_{IN} - V_{LX} = I_{LX} \times R_{ON}$. The R1270S can sense I_{LX} only during the Nch driver is On (Lx = "High"). However, if sensing it during the occurrence of the surge current right after the driver turns On, a malfunction may occur. To avoid the malfunction, the R1270S maintains a none sensing time for a while after the driver turns On.

If the current control mode and the current limit circuit will not function properly at none sensing time, the R1270S may result in a rapid deterioration of stability and current limit accuracy. Please select the output voltage settings and frequency settings so that the output voltage does not become lower than the minimum step down ratio $V_{IN} \times 160ns \times f_{OCS}$.

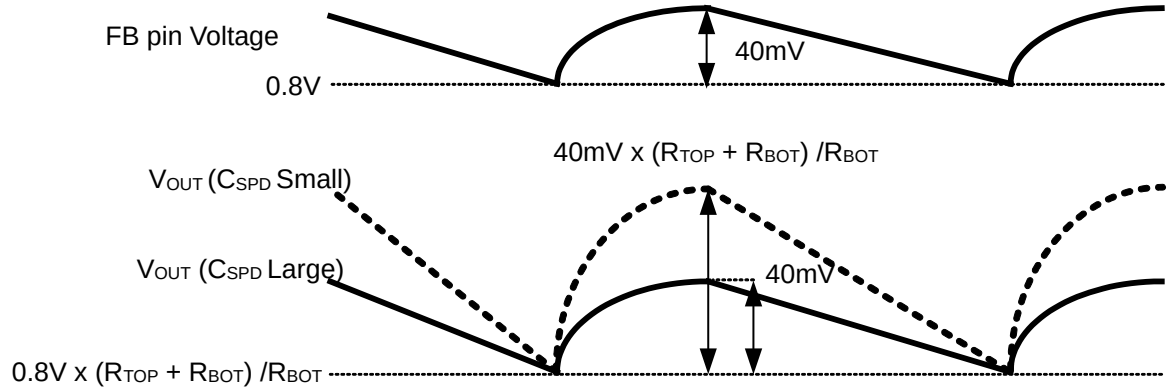
C_{SPD} Setting

The transfer function from feedback resistor of V_{OUT} to FB pin using C_{SPD} is

$$V_{OUT}/FB[s] = (R_{TOP} \times R_{BOT} \times C_{SPD} \times s + R_{BOT}) / (R_{TOP} \times R_{BOT} \times C_{SPD} \times s + R_{TOP} + R_{BOT})$$

From above equation, the zero is $R_{BOT}/(R_{TOP} \times R_{BOT} \times C_{SPD})$ and the pole is $(R_{TOP}+R_{BOT})/(R_{TOP} \times R_{BOT} \times C_{SPD})$. At low frequency level below zero V_{OUT} will be multiplication of $R_{BOT}/(R_{TOP}+R_{BOT})$ which means feedback by $0.8/V_{OUT}$ and when higher frequency level than the pole it will be feedback by 1.

At VFM mode the ripple of V_{OUT} is generated by 40mV (Typ.) higher than that of the reference voltage at PWM mode which is 0.8V. For all operating frequency range, the ripple of V_{OUT} is feedback by 1 to the FB pin despite the output voltage settings ripple of V_{OUT} will follow reference voltage by setting the C_{SPD} large. The bellow shows the example of setting the C_{SPD} large, where the ripple of V_{OUT} is feedback by 1 to the FB pin, and setting the C_{SPD} small, where the ripple of V_{OUT} is feedback by the multiple of $R_{BOT} / (R_{TOP}+R_{BOT})$.



R1270S001A/B VFM Ripple FB vs. V_{OUT}

As shown in the above figure, the ripple of V_{OUT} becomes larger when the C_{SPD} is small.

The recommended C_{SPD} value is selected to minimize the ripple of V_{OUT}. When changing the R_{BOT} value from the recommended value, please make sure the $R_{BOT} \times C_{SPD}$ is also in the range of the recommended value and change the C_{SPD} together. Also, changing L, C_{OUT}, R_{ER}, C_{EC} from the recommended value is required to change the C_{SPD}.

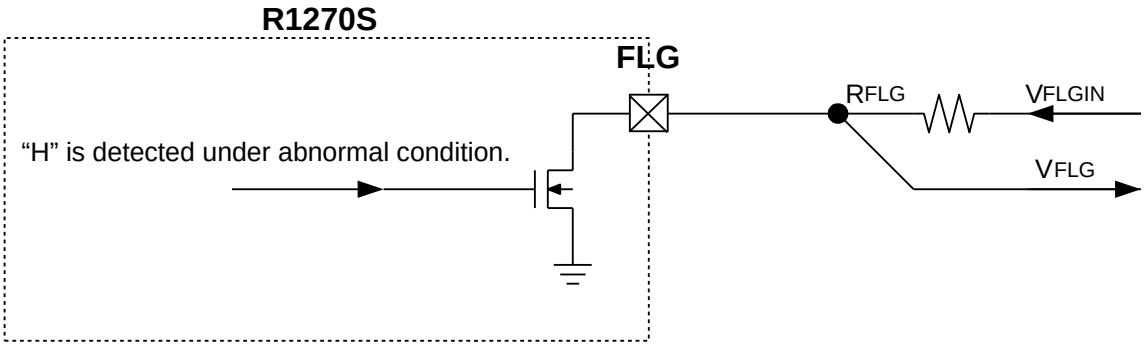
Furthermore, if the ripple of the VOUT is permissible, improving the loop stability is possible by adjusting the positive bump of the zero and pole. First, measure the voltage drop of the output by the load transient response without C_{SPD}. Then measure the voltage drop again with attachment of small enough C_{SPD}. If the selected C_{SPD} is too small, the amount of the voltage drop will be the same value as the value without C_{SPD}. Repeat the procedure with increasing C_{SPD} value gradually. When the voltage drop begins to improve, suppose that value as C_{SPD1}. Further try other C_{SPD} value by increasing it gradually, then the voltage drop improvement will stop. Suppose that the C_{SPD} value as Cspd2. The appropriate C_{SPD} value can be calculated as the next formula; $C_{SPD}=\sqrt{}(C_{SPD1} \times C_{SPD2})$. The zero will be low and pole will be high of the feedback resistor at the whole frequency range, the ripple at VFM mode will be lower than that V_{OUT} (C_{SPD} small) of above diagram

FLAG Output Function

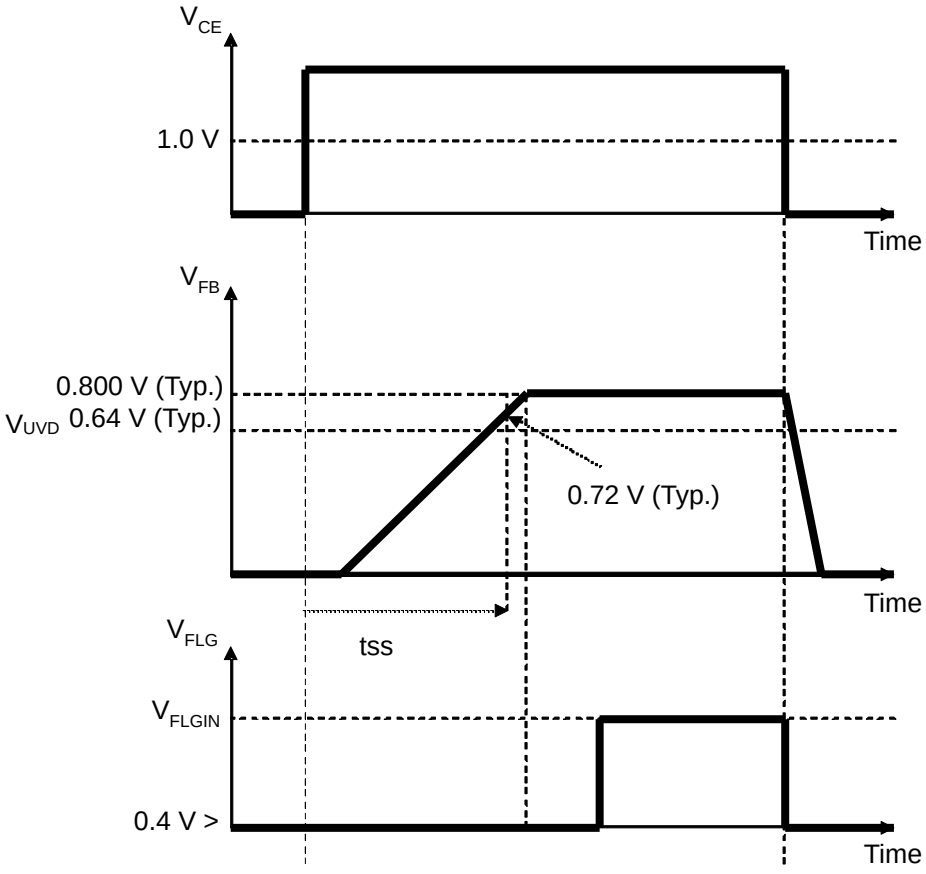
The R1270S has an Nch open drain FLAG output. When abnormality is detected, the R1270S switches the Nch transistor On, and sets the FLG pin to “Low”. When the abnormality is removed, the R1270S switches the Nch transistor Off and sets the FLG pin to “High” (V_{FLGIN}). The UVD will function only when V_{FB}<0.64V (Typ.) and at max duty detection or V_{FB}<0.64V (Typ.) and current limit detection to prevent abnormal output behavior at load transient and input transient response. The following are the abnormal conditions that the IC can detect.

- CE=”L” (Shut down)
- UVLO (Shut down)
- Thermal Shutdown
- during soft-start time (Css<0.72V)
- V_{FB} Under Voltage Detection (Typ.0.64V) and maxduty detection
- V_{FB} Under Voltage Detection (Typ.0.64V) and current limit detection
- LMT pin Over Voltage Protection (Typ.1.2V)
- Absolute maximum 6V pin (except FB pin、LMT pin、EC pin) Over Voltage Detection (Typ.3.0V)
- When the latch protection runs (R1270S001A)

The FLG pin is designed to keep 0.4V or less when the current running into the FLG pin is at 1mA. The recommended values of V_{FLGIN} and R_{FLG} are 6V or less for V_{FLGIN} and 10kΩ to 100kΩ for R_{FLG}. When the FLAG function is not used, set the FLG pin OPEN or connect to GND.



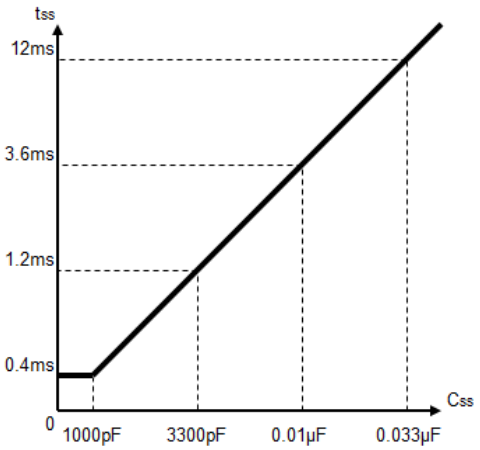
R1270S001A/B FLAG Circuit



R1270S001A/B FLG Start-up / Shut-down Sequence

Soft-Start Time Function

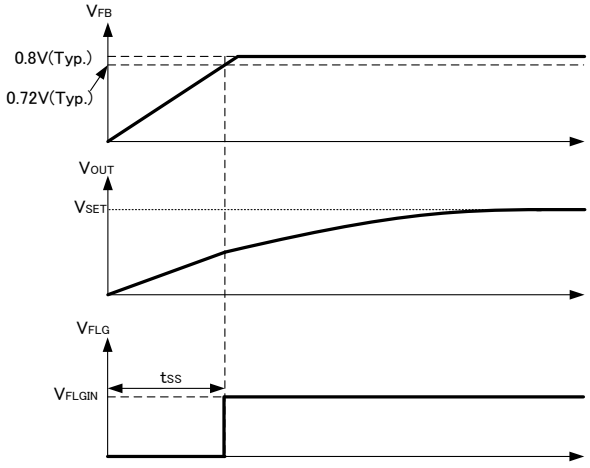
The soft-start time is between from ”H” level of CE to 90% of FB (0.72V). The soft-start time for the R1270S could be adjusted by using an external capacitor C_{SS} at the SS pin from minimum of internal soft-start time typical 0.4ms. The charging current of the external C_{SS} is 2.0μA (typ.) and the soft-start time becomes 3.6ms typically (reaching the set output voltage is 4.0ms (typ.)) when C_{SS} is 0.01μF. If not required to adjust the soft-start time, set the SS pin OPEN. On the condition described in the chapter of “Electrical Characteristics”, the R1270S guarantees each of soft-start time (tss1/tss2) when the SS pin is set to “Open” or when C_{SS} is set to 0.01μF.



C_{SS} [μF] = 2 × tss / 0.72

R1270S001A/B Capacitor for Soft-Start Time Adjustment (C_{SS}) vs. Soft-Start Time (tss)

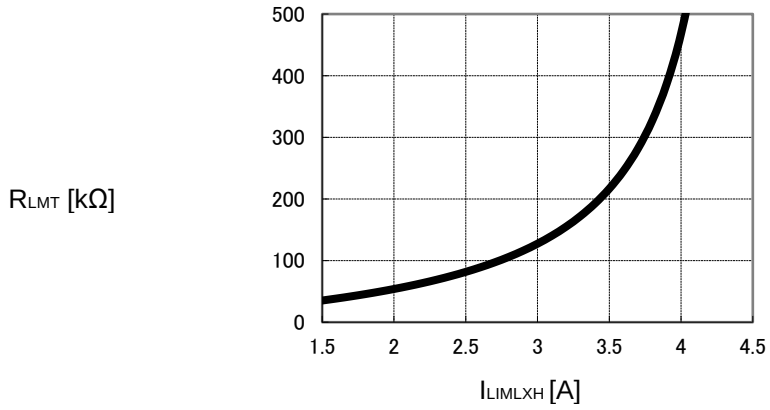
Also, when C_{SPD} is set large, the rising speed of VOUT may become slower than the soft-start time because of the bypass characteristic of the feedback resistor. Because the R1270S watches the output voltage using the FB pin voltage, the flag detection may be released before the VOUT is fully at set value.



R1270S001A/B Start-up / Shutdown Sequence

L_X Current Limit

By using external resistor R_{LMT} to the LMT pin, Lx current limit (I_{LIMLXH}), which is high-side switch current limit, can be adjusted as typical 4.5A at maximum. When R_{LMT} is 54kΩ, the Lx current limit is set at 2.0A typical. If not required to adjust Lx current limit, set LMT pin OPEN so that the Lx current limit will be set at typically 4.5A. Setting at 1.5A or less is not recommended. On the condition described in the chapter of "Electrical Characteristics", the R1270S guarantees each of LX limited current ($I_{LIMLXH1}$/$I_{LIMLXH2}$) when connected each of 39 kΩ/220kΩ resistors to the LMT pin.

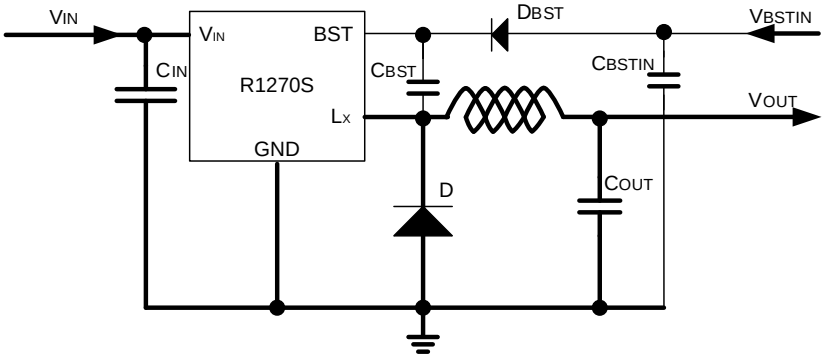


R_{LMT} [kΩ] = (1200 × (I_{LIMLXH} × 0.1033 + 0.13) − 120) / (12 − 20 × (I_{LIMLXH} × 0.1033 + 0.13))

R1270S001A/B L_X Current Limit Adjustment Resistor (R_{LMT}) vs. L_X Limit Current (I_{LIMLXH})

BST Auxiliary Charge Circuit

Under the oscillation frequency or conditions of input/output voltage level and load current, the BST capacitor charge may not be sufficient, and hence BST-Lx pin voltage level (typ.5.0V) may not be reached. However, if the output voltage or another power line at 4.5V to 6.0V is supplied to the R1270S, a drop of BST pin voltage level can be prevented by connecting BST auxiliary charge circuit with BST pin via a diode. In this case, the voltage of Lx pin must be less than the voltage of the auxiliary charge circuit to charge C_{BST}. Also, make sure not to exceed the maximum rating of 6.0V for BST-Lx. When selecting the diode, 10mA current rating is more than enough, but also be aware of the voltage rating, and the characteristic of reverse bias leak current at high temperature.



R1270S001A/B BST Charging Circuit

Sequence Composition

By using the soft-start time and the FLAG function (R1270S001A/B), a power up sequence can be composed. The following describes an example application circuit to start up both DC/DC1 and DC/DC2 in a sequence so that the 5.0V output will not to become lower than the DC/DC2 output 3.3V under the following conditions: the input voltage is 12V, two lines of output voltages are 5.0V (DC/DC1) and 3.3V (DC/DC2), the capacitor of the 5.0V output is an electrolytic 470µF, and the capacitor of the 3.3V output is electrolytic 100µF.

■ Soft-start time and charging current

During the soft-start, the R1270S occurs the charging current I_{CHRG} for the capacitor of V_{OUT} besides the output current I_{OUT}. Therefore, the output current I_{OUTSS} will be given by the following equation,

$$I_{OUTSS} = I_{OUT} + I_{CHRG}$$
$$= I_{OUT} + V_{OUT} \times (C_{OUT} + C_L)/t_{SS}$$

For the output current on the example application circuit,

(DCDC1) $I_{OUTSS} = I_{OUT} + V_{OUT}/(C_{OUT} + C_L)/t_{SS} = I_{OUT} + 5.0V \times (10\mu F + 470\mu F)/26ms = I_{OUT} + 92mA$

(DCDC2) $I_{OUT2SS} = I_{OUT2} + V_{OUT2}/(C_{OUT2} + CL2) / t_{SS} = I_{OUT} + 3.3V \times (10\mu F + 100\mu F)/2.6ms = I_{OUT2} + 140mA$

Make sure that the output current does not exceed 3.0A even at soft-start.

■ Using the output of R1270S as the flag pull-up voltage

The R1270S has an Nch open drain FLAG output. When detecting an abnormal condition, the R1270S switches the Nch transistor On and sets the FLG pin to “Low”. If the detected condition is not applicable under the FLAG output function, FLAG output will reset to “High” after the completion of the soft-start. When using the V_{OUT} as the V_{FLGIN}, “High” level of the V_{FLG} becomes the same with V_{OUT}.

■ Using the FLAG output as CE pin input for another R1270S

The minimum V_{CEL} is 0.85V and the maximum V_{CEH} is 1.15V.

The maximum V_{FLGL} is 0.4V, and V_{FLGH} for DC/DC1 on the example circuit is 5.0V. So, V_{FLG} is usable as CE input for DC/DC2.

■ Using the FLAG output as auto-discharge function

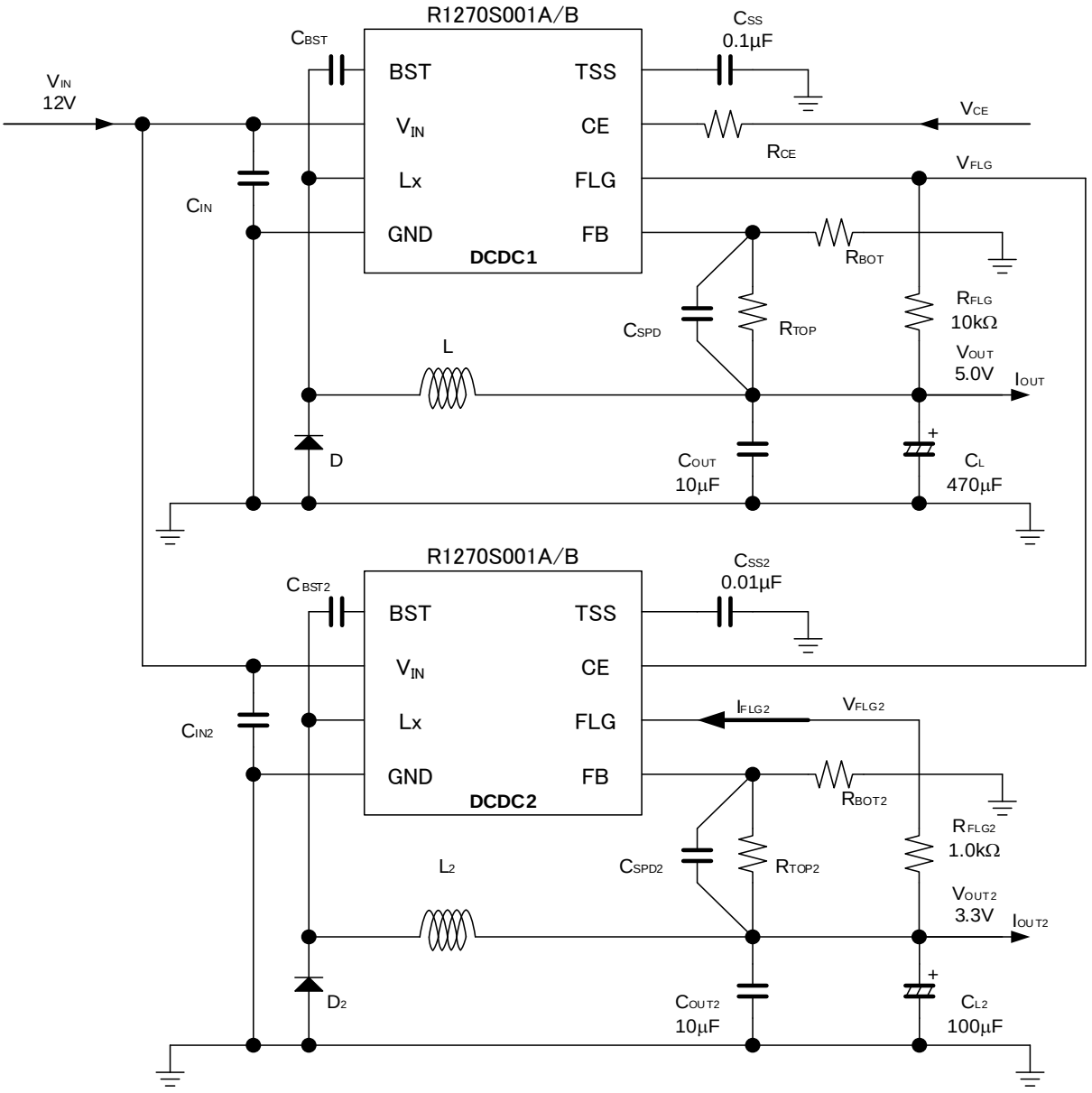
When being shut down, the R1270S switches the Nch transistor On and sets the FLG pin to “Low”. And, V_{FLGIN} sends the FLAG current I_{FLG} via R_{FLG} and Nch transistor. Thereby, the capacitor connected to V_{OUT} can be discharged by using V_{OUT} as V_{FLGIN}.

The maximum I_{FLG} is that of V_{FLGIN} divided by R_{FLG}. Set R_{FLG} so that maximum I_{FLG} becomes lower than 5mA. Do not connect V_{OUT} directly to FLG pin because the I_{FLG} may become excessive and may damage the IC.

The V_{FLGL} is regulated as I_{FLG}=1mA. When the R_{FLG} is set higher than I_{FLG}=1mA, the maximum voltage 0.4V of V_{FLGL} is not guaranteed, hence the FLAG function itself may be spoiled.

(DCDC1) R1270S001A/B: V_{IN} = 12 V, V_{OUT} = 5.0 V, tss = 40 ms (C_{SS} = 0.1 µF)

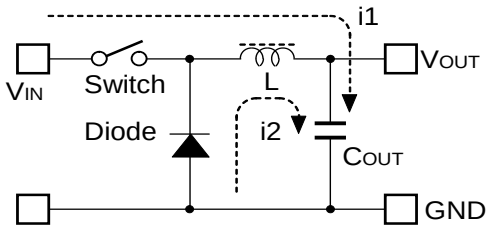
(DCDC2) R1270S001A/B: V_{IN} = 12 V, V_{OUT} = 3.3 V, tss = 4.0 ms (C_{SS} = 0.01 µF)



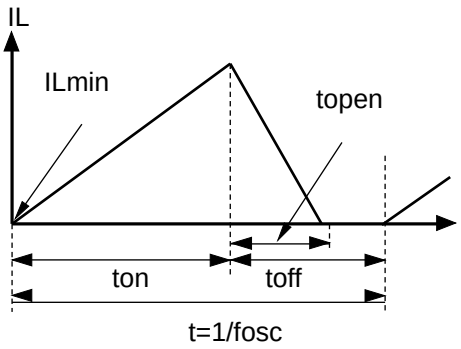
Example Circuit of Sequence Composition

Operation of Buck Converter and Output Current

The DC/DC converter charges energy in the inductor when the switch turns on, and discharges the energy from the inductor when the switch turns off and controls with less energy loss, so that a lower output voltage than the input voltage is obtained. Refer to the following figures.



Basic Circuit



Current Through Inductor

Step 1: The switch turns on and current IL (=i1) flows, and energy is charged into C_{OUT}. At this moment, IL increases from ILmin (=0) to reach ILmax in proportion to the on-time period (ton) of the switch.

Step 2: When the switch turns off, the diode turns on in order to maintain IL at I_{Lmax}, and current IL (=i2) flows.

Step 3: IL (=i2) decreases gradually and reaches IL = ILmin = 0 after a time period of topen, and the diode turns off. This case is called as discontinuous mode. If the output current becomes large, next switching cycle starts before I_L becomes 0 and the diode turns off. In this case, IL value increases from ILmin (>0), and this case is called continuous mode.

As for the PWM control system, the output voltage is maintained by controlling the on-time period (ton), with the oscillator frequency (fosc) being maintained constant.

Output Current and Selection of External Components

The relation between the output current and external components is as follows:

When the switch of L_X turns on:

(Wherein, the peak to peak value of the ripple current is described as I_{RP}, the ON resistance of the switch is described as R_{ONH}, and the diode forward voltage as V_F, and the DC resistance of the inductor is described as R_L, and on time of the switch is described as ton)

$$V_{IN} = V_{OUT} + (R_{ONH} + R_L) \times I_{OUT} + L \times I_{RP} / ton \quad \cdots\cdots \text{Equation 1}$$

When the switch turns off (the diode turns on) as t_{off}:

$$L \times I_{RP} / toff = V_F + V_{OUT} + R_L \times I_{OUT} \quad \cdots\cdots \text{Equation 2}$$

Put Equation 2 to Equation 1 and solve for ON duty of the switch, ton / (ton + toff) = D_{ON},

$$D_{ON} = (V_{OUT} + V_F + R_L \times I_{OUT}) / (V_{IN} + V_F - R_{ONH} \times I_{OUT}) \quad \cdots\cdots \text{Equation 3}$$

Ripple Current is as follows:

$$I_{RP} = (V_{IN} - V_{OUT} - R_{ONH} \times I_{OUT} - R_L \times I_{OUT}) \times D_{ON} / fosc / L \quad \cdots\cdots \text{Equation 4}$$

Then, peak current that flows through L, and the peak current ILmax is as follows:

$$ILmax = I_{OUT} + I_{RP} / 2 \quad \cdots\cdots \text{Equation 5}$$

As for the valley current ILmin,

$$ILmin = I_{OUT} - I_{RP} / 2 \quad \cdots\cdots \text{Equation 6}$$

If ILmin<0, the step-down DC/DC converter operation becomes current discontinuous mode.
Therefore the current condition of the current discontinuous mode, the next formula is true.

$$I_{OUT} < I_{RP} / 2 \quad \cdots\cdots \text{Equation 7}$$

Consider ILmax and ILmin, conditions of input and output and select external components.

*The above explanation is based on the calculation in an ideal case in continuous mode.

Ripple Current and Lx Limited Current

The ripple current of the inductor may change according to the various reasons. In the R1270S series, as an Lx current limit, Lx peak current limit is used. Therefore the upper limit of the inductor current is fixed.

The peak current limit is not the average current of the inductor (output current). If the ripple current is large, peak current becomes also large. The characteristic is used for the fold back current limit of version B/D. In other words, the peak current limit is maintained and the switching frequency is reduced, as a result, the average current of the inductor is reduced. To release this condition, the peak current must not exceed the peak current limit.

Latch Protection Function (R1270S001A)

The latch function is enabled after the completion of the soft-start. The latch function works after detecting current limit and starts the internal counter. After the internal counter reaches 2ms (Typ.), the latch function turns the output off. The R1270S has two ways to reset the latch function: one is to set the CE pin “L”, and another one is to set the VIN voltage to become equal to the detection voltage of the UVLO function, or become less. Also, the latch function is reset when the FB pin voltage is 2.0V (Typ.) or more.

The start condition for the internal counter is to detect the limited current at each clock, and the reset condition is when a frame without detecting the limit current occurs.

When a ringing between the output voltage and the short-circuit impedance including large inductance occurs and the FB pin voltage exceeds 0.80V (Typ.), take note that the latch timer might be reset.

Fold-back Protection Function

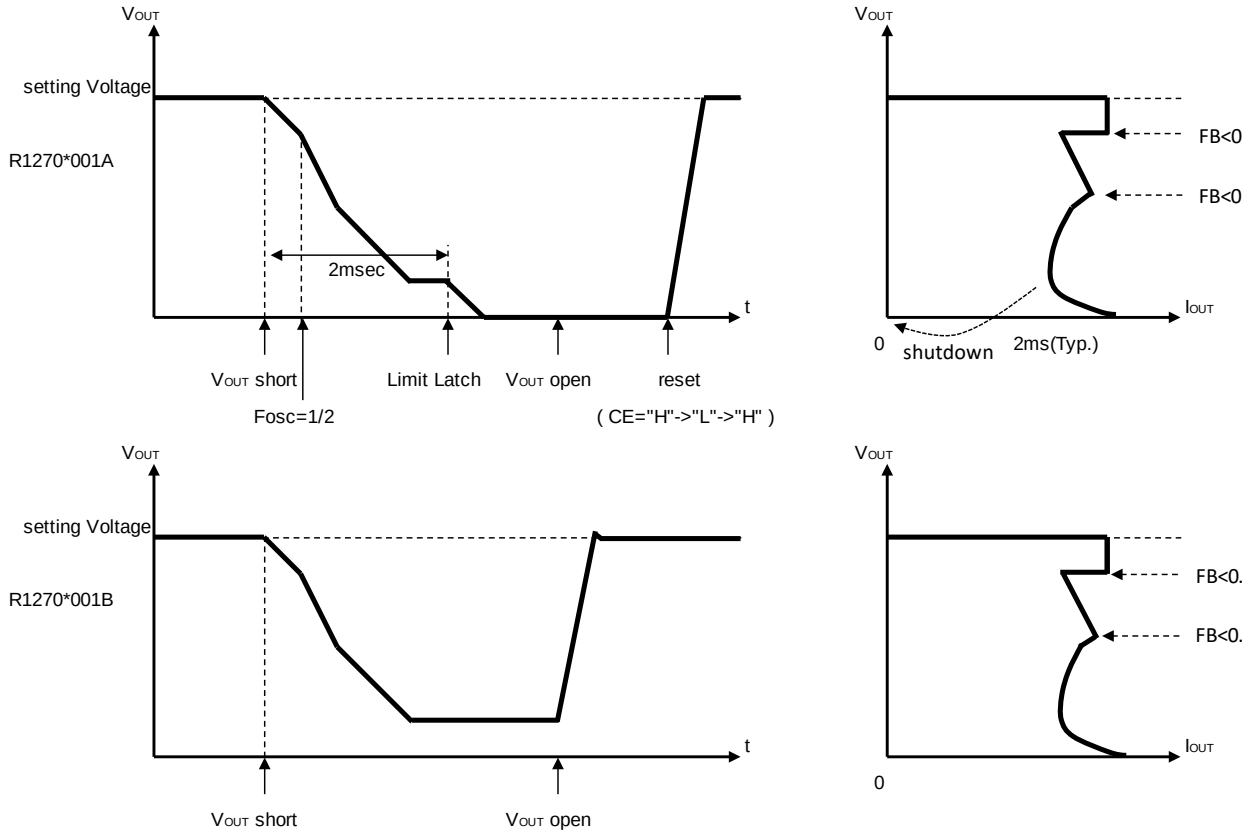
After the soft-start period, fold back protection is enabled. When there is abnormality to the output and the FB voltage becomes lower than 0.64V typical, the oscillation frequency will be limited at 1/2. Furthermore, when the output voltage drops below 50% typical from the set voltage (FB pin voltage 0.4V), oscillation frequency will be limited proportional to the FB pin voltage level.

By reducing frequency, the ripple current increases. The R1270S has the peak current limit function, therefore as in the equation 8, the Lx average current decreases by the increase of the ripple current.

$$I_{OUT} = ILmax + I_{RP} / 2 \quad \cdots\cdots \text{Equation 8}$$

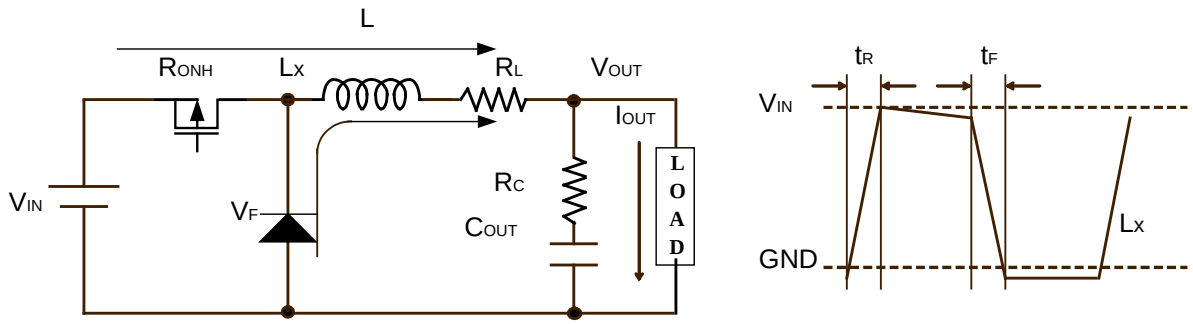
If the FB pin voltage becomes less than 0.64V, the oscillator frequency is reduced to 1/2. At heavy load, if the R1270S becomes into the fold-back protection mode, the situation may not be released by the increased ripple current.

This fold-back protection function is to provide a high degree of safety to the R1270S, not to secure reliability. When using the IC without the latch protection function (R1270S001B), a measure to prevent shorting is required.



L_X Limited Current Function Sequence

Loss and Efficiency



Illustrated Description for Loss

$P_{ON} = R_{ONH} \times I_{OUT}^2 \times Onduty$: loss at switching ON

$P_F = (t_R + t_F) / 2 \times V_{IN} \times I_{OUT} \times fosc$: switching loss

$P_{OFF} = V_F \times I_{OUT} \times Offduty$: loss of diode

$P_L = R_L \times I_{OUT}^2$: loss of inductor

$P_D = V_{IN} \times I_{SS}$: consumption current if IC

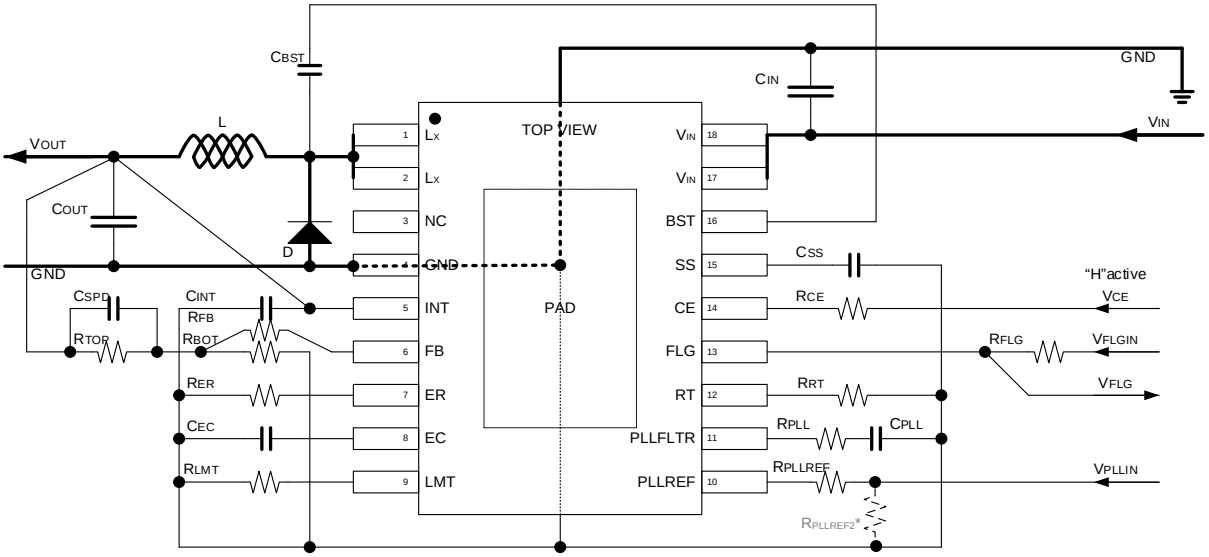
$P_{PP} = 1 / 4 \times R_C \times I_{RP}^2$: loss by ripple of the inductor current

Efficiency $\eta = (V_{OUT} \times I_{OUT}) / ((V_{OUT} \times I_{OUT}) + P_{ON} + P_F + P_{CL} + P_D + P_{PP}) \times 100\%$

The loss that generated by R1270S is P_{ON}, P_F, P_D. These losses are converted to heat inside the IC. Therefore, the R1270S must be used within the condition below is required.

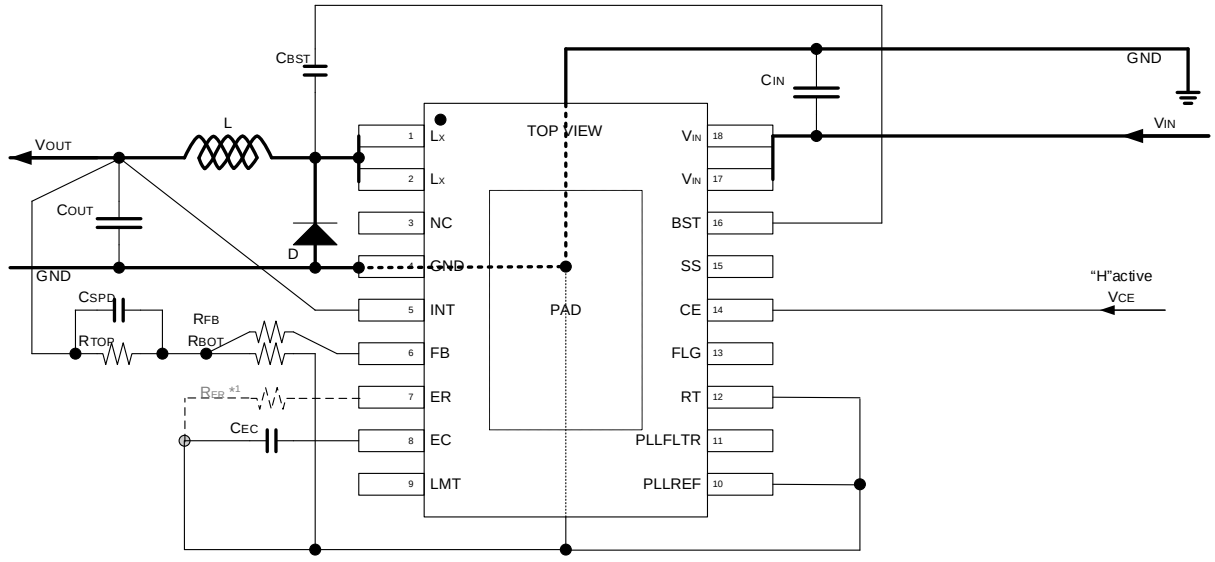
$Tj = \theta ja \times (P_{ON} + P_F + P_D) + Ta < 150^oC$

APPLICATION INFORMATION



***** PLLREF pin must not be "OPEN". When using our evaluation board, a pull-down resistor ($R_{PLLREF2}$: 100kΩ) is contained on the evaluation board.

R1270S001A/B Typical Application Circuit



***** When not connecting a phase compensation resistor of R_{ER} (the ER pin is "OPEN"), characteristics of load transient response becomes deteriorated, as compared with when connecting the R_{ER} resister. Please make through evaluation before determining whether connecting the R_{ER} resister or not.

R1270S001A/B Minimum Composition Circuit

R1270S001A/B, C_{IN}, C_{OUT} Recommended Components

V_{IN} , V_{OUT}	Capacitor	Spec.	Component Name	Maker
≤ 16 V	0.47 µF	25 V/125°C	CGA4J2X7R1E474K	TDK
≤ 16V	2.2 µF	25 V/125°C	CGA4J3X7R1E225K	
All	2.2 µF	50 V/125°C	CGA5L3X7R1H225K	
≤ 16V	4.7 µF	25 V/125°C	CGA5L1X7R1E475K	
All	4.7 µF	50 V/125°C	CGA6P3X7R1H475K	
All	10 µF	50 V/125°C	CGA6P3X7S1H106K	
≤ 16 V	10 µF	25 V/125°C	CGA6P1X7R1E106K	
≤ 10 V	22 µF	16 V/125°C	CGA6P1X7R1C226M	
≤ 16 V	22 µF	25 V/125°C	CGA8P1X7R1E226M	

R1270S001A/B, C_{BST} Recommended Components

V_{OUT}	Capacitor	Spec.	Component Name	Maker
All	0.47 µF	16 V	EMK212BJ474KD-T	Taiyo Yuden
All	0.47 µF	25 V	CGA4J2X7R1E474K	TDK

R1270S001A/B, D Recommended Components

V_{IN}	Spec.	Component Name	Maker
All	40 V/3 A	RB056L-40TE	ROHM
All	40 V/3 A	RB058L-40TE	
All	60 V/3 A	RB058L-60TE	
All	40 V/3 A	CMS30I40A	TOSHIBA

R1270S001A/B, L Recommended Components

Inductor	Spec.	Component Name	Maker
1.0 µH	6.4 A	RLF7030T-1R0N6R4	TDK
	6.5 A	CLF7045NIT-1R0N-D	
1.5 µH	7.3 A	CLF7045T-1R5-D	
	5.4 A	CLF7045NIT-1R5N-D	
2.2 µH	5.5 A	CLF7045T-2R2-D	
	5.1 A	CLF7045NIT-2R2N-D	
4.7 µH	5.4 A	CLF10040T-4R7-D	
	4.1 A	CLF10060NIT-4R7N-D	
10 µH	4.0 A	CLF10040T-100M-D	
	3.0 A	CLF10060NIT-100M-D	
10 µH	6.7 A	CLF12555T-100M-D	
	6.4 A	CLF12577NIT-100M-D	
15 µH	5.4 A	CLF12555T-150M-D	
	5.1 A	CLF12577NIT-150M-D	
22 µH	4.2 A	CLF12555T-220M-D	
	4.3 A	CLF12577NIT-220M-D	

Selection of External Components

- Using ceramic capacitors with low ESR (Equivalent Series Resistance) are recommended. The recommended capacitor for C_{IN} between VIN and GND is 4.7 µF or more. Verify the bias dependence and the temperature characteristics of the ceramic capacitors. Recommended conditions are written based on the case which the recommended parts are used with the R1270S.

- The R1270S is designed with the recommended inductance value and the C_{OUT} ceramic capacitor value to make phase compensation. If the inductance value is large, a lack of the current sensing amount in the current mode might result in an unstable operation. Oppositely, if the inductance value is small, an excess of the current sensing amount might result in the occurrence of the low frequency oscillation on when the on duty ratio is beyond 50%. Ensure that capacitors using for C_{OUT} can meet the voltage-dependent properties in order to have bias dependence. Recommended conditions are written based on the case which the recommended parts are used with the R1270S.

- If the inductance value is small, a ripple to inductor current will be increased and the peak current of the switching will be increased as the load current increases. As a result, the current might reach the current limit value and the current limit might work.

- As for the diode, connect a schottky diode with small capacitance between terminals. The reference characteristic of the capacitance between terminals is around 100 pF or less at 10 V. If using a schottky diode with large capacitance, the operation of the R1270S might be unstable by a flow of an excess switching current. When the capacitance of the schottky diode used is beyond 100 pF at 10 V or is unknown, make sure that the R1270S does not have issues of the load regulation, the line regulation, and the load transient response. And, connect a diode having the smallest possible reverse current IR. Especially, IR's rising under high temperature conditions might cause a thermal runaway and will lead to cause damage to the IC.

- Output voltage (V_{OUT}) can be set by adjustable values of R_{TOP} and R_{BOT} being expressed by the following equation, $V_{OUT} = V_{FB} \times (R_{TOP} + R_{BOT}) / R_{BOT}$.
  For example, when setting V_{OUT} = 12 V, and setting R_{BOT} = 16 kΩ, R_{TOP} = (12 V / 0.8 V-1) × (16 kΩ) = 224 kΩ. By using the E24 type resistors to make 224 kΩ, you need (200 kΩ + 24 kΩ) and use them in series. If the tolerance level of the output voltage is relatively wide you may set the output voltage as 11.80 V = 0.8 V × (220 kΩ + 16 kΩ) / 16 kΩ. In this case R_{TOP} will be a single resistor of 220 kΩ.
  When the values of R_{TOP} and R_{BOT} become larger, the R1270S is susceptible to noise with increasing the impedance of FB pin. The recommended value range of R_{BOT} is approximately between 1.0 kΩ to 160 kΩ. If the operation is unstable, reduce the impedance of FB pin.

- As for the CE pin and the PLLREF pin, an up diode for VIN, which have efficacy as ESD protection element, is internally connected to each pin. If CE pin voltage or PLLREF pin voltage may become higher than VIN pin voltage, connect a resistor between CE or PLLREF and VIN pin to prevent flowing large current from CE pin or PLLREF pin to VIN pin. When using external oscillation synchronization, the input signal must be used to become lower than the VIN voltage without using a resistor because the input voltage of PLLREF is filtered out via the resistor.

- When using a phase compensation resistor pin (ER pin), the recommended value range of RER is 220 kΩ or more. If not using phase the compensation resistor pin, the ER pin must be set to "OPEN".

- The R_{FB} is the resistance to prevent feedback of the noise to the FB pin. The appropriate value is about 1 kΩ.

- The BST voltage might fall depending on how to use the R1270S. By drops of the BST voltage, R1270S might not function properly. As result, the current limit detection may be caused by an inductor current lower than the set current limit value by reducing the effect.

- The R1270S has the driver buffer and the BST voltage detector between BST and Lx pins. When the R1270S is in PWM fixed mode and the light load current is caused by requiring the consumption current always, V_{OUT} might move up by the consumption current. In this case, the load current including the feedback resistor must be set to 0.5 mA or more. In VFM/PWM alternative mode, the R1270S has no problem, as long as RBOT is set between 1.0 kΩ and 160 kΩ.

- Recommended ratings to principal set output voltages are as following:

R1270S001A/B, 300 kHz Recommended Constant

V_{OUT}	C_{IN} [µF]	L [µH]	C_{OUT} [µF]	C_{BST} [µF]	C_{SPD} [pF]	R_{TOP} [kΩ]	R_{BOT} [kΩ]	R_{RT} [kΩ]	R_{ER} [kΩ]	C_{EC} [pF]
$0.8 \le V_{OUT} \le 1.5$	10	10	47	0.47	Open	*1	160	Open	470	2200
$1.0 \le V_{OUT} \le 6$	10	10	47	0.47	100 [1000]*4	*1	160 [16]*4	Open	470	2200
$1 \le V_{OUT} \le V_{IN} \times D_{MAX}$*2	10	15	47	0.47	100 [1000]*4	*1	160 [16]*4	Open	470	2200

R1270S001A/B, 1000 kHz Recommended Constant

V_{OUT}	C_{IN} [µF]	L [µH]	C_{OUT} [µF]	C_{BST} [µF]	C_{SPD} [pF]	R_{TOP} [kΩ]	R_{BOT} [kΩ]	R_{RT} [kΩ]	R_{ER} [kΩ]	C_{EC} [pF]
$0.8 \le V_{OUT} \le 1.5$	4.7	2.2	47	0.47	Open	*1	16	62	470	220
$1 \le V_{OUT} \le 6$	4.7	2.2	47	0.47	2200	*1	16	62	470	220
$1 \le V_{OUT} \le 15$	4.7	4.7	47	0.47	2200	*1	16	62	470	220
$5 \le V_{OUT} \le V_{IN} \times D_{MAX}$	4.7	4.7	47	0.47	470	*1	16	62	680	220
$5 \le V_{OUT} \le V_{IN} \times D_{MAX}$ *2	4.7	10.0	47	0.47	1000	*1	16	62	680	470

*1 $R_{TOP} = (V_{OUT} / V_{FB}\text{-}1) \times (R_{BOT})$
*2 Condition recommended at V_{IN} > 18 V
*4 If R_{BOT} is 16 kΩ, the constant value of C_{SPD} requires ten times as much as when R_{BOT} is 160 kΩ.

R1270S001A/B, 2400 kHz Recommended Constant

V_{OUT}	C_{IN} [µF]*3	L [µH]	C_{OUT} [µF]	C_{BST} [µF]	C_{SPD} [pF]	R_{TOP} [kΩ]	R_{BOT} [kΩ]	R_{RT} [kΩ]	R_{ER} [kΩ]	C_{EC} [pF]
$0.8 \leq V_{OUT} \leq 1.5$	4.7	1.0	10	0.47	Open	*1	16	0.0	470	220
$1 \leq V_{OUT} \leq 6$	2.2	1.0	22	0.47	1000	*1	16	0.0	470	220
$1 \leq V_{OUT} \leq 9$	2.2	2.2	22	0.47	1000	*1	16	0.0	470	220
$5 \leq V_{OUT} \leq V_{IN} \times D_{MAX}$ *2	2.2	4.7	22	0.47	1000	*1	16	0.0	680	470

*1 $R_{TOP} = (V_{OUT} / V_{FB}\text{-}1) \times (R_{BOT})$
*2 Condition recommended at $V_{IN} > 18$ V
*3 4.7 µF or more recommended at $V_{OUT} < 5$ V

TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, please be fully aware of the following points. (Refer to *PCB Layout Considerations* below.)

- External components must be connected as close as possible to the ICs and make wiring as short as possible. Especially, the capacitor connected in between VIN pin and GND pin must be wiring the shortest. If their impedance is high, internal voltage of the IC may shift by the switching current, and the operating may be unstable. Make the power supply and GND lines sufficient.

- The backside thermal pad of the HSOP-18 package must be connected to GND. To improve the thermal dissipation on multi-layered boards, the thermal must be dissipated to another layer by putting some thermal vias on the thermal pad in the land pattern.

- NC pin must be set to “OPEN”.

- Switching regulator is required some caution. Because, a large current variation occurs by the following different current loops in every switching, and a high-frequency noise occurs by parasitic current.
  - The current loop when the switch is “ON”, Input Capacitor (C_{IN}) → Hi-side Switch → Inductor → Output Capacitor (C_{OUT}) → C_{IN}
  - The current loop when the switch is “OFF”, Rectifier Diode (D) → Inductor →C_{OUT} → D
  - The current loop via Diode Parasitic Capacitor when the switch is “ON”, C_{IN} → Hi-side Switch → Parasitic Capacitor of D →C_{IN}

  A large EMI noise source is caused in this loop. Therefore, extreme caution is required. These loops have to design as short as possible, and design not to cross lines in the subsequent load side to C_{OUT} in order to avoid the influence of switching noise.

- The line between the Lx pin and the inductor have to wire as close as possible in order to avoid the parasitic capacitor.

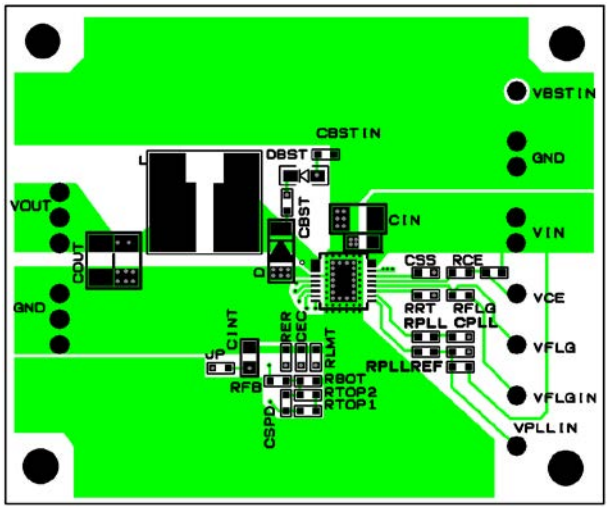
- It is recommended the input capacitor (C_{IN}) and the rectifier diode (D) be placed on the same side with the R1270x chip. If placing the other side through via-hole, noise may increase by a parasitic inductance of via. And, it may have the influence on ringing of the Lx pin voltage.

- The power lines (V_{IN}, GND) have to design as widely as possible in order to avoid the parasitic inductance. And, the C_{IN} have to place as close to between V_{IN} and GND as possible.

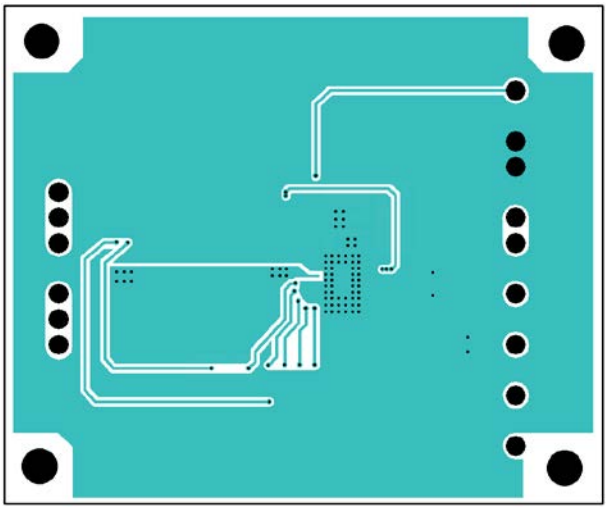
- On this evaluation board, the land for the Lx pin is wide to connect with large inductor and diode.
- V_{OUT} feedback has to be provided near C_{OUT}.
- R_{TOP}, R_{BOT}, and C_{SPD} pins have to design as close to the FB pin as possible and to keep a distance from the Lx and the BST pins in order to avoid the influence of noise.

R1270X001 Typical Board Layout

Top View



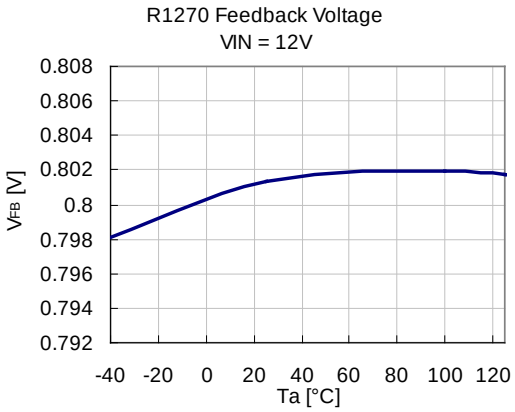
Bottom View



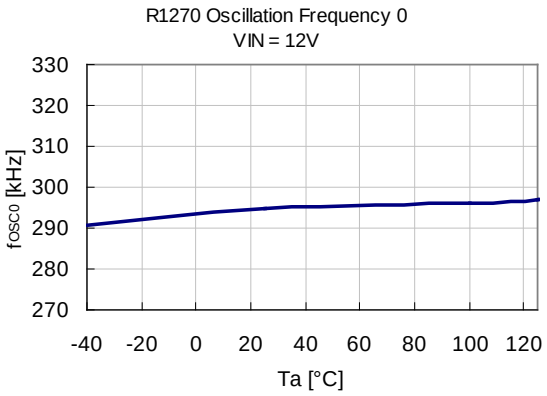
TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

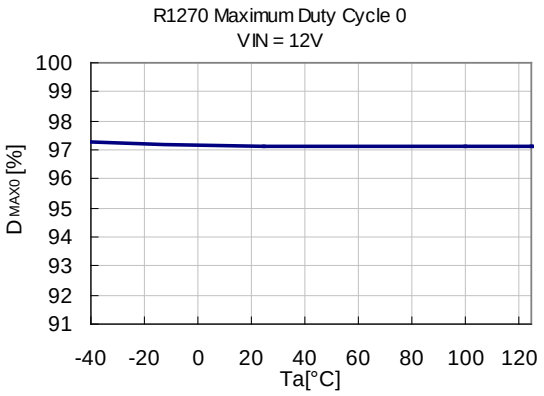
1) FB Voltage vs. Temperature



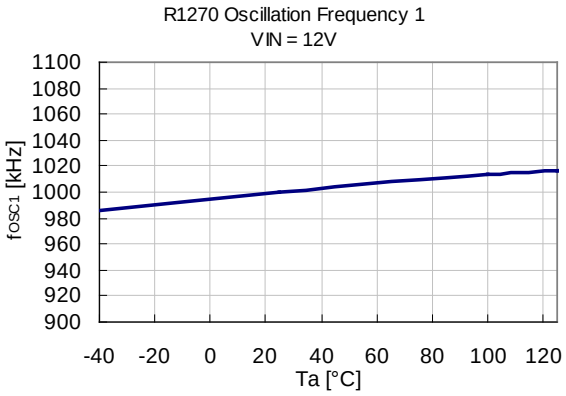
2) Oscillation Frequency 0 vs. Temperature



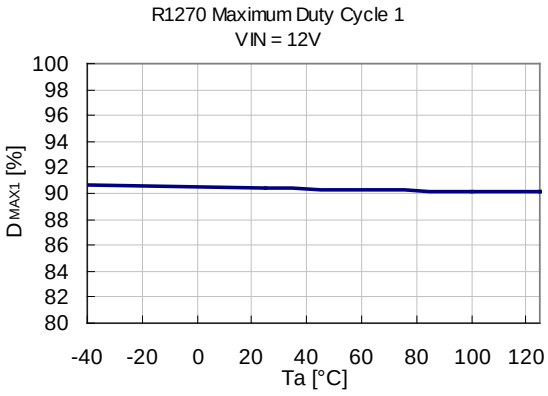
3) Maximum Duty cycle 0 vs. Temperature



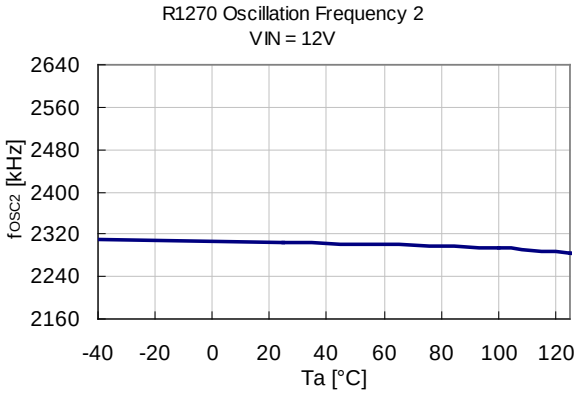
4) Oscillation Frequency 1 vs. Temperature



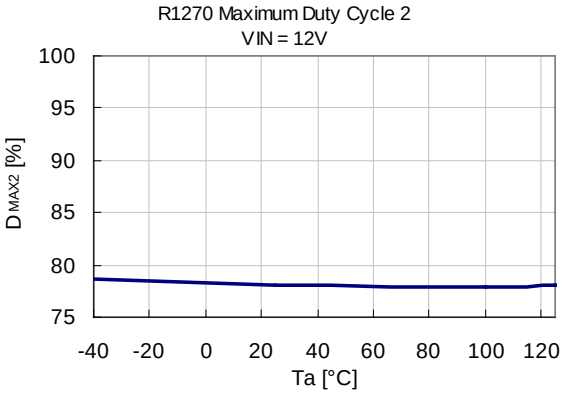
5) Maximum Duty cycle 1 vs. Temperature



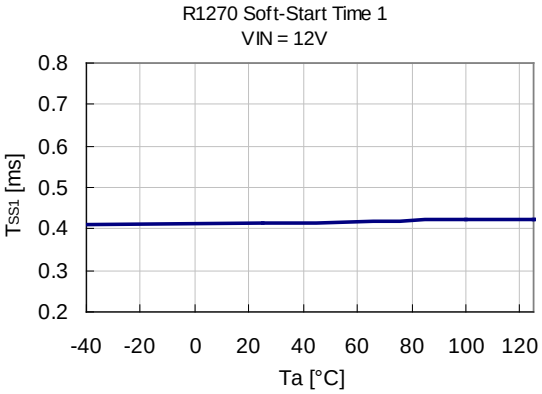
6) Oscillation Frequency 2 vs. Temperature



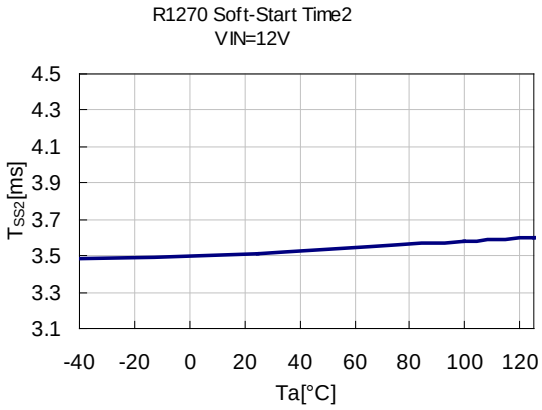
7) Maximum Duty cycle 2 vs. Temperature



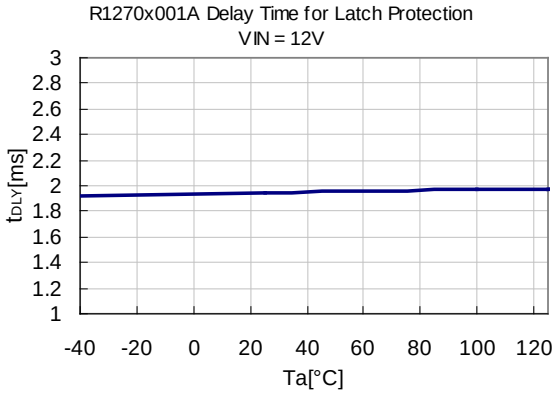
8) Soft-start time 1 vs. Temperature



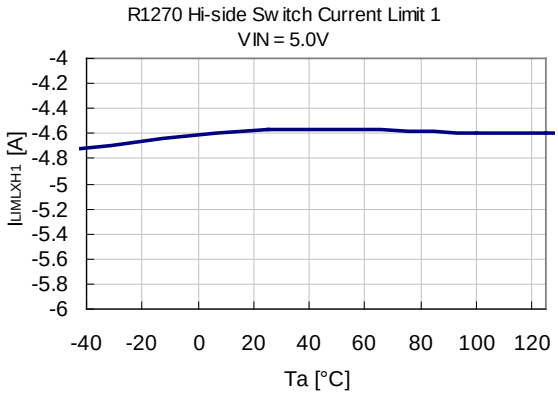
9) Soft-start time 2 vs. Temperature



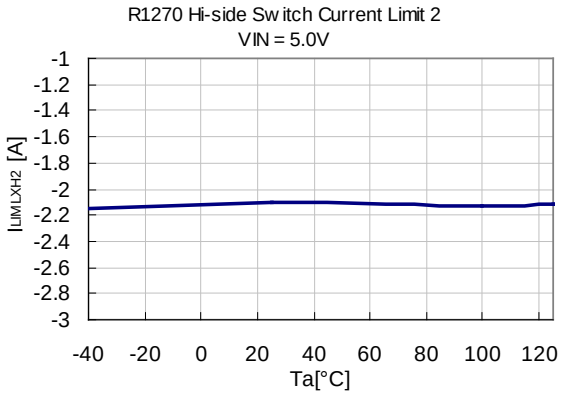
10) Delay time for latch protection vs. Temperature



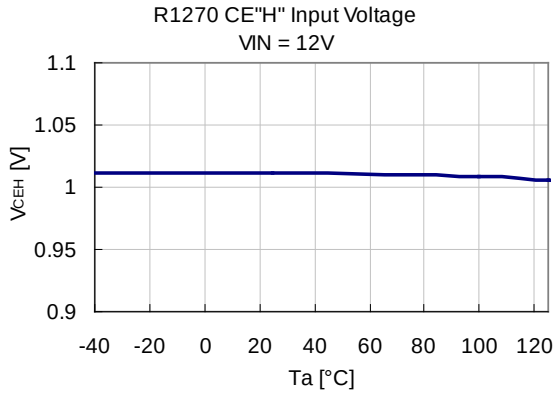
11) High side switch current limit1 vs. Temperature



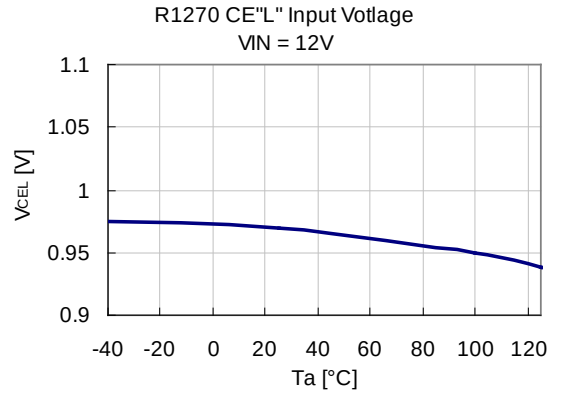
12) High side switch current limit2 vs. Temperature



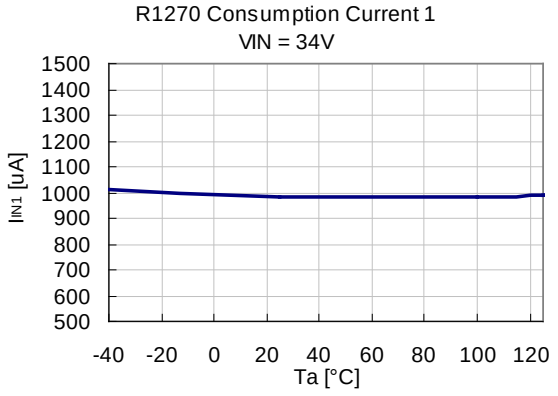
13) CE “H” Input voltage vs. Temperature



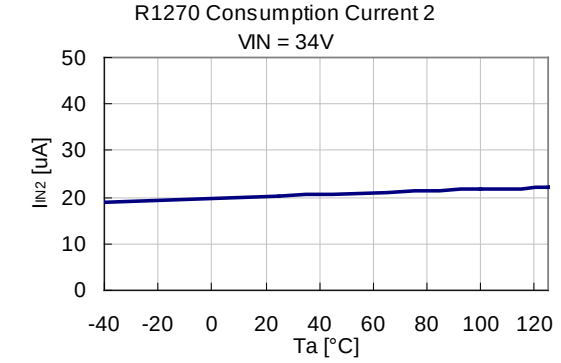
14) CE “L” Input voltage vs. Temperature



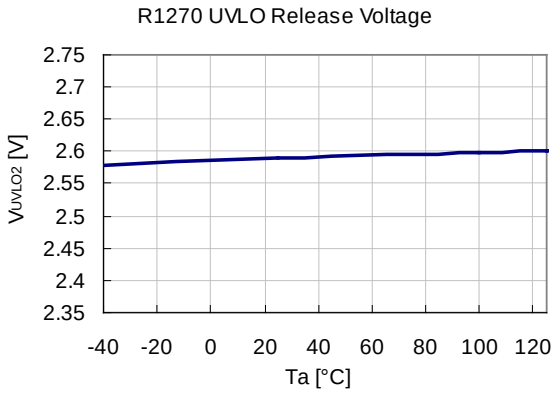
15) Consumption Current 1



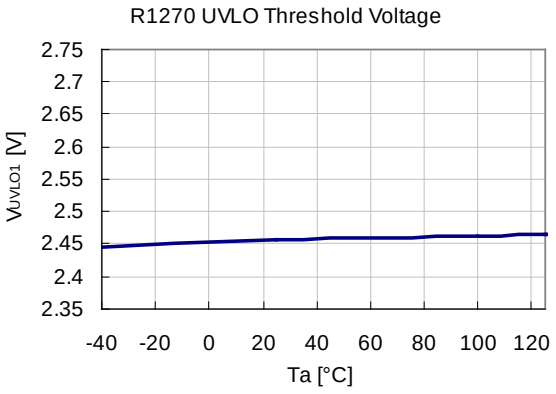
16) Consumption Current 2



17) UVLO Release voltage vs. Temperature

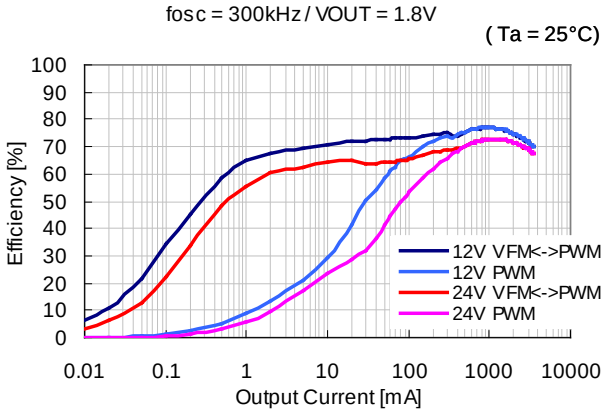


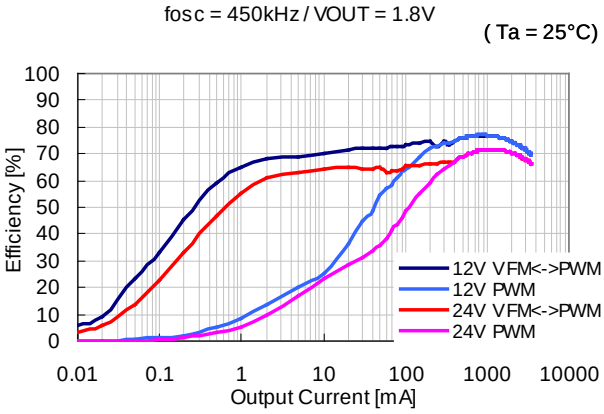
18) UVLO Threshold voltage vs. Temperature



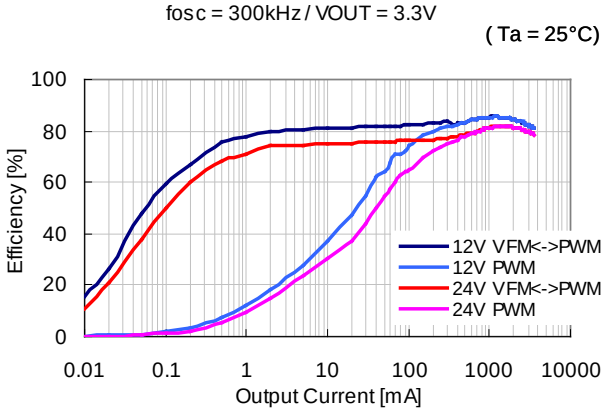
19) Output current vs. Efficiency

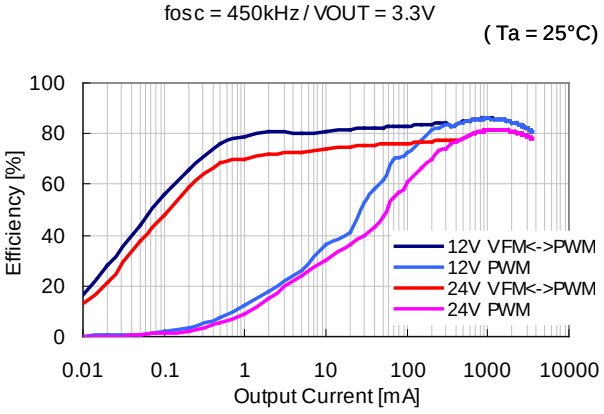
V_{OUT} = 1.8 V



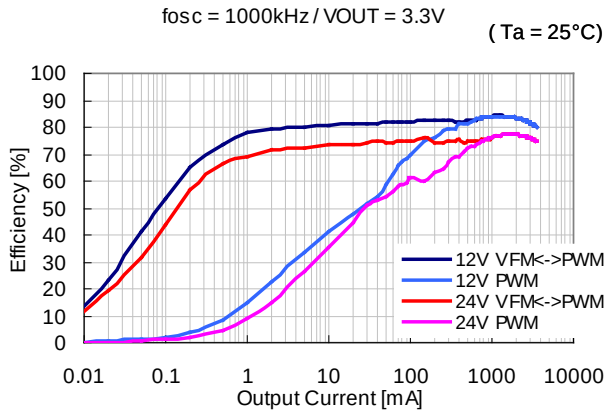


V_{OUT} = 3.3 V

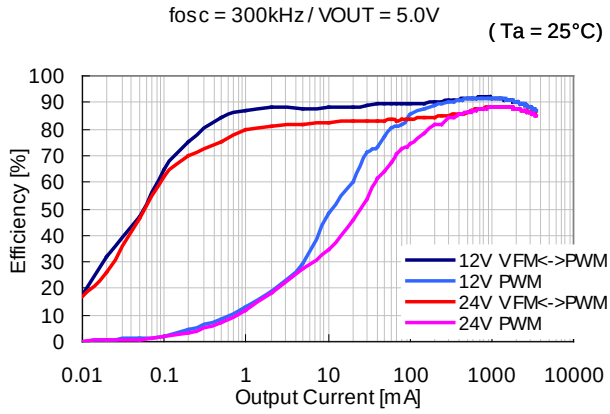


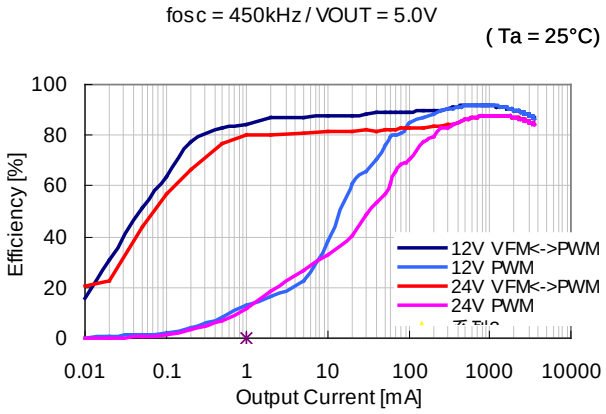


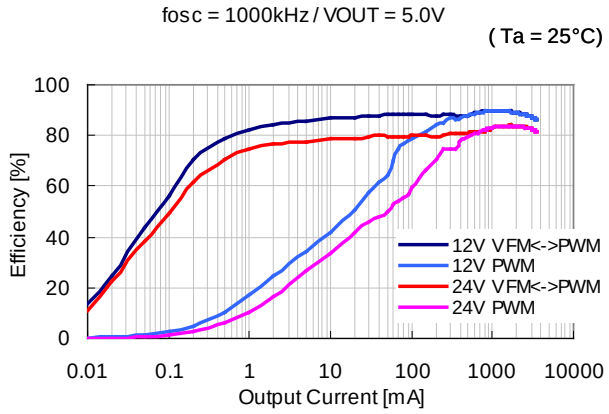
V_{OUT} = 3.3 V

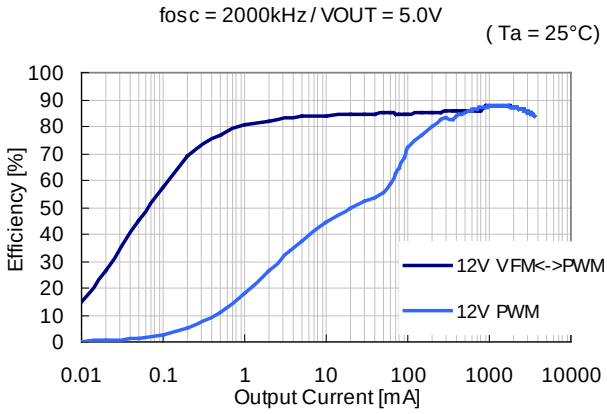


V_{OUT} = 5.0 V

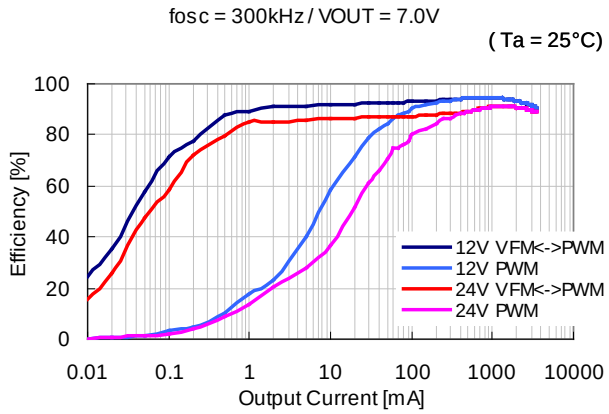


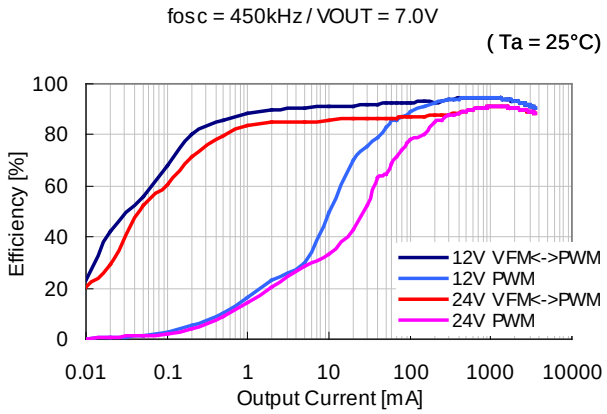


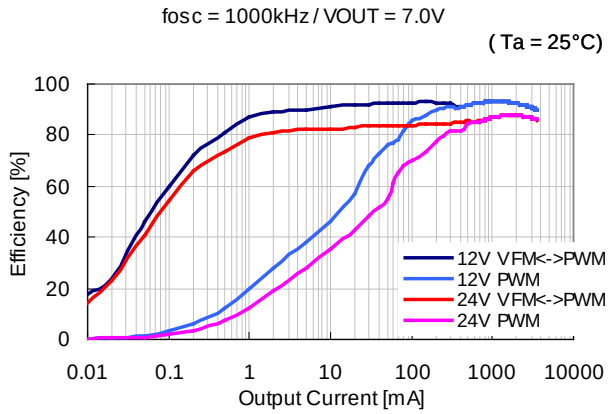


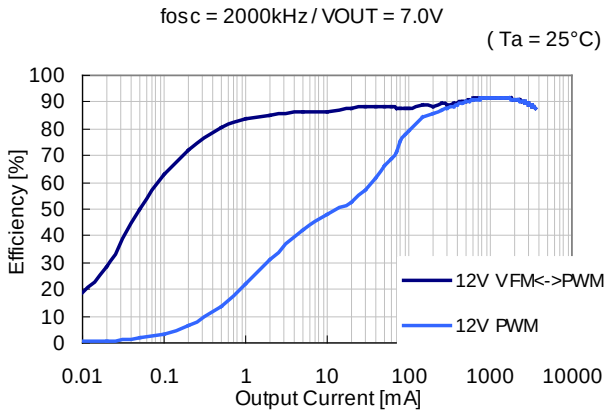


V_{OUT} = 7.0 V

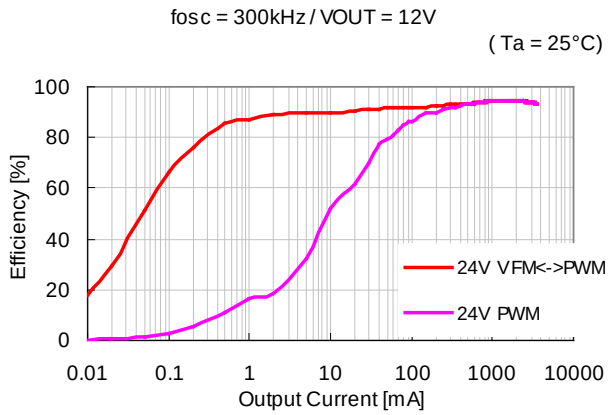


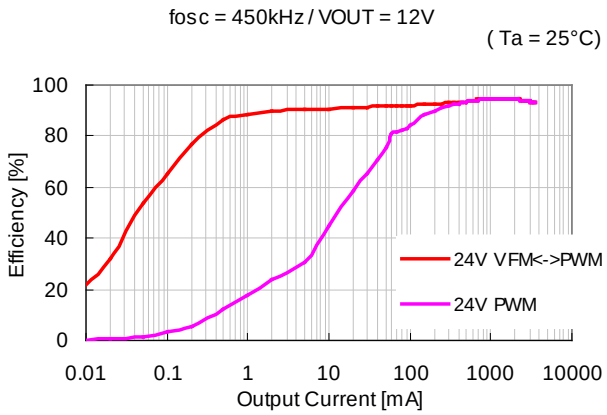




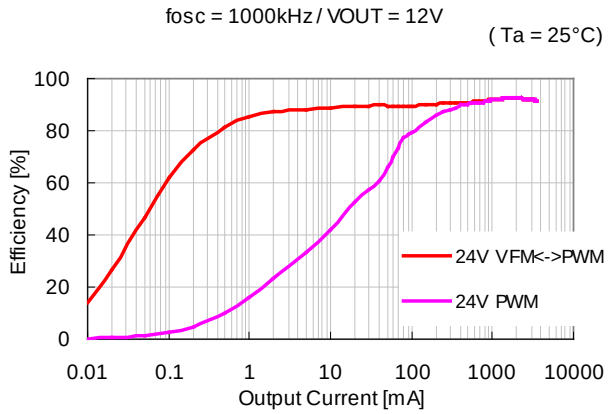


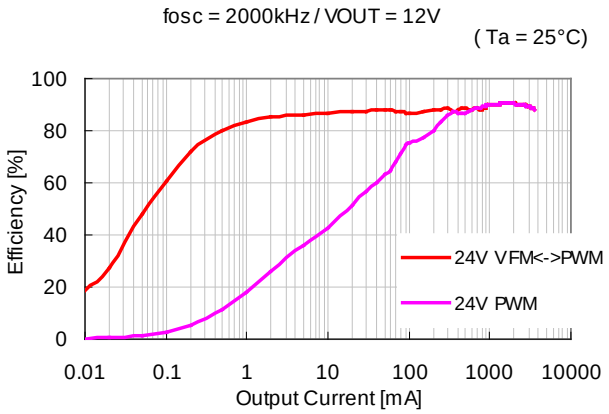
V_{OUT} = 12 V

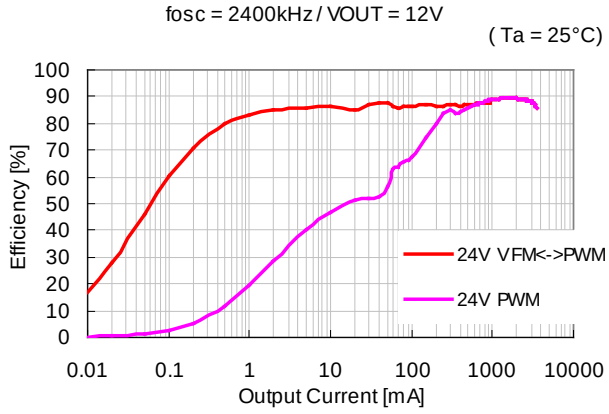




V_{OUT} = 12 V

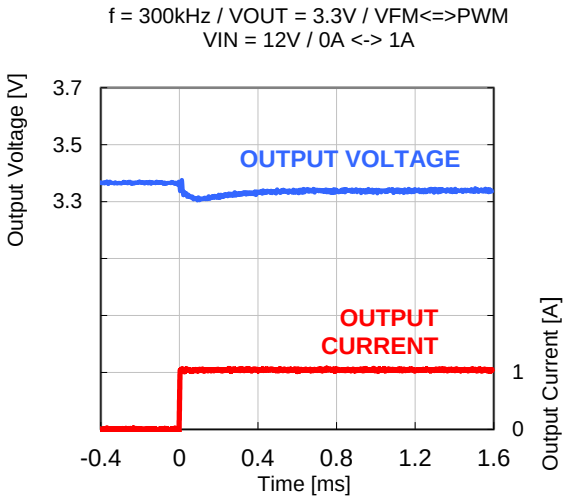

fosc = 1000kHz / VOUT = 12V
(Ta = 25°C)
Efficiency [%]
100
80
60
40
20
0
0.01
0.1
1
10
100
1000
10000
Output Current [mA]
24V VFM<->PWM
24V PWM

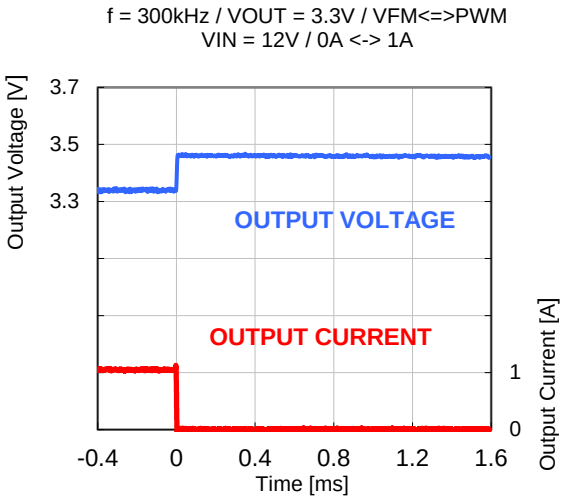

fosc = 2000kHz / VOUT = 12V
(Ta = 25°C)
Efficiency [%]
100
80
60
40
20
0
0.01
0.1
1
10
100
1000
10000
Output Current [mA]
24V VFM<->PWM
24V PWM

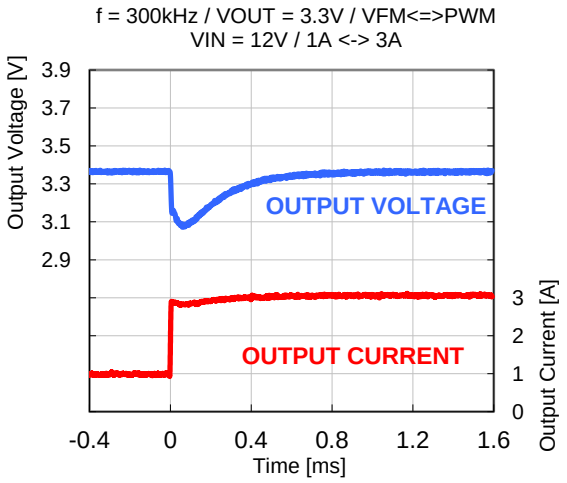

fosc = 2400kHz / VOUT = 12V
(Ta = 25°C)
Efficiency [%]
100
90
80
70
60
50
40
30
20
10
0
0.01
0.1
1
10
100
1000
10000
Output Current [mA]
24V VFM<->PWM
24V PWM

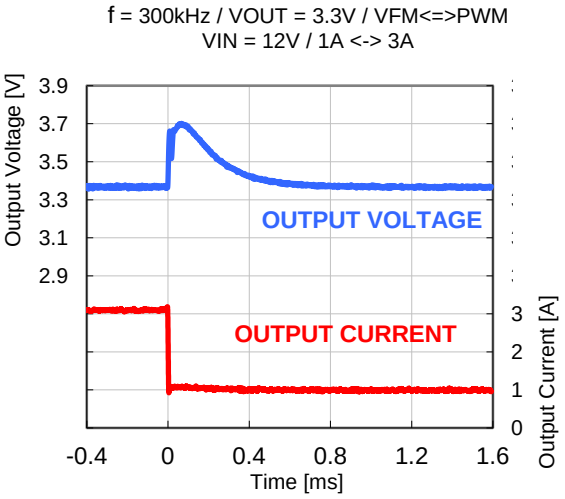
20) Load Transient Response

fosc = 300 kHz

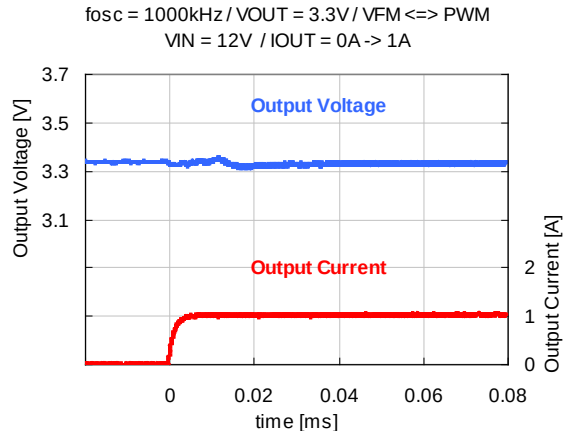


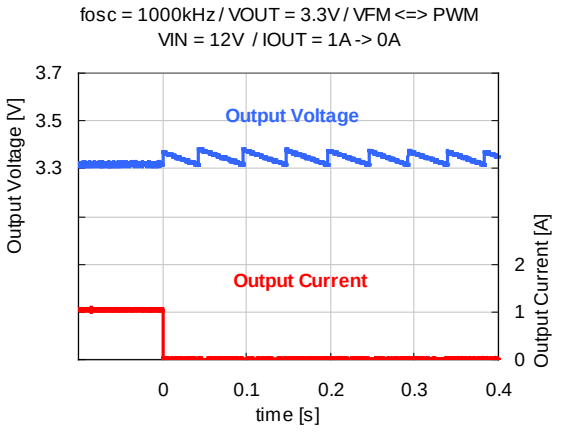




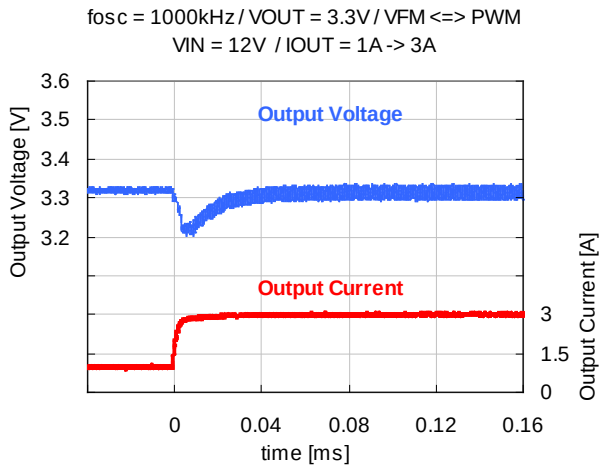


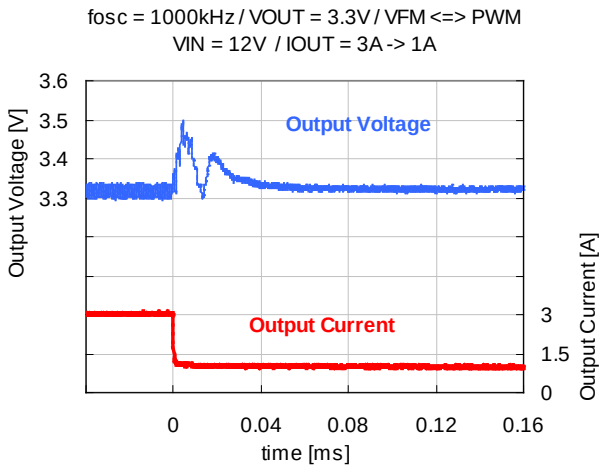
fosc = 1000 kHz



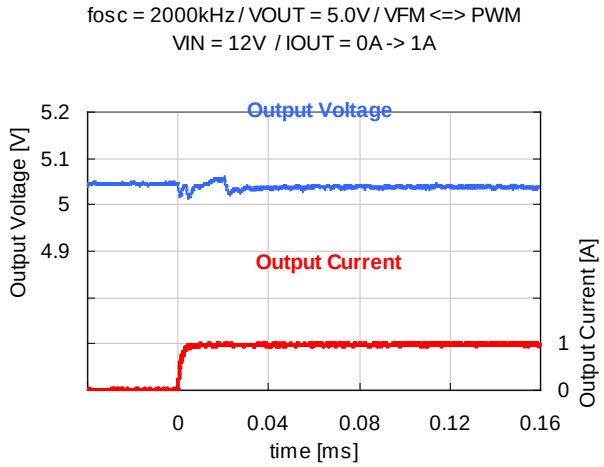


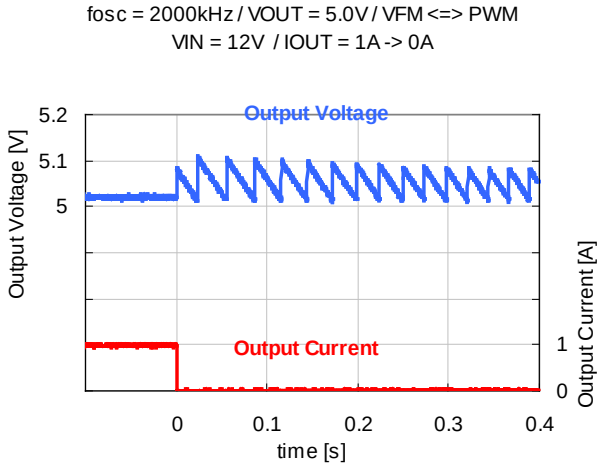
fosc = 1000 kHz

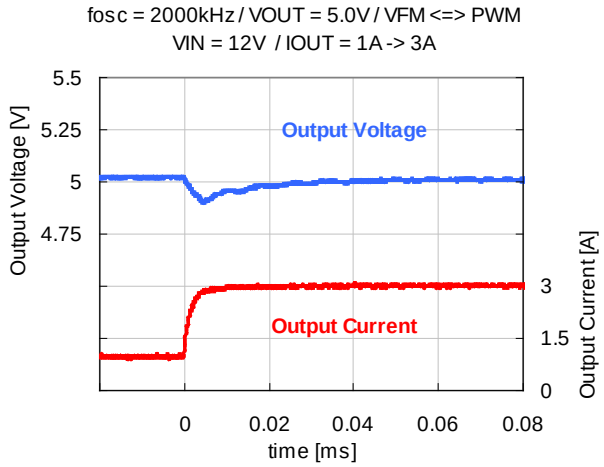


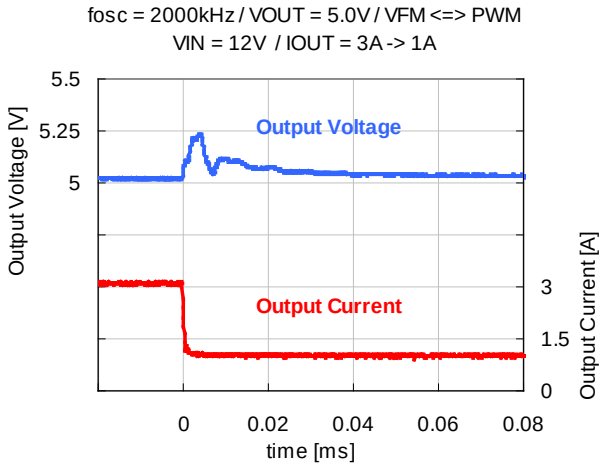


fosc = 2000 kHz



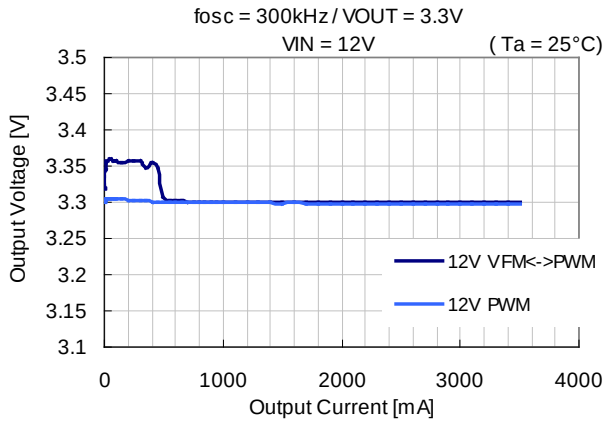




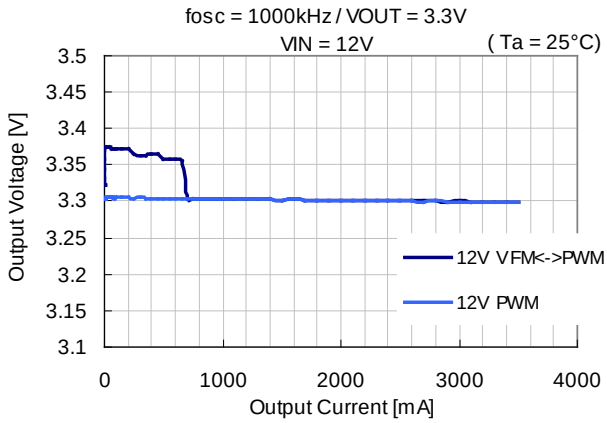


21) Output Current Vs. Output Voltage

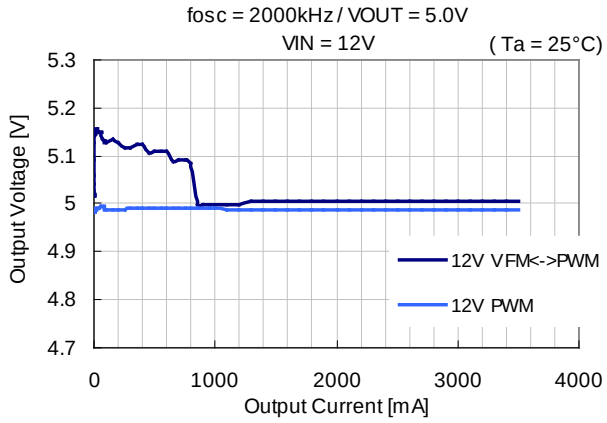
fosc = 300 kHz



fosc = 1000 kHz

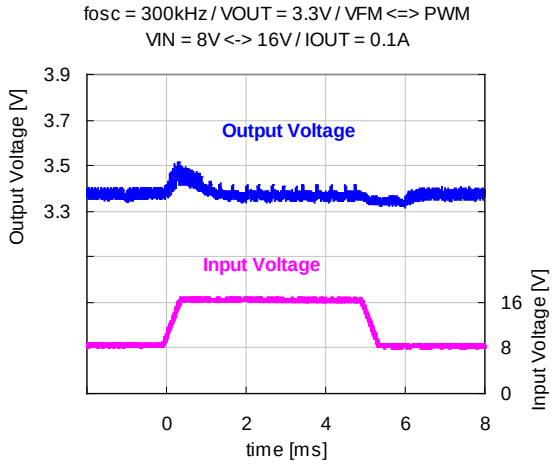


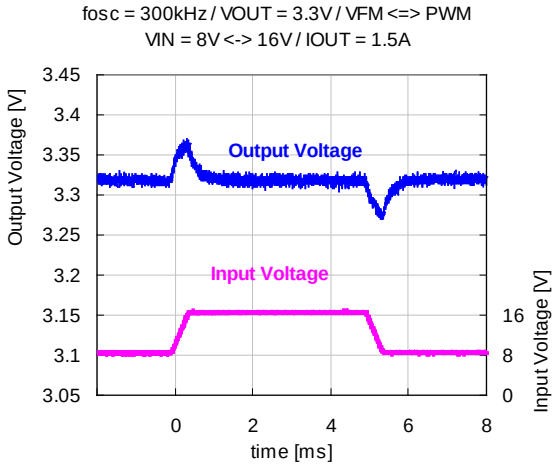
fosc = 2000 kHz



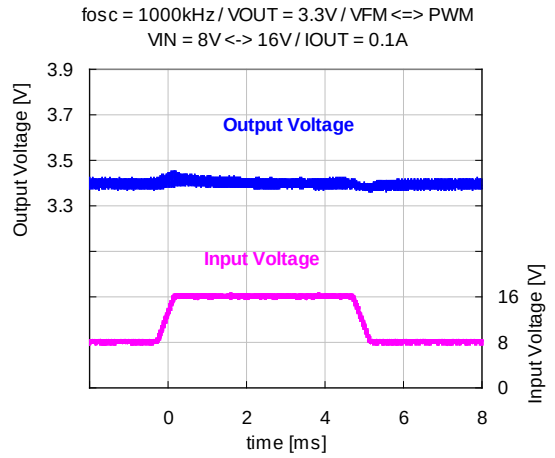
22) Input Transient Response

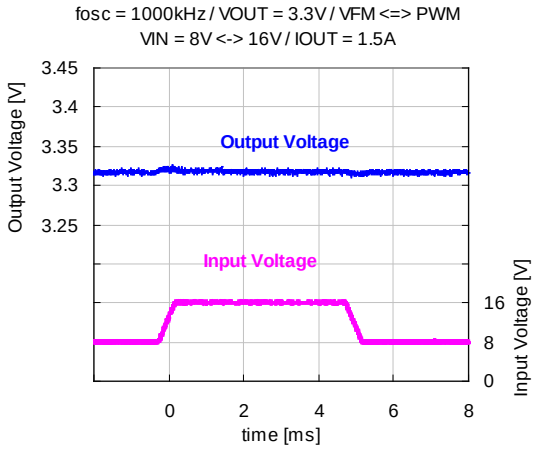
fosc = 300 kHz



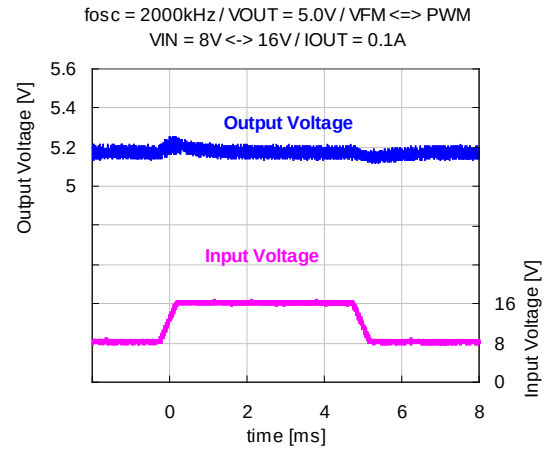


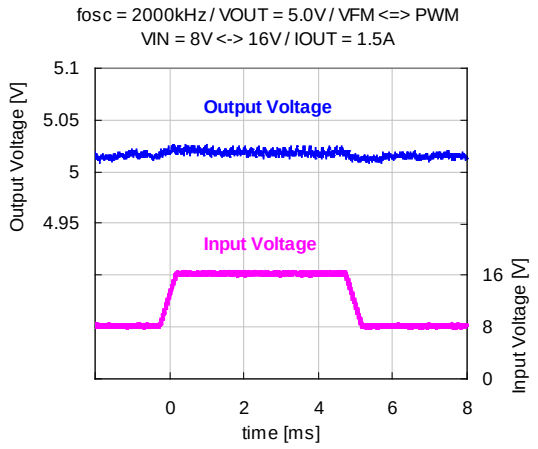
fosc = 1000 kHz





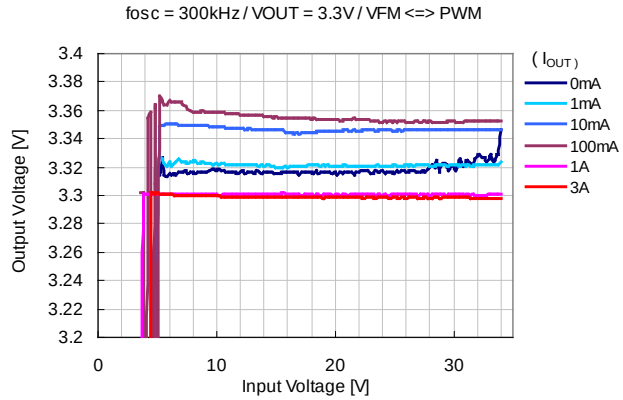
fosc = 2000 kHz

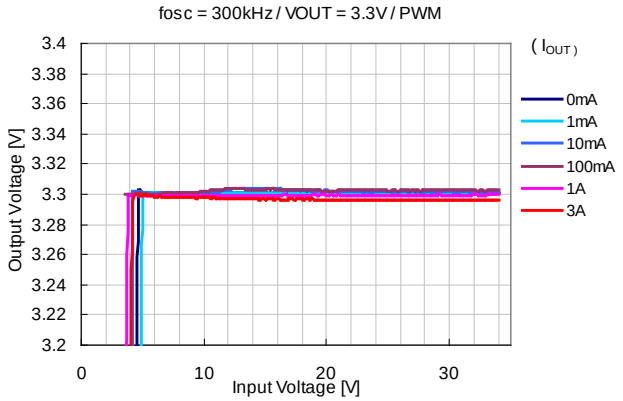




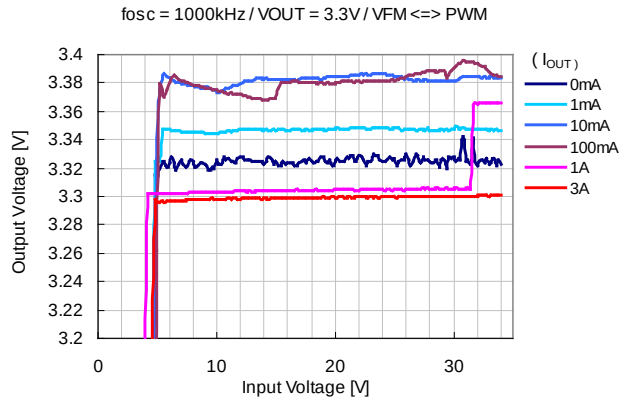
23) Input Voltage Vs. Output Voltage

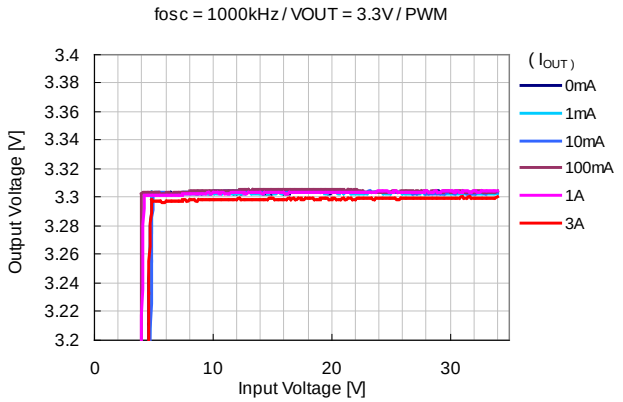
fosc = 300 kHz



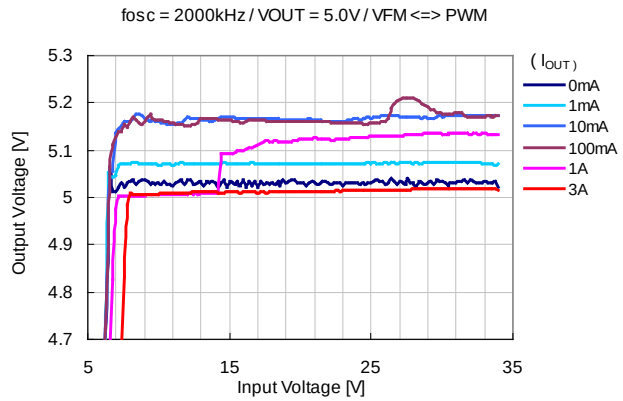


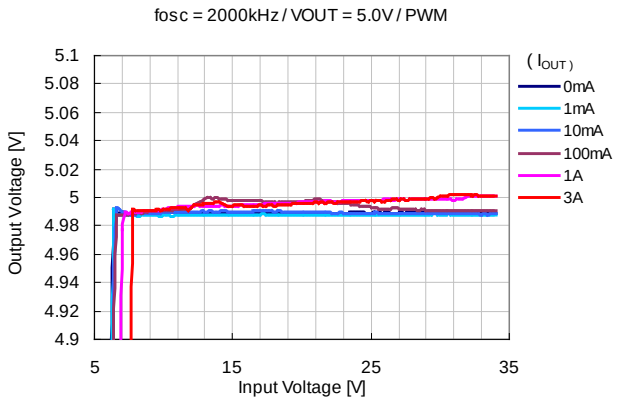
fosc = 1000 kHz





fosc = 2000 kHz





Ver. B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

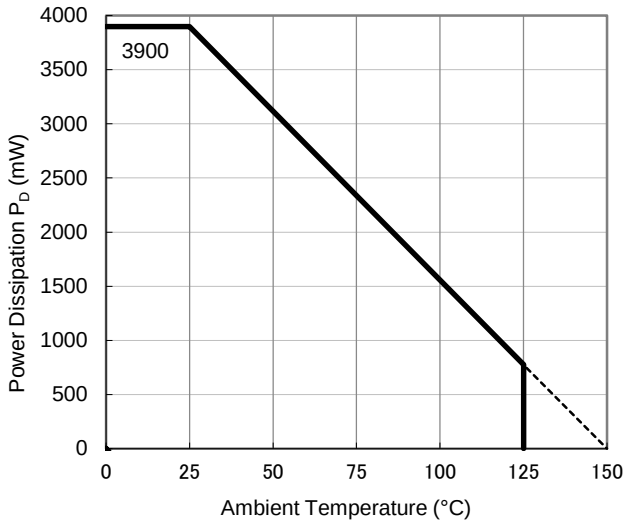
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 150°C)

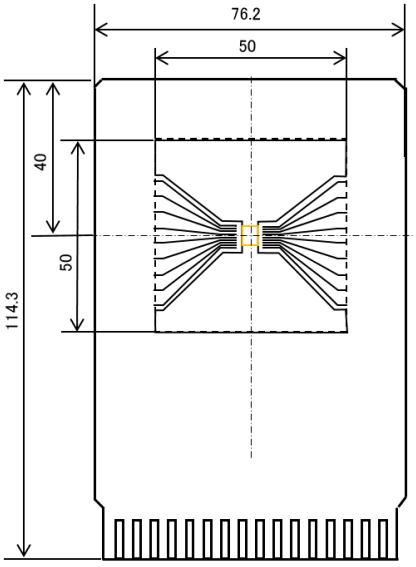
Item	Measurement Result
Power Dissipation	3900 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

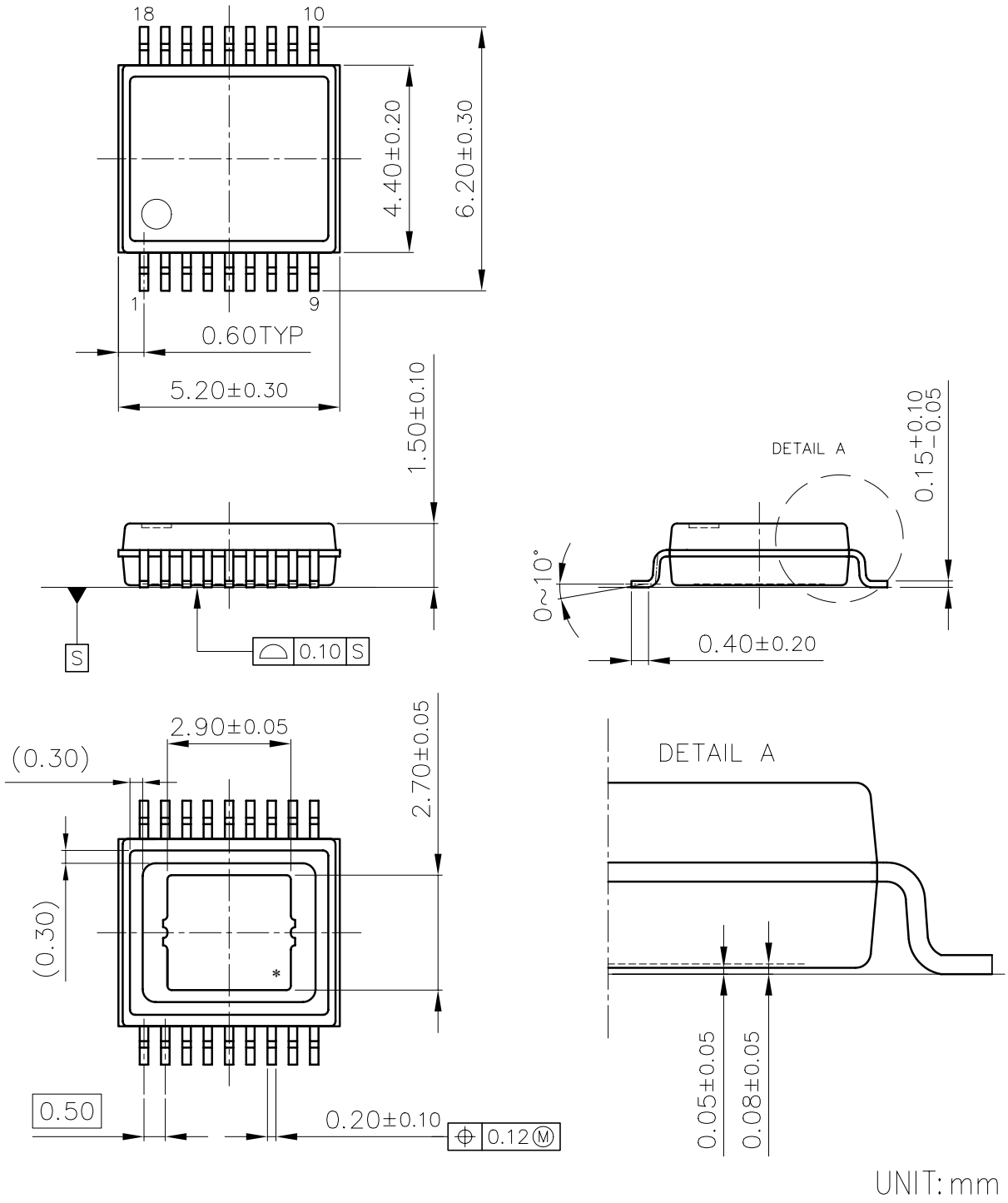


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

Ver. A



HSOP-18 Package Dimensions

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7. Anti-radiation design is not implemented in the products described in this document.
8. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
9. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
10. There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or our distributor before attempting to use AOI.
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