AWR1443 Single-Chip 77- and 79-GHz FMCW Radar Sensor

1 Features

- FMCW transceiver
  - Integrated PLL, transmitter, receiver, Baseband, and ADC
  - 76- to 81-GHz coverage with 4 GHz available bandwidth
  - Four receive channels
  - Three transmit channels (two can be used simultaneously)
  - Ultra-accurate chirp engine based on fractional-N PLL
  - TX power: 12 dBm
  - RX noise figure:
    - 14 dB (76 to 77 GHz)
    - 15 dB (77 to 81 GHz)
  - Phase noise at 1 MHz:
    - –95 dBc/Hz (76 to 77 GHz)
    - –93 dBc/Hz (77 to 81 GHz)
- Built-in calibration and self-test
  - Arm® Cortex®-R4F-based radio control system
  - Built-in firmware (ROM)
  - Self-calibrating system across process and temperature
- On-chip programmable core for embedded user application
  - Integrated Cortex®-R4F microcontroller clocked at 200 MHz
  - On-chip bootloader supports autonomous mode (loading user application from QSPI flash memory)
  - Integrated peripherals
    - Internal memories With ECC
    - Radar hardware accelerator (FFT, log-magnitude computations, and others)
    - Integrated timers (watch dog and up to four 32-Bit or Two 64-bit timers)
    - I2C (Controller and target modes supported)
    - Two SPI ports
    - CAN port
    - Up to six general-purpose ADC ports
- High-speed data interface to support distributed applications (namely, intermediate data)
- Host interface
  - Control interface with external processor over SPI
  - Interrupts for fault reporting
- AECQ-100 qualified
- Device advanced features
  - Embedded self-monitoring with no host processor involvement
  - Complex baseband architecture
  - Embedded interference detection capability
- Power management
  - Built-in LDO network for enhanced PSRR
  - I/Os support dual voltage 3.3 V/1.8 V
- Clock source
  - Supports externally driven clock (square/sine) at 40 MHz
  - Supports 40 MHz crystal connection with load capacitors
- Easy hardware design
  - 0.65-mm pitch, 161-pin 10.4 mm × 10.4 mm flip chip BGA package for easy assembly and low-cost PCB design
  - Small solution size
- Operating Conditions
  - Junction temp range: –40°C to 125°C

2 Applications

- Proximity sensing
- Parking assistance
- Occupancy detection
- Gesture recognition
- Car door opener applications

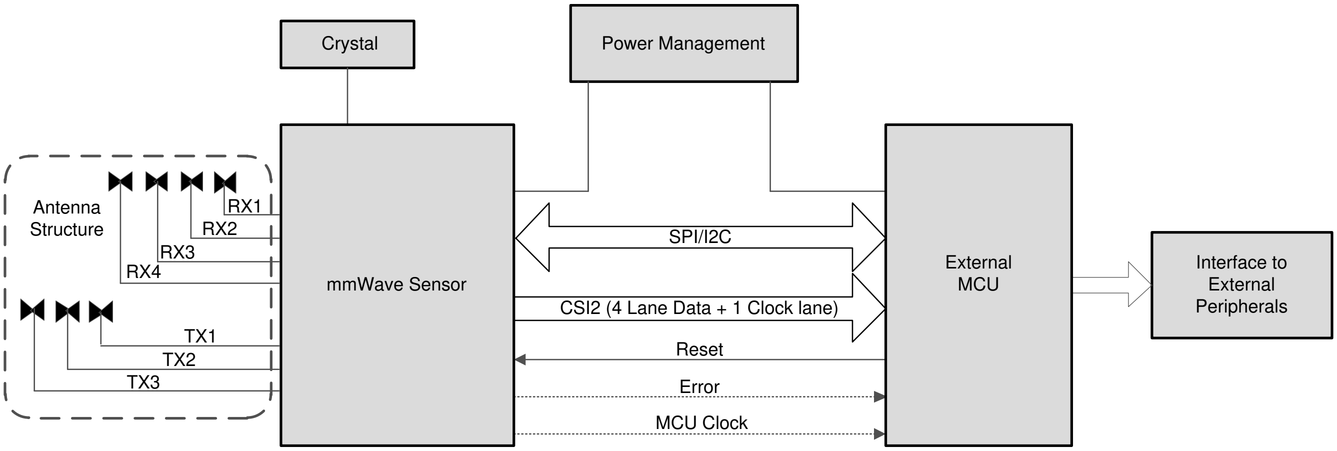


Figure 2-1. Autonomous Radar Sensor For Automotive Applications

3 Description

The AWR1443 device is an integrated single-chip FMCW radar sensor capable of operation in the 76- to 81-GHz band. The device is built with TI's low-power 45-nm RFCMOS process with an integrated ARM R4F processor and a hardware accelerator for radar data processing, and this solution enables unprecedented levels of integration in an extremely small form factor. AWR1443 is an ideal solution for low-power, self-monitored, ultra-accurate radar systems in the automotive space.

The AWR1443 device is a self-contained FMCW radar sensor single-chip solution that simplifies the implementation of Automotive Radar sensors in the band of 76 to 81 GHz. It enables a monolithic implementation of a 3TX, 4RX system with built-in PLL and ADC converters. Simple programming model changes can enable a wide variety of sensor implementation (Short, Mid, Long) with the possibility of dynamic reconfiguration for implementing a multimode sensor. Additionally, the device is provided as a complete platform solution including TI reference designs, software drivers, sample configurations, API guides, and user documentation.

The requirements for a radar device, in terms of radar data cube memory, processing capacity, and functional safety monitoring, vary for different applications. In this context, the AWR1443 can be viewed as a 77-GHz radar-on-a-chip solution for entry-level radar applications

Device Information

PART NUMBER(2)	PACKAGE(1)	BODY SIZE	TRAY / TAPE AND REEL
AWR1443FQIGABLQ1	FCBGA (161)	10.4 mm × 10.4 mm	Tray
AWR1443FQIGABLRQ1			Tape and Reel

(1) For more information, see Section 12, *Mechanical, Packaging, and Orderable Information*.
(2) For more information, see Section 11.1, *Device Nomenclature*.

4 Functional Block Diagram

Figure 4-1 shows the functional block diagram of the device.

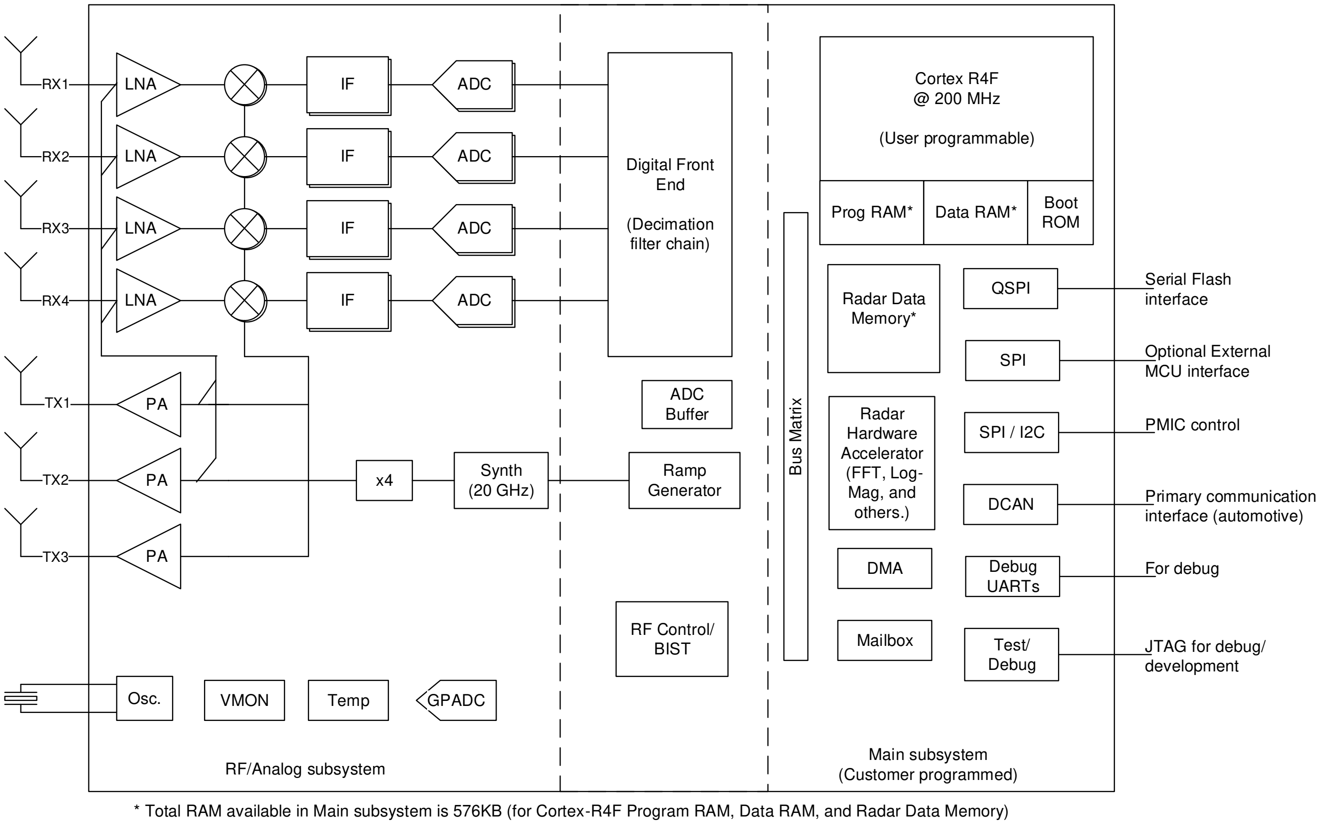


Figure 4-1. Functional Block Diagram

Table of Contents

5 Revision History

Changes from April 30, 2020 to January 10, 2022 (from Revision B (April 2020) to Revision C (January 2022)) **Page**

- *Global:* Replaced "A2D" with "ADC"; Changed Masters Subsystem and Masters R4F to Main Subsystem and Main R4F; Shift to more inclusive langauge made in terms of Master/Slave terminology.................................1
- *(Features)* : Mentioned the specific operating temperature range for the mmWave Sensor; 1
- *(Features)* : Updated/Changed Phase Noise at 1 MHz from "–94 dBc/Hz (76 to 77 GHz)" to "–95" and "–91 dBc/Hz (77 to 81 GHz)" to "–93"...1
- *(Applications)* :Added a figure...2
- Updated/Changed Functional Block Diagram for inclusive terminology..3
- *(Device Comparison):* Removed a row on Functional-Safety compliance; Added a table-note for LVDS Interface; Additional information on Device security updated...6
- *(Signal Descriptions)*: Updated descriptions for CLKP and CLKM pins for Reference Oscillator.....................12
- *(Absolute Maximum Ratings)*: Added entries for externally supplied power on the RF inputs (TX and RX) and a table-note for the signal level applied on TX..21
- (Average Power Consumption at Power Terminals): Added measurement conditions for the specified power numbers...24
- (Maximum Current Rating at Power Terminals): Updated footnotes section to add estimation assumption for VIOIN rail... 24
- *(Synchronized Frame Triggering):* Updated the maximum pulse width to 4000ns.. 27
- *(Clock Specifications):* Updated/Changed Table 8-6 to reflect correct device operating temperature range... 29
- *(Table. External Clock Mode Specifications):* Revised frequency tolerance specs from +/-50 to +/-100 ppm..29
- *(Reference Schematics) :* Added weblinks to device EVM documentation collateral 63

6 Device Comparison

FUNCTION		AWR1243	AWR1443	AWR1642	AWR1843
Number of receivers		4	4	4	4
Number of transmitters		3	3	2	3
On-chip memory		—	576KB	1.5MB	2MB
Max I/F (Intermediate Frequency) (MHz)		15	5	5	10
Max real/complex 2x sampling rate (Msps)		37.5	12.5	12.5	25
Max complex 1x sampling rate (Msps)		18.75	6.25	6.25	12.5
Device Security(1)		—	—	Yes	Yes
Processor					
MCU (R4F)		—	Yes	Yes	Yes
DSP (C674x)		—	—	Yes	Yes
Peripherals					
Serial Peripheral Interface (SPI) ports		1	1	2	2
Quad Serial Peripheral Interface (QSPI)		—	Yes	Yes	Yes
Inter-Integrated Circuit (I^2C) interface		—	1	1	1
Controller Area Network (DCAN) interface		—	Yes	Yes	Yes
CAN-FD		—	—	Yes	Yes
Trace		—	—	Yes	Yes
PWM		—	—	Yes	Yes
Hardware In Loop (HIL/DMM)		—	—	Yes	Yes
GPADC		—	Yes	Yes	Yes
LVDS/Debug(2)		Yes	Yes	Yes	Yes
CSI2		Yes	—	—	—
Hardware accelerator		—	Yes	—	Yes
1-V bypass mode		Yes	Yes	Yes	Yes
Cascade (20-GHz sync)		—	—	—	—
JTAG		—	Yes	Yes	Yes
Number of Tx that can be simultaneously used		2	2	2	3(3)
Per chirp configurable Tx phase shifter		—	—	—	Yes
Product status(4)	PRODUCT PREVIEW (PP), ADVANCE INFORMATION (AI), or PRODUCTION DATA (PD)	PD	PD	PD	PD

(1) Device security features including Secure Boot and Customer Programmable Keys are available in select devices for only select part variants as indicated by the Device Type identifier in Section 3, Device Information table.
(2) The LVDS interface is not a production interface and is only used for debug.
(3) 3 Tx Simultaneous operation is supported only in AWR1843 with 1V LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin. Rest of the other devices only support simultaneous operation of 2 Transmitters.
(4) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

6.1 Related Products

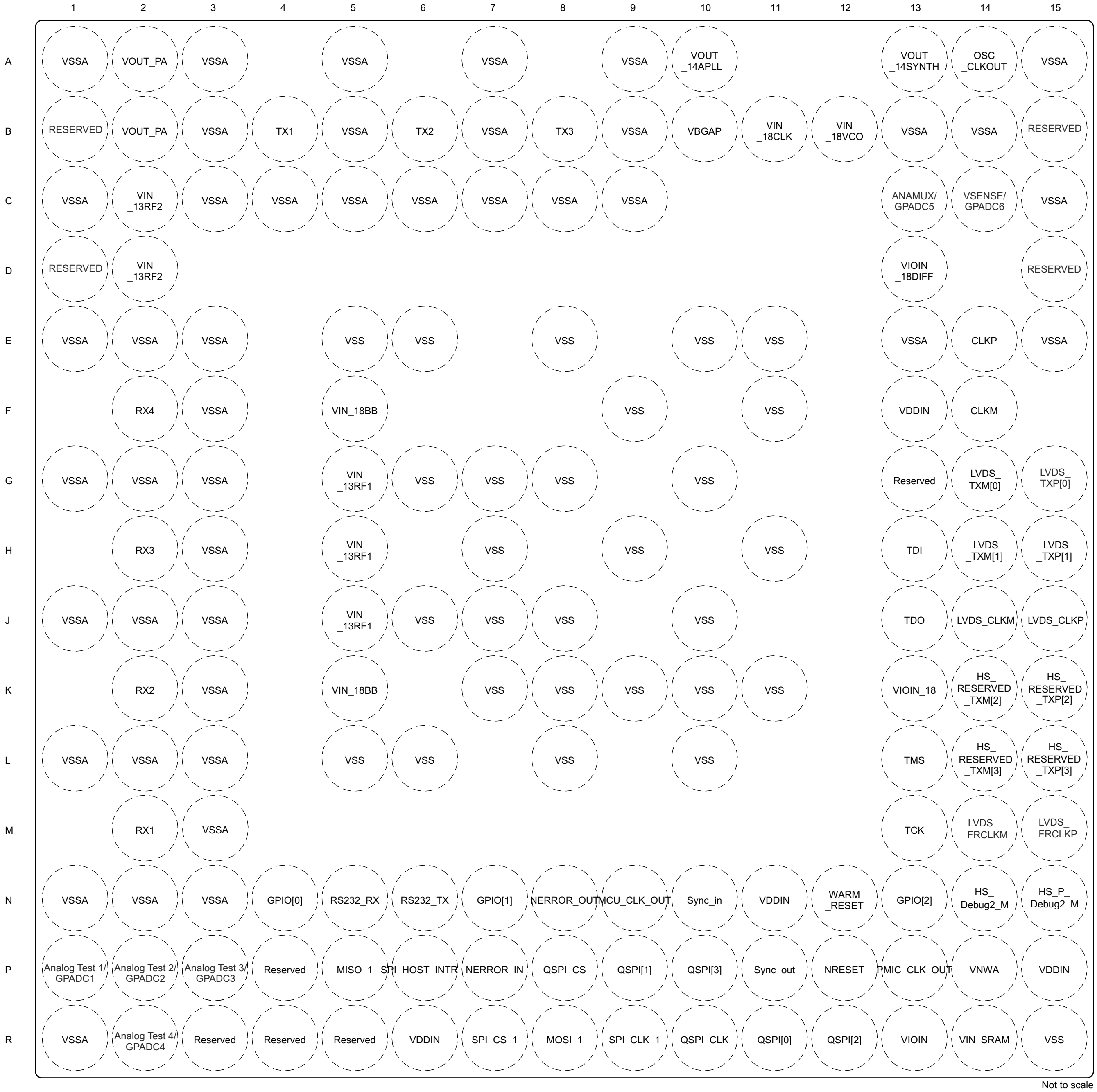
For information about other devices in this family of products or related products see the links that follow.

mmWave sensors	TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for automotive applications.
Automotive mmWave sensors	TI's automotive mmWave sensor portfolio offers high-performance radar front end to ultra-high resolution, small and low-power single-chip radar solutions. TI's scalable sensor portfolio enables design and development of ADAS system solution for every performance, application and sensor configuration ranging from comfort functions to safety functions in all vehicles.
Companion products for AWR1443	Review products that are frequently purchased or used in conjunction with this product.

7 Terminal Configuration and Functions

7.1 Pin Diagram

Figure 7-1 shows the pin locations for the 161-pin FCBGA package. Figure 7-2, Figure 7-3, Figure 7-4, and Figure 7-5 show the same pins, but split into four quadrants.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VSSA	VOUT_PA	VSSA		VSSA		VSSA		VSSA	VOUT_14APLL			VOUT_14SYNTH	OSC_CLKOUT	VSSA
B	RESERVED	VOUT_PA	VSSA	TX1	VSSA	TX2	VSSA	TX3	VSSA	VBGAP	VIN_18CLK	VIN_18VCO	VSSA	VSSA	RESERVED
C	VSSA	VIN_13RF2	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA				ANAMUX/GPADC5	VSENSE/GPADC6	VSSA
D	RESERVED	VIN_13RF2											VIOIN_18DIFF		RESERVED
E	VSSA	VSSA	VSSA		VSS	VSS		VSS		VSS	VSS		VSSA	CLKP	VSSA
F		RX4	VSSA		VIN_18BB				VSS		VSS		VDDIN	CLKM	
G	VSSA	VSSA	VSSA		VIN_13RF1	VSS	VSS	VSS		VSS			Reserved	LVDS_TXM[0]	LVDS_TXP[0]
H		RX3	VSSA		VIN_13RF1		VSS		VSS		VSS		TDI	LVDS_TXM[1]	LVDS_TXP[1]
J	VSSA	VSSA	VSSA		VIN_13RF1	VSS	VSS	VSS		VSS			TDO	LVDS_CLKM	LVDS_CLKP
K		RX2	VSSA		VIN_18BB		VSS	VSS	VSS	VSS	VSS		VIOIN_18	HS_RESERVED_TXM[2]	HS_RESERVED_TXP[2]
L	VSSA	VSSA	VSSA		VSS	VSS		VSS		VSS			TMS	HS_RESERVED_TXM[3]	HS_RESERVED_TXP[3]
M		RX1	VSSA										TCK	LVDS_FRCLKM	LVDS_FRCLKP
N	VSSA	VSSA	VSSA	GPIO[0]	RS232_RX	RS232_TX	GPIO[1]	NERROR_OUT	MCU_CLK_OUT	Sync_in	VDDIN	WARM_RESET	GPIO[2]	HS_Debug2_M	HS_P_Debug2_M
P	Analog Test 1/GPADC1	Analog Test 2/GPADC2	Analog Test 3/GPADC3	Reserved	MISO_1	SPI_HOST_INTR	NERROR_IN	QSPI_CS	QSPI[1]	QSPI[3]	Sync_out	NRESET	PMIC_CLK_OUT	VNWA	VDDIN
R	VSSA	Analog Test 4/GPADC4	Reserved	Reserved	Reserved	VDDIN	SPI_CS_1	MOSI_1	SPI_CLK_1	QSPI_CLK	QSPI[0]	QSPI[2]	VIOIN	VIN_SRAM	VSS

Not to scale

Figure 7-1. Pin Diagram

	1	2	3	4	5	6	7	8
A	VSSA	VOUT_PA	VSSA		VSSA		VSSA	
B	RESERVED	VOUT_PA	VSSA	TX1	VSSA	TX2	VSSA	TX3
C	VSSA	VIN_13RF2	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
D	RESERVED	VIN_13RF2						
E	VSSA	VSSA	VSSA		VSS	VSS		VSS
F		RX4	VSSA		VIN_18BB			
G	VSSA	VSSA	VSSA		VIN_13RF1	VSS	VSS	VSS

Not to scale

▨ 1	2
3	4

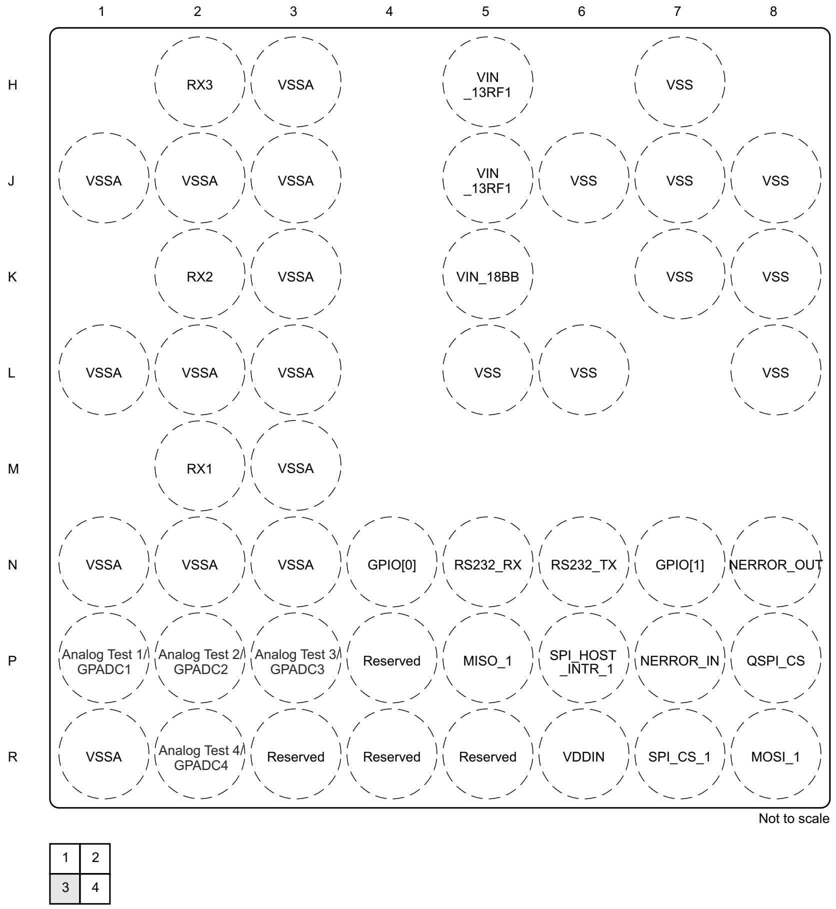
Figure 7-2. Top Left Quadrant

	9	10	11	12	13	14	15
A	VSSA	VOUT_14APLL			VOUT_14SYNTH	OSC_CLKOUT	VSSA
B	VSSA	VBGAP	VIN_18CLK	VIN_18VCO	VSSA	VSSA	RESERVED
C	VSSA				ANAMUX/ GPADC5	VSENSE/ GPADC6	VSSA
D					VIOIN_18DIFF		RESERVED
E		VSS	VSS		VSSA	CLKP	VSSA
F	VSS		VSS		VDDIN	CLKM	
G		VSS			Reserved	LVDS_TXM[0]	LVDS_TXP[0]

Not to scale

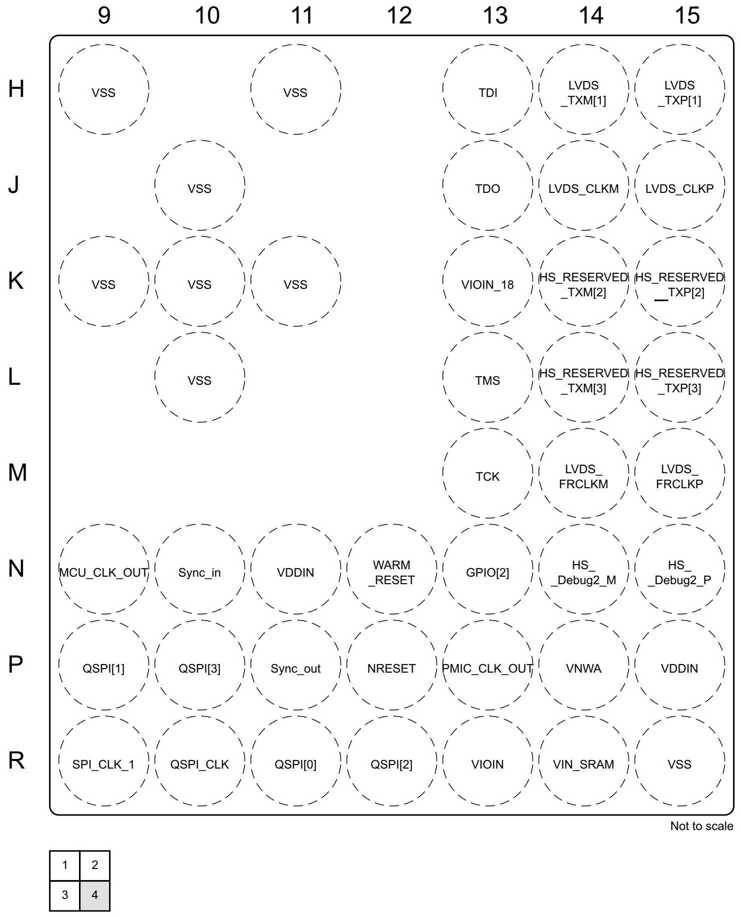
1	▨ 2
3	4

Figure 7-3. Top Right Quadrant



	1	2	3	4	5	6	7	8
H		RX3	VSSA		VIN_13RF1		VSS	
J	VSSA	VSSA	VSSA		VIN_13RF1	VSS	VSS	VSS
K		RX2	VSSA		VIN_18BB		VSS	VSS
L	VSSA	VSSA	VSSA		VSS	VSS		VSS
M		RX1	VSSA					
N	VSSA	VSSA	VSSA	GPIO[0]	RS232_RX	RS232_TX	GPIO[1]	NERROR_OUT
P	Analog Test 1/ GPADC1	Analog Test 2/ GPADC2	Analog Test 3/ GPADC3	Reserved	MISO_1	SPI_HOST_INTR_1	NERROR_IN	QSPI_CS
R	VSSA	Analog Test 4/ GPADC4	Reserved	Reserved	Reserved	VDDIN	SPI_CS_1	MOSI_1

Figure 7-4. Bottom Left Quadrant



	9	10	11	12	13	14	15
H	VSS		VSS		TDI	LVDS _TXM[1]	LVDS _TXP[1]
J		VSS			TDO	LVDS_CLKM	LVDS_CLKP
K	VSS	VSS	VSS		VIOIN_18	HS_RESERVED _TXM[2]	HS_RESERVED _TXP[2]
L		VSS			TMS	HS_RESERVED _TXM[3]	HS_RESERVED _TXP[3]
M					TCK	LVDS_ FRCLKM	LVDS_ FRCLKP
N	MCU_CLK_OUT	Sync_in	VDDIN	WARM _RESET	GPIO[2]	HS_ _Debug2_M	HS_ _Debug2_P
P	QSPI[1]	QSPI[3]	Sync_out	NRESET	PMIC_CLK_OUT	VNWA	VDDIN
R	SPI_CLK_1	QSPI_CLK	QSPI[0]	QSPI[2]	VIOIN	VIN_SRAM	VSS

Figure 7-5. Bottom Right Quadrant

7.2 Signal Descriptions

Note

All digital IO pins of the device (except NERROR IN, NERROR_OUT, and WARM_RESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device.

Note

The GPIO state during the power supply ramp is not ensured. In case the GPIO is used in the application where the state of the GPIO is critical, even when NRESET is low, a tri-state buffer should be used to isolate the GPIO output from the radar device and a pull resister used to define the required state in the application. The NRESET signal to the radar device could be used to control the output enable (OE) of the tri-state buffer.

7.2.1 Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS[(1)]	DESCRIPTION
Transmitters	TX1	B4	O	—	Single-ended transmitter1 o/p
	TX2	B6	O	—	Single-ended transmitter2 o/p
	TX3	B8	O	—	Single-ended transmitter3 o/p
Receivers	RX1	M2	I	—	Single-ended receiver1 i/p
	RX2	K2	I	—	Single-ended receiver2 i/p
	RX3	H2	I	—	Single-ended receiver3 i/p
	RX4	F2	I	—	Single-ended receiver4 i/p
LVDS TX	LVDS_TXP[0]	G15	O	—	Differential data Out – Lane 0
	LVDS_TXM[0]	G14	O	—	
	LVDS_CLKP	J15	O	—	Differential clock Out
	LVDS_CLKM	J14	O	—	
	LVDS_TXP[1]	H15	O	—	Differential data Out – Lane 1
	LVDS_TXM[1]	H14	O	—	
	HS_RESERVED_TXP[2]	K15	O	—	Differential data Out – Lane 2
	HS_RESERVED_TXM[2]	K14	O	—	
	HS_RESERVED_TXP[3]	L15	O	—	Differential data Out – Lane 3
	HS_RESERVED_TXM[3]	L14	O	—	
	LVDS_FRCLKP	M15	O	—	Differential debug port 1
	LVDS_FRCLKM	M14	O	—	
	HS_DEBUG2_P	N15	O	—	Differential debug port 2
	HS_DEBUG2_M	N14	O	—	
	RESERVED	B1, B15, D1, D15		—	
Reference clock	OSC_CLKOUT	A14	O	—	Reference clock output from clocking subsystem after cleanup PLL. Can be used by peripheral chip in multichip cascading

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS(1)	DESCRIPTION
System synchronization	SYNC_OUT	P11	O	Pull Down	Low-frequency frame synchronization signal output. Can be used by peripheral chip in multichip cascading
	SYNC_IN	N10	I	Pull Down	Low-frequency frame synchronization signal input. This signal could also be used as a hardware trigger for frame start
SPI control interface from external MCU (default peripheral mode)	SPI_CS_1	R7	I	Pull Up	SPI chip select
	SPI_CLK_1	R9	I	Pull Down	SPI clock
	MOSI_1	R8	I	Pull Up	SPI data input
	MISO_1	P5	O	Pull Up	SPI data output
	SPI_HOST_INTR_1	P6	O	Pull Down	SPI interrupt to host
	RESERVED	R3, R4, R5, P4		—	
Reset	NRESET	P12	I	—	Power on reset for chip. Active low
	WARM_RESET	N12	IO	Open Drain	Open-drain fail-safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.
Safety	NERROR_OUT	N8	O	Open Drain	Open-drain fail-safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.
	NERROR_IN	P7	I	Open Drain	Fail-safe input to the device. Error output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by firmware
JTAG	TMS	L13	I	Pull Up	JTAG port for standard boundary scan
	TCK	M13	I	Pull Down	
	TDI	H13	I	Pull Up	
	TDO	J13	O	—	
Reference oscillator	CLKP	E14	I	—	In XTAL mode: Input for the reference crystal In External clock mode: Single ended input reference clock port
	CLKM	F14	O	—	In XTAL mode: Feedback drive for the reference crystal In External clock mode: Connect this port to ground
Band-gap voltage	VBGAP	B10	O	—	

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS[1]	DESCRIPTION
Power supply	VDDIN	F13,N11,P15,R6	POW	—	1.2-V digital power supply
	VIN_SRAM	R14	POW	—	1.2-V power rail for internal SRAM
	VNWA	P14	POW	—	1.2-V power rail for SRAM array back bias
	VIOIN	R13	POW	—	I/O supply (3.3-V or 1.8-V): All CMOS I/Os would operate on this supply.
	VIOIN_18	K13	POW	—	1.8-V supply for CMOS IO
	VIN_18CLK	B11	POW	—	1.8-V supply for clock module
	VIOIN_18DIFF	D13	POW	—	1.8-V supply for high speed interface port
	Reserved	G13	POW	—	No connect
	VIN_13RF1	G5,J5,H5	POW	—	1.3-V Analog and RF supply,VIN_13RF1 and VIN_13RF2 could be shorted on the board
	VIN_13RF2	C2,D2	POW	—	
	VIN_18BB	K5,F5	POW	—	1.8-V Analog baseband power supply
	VIN_18VCO	B12	POW	—	1.8-V RF VCO supply
	VSS	E5,E6,E8,E10,E11,F9,F11,G6,G7,G8,G10,H7,H9,H11,J6,J7,J8,J10,K7,K8,K9,K10,K11,L5,L6,L8,L10,R15	GND	—	Digital ground
	VSSA	A1,A3,A5,A7,A9,A15,B3,B5,B7,B9,B13,B14,C1,C3,C4,C5,C6,C7,C8,C9,C15,E1,E2,E3,E13,E15,F3,G1,G2,G3,H3,J1,J2,J3,K3,L1,L2,L3,M3,N1,N2,N3,R1	GND	—	Analog ground
Internal LDO output/inputs	VOUT_14APLL	A10	O	—	
	VOUT_14SYNTH	A13	O	—	
	VOUT_PA	A2,B2	O	—	
External clock out	PMIC_CLK_OUT	P13	O	—	Dithered clock input to PMIC
	MCU_CLK_OUT	N9	O	—	Programmable clock given out to external MCU or the processor
General-purpose I/Os	GPIO[0]	N4	IO	Pull Down	General-purpose IO
	GPIO[1]	N7	IO	Pull Down	General-purpose IO
	GPIO[2]	N13	IO	Pull Down	General-purpose IO
QSPI for Serial Flash[2]	QSPI_CS	P8	O	Pull Up	Chip-select output from the device. Device is a controller connected to serial flash peripheral.
	QSPI_CLK	R10	O	Pull Down	Clock output from the device. Device is a controller connected to serial flash peripheral.
	QSPI[0]	R11	IO	Pull Down	Data IN/OUT
	QSPI[1]	P9	IO	Pull Down	Data IN/OUT
	QSPI[2]	R12	IO	Pull Up	Data IN/OUT
	QSPI[3]	P10	IO	Pull Up	Data IN/OUT

FUNCTION	SIGNAL NAME	PIN NUMBER	PIN TYPE	DEFAULT PULL STATUS[1]	DESCRIPTION
Flash programming and RS232 UART[2]	RS232_TX	N6	O	Pull Down	UART pins for programming external flash in preproduction/debug hardware.
	RS232_RX	N5	I	Pull Up	
Test and Debug output for preproduction phase. Can be pinned out on production hardware for field debug	Analog Test1 / GPADC1	P1	IO	—	GP ADC channel 1
	Analog Test2 / GPADC2	P2	IO	—	GP ADC channel 2
	Analog Test3 / GPADC3	P3	IO	—	GP ADC channel 3
	Analog Test4	R2	IO	—	GP ADC channel 4
	ANAMUX / GPADC5	C13	IO	—	GP ADC channel 5
	VSENSE / GPADC6	C14	IO	—	GP ADC channel 6

(1) Status of PULL structures associated with the IO after device POWER UP.
(2) This option is for development/debug in preproduction phase. Can be disabled by firmware pin mux setting.

7.3 Pin Multiplexing

Table 7-1. Pin Multiplexing

REGISTER ADDRESS(1)	PIN NAME	PIN	DIGITAL PIN MUX CONFIG VALUE [Bits3:0]	FUNCTION			PAD STATE nReset = 0 [ASSERTED]	
				SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE
EA00h	GPIO_12	P6	0	GPIO_12	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	SPI_HOST1_INTR	General Purpose IO [AWR14xx]	O		
EA04h	GPIO_0	N4	0	GPIO_13	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	GPIO_0	General Purpose IO	IO		
			2	PMIC_CLKOUT	Dithered Clock Output for PMIC	O		
EA08h	GPIO_1	N7	0	GPIO_16	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	GPIO_1	General Purpose IO	IO		
			2	SYNC_OUT	Low Frequency Synchronization Signal output	O		
EA0Ch	MOSI_1	R8	0	GPIO_19	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	MOSI_1	SPI Channel#1 Data Input	IO		
			2	CAN_RX	CAN Interface	I		
EA10h	MISO_1	P5	0	GPIO_20	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	MISO_1	SPI Channel#1 Data Output	IO		
			2	CAN_TX	CAN Interface	O		
EA14h	SPI_CLK_1	R9	0	GPIO_3	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	SPI_CLK_1	SPI Channel#1 Clock	IO		
				RCOSC_CLK		O		
EA18h	SPI_CS_1	R7	0	GPIO_30	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	SPI_CS_1	SPI Channel#1 Chip Select	IO		
				RCOSC_CLK		O		
EA1Ch	MOSI_2	R3	0	GPIO_21	General Purpose IO	IO	Hi-Z	
			1	MOSI_2	SPI Channel#2 Data Input	IO		
			2	I2C_SDA	I2C Data	IO		
EA20h	MISO_2	P4	0	GPIO_22	General Purpose IO	IO	Hi-Z	
			1	MISO_2	SPI Channel#2 Data Output	IO		
			2	I2C_SCL	I2C Clock	IO		

Table 7-1. Pin Multiplexing (continued)

REGISTER ADDRESS(1)	PIN NAME	PIN	DIGITAL PIN MUX CONFIG VALUE [Bits3:0]	FUNCTION			PAD STATE nReset = 0 [ASSERTED]	
				SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE
EA24h	SPI_CLK_2	R5	0	GPIO_5	General Purpose IO	IO	Hi-Z	
			1	SPI_CLK_2	SPI Channel#2 Clock	IO		
				MSS_UARTA_RX		IO		
			6	MSS_UARTB_TX	Debug: Firmware Trace	O		
			7	BSS_UART_TX	Debug: Firmware Trace	O		
EA28h	SPI_CS_2	R4	0	GPIO_4	General Purpose IO	IO	Hi-Z	
			1	SPI_CS_2	SPI Channel#2 Chip Select	IO		
				MSS_UARTA_TX		IO		
			6	MSS_UARTB_TX	Debug: Firmware Trace	O		
			7	BSS_UART_TX	Debug: Firmware Trace	O		
EA2Ch	QSPI[0]	R11	0	GPIO_8	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	QSPI[0]	QSPI Data IN/OUT	IO		
			2	MISO_2	SPI Channel#1 Data Output	IO		
EA30h	QSPI[1]	P9	0	GPIO_9	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	QSPI[1]	QSPI Data IN/OUT	IO		
			2	MOSI_2	SPI Channel#2 Data Input	IO		
EA34h	QSPI[2]	R12	0	GPIO_10	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	QSPI[2]	QSPI Data IN/OUT	IO		
EA38h	QSPI[3]	P10	0	GPIO_11	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	QSPI[3]	QSPI Data IN/OUT	I		
EA3Ch	QSPI_CLK	R10	0	GPIO_7	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	QSPI_CLK	QSPI Clock output from the device. Device operates as a master with the serial flash being a slave	O		
			2	SPI_CLK_2	SPI Channel#2 Clock	IO		
EA40h	QSPI_CS	P8	0	GPIO_6	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	QSPI_CS	QSPI Chip Select output from the device. Device operates as a master with the serial flash being a slave	O		
			2	SPI_CS_2	SPI Channel#2 Chip Select	IO		

Table 7-1. Pin Multiplexing (continued)

REGISTER ADDRESS[1]	PIN NAME	PIN	DIGITAL PIN MUX CONFIG VALUE [Bits3:0]	FUNCTION			PAD STATE nReset = 0 [ASSERTED]	
				SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE
	NERROR_IN	P7		NERROR_IN	Failsafe input to the device. Nerror output from any other device can be concentrated in the error signaling monitor module inside the device and appropriate action can be taken by Firmware	I	Hi-Z	
	WARM_RESET	N12		WARM_RESET	Open drain fail safe warm reset signal. Can be driven from PMIC for diagnostic or can be used as status signal that the device is going through reset.	IO	Hi-Z Input	Open Drain
	NERROR_OUT	N8		NERROR_OUT	Open drain fail safe output signal. Connected to PMIC/Processor/MCU to indicate that some severe criticality fault has happened. Recovery would be through reset.	O	Hi-Z	Open Drain
EA50h	TCK	M13	0	GPIO_17	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	TCK	JTAG Clock	I		
			2	MSS_UARTB_TX	Debug: Firmware Trace	O		
			6	BSS_UART_RX	Debug: Firmware Trace	I		
EA54h	TMS	L13	0	GPIO_18	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	TMS	JTAG Test Mode Select	IO		
			2	BSS_UART_TX	Debug: Firmware Trace	O		
EA58h	TDI	H13	0	GPIO_23	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	TDI	JTAG Test Data In	I		
				MSS_UARTA_RX		IO		
EA5Ch	TDO	J13	0	GPIO_24	General Purpose IO	IO	Hi-Z	
			1	TDO	JTAG Test Data Out	O		
				MSS_UARTA_TX		IO		
			6	MSS_UARTB_TX	Debug: Firmware Trace	O		
			7	BSS_UART_TX	Debug: Firmware Trace	O		
				SOP0	Sense On Power [Reset] Line Impacts boot mode	I		

Table 7-1. Pin Multiplexing (continued)

REGISTER ADDRESS(1)	PIN NAME	PIN	DIGITAL PIN MUX CONFIG VALUE [Bits3:0]	FUNCTION			PAD STATE nReset = 0 [ASSERTED]	
				SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE
EA60h	MCU_CLKOUT	N9	0	GPIO_25	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	MCU_CLKOUT	Programmable clock given out to external MCU or the processor	O		
			10	BSS_UART_RX	Debug: Firmware Trace	I		
EA64h	GPIO_2	N13	0	GPIO_26	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	GPIO_2	General Purpose IO	IO		
			7	MSS_UARTB_TX	Debug: Firmware Trace	O		
			8	BSS_UART_TX	Debug: Firmware Trace	O		
			9	SYNC_OUT	Low frequency Synchronization signal output	O		
			10	PMIC_CLKOUT	Dithered clock input to PMIC	O		
EA68h	PMIC_CLKOUT	P13	0	GPIO_27	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	PMIC_CLKOUT	Dithered Clock Output for PMIC	O		
				SOP2	Sense On Power [Reset] Line Impacts boot mode	I		
EA6Ch	SYNC_IN	N10	0	GPIO_28	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	SYNC_IN	Low frequency Synchronization signal input	I		
			6	MSS_UARTB_RX	Debug: Firmware Trace	I		
EA70h	SYNC_OUT	P11	0	GPIO_29	General Purpose IO	IO	Hi-Z	Weak Pull Down
			1	SYNC_OUT	Low frequency Synchronization signal output	O		
				RCOSC_CLK		O		
				SOP1	Sense On Power [Reset] Line Impacts boot mode	I		
EA74h	RS232_RX	N5	0	GPIO_15	General Purpose IO	IO	Hi-Z	Weak Pull Up
			1	RS232_RX	Debug: Firmware load to RAM	IO		
			2	MSS_UARTA_RX	FLASH Programming Bootloader Controlled	I		
			6	BSS_UART_TX	Debug: Firmware Trace	O		
			7	MSS_UARTB_RX	Debug: Firmware Trace	I		

Table 7-1. Pin Multiplexing (continued)

REGISTER ADDRESS(1)	PIN NAME	PIN	DIGITAL PIN MUX CONFIG VALUE [Bits3:0]	FUNCTION			PAD STATE nReset = 0 [ASSERTED]	
				SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL TYPE	STATE	INTERNAL WEAK PULL STATE
EA78h	RS232_TX	N6	0	GPIO_14	General Purpose IO	IO		
			1	RS232_TX	Debug: Firmware load to RAM	IO		
			5	MSS_UARTA_TX	FLASH Programming Bootloader Controlled	O		
			6	MSS_UARTB_TX	Debug: Firmware Trace	O		
			7	BSS_UART_TX	Debug: Firmware Trace	O		

(1) Register addresses are of the form FFFF XXXXh, where XXXX is listed here.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

PARAMETERS(1) (2)		MIN	MAX	UNIT
VDDIN	1.2 V digital power supply	–0.5	1.4	V
VIN_SRAM	1.2 V power rail for internal SRAM	–0.5	1.4	V
VNWA	1.2 V power rail for SRAM array back bias	–0.5	1.4	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	–0.5	3.8	V
VIOIN_18	1.8 V supply for CMOS IO	–0.5	2	V
VIN_18CLK	1.8 V supply for clock module	–0.5	2	V
VIN_13RF1	1.3 V Analog and RF supply, VIN_13RF1 and VIN_13RF2 could be shorted on the board.	–0.5	1.45	V
VIN_13RF2				
VIN_13RF1	1-V Internal LDO bypass mode. Device supports mode where external Power Management block can supply 1 V on VIN_13RF1 and VIN_13RF2 rails. In this configuration, the internal LDO of the device would be kept bypassed.	–0.5	1.4	V
VIN_13RF2				
VIN_18BB	1.8-V Analog baseband power supply	–0.5	2	V
VIN_18VCO supply	1.8-V RF VCO supply	–0.5	2	V
RX1-4	Externally applied power on RF inputs		10	dBm
TX1-3	Externally applied power on RF outputs(3)		10	dBm
Input and output voltage range	Dual-voltage LVCMOS inputs, 3.3 V or 1.8 V (Steady State)	–0.3V	VIOIN + 0.3	V
	Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input	VIOIN + 20% up to 20% of signal period		
CLKP, CLKM	Input ports for reference crystal	–0.5	2	V
Clamp current	Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O.	–20	20	mA
T_J	Operating junction temperature range	–40	125	°C
T_{STG}	Storage temperature range after soldered onto PC board	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

(3) This value is for an externally applied signal level on the TX. Additionally, a reflection coefficient up to Gamma = 1 can be applied on the TX output.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011		±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Power-On Hours (POH)

JUNCTION TEMPERATURE (T_j) (1) (2)	OPERATING CONDITION	NOMINAL CVDD VOLTAGE (V)	POWER-ON HOURS [POH] (HOURS)
–40°C	100% duty cycle	1.2	600 (6%)
75°C			2000 (20%)
95°C			6500 (65%)
125°C			900 (9%)

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) The specified POH are applicable with max Tx output power settings using the default firmware gain tables. The specified POH would not be applicable, if the Tx gain table is overwritten using an API.

8.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDIN	1.2 V digital power supply	1.14	1.2	1.32	V
VIN_SRAM	1.2 V power rail for internal SRAM	1.14	1.2	1.32	V
VNWA	1.2 V power rail for SRAM array back bias	1.14	1.2	1.32	V
VIOIN	I/O supply (3.3 V or 1.8 V): All CMOS I/Os would operate on this supply.	3.135	3.3	3.465	V
		1.71	1.8	1.89	
VIOIN_18	1.8 V supply for CMOS IO	1.71	1.8	1.9	V
VIN_18CLK	1.8 V supply for clock module	1.71	1.8	1.9	V
VIN_13RF1	1.3 V Analog and RF supply. VIN_13RF1 and VIN_13RF2 could be shorted on the board	1.23	1.3	1.36	V
VIN_13RF2					
VIN_13RF1 (1-V Internal LDO bypass mode)		0.95	1	1.05	V
VIN_13RF2 (1-V Internal LDO bypass mode)					
VIN18BB	1.8-V Analog baseband power supply	1.71	1.8	1.9	V
VIN_18VCO	1.8V RF VCO supply	1.71	1.8	1.9	V
V_{IH}	Voltage Input High (1.8 V mode)	1.17			V
	Voltage Input High (3.3 V mode)	2.25			
V_{IL}	Voltage Input Low (1.8 V mode)			0.3*VIOIN	V
	Voltage Input Low (3.3 V mode)			0.62	
V_{OH}	High-level output threshold (I_{OH} = 6 mA)	VIOIN – 450			mV
V_{OL}	Low-level output threshold (I_{OL} = 6 mA)			450	mV
NRESET SOP[2:0]	V_{IL} (1.8V Mode)			0.2	V
	V_{IH} (1.8V Mode)	0.96			
	V_{IL} (3.3V Mode)			0.3	
	V_{IH} (3.3V Mode)	1.57			

8.5 Power Supply Specifications

Table 8-1 describes the four rails from an external power supply block of the AWR1443 device.

Table 8-1. Power Supply Rails Characteristics

SUPPLY	DEVICE BLOCKS POWERED FROM THE SUPPLY	RELEVANT IOS IN THE DEVICE
1.8 V	Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, LVDS	Input: VIN_18VCO, VIN18CLK, VIN_18BB, VIOIN_18DIFF, VIOIN_18 LDO Output: VOUT_14SYNTH, VOUT_14APLL
1.3 V (or 1 V in internal LDO bypass mode)(1)	Power Amplifier, Low Noise Amplifier, Mixers and LO Distribution	Input: VIN_13RF2, VIN_13RF1 LDO Output: VOUT_PA
3.3 V (or 1.8 V for 1.8 V I/O mode)	Digital I/Os	Input VIOIN
1.2 V	Core Digital and SRAMs	Input: VDDIN, VIN_SRAM

(1) Three simultaneous transmitter operation is supported only in 1-V LDO bypass and PA LDO disable mode. In this mode 1V supply needs to be fed on the VOUT PA pin.

The 1.3-V (1.0 V) and 1.8-V power supply ripple specifications mentioned in are defined to meet a target spur level of –105 dBc (RF Pin = –15 dBm) at the RX. The spur and ripple levels have a dB-to-dB relationship, for example, a 1-dB increase in supply ripple leads to a ~1 dB increase in spur level. Values quoted are rms levels for a sinusoidal input applied at the specified frequency.

Table 8-2. Ripple Specifications

FREQUENCY (kHz)	RF RAIL		VCO/IF RAIL
	1.0 V (INTERNAL LDO BYPASS) (μV_{RMS})	1.3 V (μV_{RMS})	1.8 V (μV_{RMS})
137.5	7	648	83
275	5	76	21
550	3	22	11
1100	2	4	6
2200	11	82	13
4400	13	93	19
6600	22	117	29

8.6 Power Consumption Summary

Table 8-3 and Table 8-4 summarize the power consumption at the power terminals.

Table 8-3. Maximum Current Ratings at Power Terminals

PARAMETER	SUPPLY NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
Current consumption(1)	VDDIN, VIN_SRAM, VNWA	Total current drawn by all nodes driven by 1.2V rail			500	mA
	VIN_13RF1, VIN_13RF2	Total current drawn by all nodes driven by 1.3V rail			2000	
	VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO	Total current drawn by all nodes driven by 1.8V rail			850	
	VIOIN	Total current drawn by all nodes driven by 3.3V rail(2)		50		

(1) The specified current values are at typical supply voltage level.
(2) The exact VIOIN current depends on the peripherals used and their frequency of operation.

Table 8-4. Average Power Consumption at Power Terminals

PARAMETER	CONDITION		DESCRIPTION	MIN	TYP	MAX	UNIT
Average power consumption	1.0-V internal LDO bypass mode	1TX, 4RX	Sampling: 16.66 MSps complex Transceiver, 40-ms frame time, 512 chirps, 512 samples/chirp, 8.5-µs interchirp time (50% duty cycle) Data Port: MIPI-CSI-2		1.72		W
		2TX, 4RX			1.89		
	1.3-V internal LDO enabled mode	1TX, 4RX			1.90		
		2TX, 4RX			2.10		

8.7 RF Specification

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Receiver	Noise figure	76 to 77 GHz		14		dB
		77 to 81 GHz		15		
	1-dB compression point (Out Of Band)(1)			–8		dBm
	Maximum gain			48		dB
	Gain range			24		dB
	Gain step size			2		dB
	Image Rejection Ratio (IMRR)			30		dB
	IF bandwidth(2)				5	MHz
	ADC sampling rate (real/complex 2x)				12.5	Msps
	ADC sampling rate (complex 1x)				6.25	Msps
	ADC resolution			12		Bits
	Return loss (S11)			<–10		dB
	Gain mismatch variation (over temperature)			±0.5		dB
	Phase mismatch variation (over temperature)			±3		°
	In-band IIP2	RX gain = 30dB IF = 1.5, 2 MHz at –12 dBFS		16		dBm
	Out-of-band IIP2	RX gain = 24dB IF = 10 kHz at -10dBm, 1.9 MHz at -30 dBm		24		dBm
	Idle Channel Spurs			–90		dBFS
Transmitter	Output power			12		dBm
	Amplitude noise			–145		dBc/Hz
Clock subsystem	Frequency range		76		81	GHz
	Ramp rate				100	MHz/µs
	Phase noise at 1-MHz offset	76 to 77 GHz		–95		dBc/Hz
		77 to 81 GHz		–93		

(1) 1-dB Compression Point (Out Of Band) is measured by feed a Continuous wave Tone (10 kHz) well below the lowest HPF cut-off frequency.

(2) The analog IF stages include high-pass filtering, with two independently configurable first-order high-pass corner frequencies. The set of available HPF corners is summarized as follows:

Available HPF Corner Frequencies (kHz)	
HPF1	HPF2
175, 235, 350, 700	350, 700, 1400, 2800

The filtering performed by the digital baseband chain is targeted to provide:

- Less than ±0.5 dB pass-band ripple/droop, and
- Better than 60 dB anti-aliasing attenuation for any frequency that can alias back into the pass-band.

Figure 8-1 shows variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed.

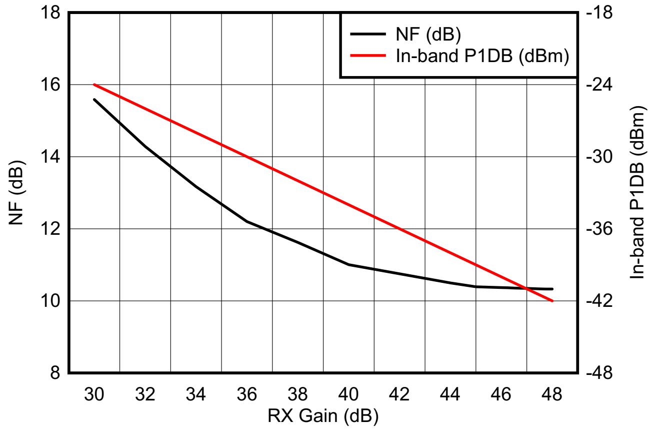


Figure 8-1. Noise Figure, In-band P1dB vs Receiver Gain

8.8 Thermal Resistance Characteristics for FCBGA Package [ABL0161]

THERMAL METRICS(1)		°C/W(2) (3)
$R\Theta_{JC}$	Junction-to-case	5
$R\Theta_{JB}$	Junction-to-board	5.9
$R\Theta_{JA}$	Junction-to-free air	21.6
$R\Theta_{JMA}$	Junction-to-moving air	15.3 (4)
Psi_{JT}	Junction-to-package top	0.69
Psi_{JB}	Junction-to-board	5.8

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

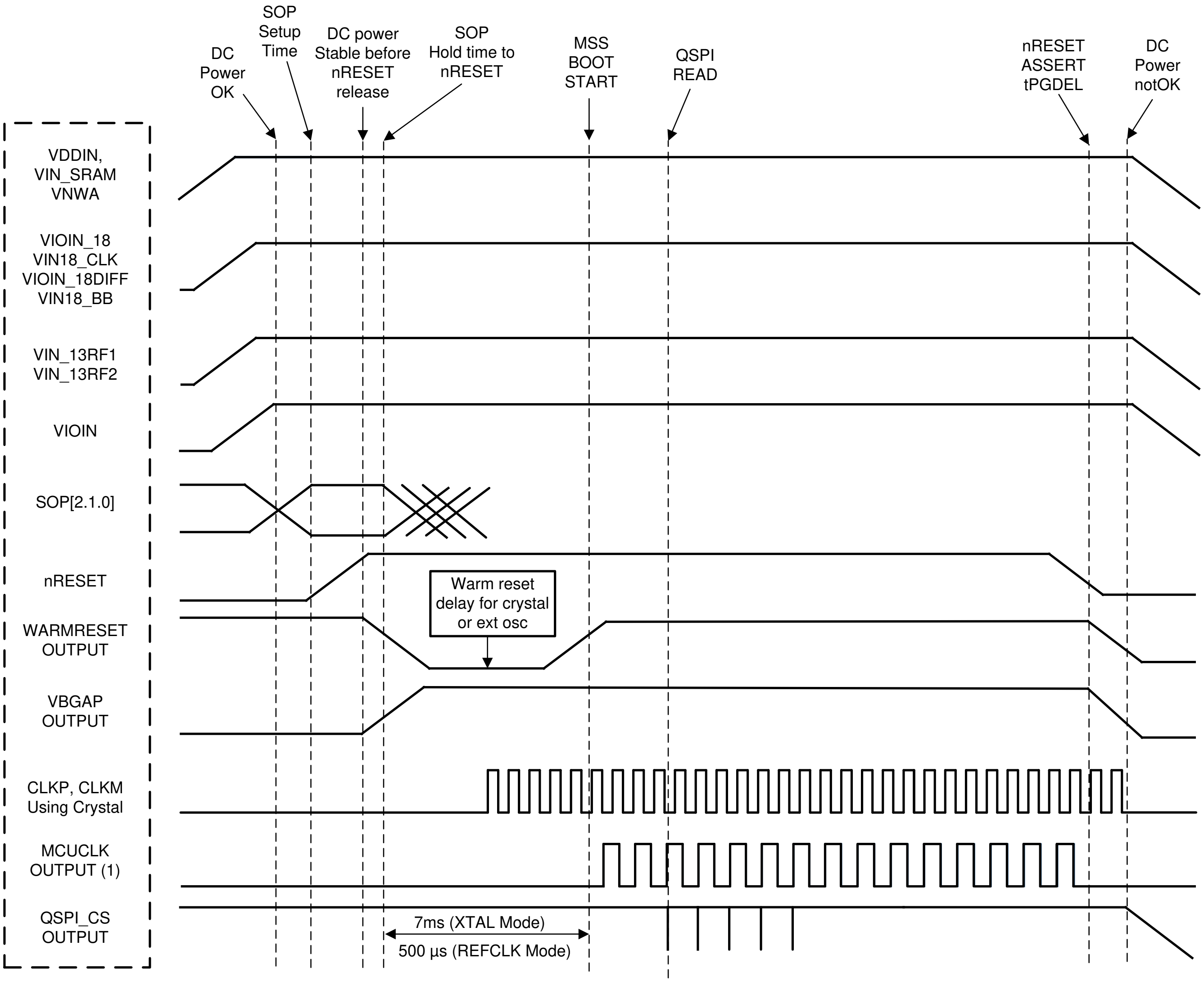
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(4) Air flow = 1 m/s

8.9 Timing and Switching Characteristics

8.9.1 Power Supply Sequencing and Reset Timing

The AWR1443 device expects all external voltage rails to be stable before reset is deasserted. Figure 8-2 describes the device wake-up sequence.



A. MCU_CLK_OUT in autonomous mode, where AWR1443 application is booted from the serial flash, MCU_CLK_OUT is not enabled by default by the device bootloader.

Figure 8-2. Device Wake-up Sequence

8.9.2 Synchronized Frame Triggering

The AWR1443 device supports a hardware based mechanism to trigger radar frames. An external host can pulse the SYNC_IN signal to start radar frames. The typical time difference between the rising edge of the external pulse and the frame transmission on air (Tlag) is about 160 ns. There is also an additional programmable delay that the user can set to control the frame start time.

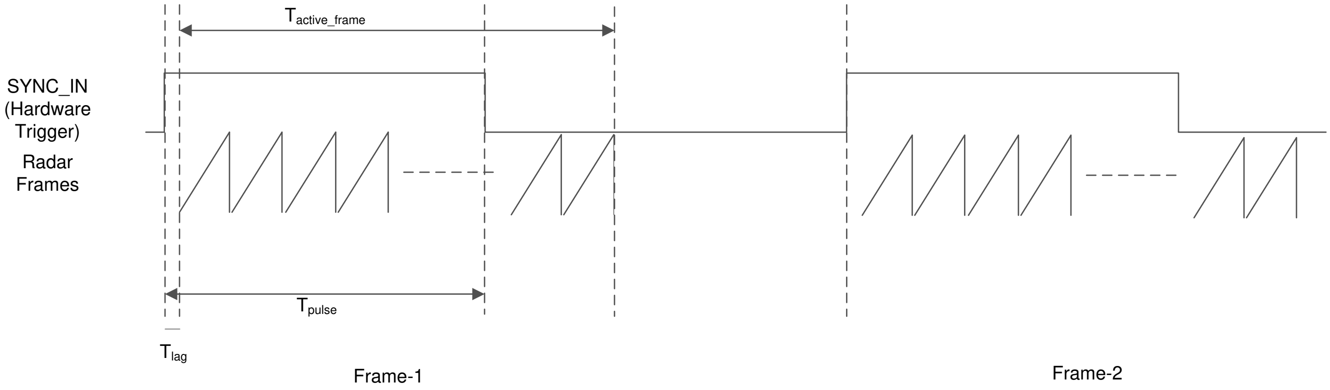


Figure 8-3. Sync In Hardware Trigger

Table 8-5. Frame Trigger Timing

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T_{active_frame}	Active frame duration	User defined		ns
T_{pulse}		25	4000	

8.9.3 Input Clocks and Oscillators

8.9.3.1 Clock Specifications

An external crystal is connected to the device pins. Figure 8-4 shows the crystal implementation.

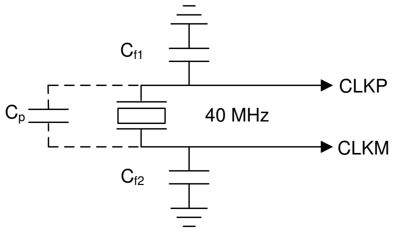


Figure 8-4. Crystal Implementation

Note

The load capacitors, C_{f1} and C_{f2} in Figure 8-4, should be chosen such that Equation 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.Note that Cf1 and Cf2 include the parasitic capacitances due to PCB routing.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \qquad (1)$$

Table 8-6 lists the electrical characteristics of the clock crystal.

Table 8-6. Crystal Electrical Characteristics (Oscillator Mode)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_P	Parallel resonance crystal frequency		40		MHz
C_L	Crystal load capacitance	5	8	12	pF
ESR	Crystal ESR			50	Ω
Temperature range	Expected temperature range of operation	–40		125	°C
Frequency tolerance	Crystal frequency tolerance(1) (2)	–200		200	ppm
Drive level			50	200	µW

(1) The crystal manufacturer's specification must satisfy this requirement.
(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40-MHz clock is fed externally. Table 8-7 lists the electrical characteristics of the external clock signal.

Table 8-7. External Clock Mode Specifications

PARAMETER		SPECIFICATION			UNIT
		MIN	TYP	MAX	
Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 40 MHz	Frequency		40		MHz
	AC-Amplitude	700		1200	mV (pp)
	DC-$t_{rise/fall}$			10	ns
	Phase Noise at 1 kHz			–132	dBc/Hz
	Phase Noise at 10 kHz			–143	dBc/Hz
	Phase Noise at 100 kHz			–152	dBc/Hz
	Phase Noise at 1 MHz			–153	dBc/Hz
	Duty Cycle	35		65	%
	Freq Tolerance	–100		100	ppm

8.9.4 Multibuffered / Standard Serial Peripheral Interface (MibSPI)

8.9.4.1 Peripheral Description

The SPI uses a MibSPI Protocol by TI.

The MibSPI/SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The MibSPI/SPI is normally used for communication between the microcontroller and external peripherals or another microcontroller.

Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 8-bit baud clock generator
- SPICLK can be internally-generated (controller mode) or received from an external clock source (peripheral mode)
- Each word transferred can have a unique format.
- SPI I/Os not used in the communication can be used as digital input/output signals

8.9.4.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 256 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each.

Section 8.9.4.2.2 and Section 8.9.4.2.3 assume the operating conditions stated in Section 8.9.4.2.1.

8.9.4.2.1 SPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

8.9.4.2.2 SPI Controller Mode Switching Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1) (2) (3)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)	25		$256_{tc(VCLK)}$	ns
2(4)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} – 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} – 4$		$0.5t_{c(SPC)M} + 4$	
3(4)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} – 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} – 4$		$0.5t_{c(SPC)M} + 4$	
4(4)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)	$0.5t_{c(SPC)M} – 3$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)	$0.5t_{c(SPC)M} – 3$			
5(4)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)	$0.5t_{c(SPC)M} – 10.5$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)	$0.5t_{c(SPC)M} – 10.5$			

NO.	PARAMETER			MIN	TYP	MAX	UNIT
6(5)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	(C2TDELAY+2)* $t_{c(VCLK)}$ – 7.5		(C2TDELAY+2) * $t_{c(VCLK)}$ + 7	ns
			CSHOLD = 1	(C2TDELAY +3) * $t_{c(VCLK)}$ – 7.5		(C2TDELAY+3) * $t_{c(VCLK)}$ + 7	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	(C2TDELAY+2)* $t_{c(VCLK)}$ – 7.5		(C2TDELAY+2) * $t_{c(VCLK)}$ + 7	
			CSHOLD = 1	(C2TDELAY +3) * $t_{c(VCLK)}$ – 7.5		(C2TDELAY+3) * $t_{c(VCLK)}$ + 7	
7(5)	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) *$t_{c(VCLK)}$ – 7		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)}$ + 7.5	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) *$t_{c(VCLK)}$ – 7		0.5*$t_{c(SPC)M}$ + (T2CDELAY + 1) * $t_{c(VCLK)}$ + 7.5	
8(4)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		5			
9(4)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		3			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		3			

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared (where x= 0 or 1).
(2) $t_{c(MSS\_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Controller mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS +1) t_{c(MSS\_VCLK)} \geq$ 25ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2 t_{c(MSS\_VCLK)} \geq$ 25ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

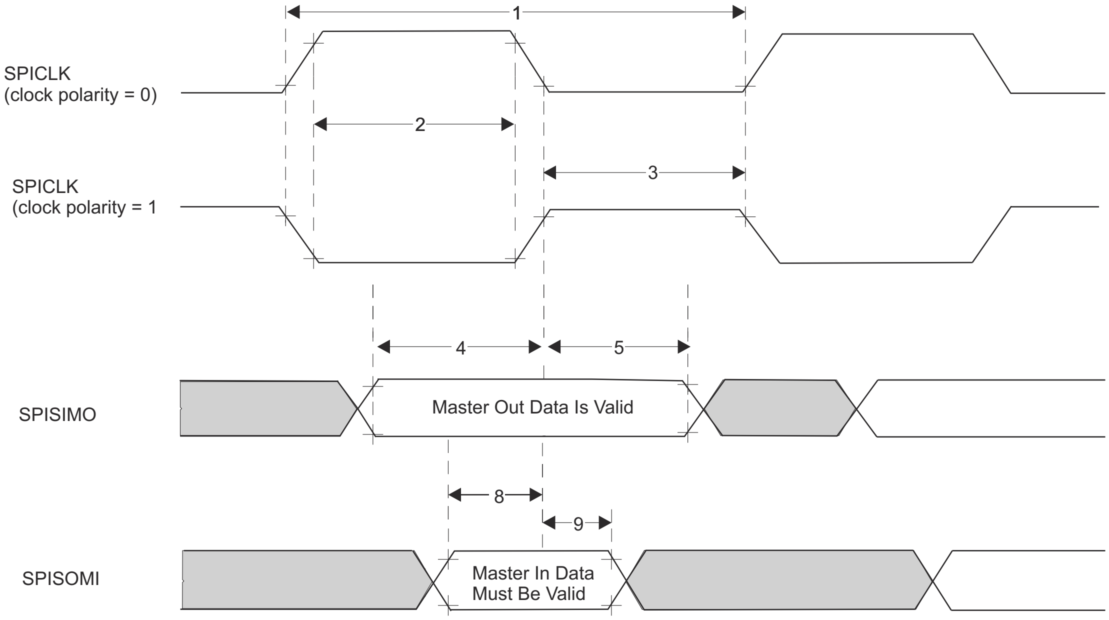


Figure 8-5. SPI Controller Mode External Timing (CLOCK PHASE = 0)

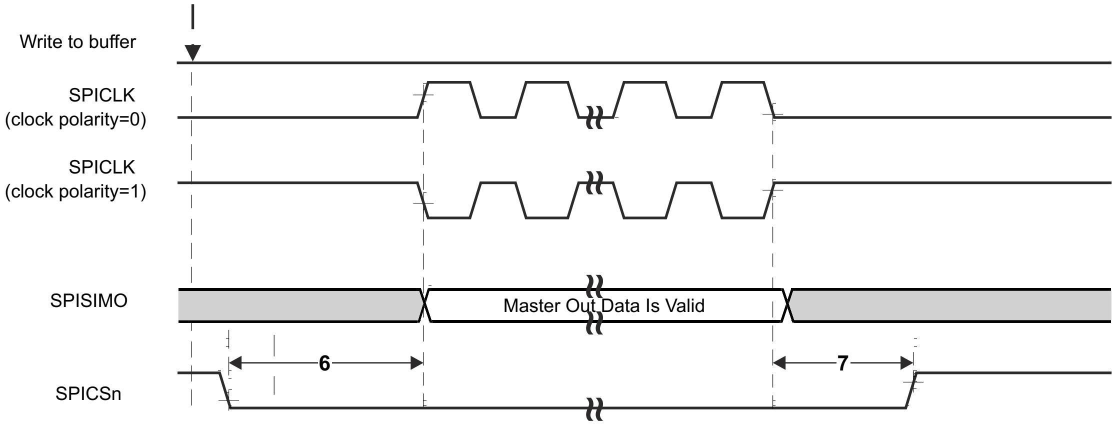


Figure 8-6. SPI Controller Mode Chip Select Timing (CLOCK PHASE = 0)

8.9.4.2.3 SPI Controller Mode Switching Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1) (2) (3)

NO.	PARAMETER			MIN	TYP	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)		25		$256t_{c(VCLK)}$	ns
2(4)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} – 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} – 4$		$0.5t_{c(SPC)M} + 4$	
3(4)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} – 4$		$0.5t_{c(SPC)M} + 4$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} – 4$		$0.5t_{c(SPC)M} + 4$	
4(4)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} – 3$			ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} – 3$			
5(4)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low, (clock polarity = 0)		$0.5t_{c(SPC)M} – 10.5$			ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high, (clock polarity = 1)		$0.5t_{c(SPC)M} – 10.5$			
6(5)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} – 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY + 2)*t_{c(VCLK)} – 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2)*t_{c(VCLK)} – 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} + 7.5$	
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3)*t_{c(VCLK)} – 7$		$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} + 7.5$	
7(5)	$t_{T2CDELAY}$	Hold time, SPICLK low until CS inactive (clock polarity = 0)		$(T2CDELAY + 1) *t_{c(VCLK)} – 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	ns
		Hold time, SPICLK high until CS inactive (clock polarity = 1)		$(T2CDELAY + 1) *t_{c(VCLK)} – 7.5$		$(T2CDELAY + 1) *t_{c(VCLK)} + 7$	

NO.	PARAMETER		MIN	TYP	MAX	UNIT
8(4)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	5			ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	5			
9(4)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	3			ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	3			

(1) The MASTER bit (SPIGCRx.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set (where x = 0 or 1).
(2) $t_{c(MSS\_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(3) When the SPI is in Controller mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS + 1)t_{c(MSS\_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits. For PS values of 0: $t_{c(SPC)M} = 2t_{c(MSS\_VCLK)} \geq 25$ ns.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(5) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

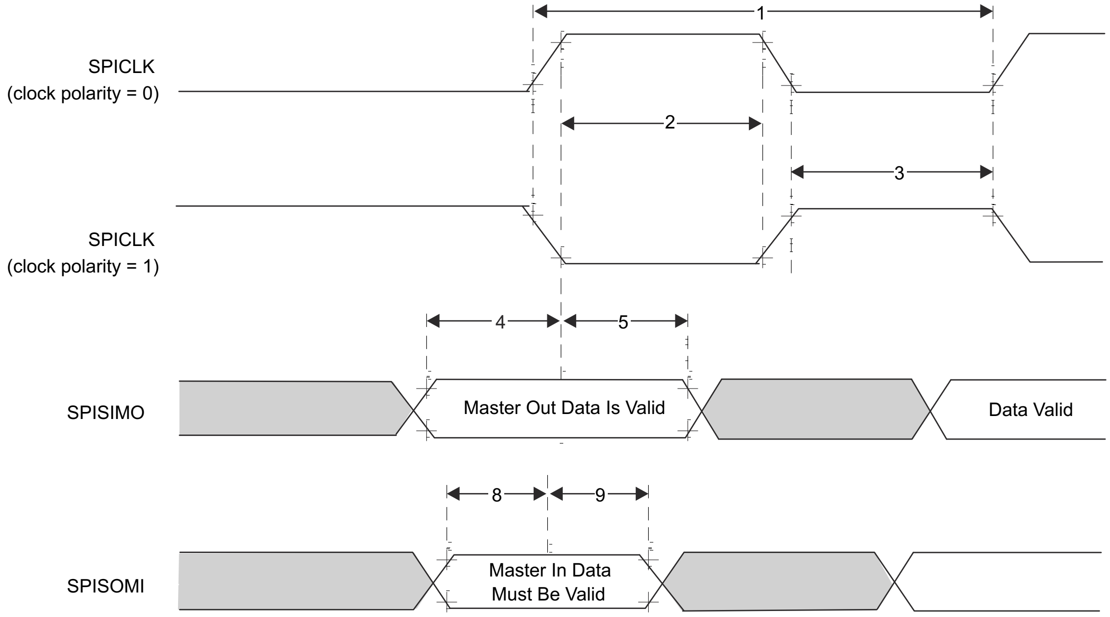


Figure 8-7. SPI Controller Mode External Timing (CLOCK PHASE = 1)

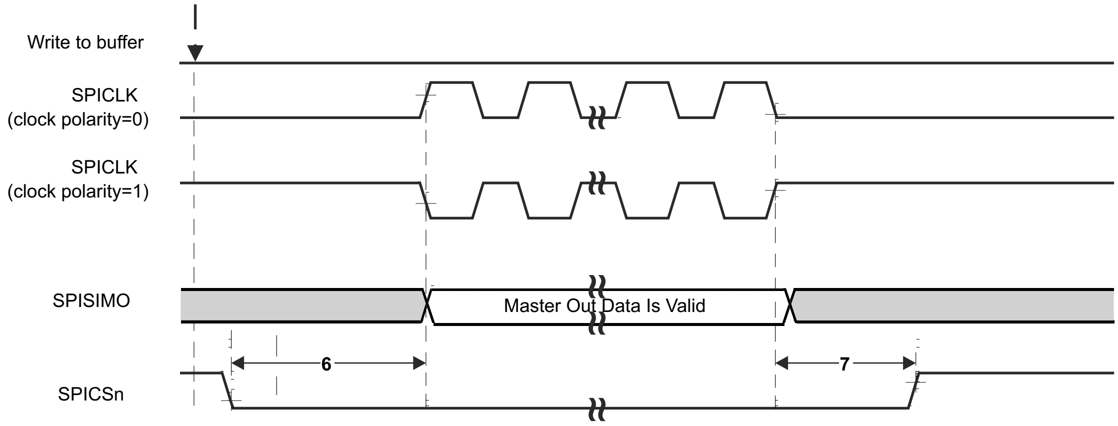


Figure 8-8. SPI Controller Mode Chip Select Timing (CLOCK PHASE = 1)

8.9.4.3 SPI Peripheral Mode I/O Timings

8.9.4.3.1 SPI Peripheral Mode Switching Parameters (SPICLK = input, SPISIMO = input, and SPISOMI = output)(1) (2) (3)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPICLK(4)	25			ns
2(5)	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	10			ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	10			
3(5)	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	10			ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	10			
4(5)	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)			10	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)			10	
5(5)	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	2			
4(5)	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)			10	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)			10	
5(5)	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	2			ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	2			
6(5)	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	3			ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	3			
7(5)	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0; clock phase = 0) OR (clock polarity = 1; clock phase = 1)	1			ns
	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK high (clock polarity = 1; clock phase = 0) OR (clock polarity = 0; clock phase = 1)	1			

(1) The MASTER bit (SPIGCRx.0) is cleared (where x = 0 or 1).
(2) The CLOCK PHASE bit (SPIFMTx.16) is either cleared or set for CLOCK PHASE = 0 or CLOCK PHASE = 1 respectively.
(3) $t_{c(MSS\_VCLK)}$ = main subsystem clock time = 1 / $f_{(MSS\_VCLK)}$. For more details, see the Technical Reference Manual.
(4) When the SPI is in peripheral mode, the following must be true: For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS+1)t_{c(MSS\_VCLK)} \geq 25$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.For PS values of 0: $t_{c(SPC)S} = 2t_{c(MSS\_VCLK)} \geq 25$ ns.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

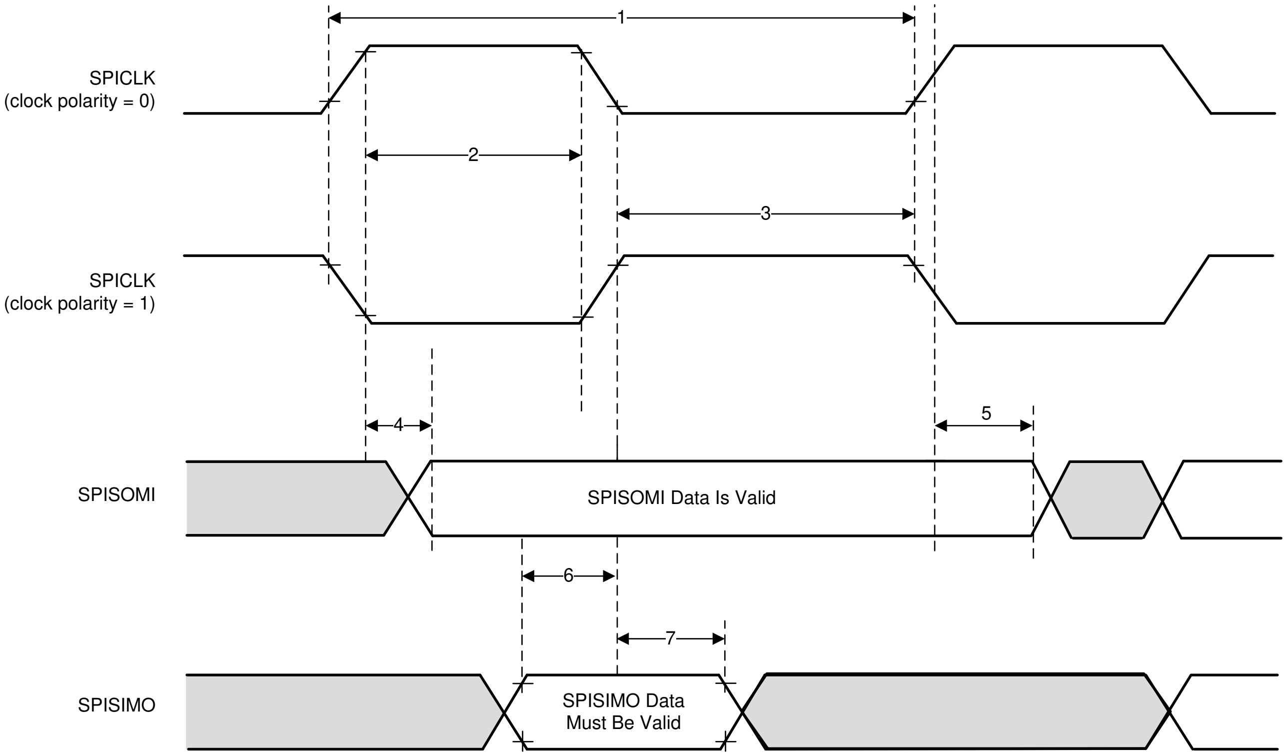


Figure 8-9. SPI peripheral Mode External Timing (CLOCK PHASE = 0)

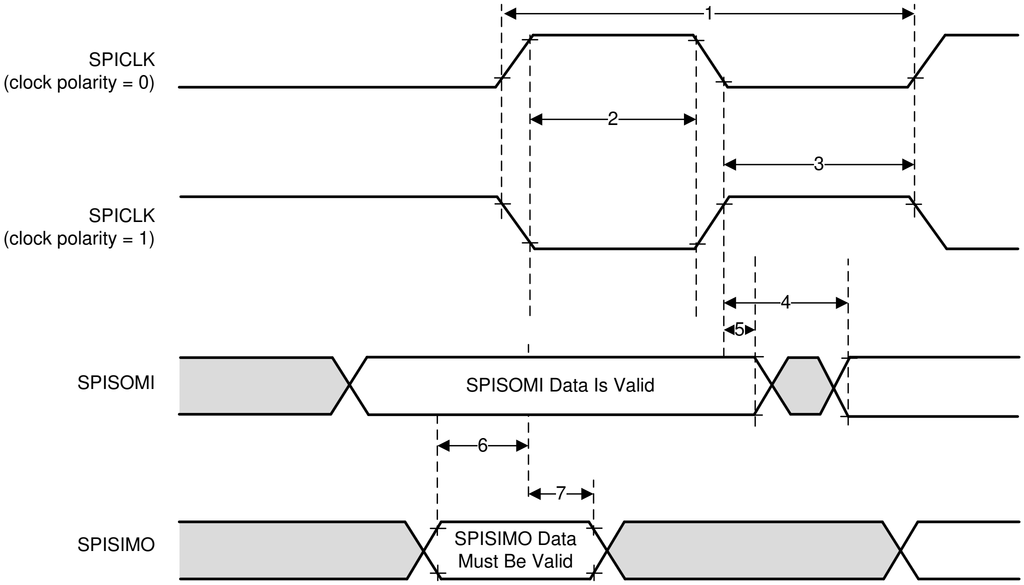


Figure 8-10. SPI peripheral Mode External Timing (CLOCK PHASE = 1)

8.9.4.4 Typical Interface Protocol Diagram (Peripheral Mode)

1. Host should ensure that there is a delay of two SPI clocks between CS going low and start of SPI clock.
2. Host should ensure that CS is toggled for every 16 bits of transfer through SPI.

Figure 8-11 shows the SPI communication timing of the typical interface protocol.

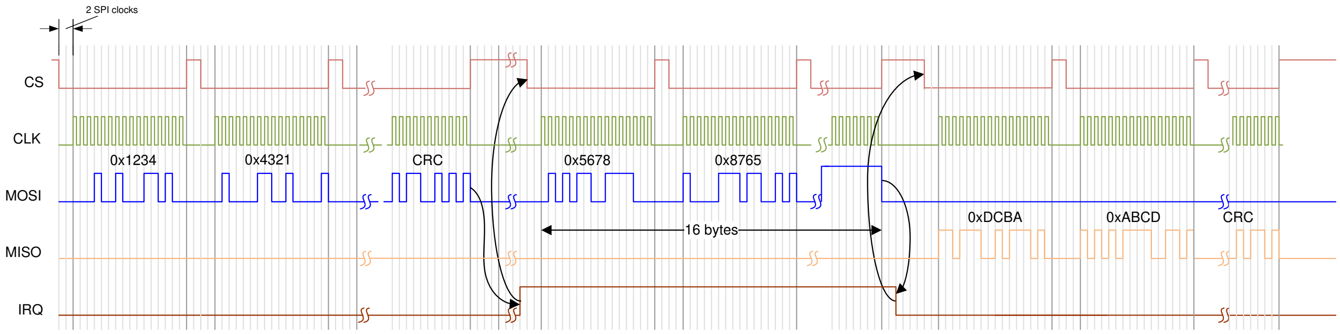


Figure 8-11. SPI Communication

8.9.5 LVDS Interface Configuration

The AWR1443 supports seven differential LVDS IOs/Lanes. The lane configuration supported is four Data lanes (LVDS_TXP/M), one Bit Clock lane (LVDS_CLKP/M) and one Frame clock lane (LVDS_FRCLKP/M), and one HS_DEBUG LVDS pair. The LVDS interface is used for debugging. The LVDS interface supports the following data rates:

- 900 Mbps (450 MHz DDR Clock)
- 600 Mbps (300 MHz DDR Clock)
- 450 Mbps (225 MHz DDR Clock)
- 400 Mbps (200 MHz DDR Clock)
- 300 Mbps (150 MHz DDR Clock)
- 225 Mbps (112.5 MHz DDR Clock)
- 150 Mbps (75 MHz DDR Clock)

Note that the bit clock is in DDR format and hence the numbers of toggles in the clock is equivalent to data.

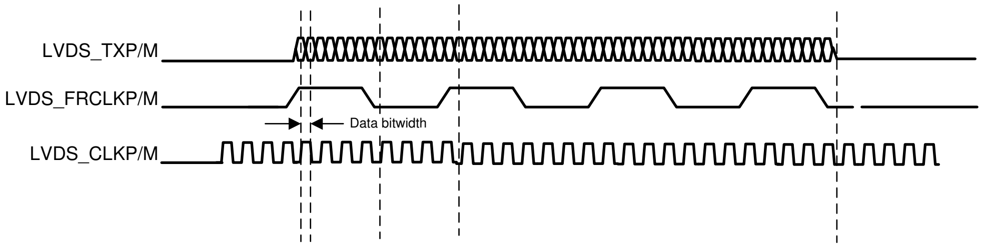


Figure 8-12. LVDS Interface Lane Configuration And Relative Timings

8.9.5.1 LVDS Interface Timings

Table 8-8. LVDS Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty Cycle Requirements	max 1 pF lumped capacitive load on LVDS lanes	48%		52%	
Output Differential Voltage	peak-to-peak single-ended with 100 Ω resistive load between differential pairs	250		450	mV
Output Offset Voltage		1125		1275	mV
Trise and Tfall	20%-80%, 900 Mbps		330		ps
Jitter (pk-pk)	900 Mbps		80		ps

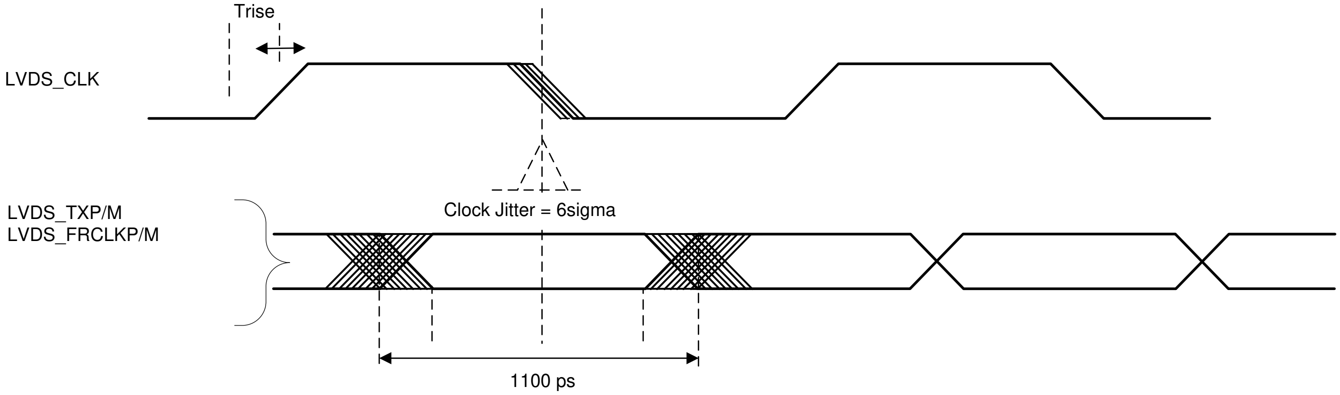


Figure 8-13. Timing Parameters

8.9.6 General-Purpose Input/Output

Section 8.9.6.1 lists the switching characteristics of output timing relative to load capacitance.

8.9.6.1 Switching Characteristics for Output Timing versus Load Capacitance (C_L)

PARAMETER[1] [2]		TEST CONDITIONS		VIOIN = 1.8V	VIOIN = 3.3V	UNIT
t_r	Max rise time	Slew control = 0	C_L = 20 pF	2.8	3.0	ns
			C_L = 50 pF	6.4	6.9	
			C_L = 75 pF	9.4	10.2	
t_f	Max fall time		C_L = 20 pF	2.8	2.8	ns
			C_L = 50 pF	6.4	6.6	
			C_L = 75 pF	9.4	9.8	
t_r	Max rise time	Slew control = 1	C_L = 20 pF	3.3	3.3	ns
			C_L = 50 pF	6.7	7.2	
			C_L = 75 pF	9.6	10.5	
t_f	Max fall time		C_L = 20 pF	3.1	3.1	ns
			C_L = 50 pF	6.6	6.6	
			C_L = 75 pF	9.6	9.6	

(1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

8.9.7 Controller Area Network Interface (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multi-commander communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 Mbps. The DCAN is ideal for applications operating in noisy and harsh environments that require reliable serial communication or multiplexed wiring.

The DCAN has the following features:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 Mbps
- Configurable Message objects
- Individual identifier masks for each message object
- Programmable FIFO mode for message objects
- Suspend mode for debug support
- Programmable loop-back modes for self-test operation
- Direct access to Message RAM in test mode
- Supports two interrupt lines - Level 0 and Level 1
- Automatic Message RAM initialization

8.9.7.1 Dynamic Characteristics for the DCANx TX and RX Pins

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(CAN\_tx)}$	Delay time, transmit shift register to CAN_tx pin(1)			15	ns
$t_{d(CAN\_rx)}$	Delay time, CAN_rx pin to receive shift register(1)			10	ns

(1) These values do not include rise/fall times of the output buffer.

8.9.8 Serial Communication Interface (SCI)

The SCI has the following features:

- Standard universal asynchronous receiver-transmitter (UART) communication
- Standard non-return to zero (NRZ) format
- Double-buffered receive and transmit functions
- Asynchronous or iso-synchronous communication modes with no CLK pin
- Capability to use Direct Memory Access (DMA) for transmit and receive data
- Two external pins: RS232_RX and RS232_TX

8.9.8.1 SCI Timing Requirements

		MIN	TYP	MAX	UNIT
f(baud)	Supported baud rate at 20 pF		921.6		kHz

8.9.9 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multicontroller communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I^{2}C-bus™. This module will support any target or controller I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multi-controller transmitter/ target receiver mode
  - Multi-controller receiver/ target transmitter mode
  - Combined controller transmit/receive and receive/transmit mode
  - Transfer rates of 100 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

Note

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the target address second byte every time it sends the target address first byte)

8.9.9.1 I2C Timing Requirements(1)

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCL)}$	Cycle time, SCL	10		2.5		μs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		μs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4		0.6		μs
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		μs
$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		μs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		100		μs
$t_{h(SCLL-SDA)}$	Hold time, SDA valid after SCL low	0	3.45(1)	0	0.9	μs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		μs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4		0.6		μs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
C_b (2) (3)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

(2) The maximum th(SDA-SCLL) for I2C bus devices has only to be met if the device does not stretch the low period (tw(SCLL)) of the SCL signal.

(3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

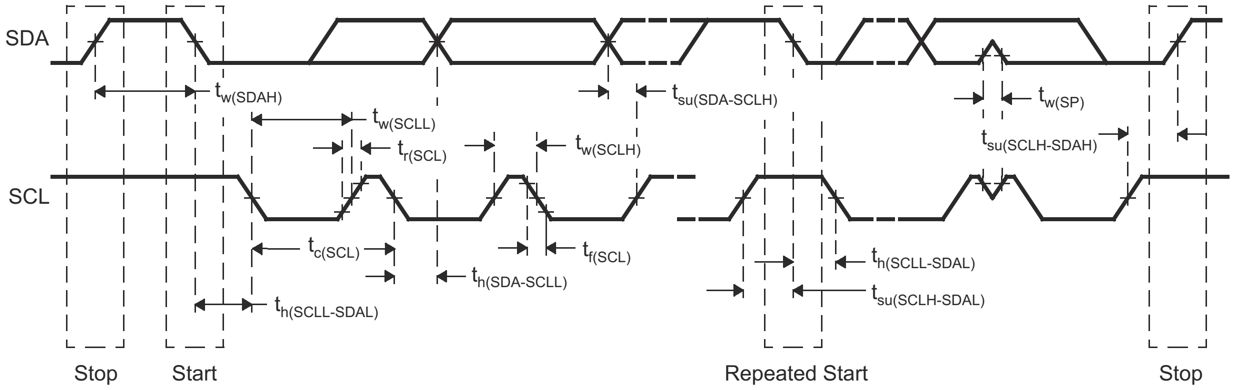


Figure 8-14. I2C Timing Diagram

Note

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum th(SDA-SCLL) has only to be met if the device does not stretch the LOW period (tw(SCLL)) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.

8.9.10 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a controller only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Support for 3-, 4-, or 6-pin SPI interface
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

Section 8.9.10.2 and Section 8.9.10.3 assume the operating conditions stated in Section 8.9.10.1.

8.9.10.1 QSPI Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

8.9.10.2 Timing Requirements for QSPI Input (Read) Timings(1) (2)

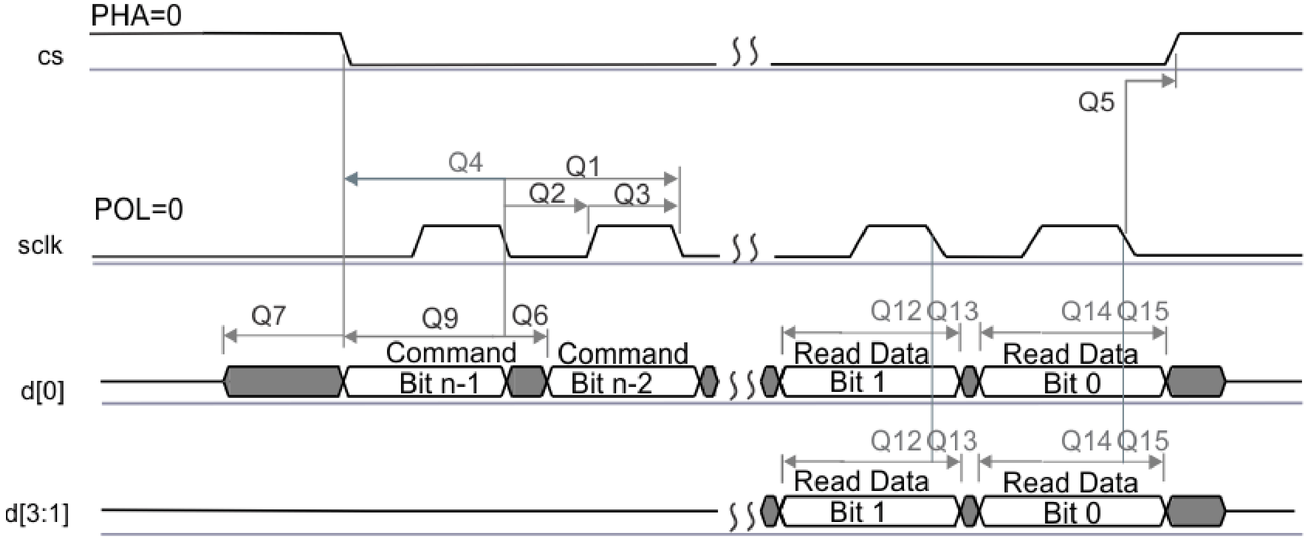
		MIN	TYP	MAX	UNIT
$t_{su(D-SCLK)}$	Setup time, d[3:0] valid before falling sclk edge (Q12)	7.3			ns
$t_{h(SCLK-D)}$	Hold time, d[3:0] valid after falling sclk edge (Q13)	1.5			ns
$t_{su(D-SCLK)}$	Setup time, final d[3:0] bit valid before final falling sclk edge	7.3 – P(3)			ns
$t_{h(SCLK-D)}$	Hold time, final d[3:0] bit valid after final falling sclk edge	1.5 + P(3)			ns

(1) Clock Mode 0 (clk polarity = 0 ; clk phase = 0) is the mode of operation.
(2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
(3) P = SCLK period in ns.

8.9.10.3 QSPI Switching Characteristics

NO.	PARAMETER		MIN	TYP	MAX	UNIT
Q1	$t_{c(SCLK)}$	Cycle time, sclk	25			ns
Q2	$t_{w(SCLKL)}$	Pulse duration, sclk low	0.5*P – 3(1)			ns
Q3	$t_{w(SCLKH)}$	Pulse duration, sclk high	0.5*P – 3			ns
Q4	$t_{d(CS-SCLK)}$	Delay time, sclk falling edge to cs active edge	–M*P – 1(2)		–M*P + 2.5(2)	ns
Q5	$t_{d(SCLK-CS)}$	Delay time, sclk falling edge to cs inactive edge	N*P – 1(2)		N*P + 2.5(2)	ns
Q6	$t_{d(SCLK-D1)}$	Delay time, sclk falling edge to d[0] transition	–3.5		7	ns
Q7	$t_{ena(CS-D1LZ)}$	Enable time, cs active edge to d[0] driven (lo-z)	–P – 4(2)		–P +1(2)	ns
Q8	$t_{dis(CS-D1Z)}$	Disable time, cs active edge to d[0] tri-stated (hi-z)	–P – 4(2)		–P +1(2)	ns
Q9	$t_{d(SCLK-D1)}$	Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only)	–3.5 – P(2)		7 – P(2)	ns

(1) P = SCLK period in ns.
(2) M = QSPI_SPI_DC_REG.DDx + 1, N = 2



SPRS85v TIMING QSPI1 02

Figure 8-15. QSPI Read (Clock Mode 0)

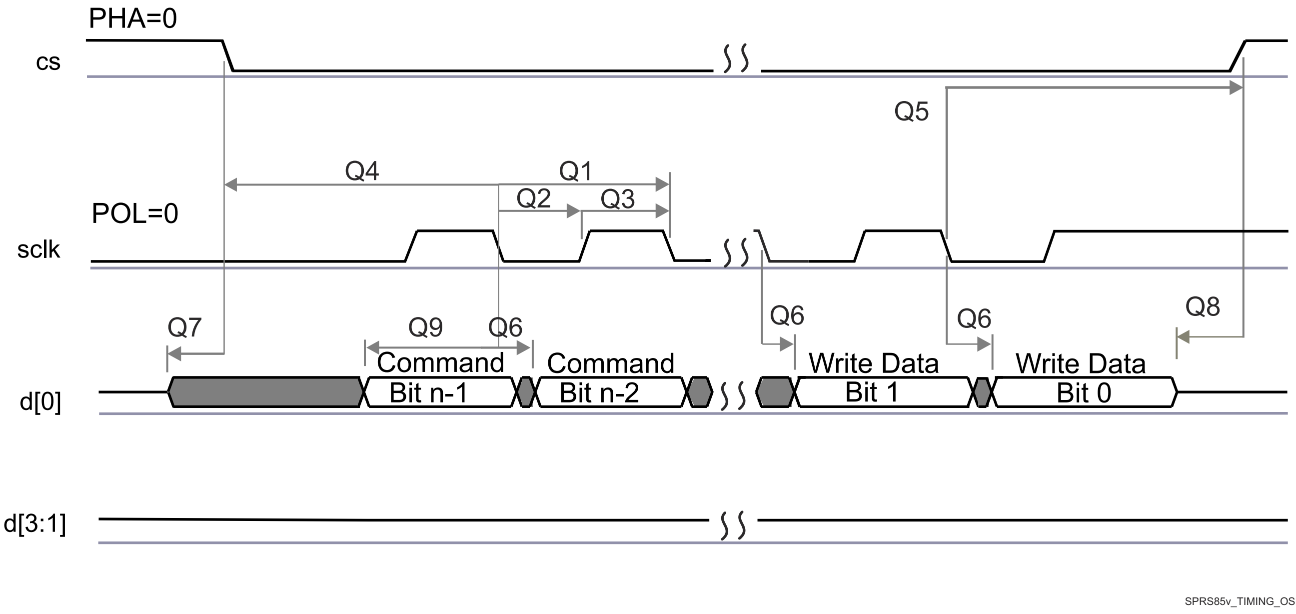


Figure 8-16. QSPI Write (Clock Mode 0)

8.9.11 JTAG Interface

Section 8.9.11.2 and Section 8.9.11.3 assume the operating conditions stated in Section 8.9.11.1.

8.9.11.1 JTAG Timing Conditions

		MIN	TYP	MAX	UNIT
Input Conditions					
t_R	Input rise time	1		3	ns
t_F	Input fall time	1		3	ns
Output Conditions					
C_{LOAD}	Output load capacitance	2		15	pF

8.9.11.2 Timing Requirements for IEEE 1149.1 JTAG

NO.			MIN	TYP	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time TCK	66.66			ns
1a	$t_{w(TCKH)}$	Pulse duration TCK high (40% of tc)	26.67			ns
1b	$t_{w(TCKL)}$	Pulse duration TCK low(40% of tc)	26.67			ns
3	$t_{su(TDI-TCK)}$	Input setup time TDI valid to TCK high	2.5			ns
	$t_{su(TMS-TCK)}$	Input setup time TMS valid to TCK high	2.5			ns
4	$t_{h(TCK-TDI)}$	Input hold time TDI valid from TCK high	18			ns
	$t_{h(TCK-TMS)}$	Input hold time TMS valid from TCK high	18			ns

8.9.11.3 Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

NO.	PARAMETER		MIN	TYP	MAX	UNIT
2	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0		25	ns

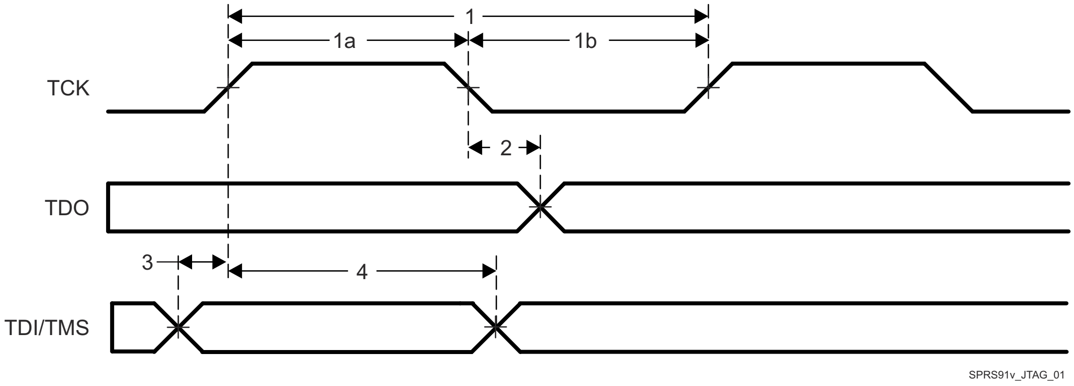


Figure 8-17. JTAG Timing

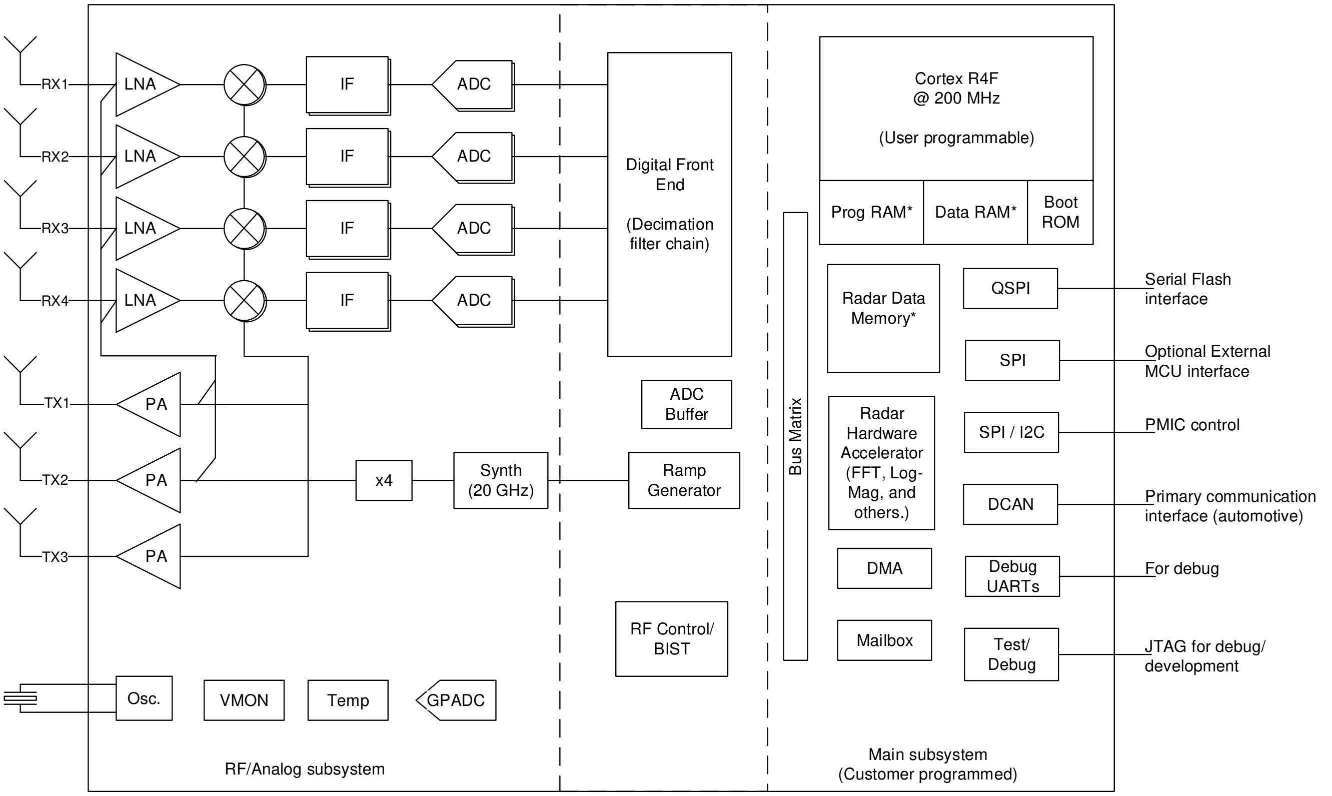
9 Detailed Description

9.1 Overview

The AWR1443 device includes the entire millimeter wave blocks and analog baseband signal chain for three transmitters (two usable at the same instance) and four receivers, as well as a customer-programmable MCU with a hardware accelerator for radar signal processing. This device is applicable as a radar-on-a-chip in use-cases with modest requirements for memory, processing capacity and application code size. These could be cost-sensitive automotive applications that are evolving from 24 GHz narrowband implementation and some emerging simple ultra-short-range radar applications. Typical application examples for this device include basic Blind Spot Detect, Parking Assist, and so forth.

In terms of scalability, the AWR1443 device could be paired with a low-end external MCU, to address more complex applications that might require additional memory for larger application software footprint and faster interfaces. Because the AWR1443 device also provides high speed data interfaces, it is suitable for interfacing with more capable external processing blocks. Here system designers can choose the AWR1443 to provide raw ADC data or use the on-chip Hardware Accelerator for partial processing viz. first stage Fast Fourier Transform.

9.2 Functional Block Diagram



* Total RAM available in Main subsystem is 576KB (for Cortex-R4F Program RAM, Data RAM, and Radar Data Memory)

Figure 9-1. Functional Block Diagram

9.3 External Interfaces

The AWR1443 device provides the following external interfaces:

- Reference Clock – Reference clock available for Host Processor after device wakeup.
- Low speed control information
  - Up to two 4-line standard SPI interface
  - One I^2C interface (Pin multiplexed with one of the SPI ports)
- One Controller Area Network (CAN) Port for Automotive Interfacing
- Reset – Active Low reset for device wakeup from host General Purpose IOs
- Error Signaling – Used for notifying the host in case the Radio Controller detects a fault

The AWR1443 device comprises of three main blocks – Radar (or the Millimeter Wave) System, Main (or the Control) System and Processing System.

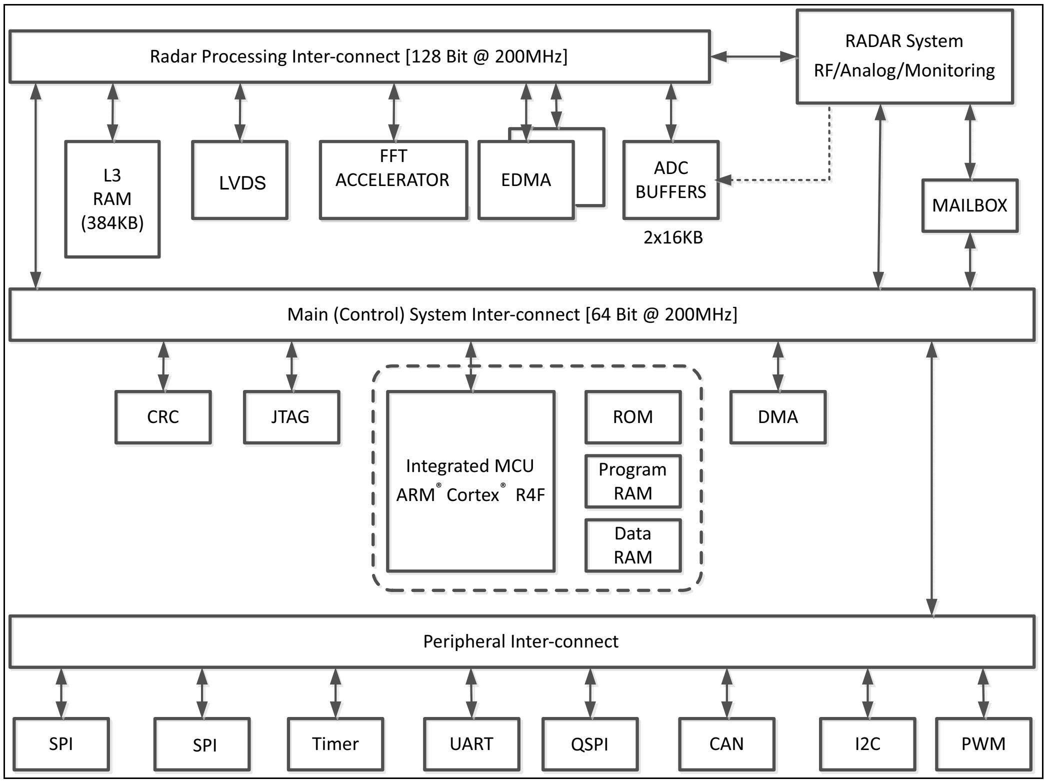


Figure 9-2. System Interconnect

9.4 Subsystems

9.4.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. The three transmit channels can be operated up to a maximum of two at a time (simultaneously) for transmit beamforming purpose as required; whereas the four receive channels can all be operated simultaneously.

9.4.1.1 Clock Subsystem

The AWR1443 clock subsystem generates 76 to 81 GHz from an input reference of 40-MHz crystal. It has a built-in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X4 multiplier to create the required frequency in the 76 to 81 GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for effective sensor operation.

The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Figure 9-3 describes the clock subsystem.

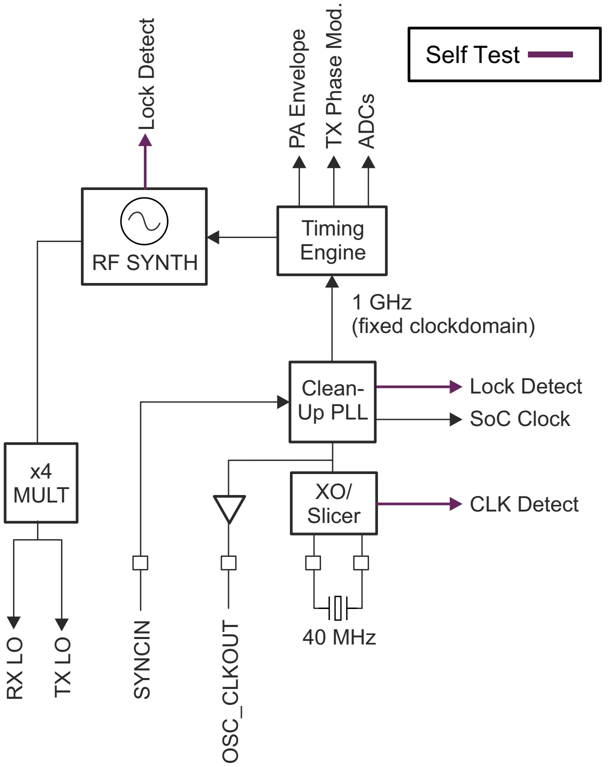


Figure 9-3. Clock Subsystem

9.4.1.2 Transmit Subsystem

The AWR1443 transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. A maximum of 2 transmit chains can be operational at the same time. However all 3 chains can be operated together in a time multiplexed fashion. The device supports binary phase modulation for MIMO radar and interference mitigation.

Each transmit chain can deliver a maximum of 12 dBm at the antenna port on the PCB. The transmit chains also support programmable backoff for system optimization.

Figure 9-4 describes the transmit subsystem.

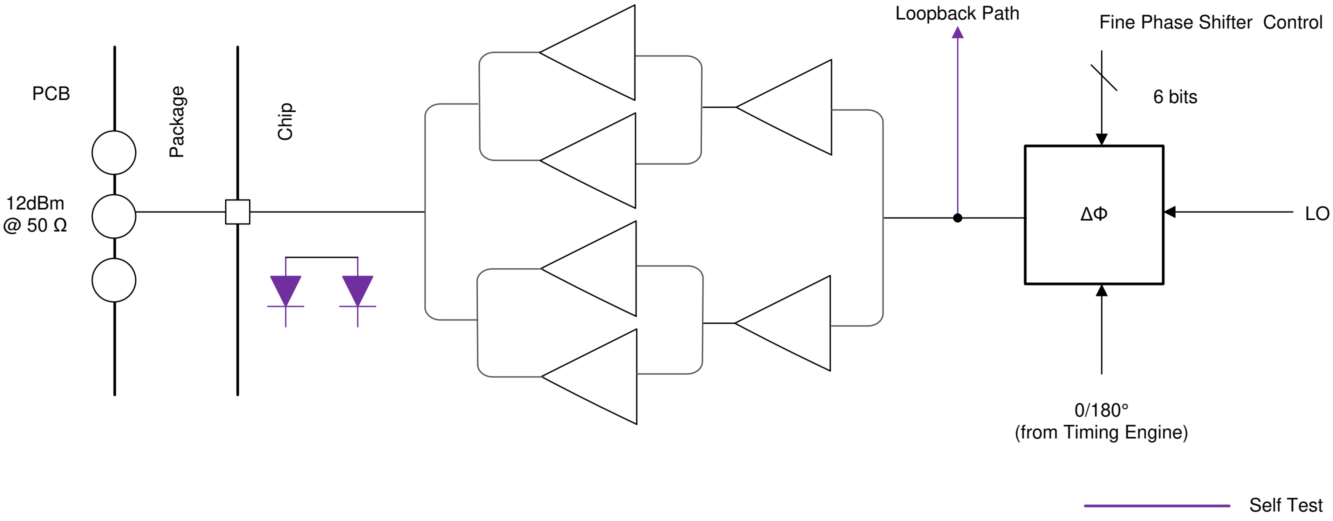


Figure 9-4. Transmit Subsystem (Per Channel)

9.4.1.3 Receive Subsystem

The AWR1443 receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, ADC conversion, and decimation. All four receive channels can be operational at the same time an individual power-down option is also available for system optimization.

Unlike conventional real-only receivers, the AWR1443 device supports a complex baseband architecture, which uses quadrature mixer and dual IF and ADC chains to provide complex I and Q outputs for each receiver channel. The AWR1443 is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175 kHz and can support bandwidths up to 5 MHz.

Figure 9-5 describes the receive subsystem.

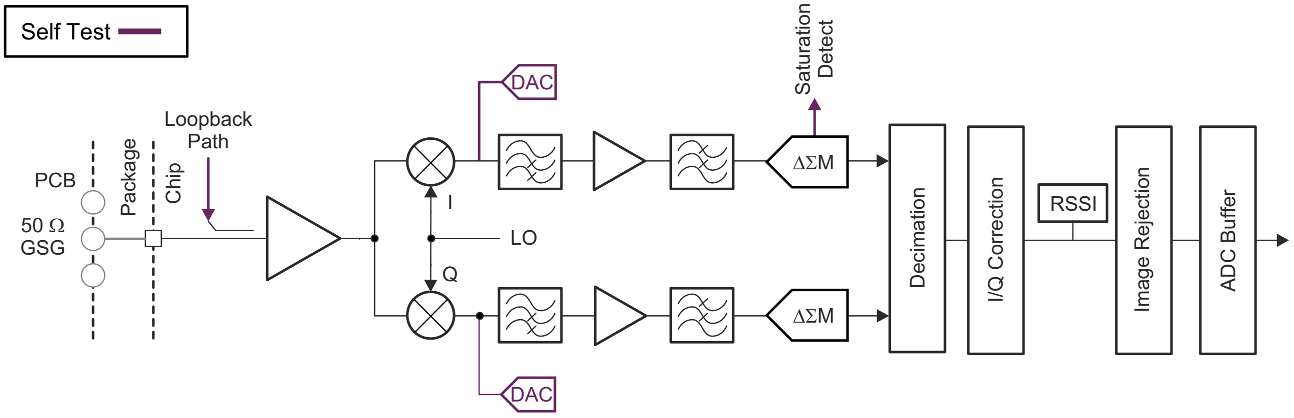


Figure 9-5. Receive Subsystem (Per Channel)

9.4.1.4 Radio Processor Subsystem

The Radio Processor subsystem (also referred to as BIST Subsystem in this document) includes the digital front-end, the ramp generator and an internal processor for control / configuration of the low-level RF/analog and ramp generator registers. The Radar Processor also schedules periodic monitoring tasks. User applications, running on

Master (Control) System, do not have direct access to Radar System; access is based on well-defined API messages (over a hardware channel) from the master subsystem.

Note

This radio processor is programmed by TI and takes care of RF calibration and self-test/monitoring functions (BIST). This processor is not available directly for customer use/application.

The digital front-end takes care of filtering and decimating the raw sigma-delta ADC output and provides the final ADC data samples at a programmable sampling rate.

9.4.2 Main (Control) System

The Main (Control) System includes ARM's automotive grade Cortex-R4F processor clocked at 200 MHz, which is user programmable. User applications executing on this processor control the overall operation of the device, including Radar Control via well-defined API messages, radar signal processing (assisted by the radar hardware accelerator) and peripherals for external interface.

The Main (Control) System plays a big role in enabling autonomous operation of AWR1443 as a radar-on-a-chip sensor. The device includes a quad serial peripheral interface (QSPI) which can be used to download customer code directly from a serial flash. A (classic) CAN interface is included that can be used to communicate directly from the device to a CAN bus. An SPI/I2C interface is available for power management IC (PMIC) control when the AWR1443 is used as an autonomous sensor.

For more complex applications, the device can operate under the control of an external MCU, which can communicate with AWR1443 device over an SPI interface. In this case, it is possible to use the AWR14xx as a radar sensor, providing raw detected objects to the external MCU. External MCU could reduce the application code complexity residing in the device and makes more memory available for radar data cube inside the AWR1443. This configuration also eliminates the need for a separate serial flash to be connected to the AWR1443.

Furthermore, the external MCU can provide faster interfaces, such as CAN-FD or Ethernet, for the radar sensor to connect to a central processing unit (CPU). In such a distributed configuration, multiple AWR1443 devices mounted around the vehicle can connect to the CPU, providing a surround view. The external MCU itself is low-cost, because the low-level radar signal processing is accomplished inside the AWR1443, using the hardware accelerator, while the higher-layer intelligence and complex algorithms reside in the common CPU, making the overall solution cost-effective.

Note that although four interfaces – one CAN, one I2C and two SPI interfaces – are present in the AWR1443 device for external communication and PMIC control, only two of these interfaces are usable at any point in time.

The total memory (RAM) available in the Main subsystem is 576 KB. This is partitioned between the R4F program RAM, R4F data RAM and radar data memory. The maximum usable size for R4F is 448 KB and this is partitioned between the R4F's tightly coupled interfaces TCMA (320 KB) and TCMB (128 KB). Although the complete 448 KB is unified memory and can be used for program or data, typical applications use TCMA as program and TCMB as data memory.

The remaining memory, starting at a minimum of 128 KB, is available to be used as radar data memory for storing the 'radar data cube'. It is possible to increase the radar data memory size in 64 KB increments, at the cost of corresponding reduction in R4F program or data RAM size. The maximum size of radar data memory possible is 384 KB. A few example configurations supported are listed in Table 9-1.

Table 9-1. R4F RAM(1)

OPTION	R4F PROGRAM RAM	R4F DATA RAM	RADAR DATA MEMORY
1	320KB	128KB	128KB
2	256KB	128KB	192KB
3	256KB	64KB	256KB
4	128KB	64KB	384KB

(1) For AWR1443 ES version 1.0, available RAM is 448 KB instead of 576KB.

The Main Subsystem, Cortex-R4F memory map is shown in Table 9-2.

Table 9-2. Main System Memory Map

Name	Frame Address (Hex)		Size	Description
	Start	End		
CPU Tightly Coupled Memories				
TCMA ROM	0x0000_0000	0x0001_FFFF	96KiB	Program ROM
TCM RAM-A	0x0020_0000	0x0024_FFFF	128–320KiB	Memory size is dependant on the allocation done in Table 9-1, R4F RAM
TCM RAM-B	0x0800_0000	0x0802_FFFF	64–128KiB	
System Peripherals				
Mail Box MSS<->RADARSS	0xF060_1000	0xF060_17FF	2KiB	RADARSS to MSS mailbox memory space
	0xF060_2000	0xF060_27FF	2KiB	MSS to RADARSS mailbox memory space
	0xF060_8000	0xF060_80FF	188B	MSS to RADARSS mailbox Configuration Registers
	0xF060_8060	0xF060_86FF	188B	RADARSS to MSS mailbox Configuration Registers
PRCM & Control Module	0xFFFF_E100	0xFFFF_E2FF	756B	TOP Level Reset, Clock management registers
	0xFFFF_FF00	0xFFFF_FFFF	256B	MSS Reset, Clock management registers
	0xFFFF_EA00	0xFFFF_EBFF	512KiB	IO Mux module registers
	0xFFFF_F800	0xFFFF_FBFF	352B	General-purpose control registers
	0x5000_0400		584B	TPCC,TPTC,ADC buffer configuration, status registers
GIO	0xFFF7_BC00	0xFFF7_BDFF	180B	GIO module configuration registers
DMA	0xFFFF_F000	0xFFFF_F3FF	1KiB	DMA-1 module configuration registers
VIM	0xFFFF_FD00	0xFFFF_FEFF	512B	VIM module configuration registers
RTI-A	0xFFFF_FC00	0xFFFF_FCFF	192B	RTI-A module
RTI-B	0xFFFF_EE00	0xFFFF_EEFF	192B	RTI-B module register space
Serial Interfaces and Connectivity				
QSPI	0xC000_0000	0xC07F_FFFF	8MB	QSPI –Flash Memory space
	0xC080_0000	0xC0FF_FFFF	116B	QSPI module configuration registers
MIBSPI	0xFFF7_F400	0xFFF7_F5FF	512B	MIBSPI-A module configuration registers
SPI	0xFFF7_F600	0xFFF7_F7FF	512B	SPI module configuration registers
SCI-A/UART	0xFFF7_E500	0xFFF7_E5FF	148B	SCI-A module configuration registers
SCI-B/UART	0xFFF7_E700	0xFFF7_E7FF	148B	SCI-B module configuration registers
CAN	0xFFF7_DC00	0xFFF7_DDFF	512B	CAN module configuration registers
I2C	0xFFF7_D400	0xFFF7_D4FF	112B	I2C module configuration registers
ADC Buffer	0x5200_0000		16KiB	ADC ping pong buffer memory space
CBUF_FIFO	0x5202_0000		16KiB	Common buffer memory space

Table 9-2. Main System Memory Map (continued)

Name	Frame Address (Hex)		Size	Description
	Start	End		
Hardware FFT accelerator	0x5008_0000	0x5008_07FF	512B	FFT Accelerator PARAM memory
	0x5008_0800	0x5008_0FFF	264B	FFT accelerator Configuration registors
	0x5008_1000		4KiB	FFT accelerator Window registers
	0x5203_0000	0x5203_7FFF	32KiB	FFT accelerator Memory -1 space
	0x5203_8000		32KiB	FFT accelerator Memory -2 space
L3 Memory				
L3 Shared Memory	0x5100_0000		384KiB	L3 Shared memory space
Interconnects				
PCR	0xFFF7_8000	0xFFF7_87FF	1KiB	PCR-1 interconnect configuration port
PCR-2	0xFCFF_1000	0xFCFF_17FF	1KiB	PCR-2 interconnect configuration port
128 bit SCR	0x5207_0000		128B	128 bit SCR configuration port
Safety Modules				
CRC	0xFE00_0000	0xFEFF_FFFF	16KiB	CRC module configuration registers
PBIST	0xFFFF_E400	0xFFFF_E5FF	464B	PBIST module configuration registers
STC	0xFFFF_E600	0xFFFF_E7FF	284B	STC module configuration registers
DCC-A	0xFFFF_EC00	0xFFFF_ECFF	44B	DCC-A module configuration registers
DCC-B	0xFFFF_F400	0xFFFF_F4FF	44B	DCC-B module configuration registers
ESM	0xFFFF_F500	0xFFFF_F5FF	156B	ESM module configuration registers
CCMR4	0xFFFF_F600	0xFFFF_F6FF	136B	CCMR4 module configuration registers
Peripheral Memories (System & Non System)				
CAN RAM	0xFF1E_0000	0xFF1F_FFFF	128KB	CAN RAM memory space
DMA RAM	0xFFF8_0000	0xFFF8_0FFF	4KB	DMA RAM memory space
VIM RAM	0xFFF8_2000	0xFFF8_2FFF	2KB	VIM RAM memory space
MIBSPIA-TX RAM	0xFF0E_0000	0xFF0E_01FF	0.5KB	MIBSPIA-TX RAM memory space
MIBSPIA- RX RAM	0xFF0E_0200	0xFF0E_03FF	0.5KB	MIBSPIA- RX RAM memory space
Debug Modules				
Debug Sub System	0xFFA0_0000	0xFFAF_FFFF	244KiB	Debug subsystem memory space and registers

9.4.3 Host Interface

The AWR1443 device communicates with the host radar processor over the following main interfaces:

- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (peripheral) for host control . All radio control commands (and response) flow through this interface.
- Reset – Active-low reset for device wakeup from host
- Out-of-band interrupt
- Error – Used for notifying the host in case the radio controller detects a fault

9.5 Accelerators and Coprocessors

The Processing System in the AWR1443 device is an accelerator for FFT operations. The Radar Hardware Accelerator is an IP that enables off-loading the burden of certain frequently used computations in FMCW radar signal processing from the main processor. It is well-known that FMCW radar signal processing involves the use of FFT and Log-Magnitude computations in order to obtain a radar image across the range, velocity and angle dimensions. Some of the frequently used functions in FMCW radar signal processing can be done within the Radar Hardware Accelerator, while still retaining the flexibility of implementing other proprietary algorithms in the Master System processor.

Key features of the Radar Processing Accelerator are:

- FFT computation, with programmable FFT sizes (powers of 2) up to 1024-pt complex FFT
- Internal FFT bit-width of 24 bits (each for I and Q) for good SQNR performance, with fully programmable butterfly scaling at every radix-2 stage for user flexibility
- Built-in capabilities for simple pre-FFT processing – specifically, programmable windowing, basic interference zeroing-out and basic BPM removal
- Magnitude (absolute value) and Log-Magnitude computation capability
- Flexible data flow and data sample arrangement to support efficient multi-dimensional FFT operations and transpose accesses as required
- Chaining and Looping mechanism to sequence a set of accelerator operations one-after-another with minimal intervention from the main processor
- CFAR-CA detector support (linear and logarithmic)
- Miscellaneous other capabilities of the accelerator
  - Stitching two or four 1024-point FFTs to get the equivalent of 2048-point or 4096-point FFT for industrial level sensing applications where large FFT sizes are required
  - Slow DFT mode, with resolution equivalent to 16K size FFT, for FFT peak interpolation (eg. range interpolation) purpose
  - Complex Vector Multiplication and Dot product capability for vectors of size up to 512

9.6 Other Subsystems

9.6.1 ADC Channels (Service) for User Application

The AWR1443 device includes provision for an ADC service for user application, where the

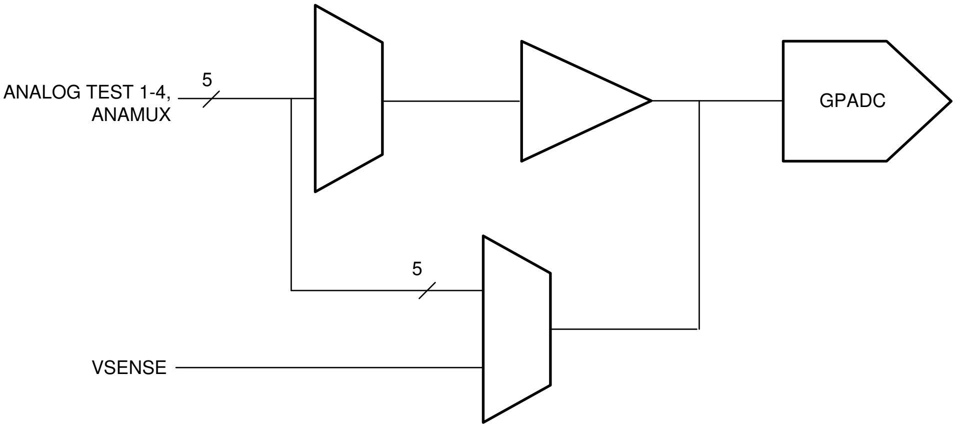
GPADC engine present inside the device can be used to measure up to six external voltages. The ADC1, ADC2, ADC3, ADC4, ADC5, and ADC6 pins are used for this purpose.

- ADC itself is controlled by TI firmware running inside the BIST subsystem and access to it for customer's external voltage monitoring purpose is via 'monitoring API' calls routed to the BIST subsystem. This API could be linked with the user application running on MSS R4F.
- BIST subsystem firmware will internally schedule these measurements along with other RF and Analog monitoring operations. The API allows configuring the settling time (number of ADC samples to skip) and number of consecutive samples to take. At the end of a frame, the minimum, maximum and average of the readings will be reported for each of the monitored voltages.

GPADC Specifications:

- 625 Ksps SAR ADC

- 0 to 1.8V input range
- 10-bit resolution
- For 5 out of the 6 inputs, an optional internal buffer is available. Without the buffer, the ADC has a switched capacitor input load modeled with 5pF of sampling capacitance and 12pF parasitic capacitance (GPADC channel 6, the internal buffer is not available).



A. GPADC structures are used for measuring the output of internal temperature sensors. The accuracy of these measurements is ±7°C.

Figure 9-6. ADC Path

9.6.1.1 GP-ADC Parameter

PARAMETER	TYP	UNIT
ADC supply	1.8	V
ADC unbuffered input voltage range	0 – 1.8	V
ADC buffered input voltage range(1)	0.4 – 1.3	V
ADC resolution	10	bits
ADC offset error	±5	LSB
ADC gain error	±5	LSB
ADC DNL	–1/+2.5	LSB
ADC INL	±2.5	LSB
ADC sample rate(2)	625	Ksps
ADC sampling time(2)	400	ns
ADC internal cap	10	pF
ADC buffer input capacitance	2	pF
ADC input leakage current	3	uA

(1) Outside of given range, the buffer output will become nonlinear.
(2) ADC itself is controlled by TI firmware running inside the BIST subsystem. For more details please refer to the API calls.

9.7 Boot Modes

As soon as device reset is de-asserted, the R4F processor of the Main (Control) system starts executing its bootloader from an on-chip ROM memory.

The bootloader of the Main system operates in two basic modes and these are specified on the user hardware (Printed Circuit Board) by configuring what are termed as “Sense on Power” (SOP) pins. These pins on the device boundary are scanned by the bootloader firmware and choice of mode for bootloader operation is made.

Table 9-3 enumerates the relevant SOP combinations and how these map to bootloader operation.

Table 9-3. SOP Combinations

SOP2 (P13)	SOP1 (P11)	SOP0 (J13)	BOOTLOADER MODE AND OPERATION
0	0	1	Functional Mode Device Bootloader loads user application from QSPI Serial Flash to internal RAM and switches the control to it
1	0	1	Flashing Mode Device Bootloader spins in loop to allow flashing of user application (or device firmware patch – Supplied by TI) to the serial flash
0	1	1	Debug Mode Bootloader is bypassed and R4F processor is halted. This allows user to connect emulator at a known point

9.7.1 Flashing Mode

In Flashing Mode, the Main System's bootloader enables the UART driver and expects a data stream comprising of User Application (Binary Image) and Device Firmware (referred to as Device Firmware Patch or Service Pack) from an external flashing utility. Figure 9-7 shows the flashing utility executing on a PC platform, but the protocol can be accomplished on an embedded platform as well.

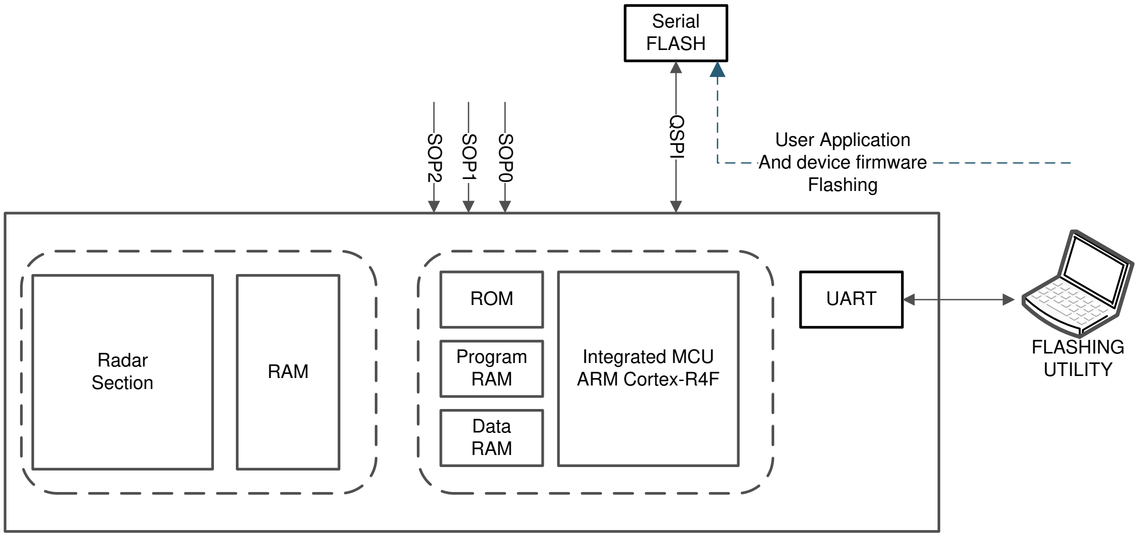


Figure 9-7. Figure 5. Bootloader Flashing Mode

9.7.2 Functional Mode

In Functional Mode, the Main System's bootloader looks for a valid image in the serial flash memory, interfaced over the QSPI port. If a valid image is found, the bootloader transfers the same to Main System's memory subsystem. If the device firmware image is found, it gets transferred to the Radar section's memory subsystem.

If a valid image (or the QSPI Serial Flash is not found), the bootloader initializes the SPI port and awaits for the image transfer. This operation comes handy for configurations where the AWR1443 is interfaced to an external processor which has its own nonvolatile storage hence can store the user application and the AWR1443 device's firmware image.

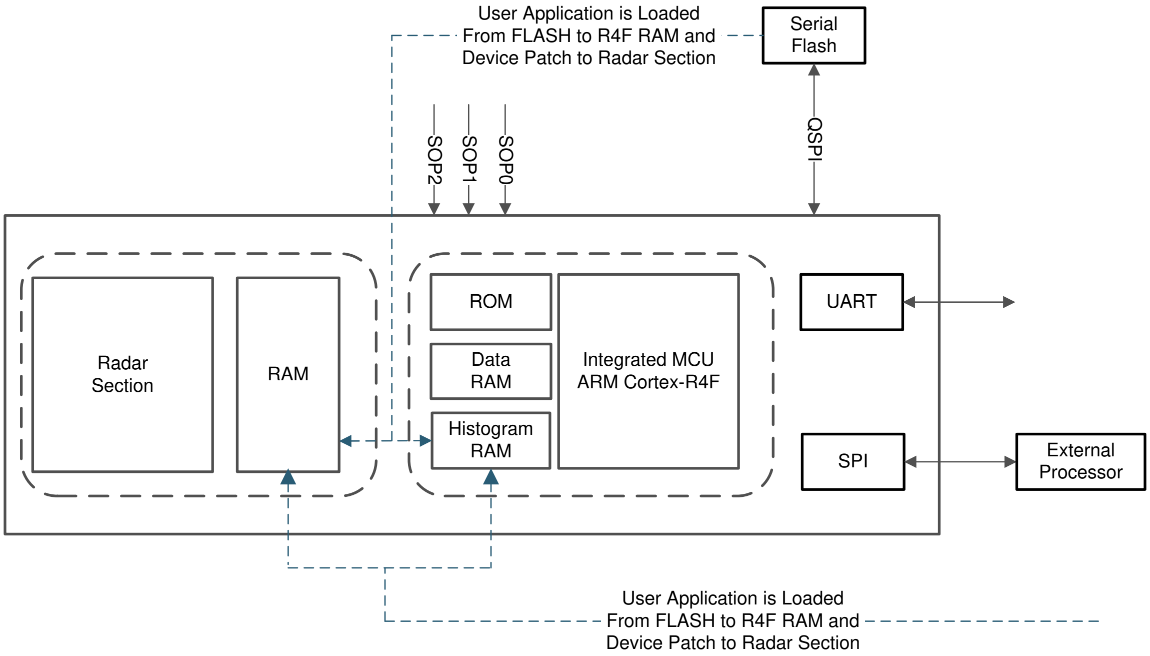


Figure 9-8. Bootloader's Functional Mode

10 Applications, Implementation, and Layout

Note

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Key device features driving the following applications are:

- Integration of Radar Front End and Programmable MCU
- On-chip Hardware Accelerator for Radar Data Processing
- Flexible boot modes: Autonomous Application boot using a serial flash or external boot over SPI.

10.2 Short-Range Radar

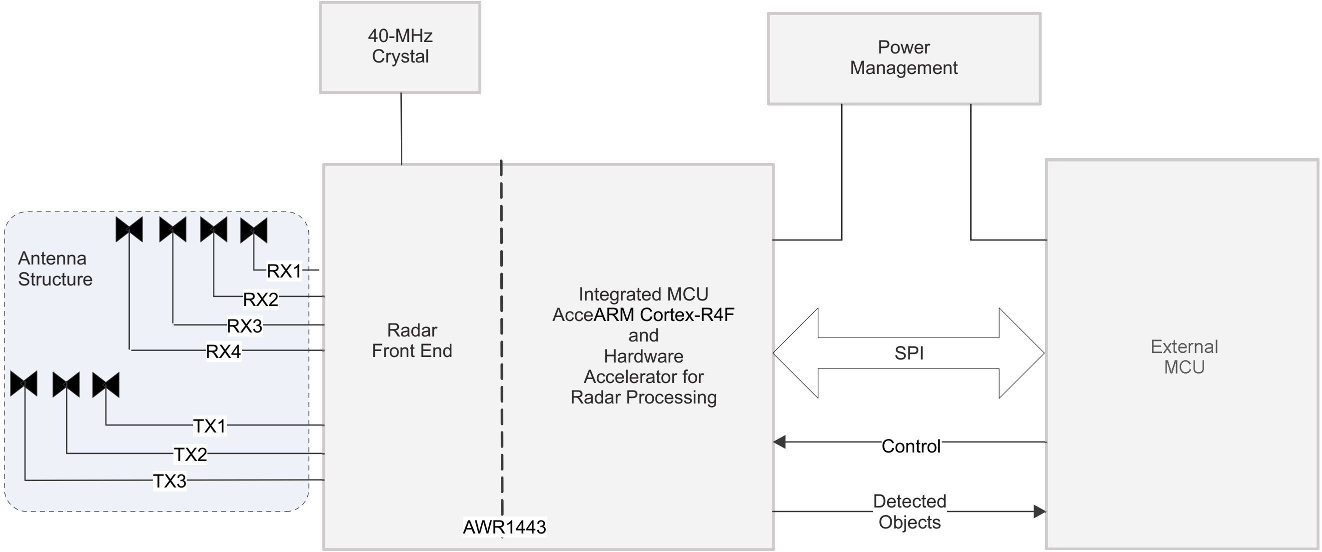
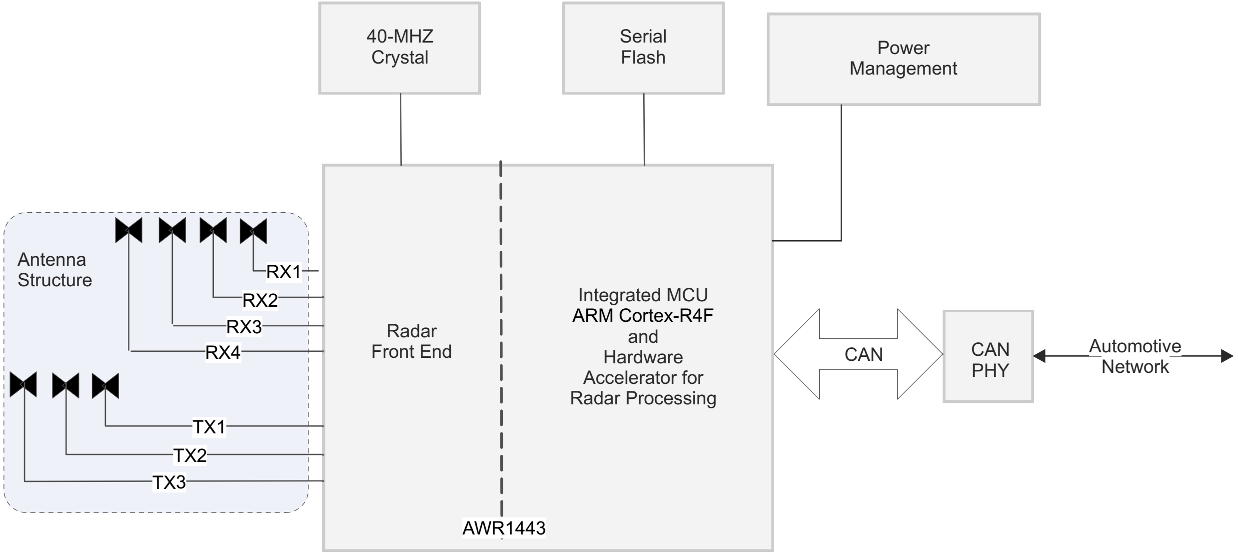


Figure 10-1. Short-Range Radar

10.3 Blind Spot Detector and Ultrasonic Upgrades



10.4 Reference Schematic

The reference schematic and power supply information can be found in the AWR1443 EVM Documentation.

Listed for convenience are: Design Files, Schematics, Layouts, and Stack up for PCB.

- Altium AWR1443 EVM Design Files
- AWR1443 EVM Schematic Drawing, Assembly Drawing, and Bill of Materials

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

11.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *AWR1443*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X	Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
P	Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
null	Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX	Development-support product that has not yet completed Texas Instruments internal qualification testing.
TMDS	Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ABL0161 ALB0161), the temperature range (for example, blank is the default commercial temperature range). Figure 11-1 provides a legend for reading the complete device name for any *AWR1443* device.

For orderable part numbers of *AWR1443* devices in the ABL0161 package types, see the Package Option Addendum of this document , the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *AWR1443 Device Errata* .

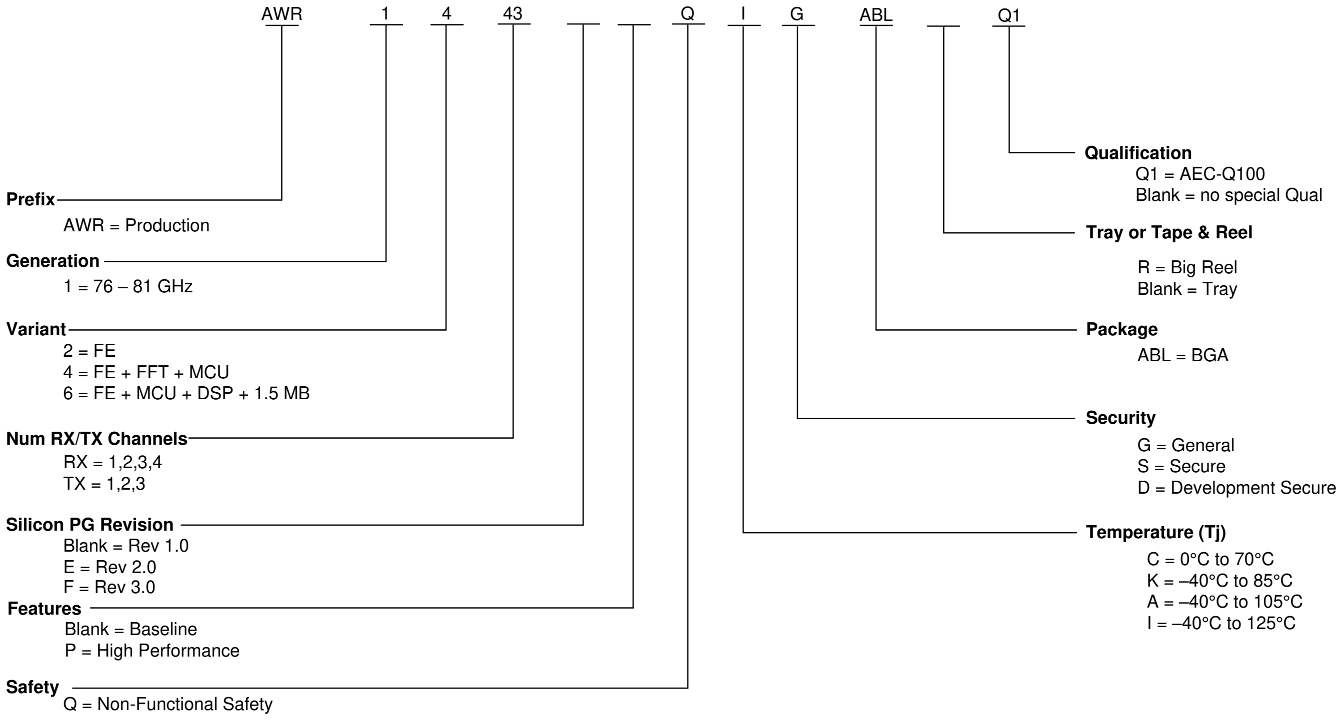


Figure 11-1. Device Nomenclature

11.2 Tools and Software

Models

AWR1443 BSDL model	Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.
AWR1x43 IBIS model	IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.
AWR1443 checklist for schematic review, layout review, bringup/wakeup	A set of steps in spreadsheet form to select system functions and pinmux options. Specific EVM schematic and layout notes to apply to customer engineering. A bringup checklist is suggested for customers.

11.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral follows.

Errata

AWR1443 device errata	Describes known advisories, limitations, and cautions on silicon and provides workarounds.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
Arm® and Cortex® are registered trademarks of ARM Limited.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

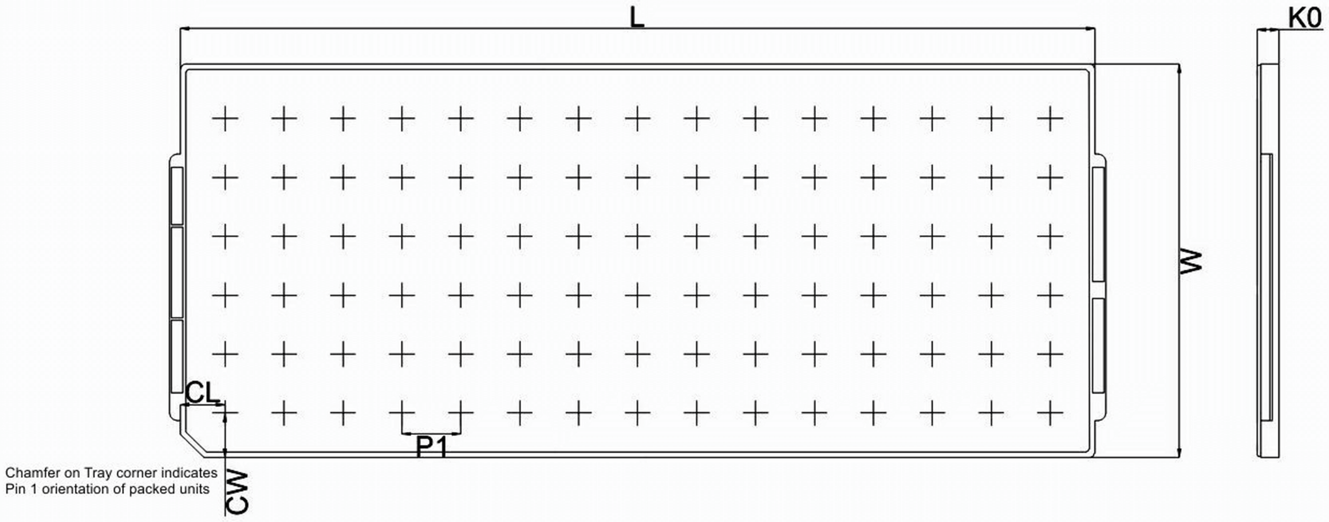
TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

12.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.2 Tray Information for



PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AWR1443FQIGABLQ1	ACTIVE	FCCSP	ABL	161	176	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	AWR1443 IG 964FC	Samples
AWR1443FQIGABLRQ1	ACTIVE	FCCSP	ABL	161	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	AWR1443 IG 964FC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

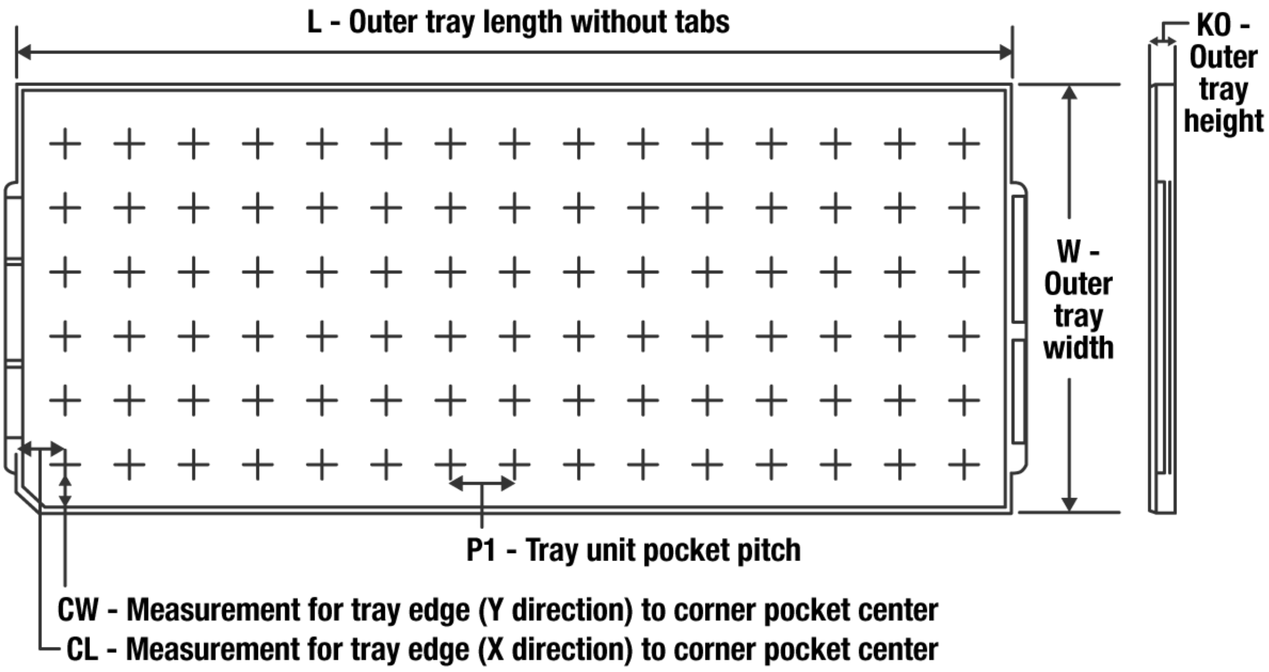
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

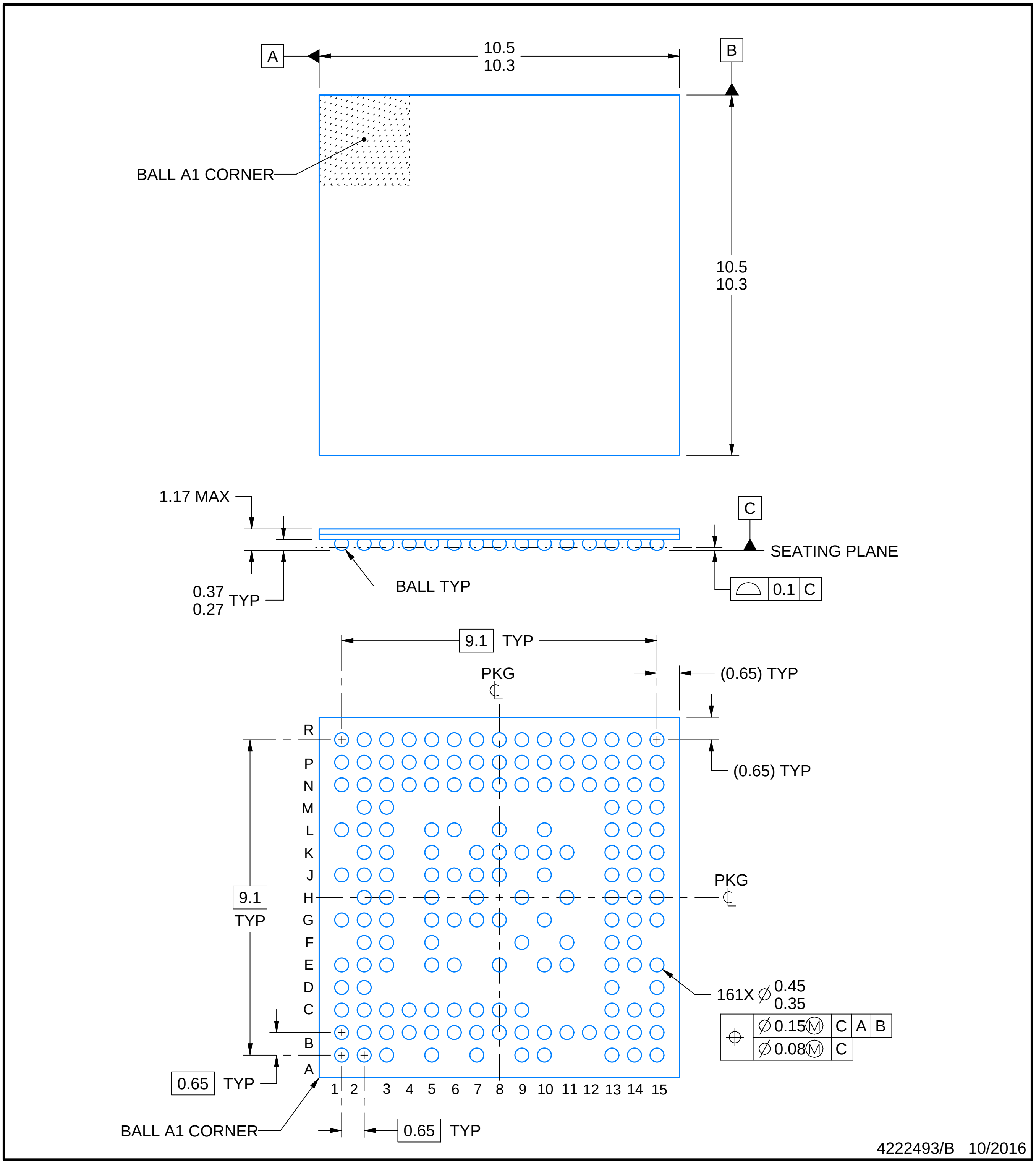
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AWR1443FQIGABLQ1	ABL	FCCSP	161	176	8 x 22	150	315	135.9	7620	13.4	16.8	17.2

PACKAGE OUTLINE

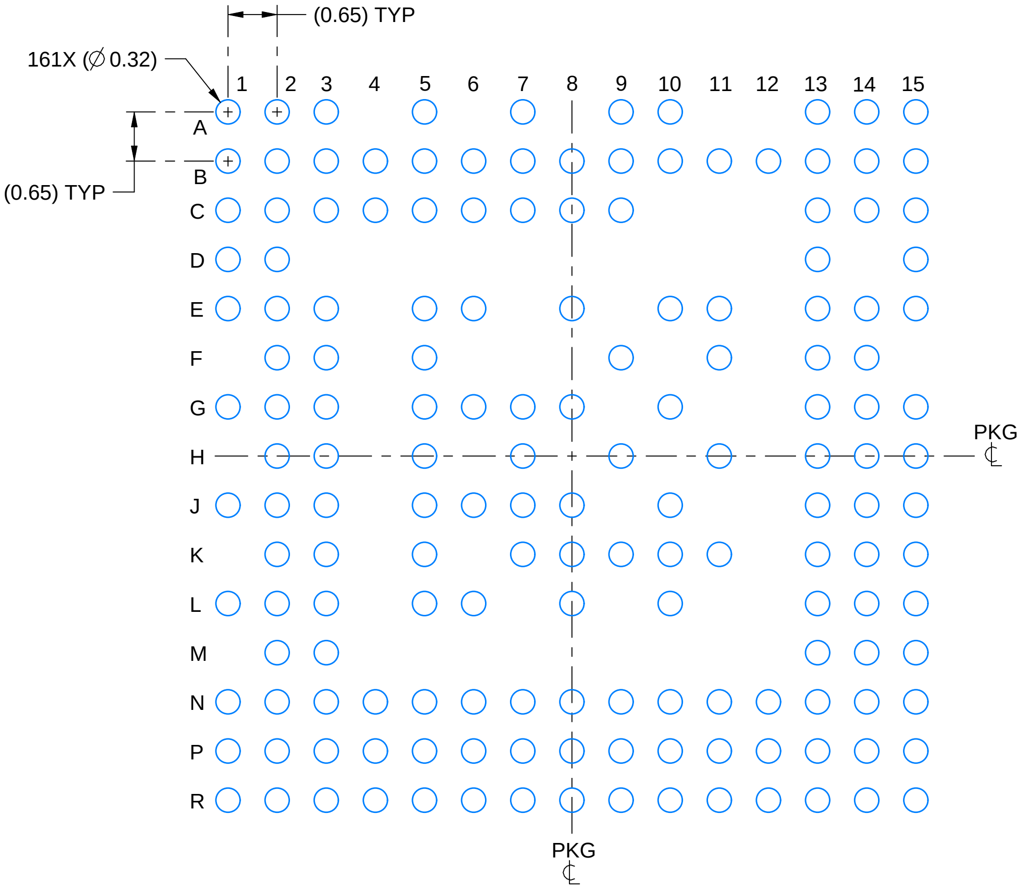
FCBGA - 1.17 mm max height

PLASTIC BALL GRID ARRAY

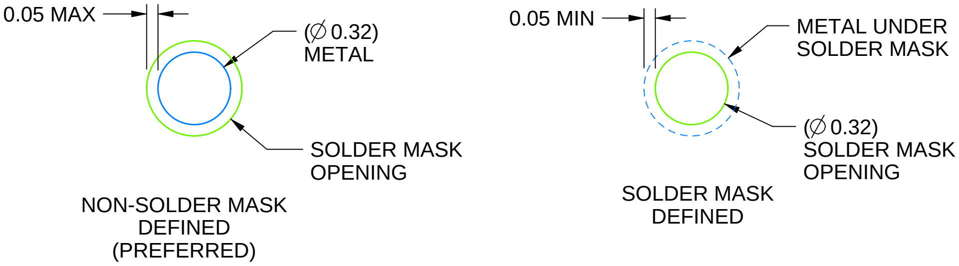


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



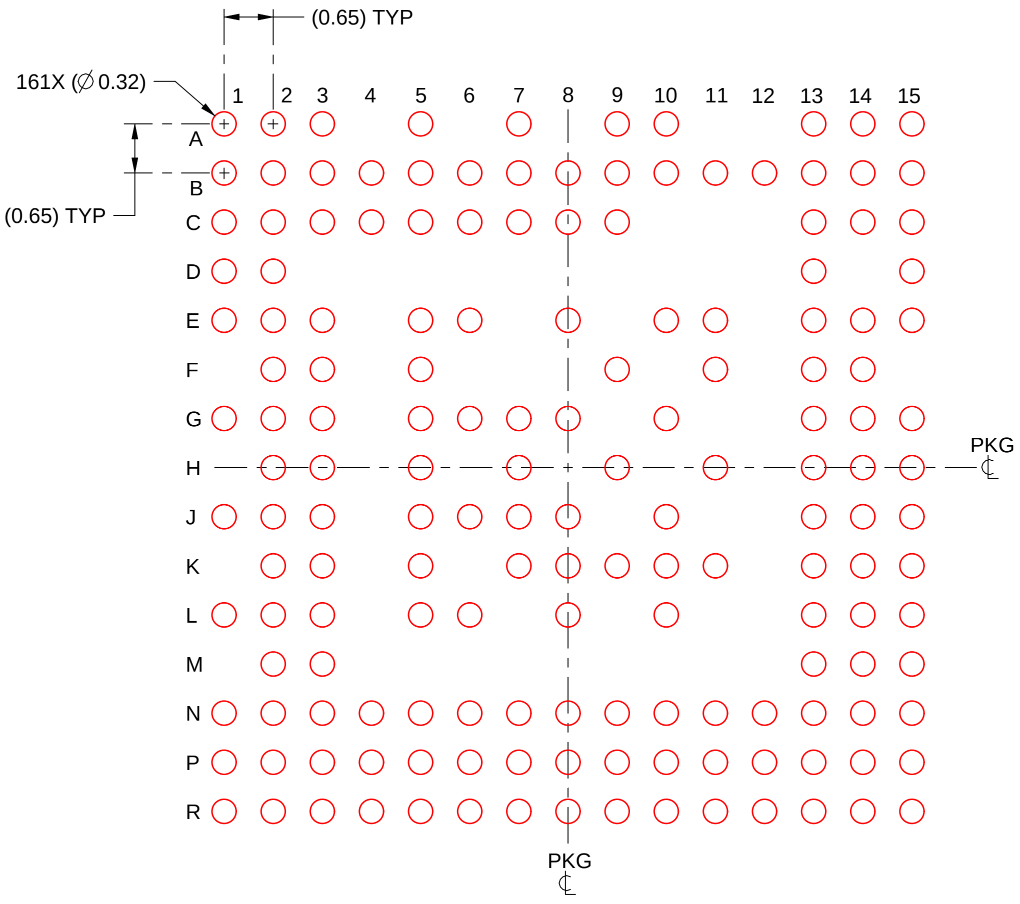
LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated