

# CBT3245A

Octal bus switch

Rev. 4 — 30 April 2019

Product data sheet

## 1. General description

The CBT3245A provides eight bits of high-speed TTL-compatible bus switching. The low ON resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3245A is organized as one 8-bit bus switches with one output enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the switch is on and port A is connected to the B port. When  $\overline{OE}$  is HIGH, each switch is disabled.

## 2. Features and benefits

- 5  $\Omega$  switch connection between two ports
- TTL-compatible control input levels
- Multiple package options
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115B exceeds 150 V
  - CDM JESD22-C101C exceeds 1000 V
- Specified from -40 °C to +85 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
CBT3245AD	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
CBT3245ADB	-40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
CBT3245APW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
CBT3245ABQ	-40 °C to +85 °C	DHVQFN20	plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm	SOT764-1

## 4. Functional diagram

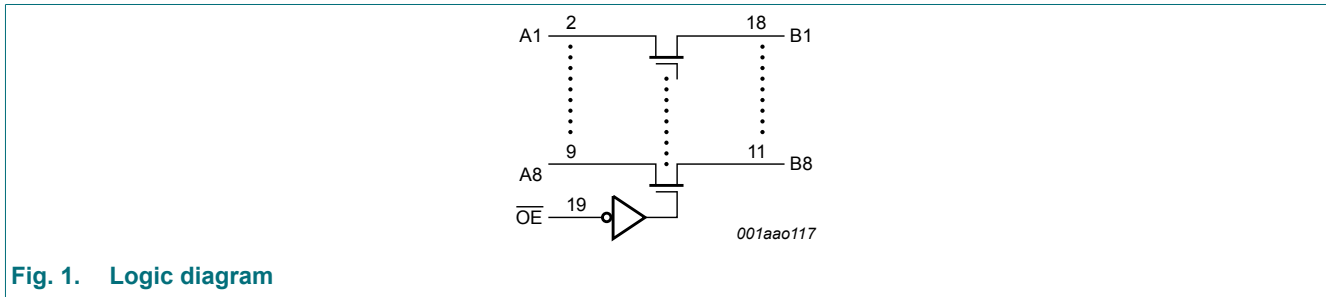


Fig. 1. Logic diagram

## 5. Pinning information

### 5.1. Pinning

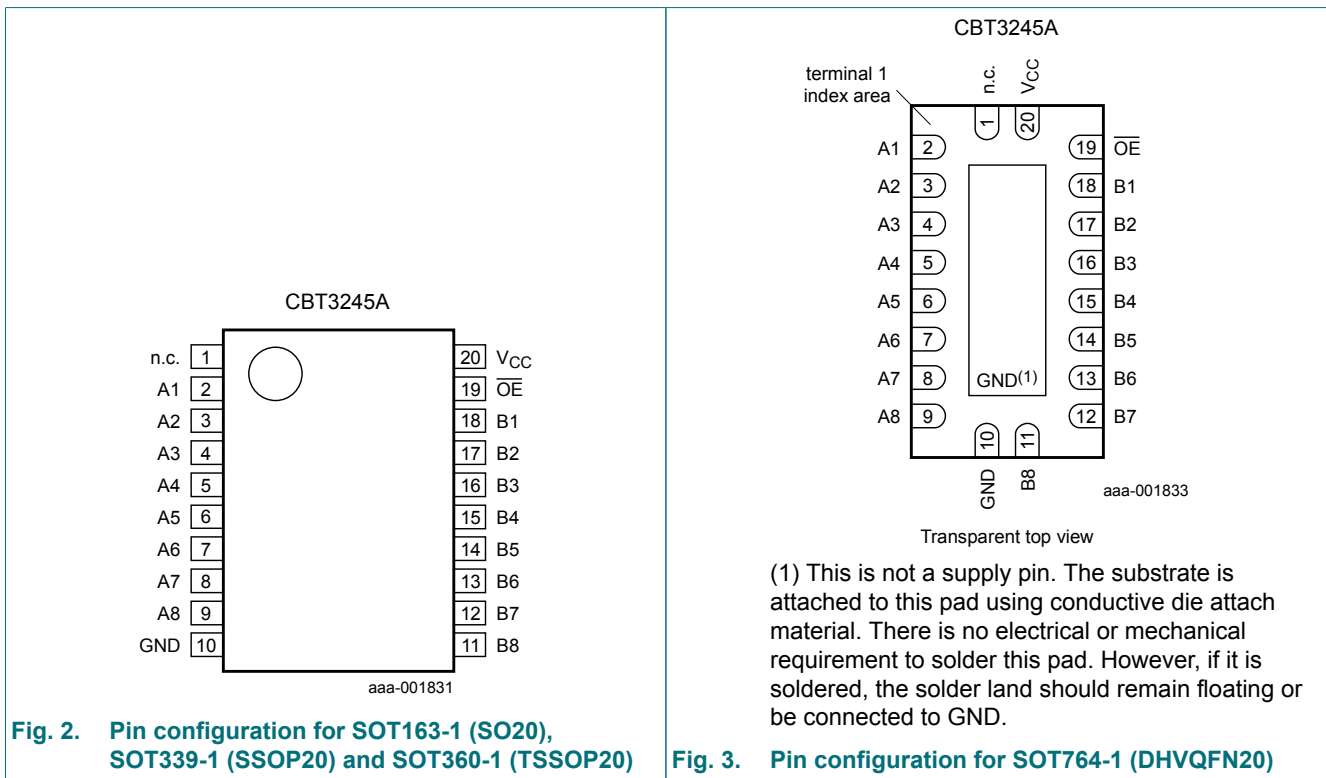


Fig. 2. Pin configuration for SOT163-1 (SO20), SOT339-1 (SSOP20) and SOT360-1 (TSSOP20)

Fig. 3. Pin configuration for SOT764-1 (DHVQFN20)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
n.c.	1	not connected
A1 to A8	2, 3, 4, 5, 6, 7, 8, 9	data input/output (A port)
GND	10	ground (0 V)
B1 to B8	18, 17, 16, 15, 14, 13, 12, 11	data input/output (B port)
OE	19	output enable input (active LOW)
V <sub>CC</sub>	20	positive supply voltage

## 6. Functional description

**Table 3. Functional description**

*H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.*

Input	Input/output
<b>OE</b>	<b>An, Bn</b>
L	An = Bn
H	Z

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

*T<sub>amb</sub> = -40 °C to +85 °C, unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage	[1]	-0.5	+7.0	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
V <sub>O</sub>	output voltage	[1]	-0.5	+7.0	V
I <sub>O</sub>	output current	V <sub>O</sub> < 0 V	-	±128	mA
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C

[1] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

*All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		4.0	-	5.5	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V
T <sub>amb</sub>	ambient temperature	operating in free air	-40	-	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 4.5 V; I <sub>I</sub> = -18 mA	-	-	-1.2	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	-	-	±5	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0 mA; V <sub>I</sub> = V <sub>CC</sub> or GND	-	1	3	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 5.5 V; one input at 3.4 V, other inputs at V <sub>CC</sub> or GND [2]	-	-	3.5	mA
C <sub>I</sub>	input capacitance	control pins; V <sub>I</sub> = 3 V or 0 V	-	3.2	-	pF
C <sub>io(off)</sub>	off-state input/output capacitance	port off; V <sub>I</sub> = 3 V or 0 V; $\overline{OE} = V_{CC}$	-	6.6	-	pF
R <sub>ON</sub>	ON resistance	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 64 mA [3]	-	5	7	Ω
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 30 mA [3]	-	5	7	Ω
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 2.4 V; I <sub>I</sub> = -15 mA [3]	-	10	15	Ω

[1] All typical values are measured at V<sub>CC</sub> = 5 V and T<sub>amb</sub> = 25 °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

[3] Measured by the voltage drop between the An and the Bn terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (An or Bn) terminals.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C		Unit
			Min	Max	
t <sub>pd</sub>	propagation delay	An, Bn to Bn, An; see Fig. 4 [1][2]			
		V <sub>CC</sub> = 5.0 V ± 0.5 V	-	0.25	ns
t <sub>en</sub>	enable time	$\overline{OE}$ to An or Bn; see Fig. 5 [2]			
		V <sub>CC</sub> = 5.0 V ± 0.5 V	1.0	5.9	ns
t <sub>dis</sub>	disable time	$\overline{OE}$ to An or Bn; see Fig. 5 [2]			
		V <sub>CC</sub> = 5.0 V ± 0.5 V	1.0	6.0	ns

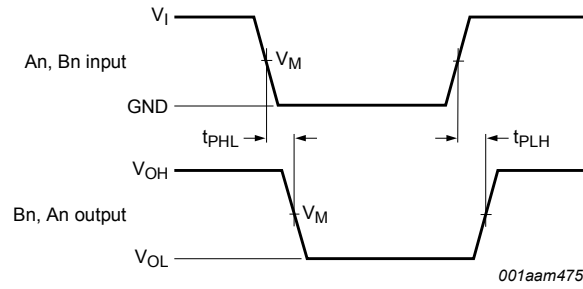
[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

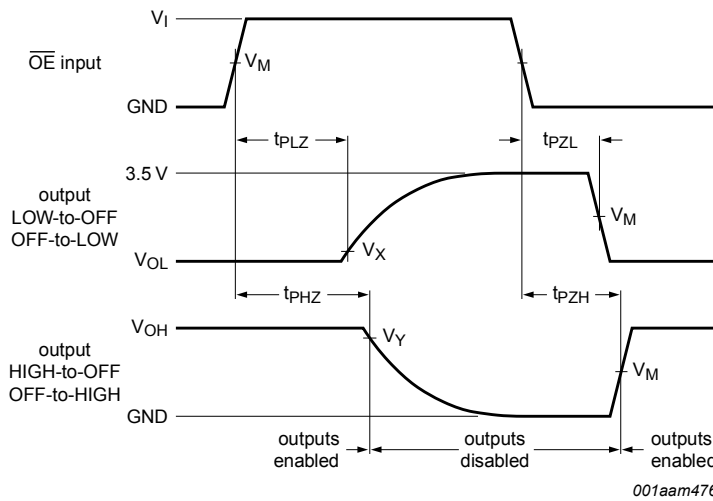
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 4. The data input (An, Bn) to output (Bn, An) propagation delay times



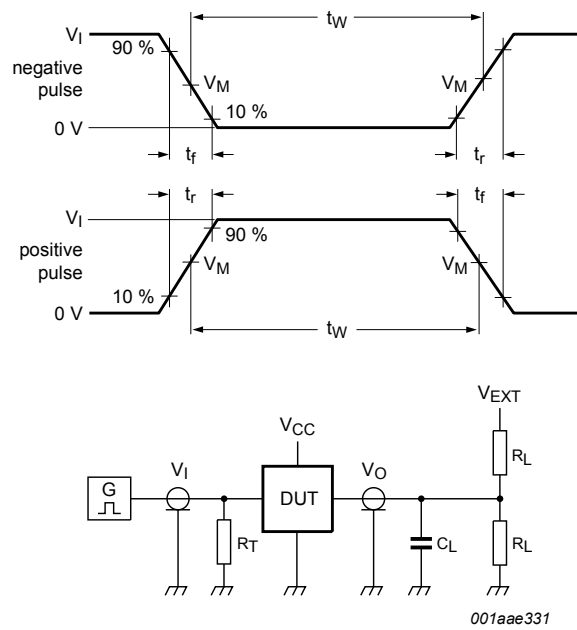
Measurement points are given in [Table 8](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 5. Enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	GND to 3.0 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$



Test data is given in [Table 9](#).  
 All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz;  $Z_o = 50 \Omega$ .  
 The outputs are measured one at a time with one transition per measurement.  
 Definitions for test circuit:  
 $R_L$  = Load resistance.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.  
 $V_{EXT}$  = External voltage for measuring switching times.

**Fig. 6. Test circuit for measuring switching times**

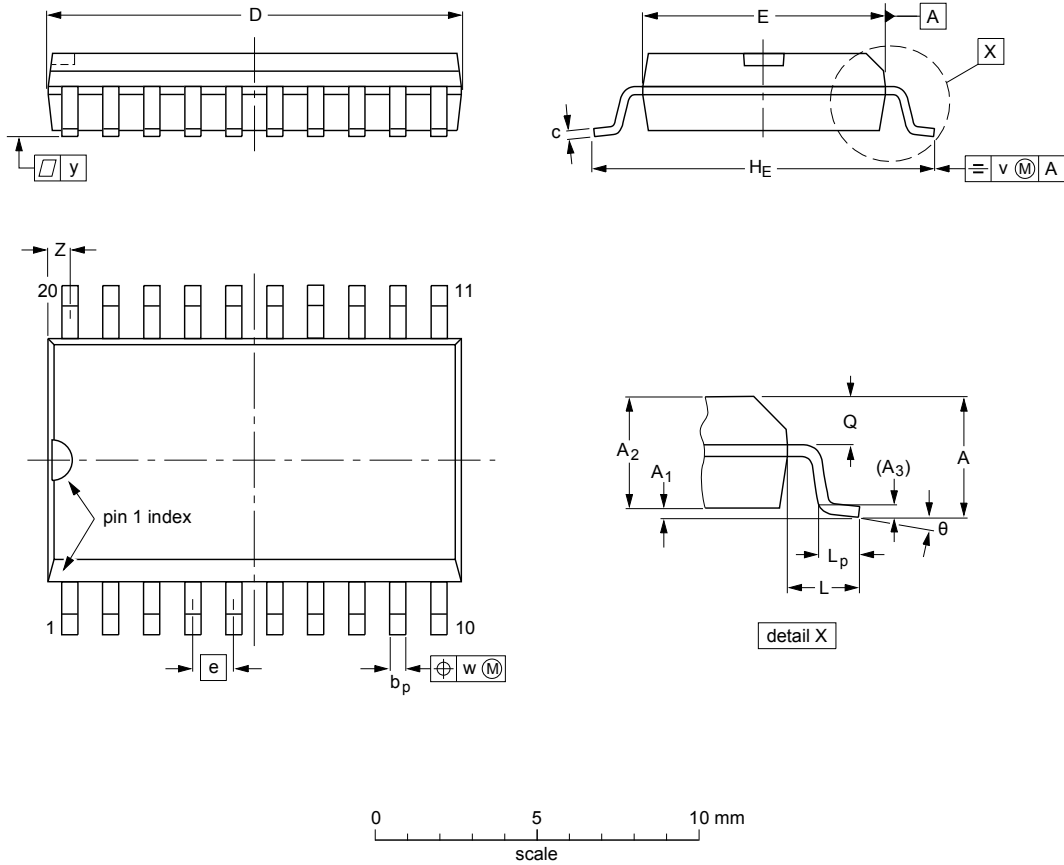
**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	GND to 3.0 V	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$	open	7.0 V	open

### 11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

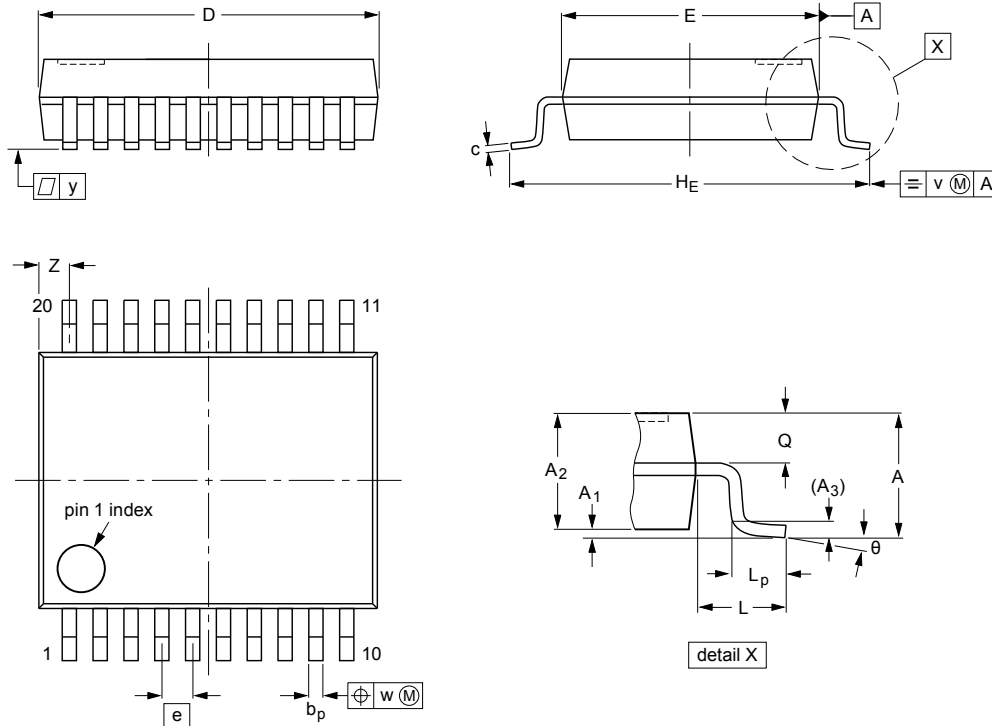
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				-99-12-27 03-02-19

**Fig. 7. Package outline SOT163-1 (SO20)**

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				99-12-27 03-02-19

Fig. 8. Package outline SOT339-1 (SSOP20)



TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

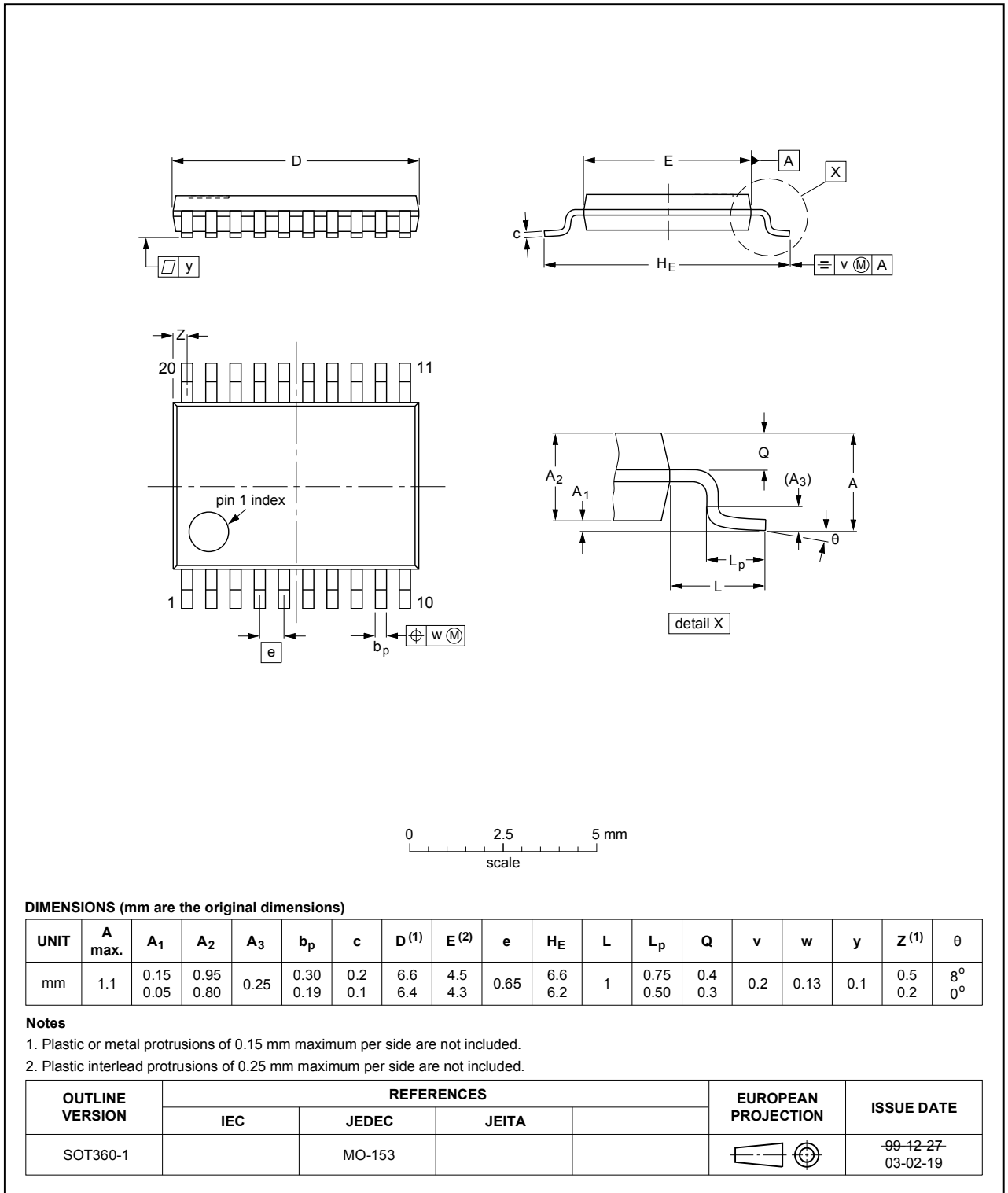
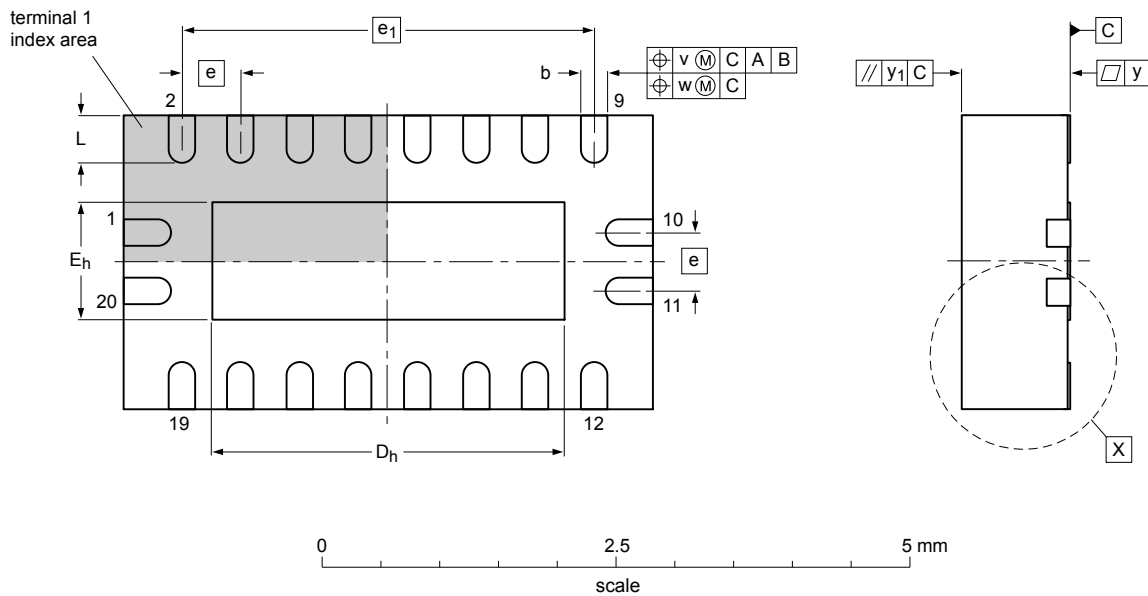
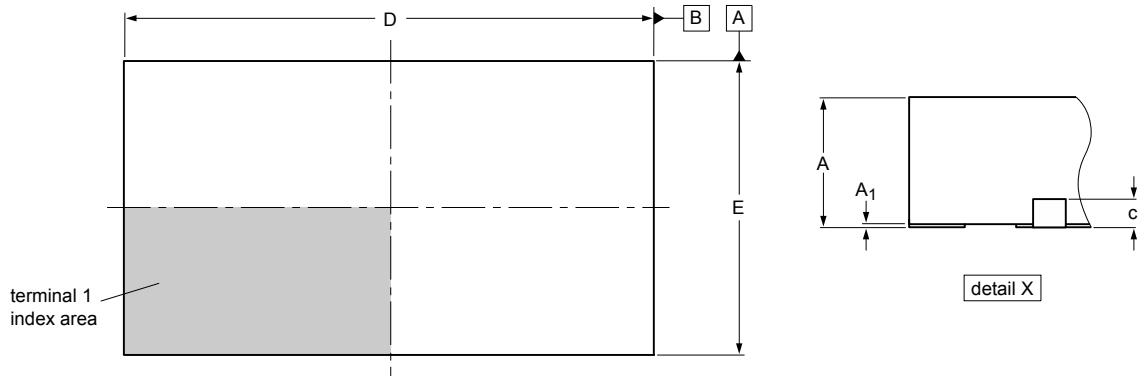


Fig. 9. Package outline SOT360-1 (TSSOP20)

**DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm**

**SOT764-1**



Dimensions (mm are the original dimensions)

Unit	A <sup>(1)</sup>	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	L	v	w	y	y <sub>1</sub>
max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot764-1\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT764-1	---	MO-241	---		-03-01-27- 14-12-12

**Fig. 10. Package outline SOT764-1 (DHVQFN20)**

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
DUT	Device Under Test
HBM	Human Body Model
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3245A v.4	20190430	Product data sheet	-	CBT3245A v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number CBT3245ADS (SOT724-1/SSOP20) removed.</li> <li>Package outline drawing SOT764-1 updated.</li> </ul>			
CBT3245A v.3	20120105	Product data sheet	-	CBT3245A v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Marking code removed from order information section.</li> <li>Description of <math>C_1</math> and <math>C_{I/O}</math> corrected (errata).</li> </ul>			
CBT3245A v.2	20020627	Product data sheet	-	CBT3245A v.1
CBT3245A v.1	20020218	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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Date of release: 30 April 2019

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