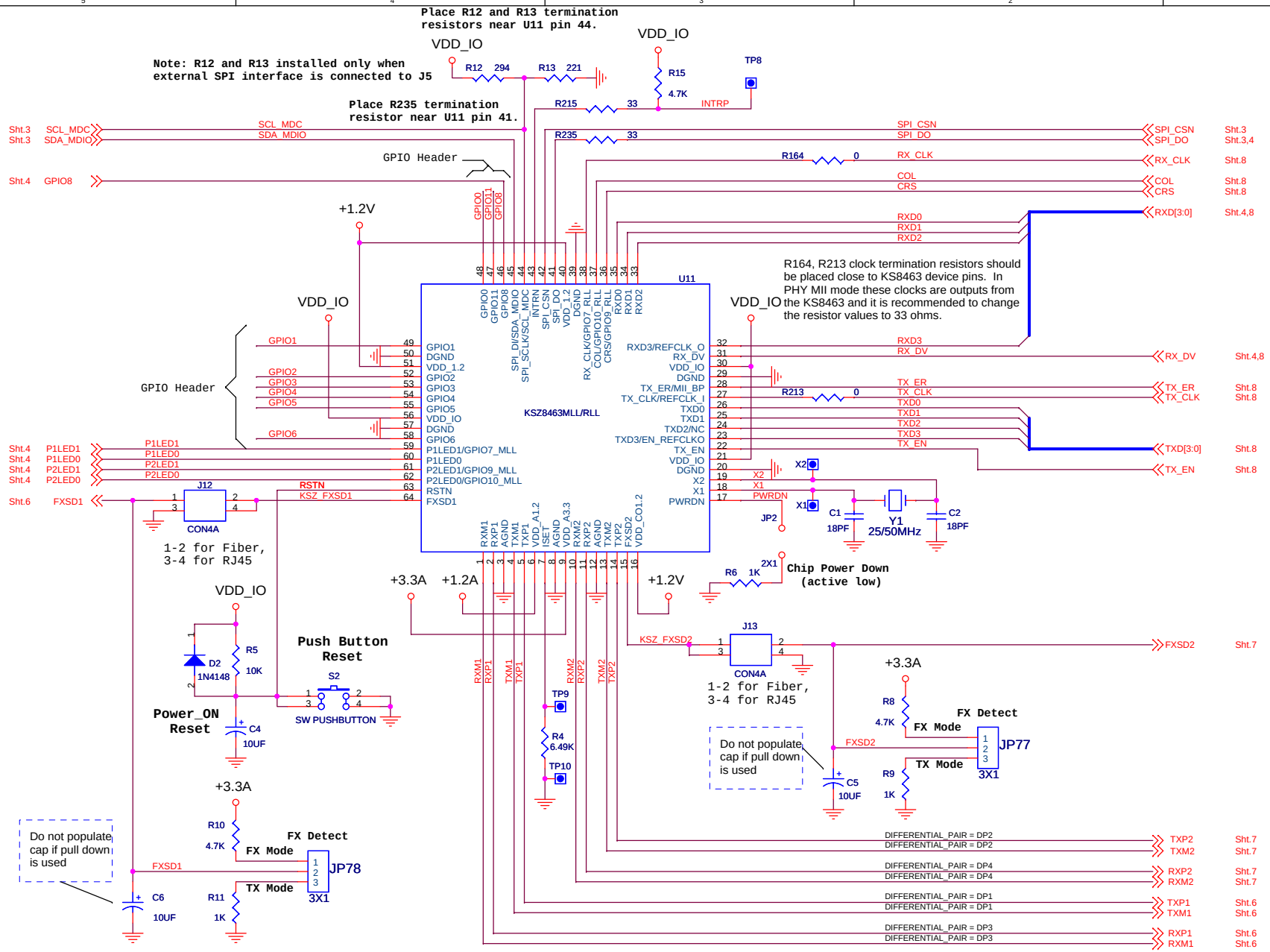
KSZ8463MLL/RLL_LQFP Demo Board Revision 1.3

REVISION HISTORY

DATE:	DESCRIPTION	REVISION
10/02/2010	Initial release	1.0
3/21/2011	Add 4.7K pull-up on J5-2 (spi rdy) and 2.2K pull-down at TP6 (TXEN)	1.1
4/29/2011	Change R46-R50, R52, R54, R55 to 0 ohm	1.2
11/14/2011	2.5V/1.8V regulator schematic is corrected.	1.3

Table of Contents

Title: KSZ8463MLL/RLL DEMO BOARD		
Size	Document Number: Revision History	Rev: 1.3
Date: Monday, November 14, 2011	Sheet 1 of 9	



GPIO HEADERS

GPIO10 SELECT

GPIO09 SELECT

GPIO07 SELECT

HEADER 6X2

Note: place all series resistors near pin of KSZ8463

Note: place header to minimize RX_CLK stub length.

MICREL KENDIN OPERATIONS

CONFIDENTIAL & PROPRIETARY

Title	KSZ8463MLL/RLL DEMO BOARD
Size	Document Number: KSZ8463 Device
Rev	1.3
Date:	Monday, November 14, 2011
Sheet	2 of 9

Bus Selection	Jumper Setting
SMI / MIIM (SW)	open JP32 and JP33. close JP34 and JP35. place Jumper between pin3 and pin4 of J5
I2C Master / I2C Slave / SPI Slave	open JP32 and JP33 close JP34 and JP35.
MIIM (PHY only)	close JP32 and JP33 open JP34 and JP35. place Jumper between pin3 and pin4 of J5

These components are DNI

	KSZ8463 I2C Master Mode	KSZ8463 SMI, SPI / I2C Slave Mode
JP3	CLOSE	OPEN
JP9	CLOSE	OPEN

Serial EEPROM

U2 AT24C02

VDD_IO

R7 10K R1 10K

SR_EEPRM_SCL SR_EEPRM_SDA JP9 JP3 SCL SDA

JP32 2X1 MDC_PHY MDC_PHY Sht.8

JP33 2X1 MDIO_PHY MDIO_PHY Sht.8

SCL JP34 2X1 SCL_MDC SCL_MDC Sht.2

SDA JP35 2X1 SDA_MDIO SDA_MDIO Sht.2

USB5V

FB12 FBEAD

C96 10uF R165 470R C97 0.1uF C98 0.01uF C117 0.1uF

+3.3V_EXT J14

2-3 Close for default	
1-2	USB 3.3V from LDO
2-3	USB 5.0V from USB Port

FT2232_VCCIO C116 0.1uF C113 0.01uF

USB Port

CN1 CN-USB FB13 USBM USBP DIFFERENTIAL_PAIR = DP5 DIFFERENTIAL_PAIR = DP5

Note: place 27 ohm resistors R182, R166 close to FT2232D device pins.

R182 27 R166 27 C108 33nF

R222 4.7K R221 4.7K R219 4.7K R220 4.7K R223 200K R218 200K

U19 PCA9306DCU C145 0.1uF

U20 PCA9306DCU C146 0.1uF

R236 0

VDD_IO

R169 4.7K R168 4.7K R167 4.7K R170 4.7K R175 4.7K

SPI Signals

68001-206HLF J5

SPI_CSN SPI_RDY SPI_DO SDA SCL

SPI Port

To SoC Board

JP79 HEADER 4X2

SPI_DO SPI_CSN Sht.2,4 Sht.2

Install jumpers to connect FT2232D to SPI Bus:

1 - 2
3 - 4
5 - 6
7 - 8

U18 FT2232D (SPI PINOUT)

3V3OUT USBDM USBDP RSTOUT# XTIN XTOUT RESET# EECS EESK EEDATA TEST

TXDA RXDA RTSA# CTSA# DTRA# DSRA# DCDA# RIA# FT_SCK FT_MOSI FT_MISO FT_CSN

TXDENA SLEEPA# RXLED# TXLED# SI/WUA

TXDB RXDB RTSB# CTSB# DTRB# DRSB# DCDB# RIB# TXDENB# SLEEPB# RXLEDB# TXLEDB# SI/WUB PWREN#

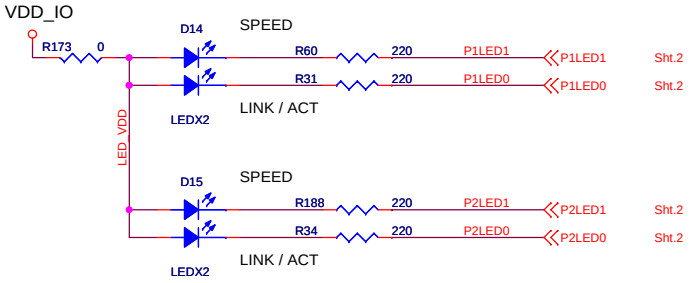
R189 1.5K R190 10k R192 10K R193 10K R191 1K

Y3 6MHz CRYSTAL C104 47pF C105 47pF

+3.3V_EXT

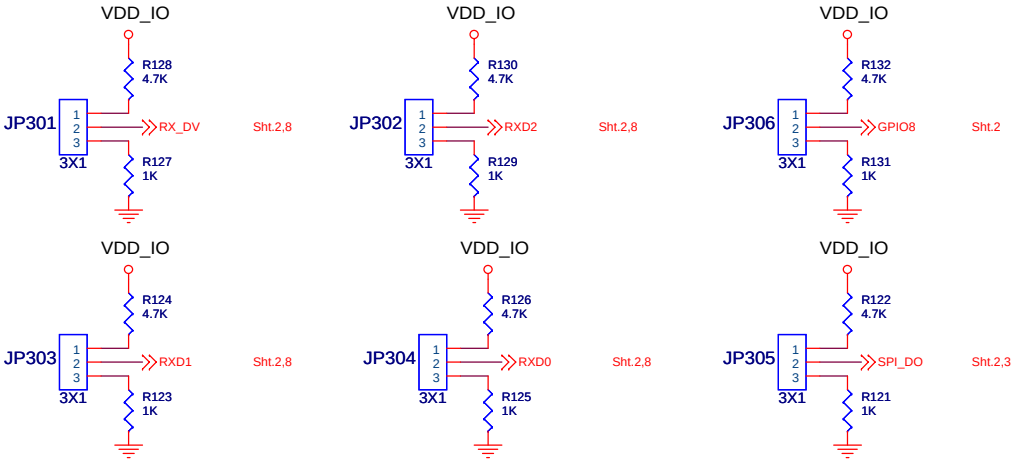
CONFIDENTIAL & PROPRIETARY

Title	KSZ8463MLL/RLL DEMO BOARD
Size	Document Number: USB Interface Bridge — Rev 1.3
Date:	Monday, November 14, 2011 — Sheet 3 of 9



Strapping / Configuration Options

Note: for 8462 only supports VDD_IO=3.3V or 2.5V due to strap in requirements



JP301	**PHY / MAC mode select** 1 = PHY MII mode (default) 0 = MAC MII mode
JP302	**Hi/Low Speed SPI mode select** 1 = High Speed (default) 0 = Low Speed
{JP303, JP304}	**Serial Bus mode select** {0, 0} - I2C Master (EEPROM) mode {0, 1} - I2C Slave mode {1, 0} - SPI Slave mode (default) {1, 1} - SMI / MIIM mode
JP305	**XCLK Frequency** 1 = 25MHz from X1/X2 (default) 0 = 50MHz from REFCLK_I

Title	KSZ8463MLL/RLL DEMO BOARD	
Size	Document Number Device Configuration and LEDs	Rev 1.3
Date: Monday, November 14, 2011	Sheet 4 of 9	

1000pf/2KV

C87

1000pf/2KV

CHASSIS GND

Compatible Isolation Transformers

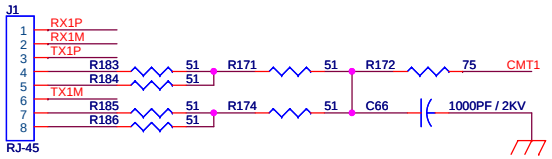
Pulse H1102

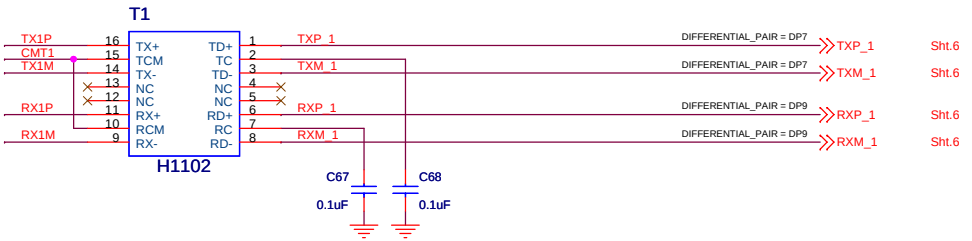
Transpower HB726

Bel Fuse S558-5999-U7

YCL PT163020

DELTA LF8505

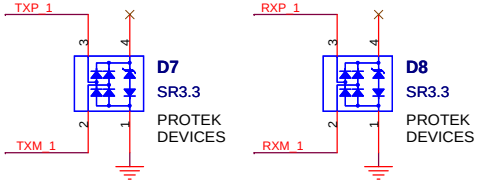




Line Side Protection (test option)

Place near RJ-45 connector

Chip Side Protection (test option)



1000pf/2KV

C88

1000pf/2KV

CHASSIS GND

Compatible Isolation Transformers

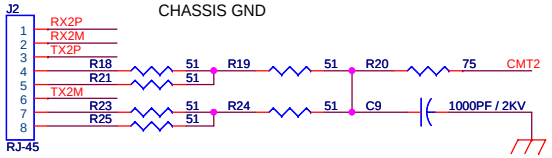
Pulse H1102

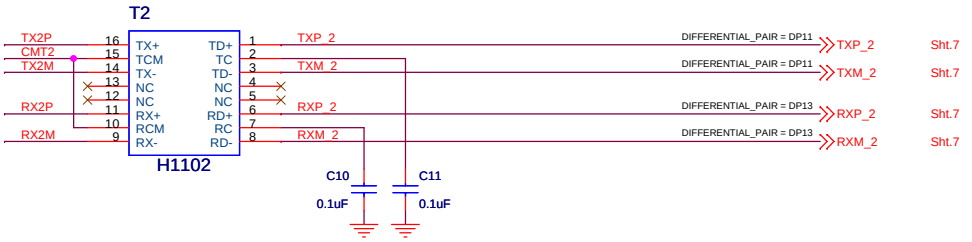
Transpower HB726

Bel Fuse S558-5999-U7

YCL PT163020

DELTA LF8505

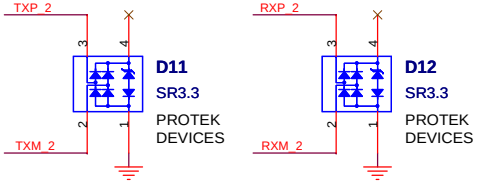




Line Side Protection (test option)

Place near RJ-45 connector

Chip Side Protection (test option)

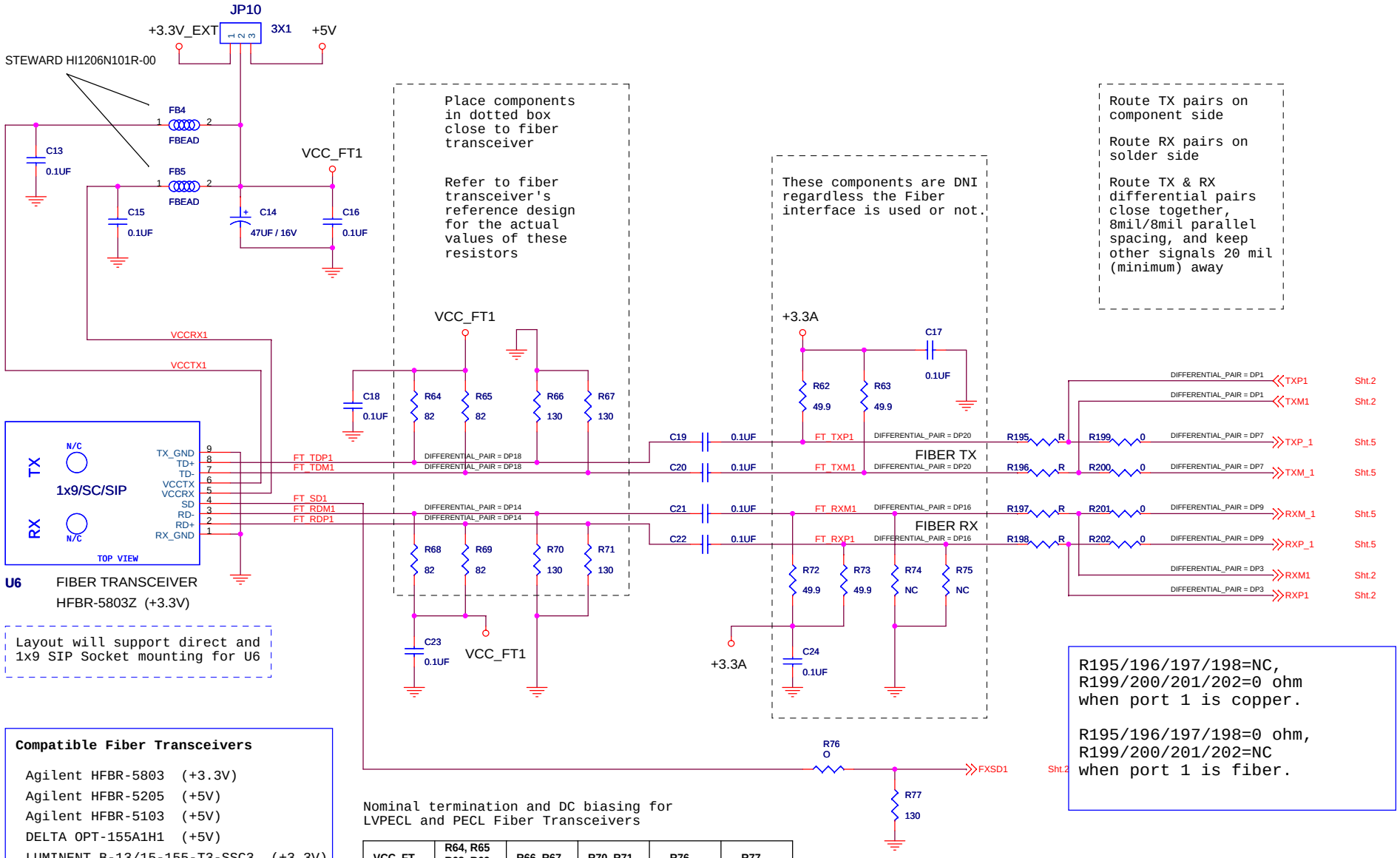


MICREL

KENDIN OPERATIONS

CONFIDENTIAL & PROPRIETARY

Title: KSZ8463MLL/RLL DEMO BOARD		
Size	Document Number: Ethernet Interface	Rev: 1.3
Date: Monday, November 14, 2011	Sheet 5 of 9	



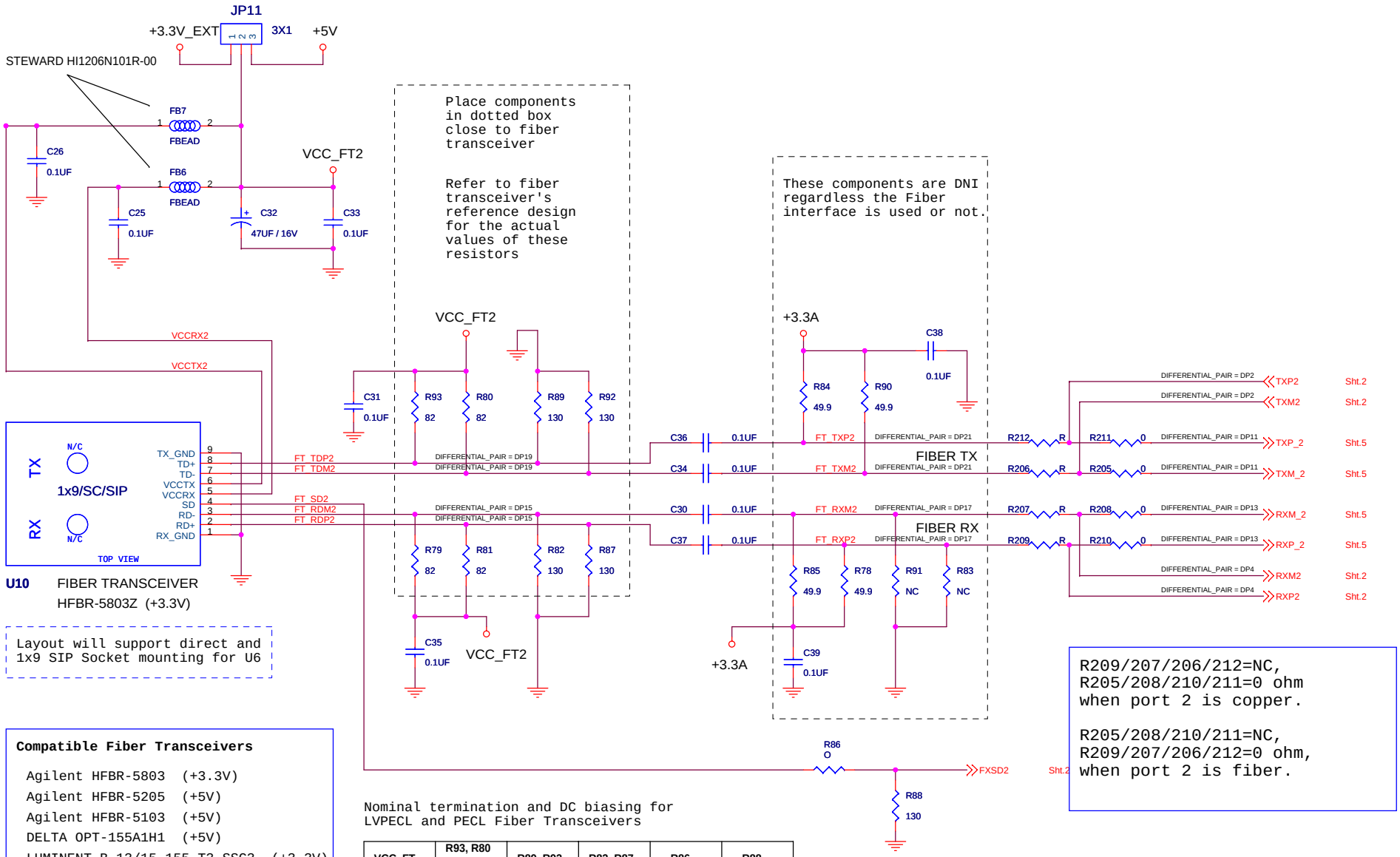
Nominal termination and DC biasing for LVPECL and PECL Fiber Transceivers

VCC_FT	R64, R65 R68, R69	R66, R67	R70, R71	R76	R77
+3.3V	82 Ohms	130 Ohms	130 Ohms	O Ohm	130 Ohms
+5V	68 Ohms	191 Ohms	270 Ohms	4.75K 1%	5.62K 1%

KENDIN OPERATIONS

CONFIDENTIAL & PROPRIETARY

Title: KSZ8463MLL/RLL DEMO BOARD		
Size	Document Number: Fiber Interface	Rev: 1.3
Date: Monday, November 14, 2011	Sheet 6 of 9	



Compatible Fiber Transceivers

- Agilent HFBR-5803 (+3.3V)
- Agilent HFBR-5205 (+5V)
- Agilent HFBR-5103 (+5V)
- DELTA OPT-155A1H1 (+5V)
- LUMINENT B-13/15-155-T3-SSC3 (+3.3V)
- LUMINENT B-13/15-155-T-SSC3 (+5V)

Nominal termination and DC biasing for LVPECL and PECL Fiber Transceivers

VCC_FT	R93, R80 R79, R81	R89, R92	R82, R87	R86	R88
+3.3V	82 Ohms	130 Ohms	130 Ohms	O Ohm	130 Ohms
+5V	68 Ohms	191 Ohms	270 Ohms	4.75K 1%	5.62K 1%

KENDIN OPERATIONS

CONFIDENTIAL & PROPRIETARY

Title: KSZ8463MLL/RLL DEMO BOARD			
Size	Document Number: Fiber Interface		Rev: 1.3
Date: Monday, November 14, 2011	Sheet 7 of 9		

RMII option

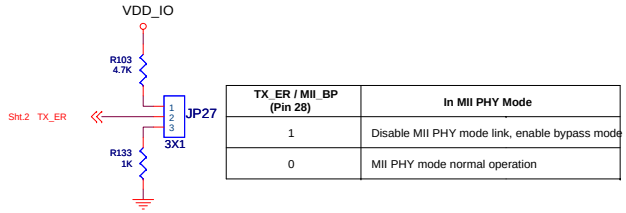
KS8463RLL provides RMII signals with respect to both PHY and MAC sides.

For this board, the KS8463RLL provides RMII signals with respect to MAC side only. The RMII signal connections between KS8463RLL and external PHY are shown in the table to the right.

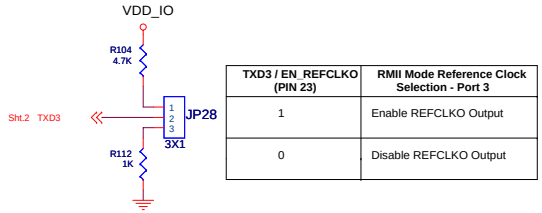
The KSZ8463RLL can provide the 50MHz reference clock by jumpering JP28 1-2 to enable REFCLKO. Remove R 51 and R53.

The KSZ8463RLL can use internal or external reference clock which is selected by register CFGR bit 3. For external, it is set to 1, vice reverse.

External PHY RMII (with respect to PHY)		KSZ8463RLL RMII (with respect to MAC)		
Signal	**Type**	**Signal**	**Pin #**	**Type**
REF_CLK	Input	TX_CLK	27	Input
CRS_DV	Output	TX_EN	22	Input
RXD[1]	Output	TXD1	25	Input
RXD[0]	Output	TXD0	26	Input
TX_EN	Input	RX_DV	31	Output
TXD[1]	Input	RXD1	34	Output
TXD[0]	Input	RXD0	35	Output
RX_ER	Output	TX_ER	28	Input



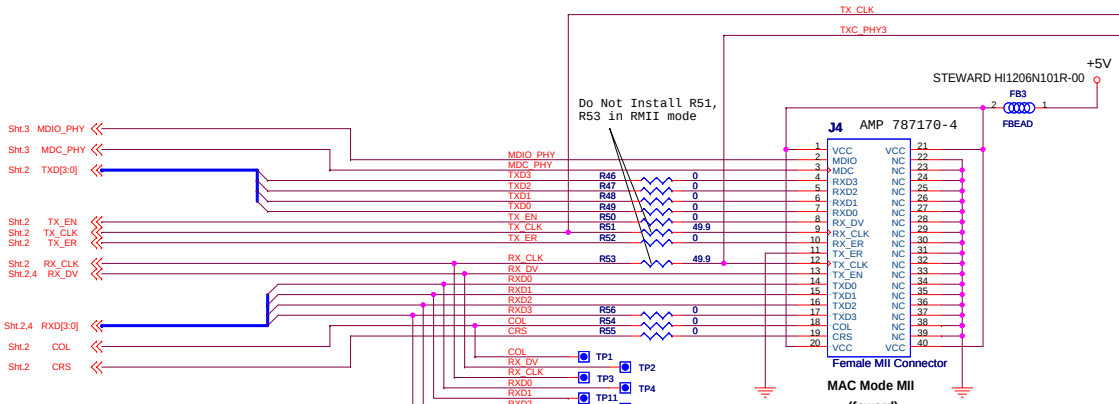
TX_ER / MII_BP (Pin 28)	In MII PHY Mode
1	Disable MII PHY mode link, enable bypass mode
0	MII PHY mode normal operation

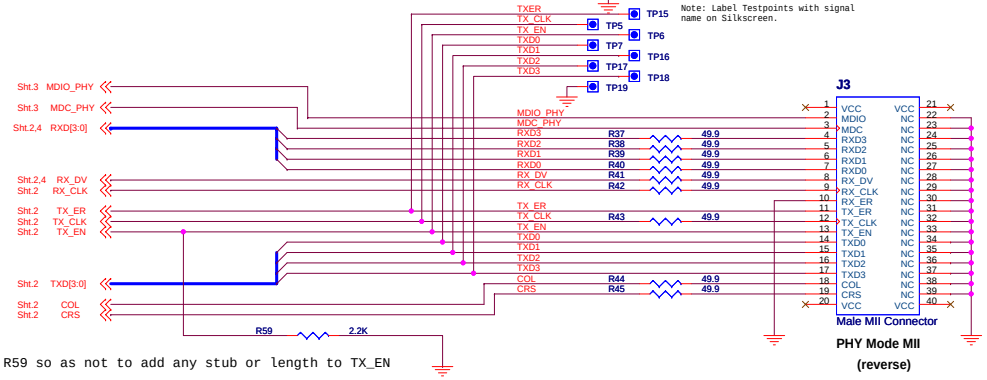


TXD3 / EN_REFCLKO (PIN 23)	RMII Mode Reference Clock Selection - Port 3
1	Enable REFCLKO Output
0	Disable REFCLKO Output

Layout will support SMD and HALF CAN packages for Y2

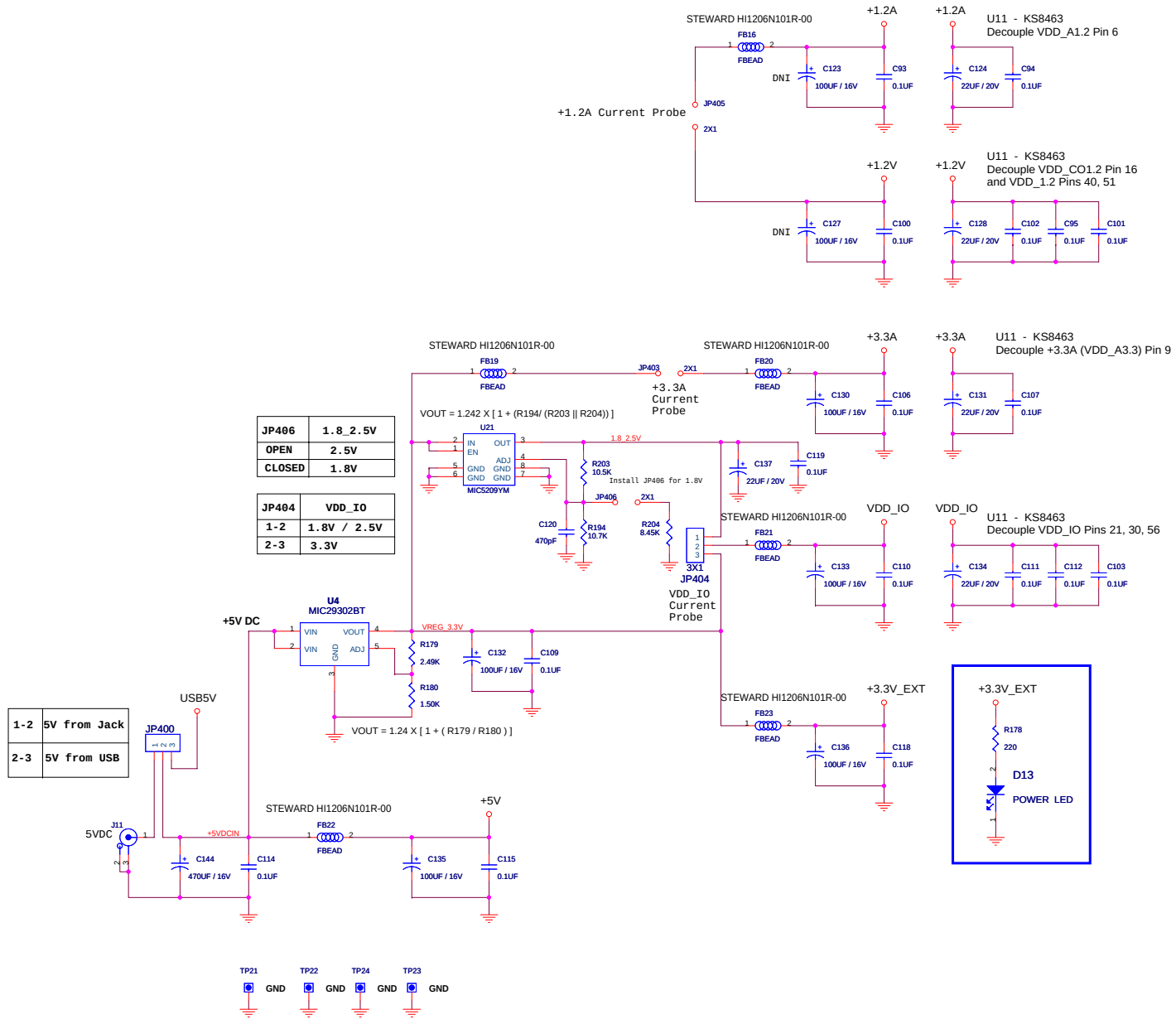
If 50MHz comes from Internal KSZ8463RLL. NC R57





CONFIDENTIAL & PROPRIETARY

Title	KSZ8463MLL/RLL DEMO BOARD		
Size	Document Number: MII / RMII Interface		Rev 1.3
Date: Monday, November 14, 2011	Sheet 8 of 9		



CONFIDENTIAL & PROPRIETARY

Title	KSZ8463MLL/RLL DEMO BOARD
Size	Document Number: Power — Rev: 1.3
Date:	Monday, November 21, 2011 — Sheet 9 of 9