User's Guide
LM25149-Q1 EVM User's Guide

ABSTRACT

With an input operating voltage as low as 3.5 V and up to 100 V as specified in Table 1-1, the LM514x-Q1 family of automotive synchronous buck controllers from TI provides flexibility, scalability, and optimized solution size for a range of applications. These controllers enable DC/DC solutions with high density, low EMI, and increased flexibility. Available EMI mitigation features include dual-random spread spectrum (DRSS) or triangular spread spectrum (TRSS), split gate driver outputs for slew rate (SR) control, and integrated active EMI filtering (AEF). All controllers are rated for a maximum operating junction temperature of 150°C and have AEC-Q100 grade 1 qualification.

Table 1-1. Automotive Synchronous Buck DC/DC Controller Family

DC/DC Controller	Single or Dual	V_{IN} Range	Control Method	Gate Drive Voltage	Sync Output	EMI Mitigation
LM5140-Q1	Dual	3.8 V to 65 V	Peak current mode	5 V	180° phase shift	N/A
LM25149-Q1	Single	3.5 V to 42 V	Peak current mode	5 V	180° phase shift	AEF, DRSS
LM25148-Q1	Single	3.5 V to 42 V	Peak current mode	5 V	180° phase shift	DRSS
LM5141-Q1	Single	3.8 V to 65 V	Peak current mode	5 V	N/A	SR control, TRSS
LM25141-Q1	Single	3.8 V to 42 V	Peak current mode	5 V	N/A	SR control, TRSS
LM5143-Q1	Dual	3.5 V to 65 V	Peak current mode	5 V	90° phase shift	SR control, TRSS
LM5145-Q1	Single	5.5 V to 75 V	Voltage mode	7.5 V	180° phase shift	N/A
LM5146-Q1	Single	5.5 V to 100 V	Voltage mode	7.5 V	180° phase shift	N/A

The LM25149-Q1EVM-2100 evaluation module (EVM) is a synchronous buck DC/DC regulator that employs synchronous rectification to achieve high conversion efficiency in a small footprint. It operates over a wide input voltage range of 5.5 V to 36 V, providing a regulated output of 5 V. The output voltage has better than 1% setpoint accuracy and are adjustable by modifying the feedback resistor values, permitting the user to customize the output voltage from 3.3 V to 5.5 V as needed.

The LM25149-Q1 synchronous buck controller used in the EVM has the following features:

- Wide input voltage (wide V_{IN}) range of 3.5 V to 42 V
- Spread spectrum modulation and active EMI filtering for lower EMI
- Wide duty cycle range with low $t_{ON(min)}$ and $t_{OFF(min)}$
- Ultra-low shutdown and no-load standby quiescent currents
- Multiphase capability
- Peak current-mode control loop architecture
- Integrated, high-current MOSFET gate drivers
- Cycle-by-cycle overcurrent protection with hiccup
- Functional-safety capable

The free-running switching frequency of the EVM is 2.1 MHz and is synchronizable to a higher or lower frequency, if required. Moreover, a synchronization output signal (SYNCOUT) 180° phase-shifted relative to the internal clock is available for dual-phase leader-follower configurations. VCC and gate drive UVLO protects the regulator at low input voltage conditions, and EN pins for each channel support application-specific power-up and power-down requirements.

The LM25149-Q1 is available in a 24-pin VQFN package with 5.5-mm × 3.5-mm footprint to enable DC/DC solutions with high density and low component count. See the *LM25149-Q1 3.5-V to 42-V Synchronous Buck DC/DC Controller Data Sheet* for more information. Use the LM25149-Q1 with WEBENCH® Power Designer

to create a custom regulator design. To optimize component selection and examine predicted efficiency performance across line and load ranges, download the *LM25149-Q1 Quickstart Calculator*.

The LM25149-Q1 on the EVM can be substituted with LM25148-Q1 for evaluation.

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1 High Density EVM Description

The LM25149-Q1EVM-2100 high-density EVM is designed to use a regulated or non-regulated high-voltage input rail ranging from 5.5 V to 36 V to produce a tightly-regulated output voltage of 5 V at load currents up to 8 A. This wide V_{IN} range DC/DC solution offers outsized voltage rating and operating margin to withstand supply rail voltage transients.

The free-running switching frequency is 2.1 MHz and is synchronizable to an external clock signal at a higher or lower frequency. The power-train passive components selected for this EVM, including buck inductors and ceramic input and output capacitors, are automotive AEC-Q200 rated and are available from multiple component vendors.

1.1 Typical Applications

- High-current automotive electronic systems
- ADAS and body electronics
- Infotainment systems and instrument clusters
- Automotive HEV/EV powertrain systems

1.2 Features and Electrical Performance

- Wide input voltage operating range of 5.5 V to 36 V
- 1% accurate fixed 3.3 V, 5 V, or adjustable output down to 0.8 V
- Switching frequency of 2.1 MHz externally synchronizable up or down by 20%
- Full-load efficiency of 92.8% at V_{IN} = 12 V
- 12-µA controller standby current at V_{IN} = 12 V
- Optimized for ultra-low EMI
  - Dual-Random Spread Spectrum and Active EMI filtering
  - Meets CISPR 25 and UNECE Reg 10 EMI standards
- Peak current-mode control architecture provides fast line and load transient response
  - Integrated slope compensation adaptive with switching frequency
  - Forced PWM (FPWM) or Pulsed-Frequency Modulation (PFM) operation
  - Optional internal or external loop compensation
- Integrated high-side and low-side power MOSFET gate drivers
  - 2.2-A and 3.2-A sink and source gate drive current capability
  - 13-ns adaptive dead-time control reduces power dissipation and MOSFET temperature rise
- Overcurrent protection (OCP) with hiccup mode for sustained overload conditions
- SYNCOUT signal 180° out-of-phase with internal clock
- Power Good signal with 100-kΩ pullup resistor to VCC
- Internal 3-ms soft start
- Fully assembled, tested, and proven PCB layout with 70-mm × 40-mm total footprint

2 EVM Characteristics

Table 2-1 lists the electrical characteristics.

Table 2-1. Electrical Performance Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage range, V_{IN}	Operating		5.5	12	36	V
Input current, no load, I_{IN-NL}	I_{OUT} = 0 A, PFM tied to VDDA, UVLO removed	V_{IN} = 12 V		12		µA
		V_{IN} = 24 V		9		
		V_{IN} = 36 V		9		
Input current, shutdown, I_{IN-OFF}	V_{EN} = 0 V	V_{IN} = 12 V		3		µA
OUTPUT CHARACTERISTICS						
Output voltage, V_{OUT} [1]			4.95	5	5.05	V
Output current, I_{OUT}	V_{IN} = 5.5 V to 36 V, airflow = 100 LFM[2]		0		8	A
Output voltage regulation, ΔV_{OUT}	Load regulation	I_{OUT} = 0 A to 8 A		0.1%		
	Line regulation	V_{IN} = 5.5 V to 36 V		1%		
Output voltage ripple, V_{OUT-AC}	V_{IN} = 12 V, I_{OUT} = 8 A			5		mVrms
Output overcurrent protection, I_{OCP}	V_{IN} = 12 V			10		A
Soft-start time, t_{SS}				3		ms
SYSTEM CHARACTERISTICS						
Switching frequency, F_{SW-nom}	V_{IN} = 12 V			2.1		MHz
Half-load efficiency, η_{HALF} [1]	I_{OUT} = 4 A	V_{IN} = 8 V		94.3%		
		V_{IN} = 12 V		92.9%		
		V_{IN} = 18 V		90.5%		
Full load efficiency, η_{FULL}	I_{OUT} = 8 A	V_{IN} = 8 V		93.5%		
		V_{IN} = 12 V		92.8%		
		V_{IN} = 18 V		90.7%		
LM25149-Q1 junction temperature, T_J			–40		150	°C

(1) The default output voltage of this EVM is 5 V. Efficiency and other performance metrics can change based on operating input voltage, load currents, externally-connected output capacitors, and other parameters.
(2) The recommended airflow when operating at input voltages greater than 18 V is 100 LFM.

3 Application Circuit Diagram

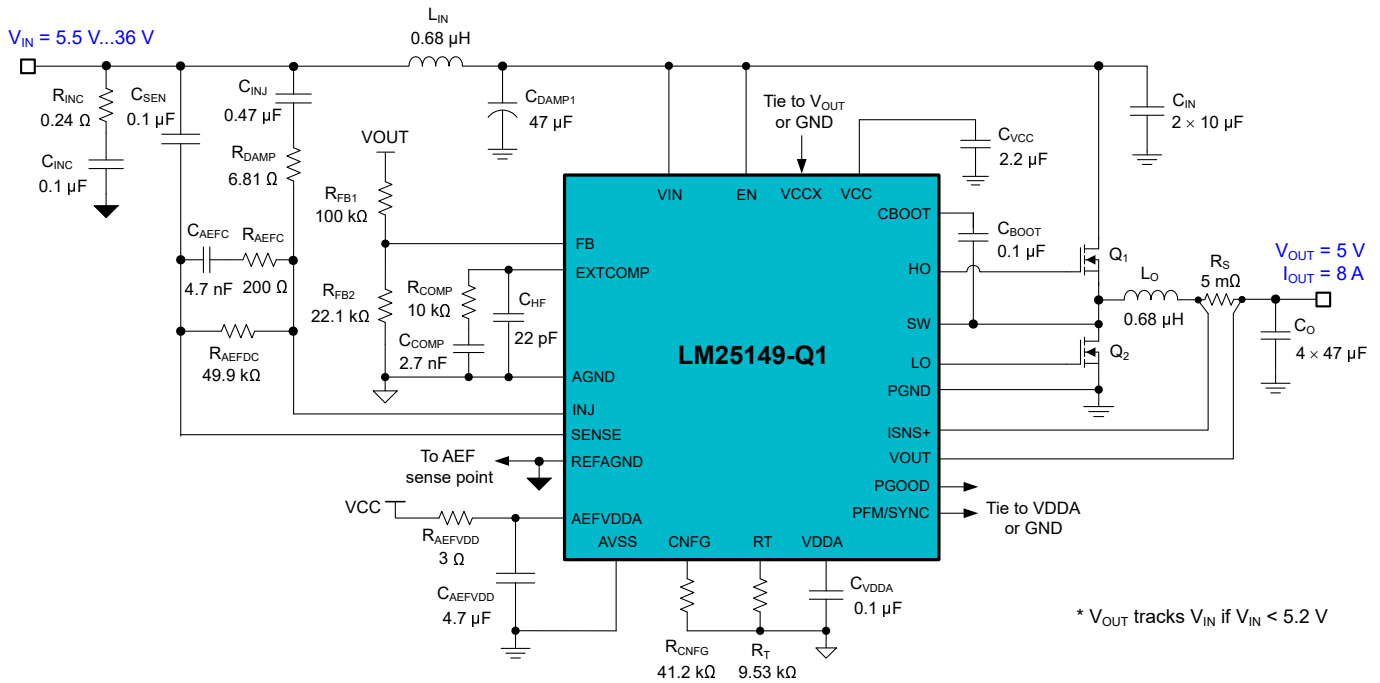Figure 3-1 shows the schematic of an LM25149-Q1-based synchronous buck regulator with active EMI filter.

Figure 3-1. LM25149-Q1 Synchronous Buck Regulator Simplified Schematic

4 EVM Photo
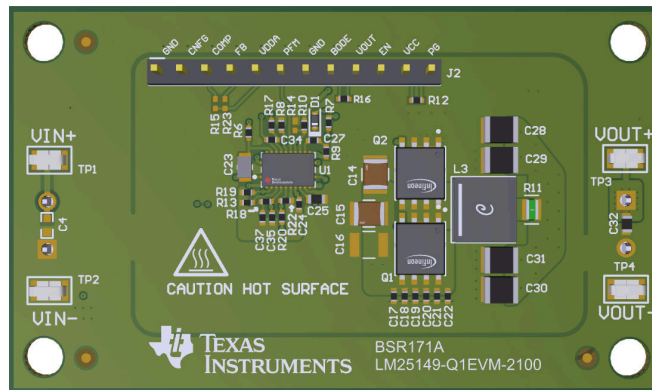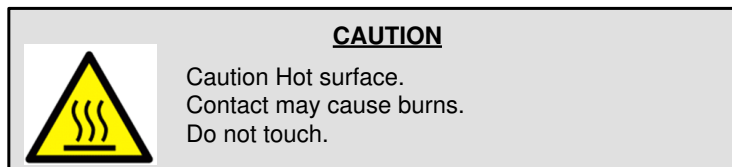
Figure 4-1 shows the EVM photo.

**Figure 4-1. LM25149-Q1 EVM Photo, 70 mm × 40 mm**

CAUTION
Caution Hot surface. Contact may cause burns. Do not touch.

5 Test Setup and Procedure

5.1 EVM Connections

Referencing the EVM connections described in Table 5-1, the recommended test setup to evaluate the LM25149-Q1EVM-2100 is shown in Figure 5-1. Working at an ESD-protected workstation, make sure that any wrist straps, boot straps, or mats are connected and referencing the user to earth ground before handling the EVM.
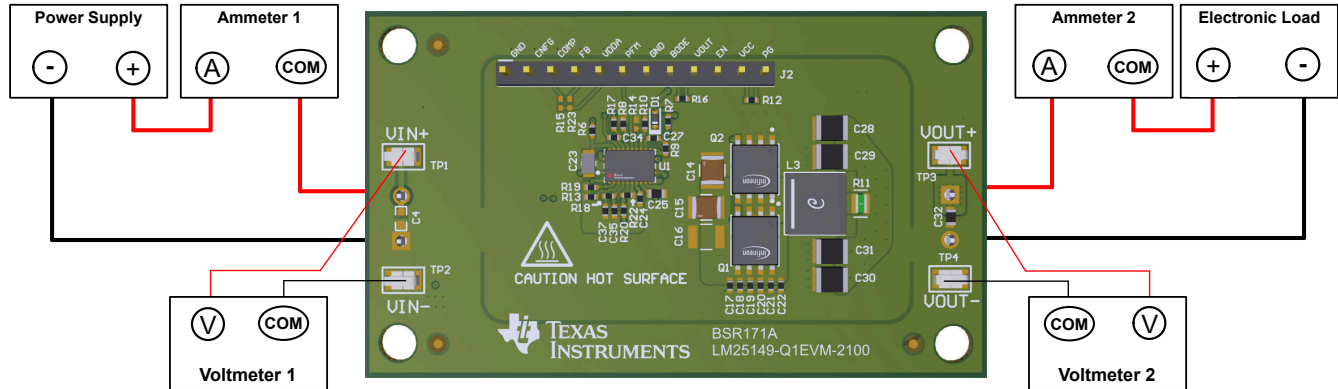
Figure 5-1. EVM Test Setup

CAUTION

Refer to the LM25149-Q1 data sheet, LM25149-Q1 Quickstart Calculator and WEBENCH® Power Designer for additional guidance pertaining to component selection and controller operation.

Table 5-1. EVM Power Connections

Label	Description
VIN+	Positive input voltage power and sense connection
VIN –	Negative input voltage power and sense connection
VOUT+	Positive output voltage power and sense connection
VOUT–	Negative output voltage power and sense connection

Table 5-2. EVM Signal Connections

Label	Description
GND	GND connection
CNFG	Configuration input - tie to GND to disable AEF
COMP	Error amplifier output
FB	FB node
VDDA	Bias supply connection for the analog circuits
PFM	PFM/FPWM selection and Synchronization input
GND	GND connection
BODE	50-Ω injection point for loop response
VOUT	Output voltage
EN	ENABLE input – tie to GND to disable the device
VCC	Bias supply connection for the gate drivers and AEF
PGOOD	Power Good indicator

5.2 Test Equipment

Voltage Source: Use an input voltage source capable of supplying 0 V to 40 V and 12 A.

Multimeters:

- **Voltmeter 1:** Input voltage at VIN+ to VIN–. Set voltmeter to an input impedance of 100 MΩ.
- **Voltmeter 2:** Output voltage at VOUT to GND. Set voltmeter to an input impedance of 100 MΩ.
- **Ammeter 1:** Input current. Set ammeter to 1-second aperture time.
- **Ammeter 2:** Output current. Set ammeter to 1-second aperture time.

Electronic Load: The load must be an electronic constant-resistance (CR) or constant-current (CC) mode load capable of 0 Adc to 10 Adc at 12 V. For a no-load input current measurement, disconnect the electronic load as it may draw a small residual current.

Oscilloscope: With the scope set to 20-MHz bandwidth and AC coupling, measure the output voltage ripple directly across an output capacitor with a short ground lead normally provided with the scope probe. Place the oscilloscope probe tip on the positive terminal of the output capacitor, holding the ground barrel of the probe through the ground lead to the negative terminal of the capacitor. TI does not recommend using a long-leaded ground connection because this can induce additional noise given a large ground loop. To measure other waveforms, adjust the oscilloscope as needed.

Safety: Always use caution when touching any circuits that may be live or energized.

5.3 Recommended Test Setup

5.3.1 Input Connections

- Prior to connecting the DC input source, set the current limit of the input supply to 0.1 A maximum. Ensure the input source is initially set to 0 V and connected to the VIN+ and VIN– connection points as shown in Figure 5-1. An additional input bulk capacitor is recommended to provide damping if long input lines are used.
- Connect voltmeter 1 at VIN+ and VIN– connection points to measure the input voltage.
- Connect ammeter 1 to measure the input current and set to at least 1-second aperture time.

5.3.2 Output Connections

- Connect electronic load to VOUT connection. Set the load to constant-resistance mode or constant-current mode at 0 A before applying input voltage.
- Connect voltmeter 2 at VOUT and GND connections to measure the output voltage.
- Connect ammeter 2 to measure the output current.

5.4 Test Procedure

5.4.1 Line and Load Regulation, Efficiency

- Set up the EVM as previously described.
- Set load to constant resistance or constant current mode and to sink 0 A.
- Increase input source from 0 V to 12 V; use voltmeter 1 to measure the input voltage.
- Increase the current limit of the input supply to 12 A.
- Using voltmeter 2 to measure the output voltage, V_{OUT}, vary the load current from 0 A to 8 A DC; V_{OUT} must remain within the load regulation specification.
- Set the load current to 4 A (50% rated load) and vary the input source voltage from 5.5 V to 36 V; V_{OUT} must remain within the line regulation specification.
- Decrease load to 0 A. Decrease input source voltage to 0 V.

6 Test Data and Performance Curves

Figure 6-1 through Figure 6-15 present typical performance curves for the LM25149-Q1EVM-2100. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and can differ from actual field measurements.

6.1 Conversion Efficiency
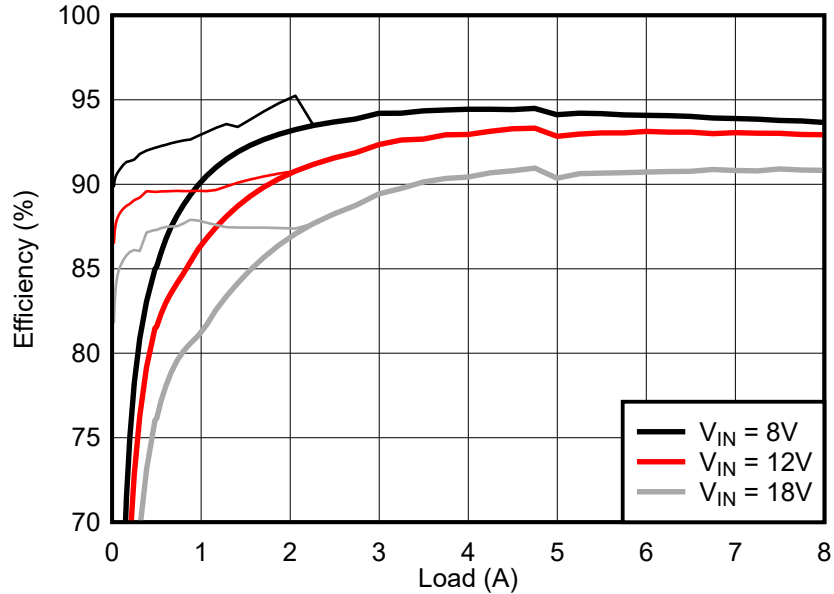
The curves with higher efficiency at light load correspond to when diode emulation is enabled (PFM tied to VDDA).
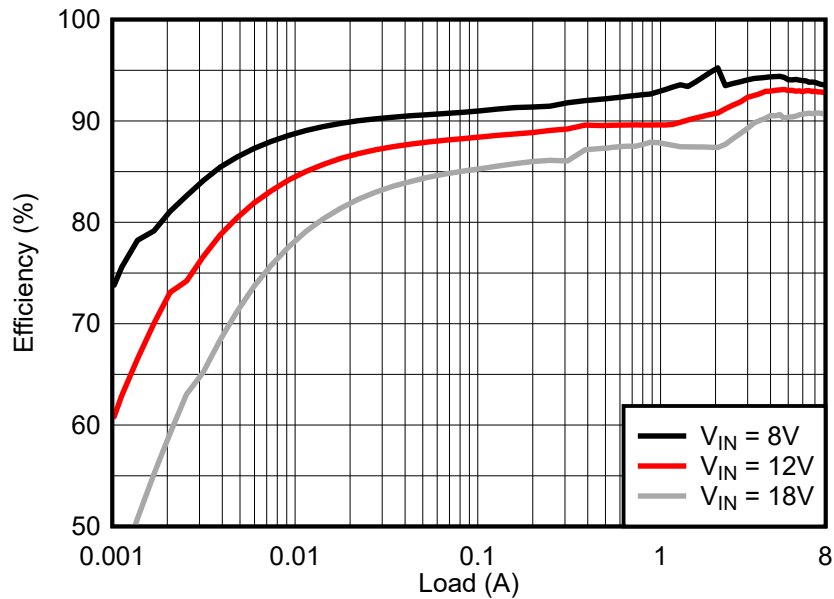
Figure 6-1. Efficiency, V_{OUT} = 5 V

Figure 6-2. Efficiency, V_{IN} = 12 V, V_{OUT} = 5 V, PFM (Log Scale)

6.2 Operating Waveforms

6.2.1 Switching
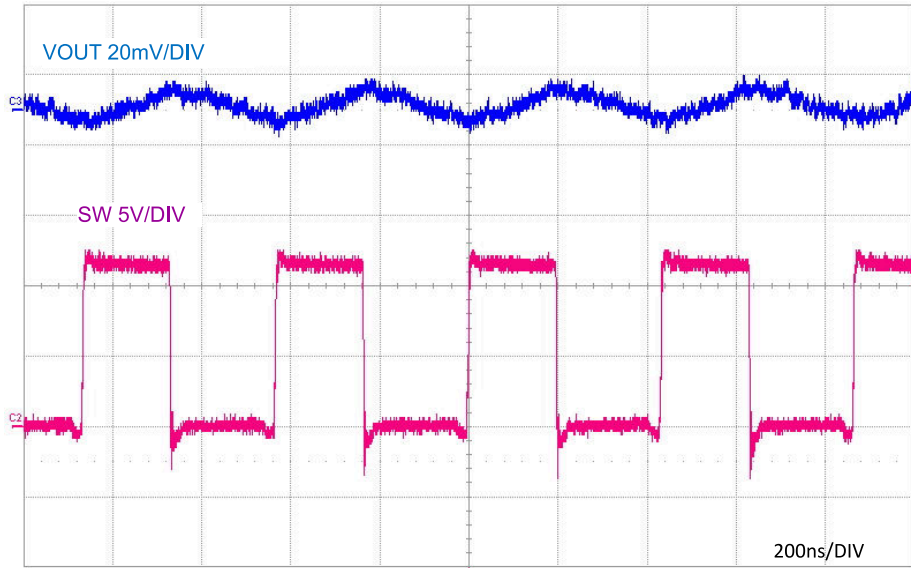
Figure 6-3. SW Node Voltage, V_{IN} = 12 V, I_{OUT} = 8 A
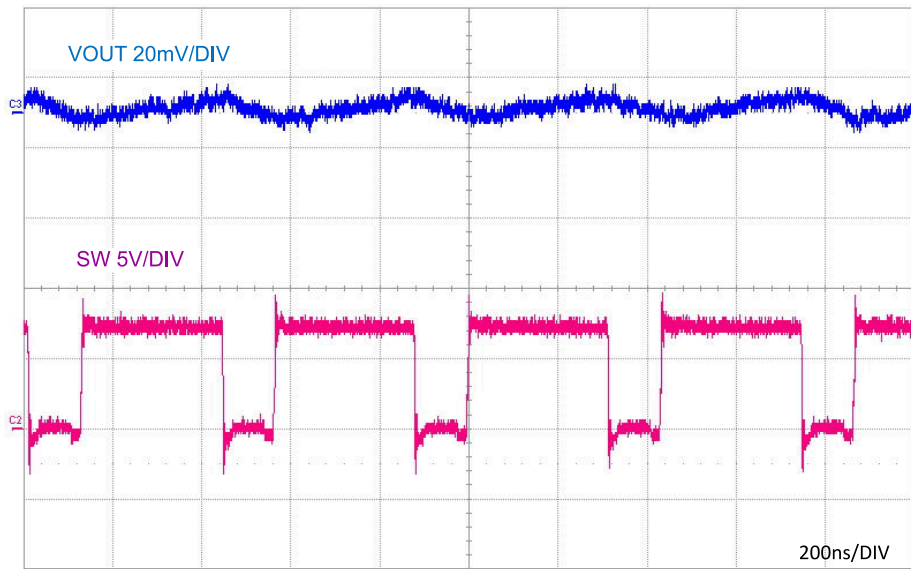
Figure 6-4. SW Node Voltage, V_{IN} = 8 V, I_{OUT} = 8 A
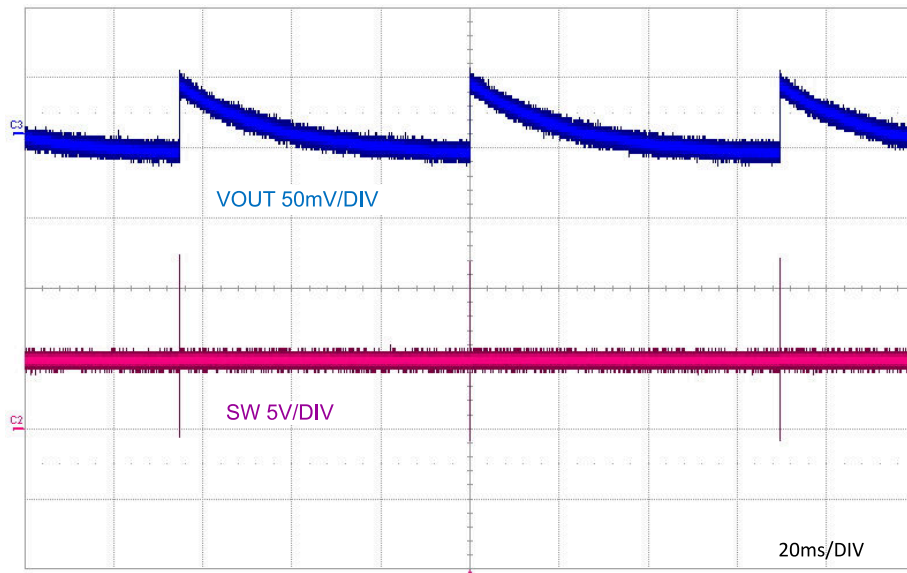
Figure 6-5. PFM Mode SW Node Voltage, V$_{IN}$ = 12 V, I$_{OUT}$ = 0 A

6.2.2 Load Transient Response
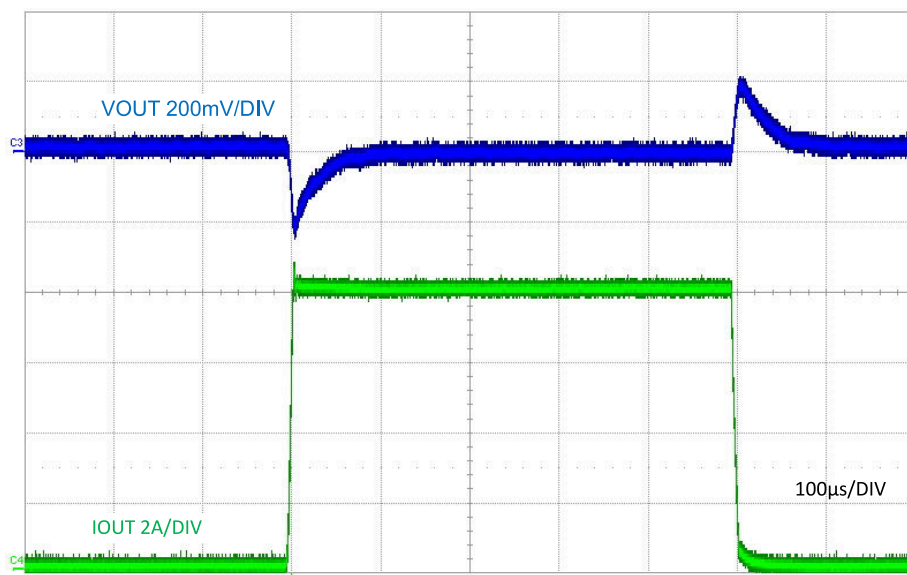
Figure 6-6. Load Transient Response, V$_{IN}$ = 12 V, FPWM, 0 A to 8 A at 1 A/µs
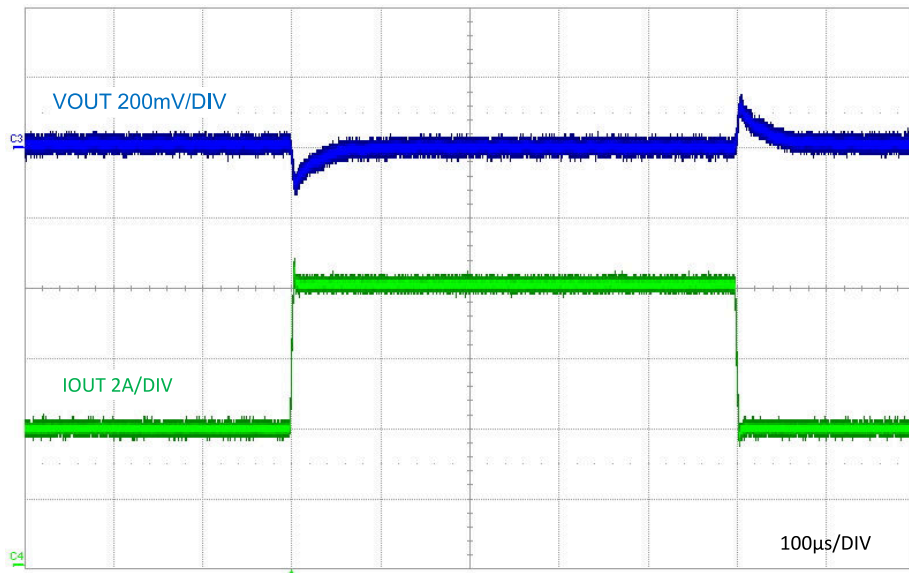
Figure 6-7. Load Transient Response, V$_{IN}$ = 12 V, FPWM, 4 A to 8 A at 1 A/µs

6.2.3 Line Transient Response
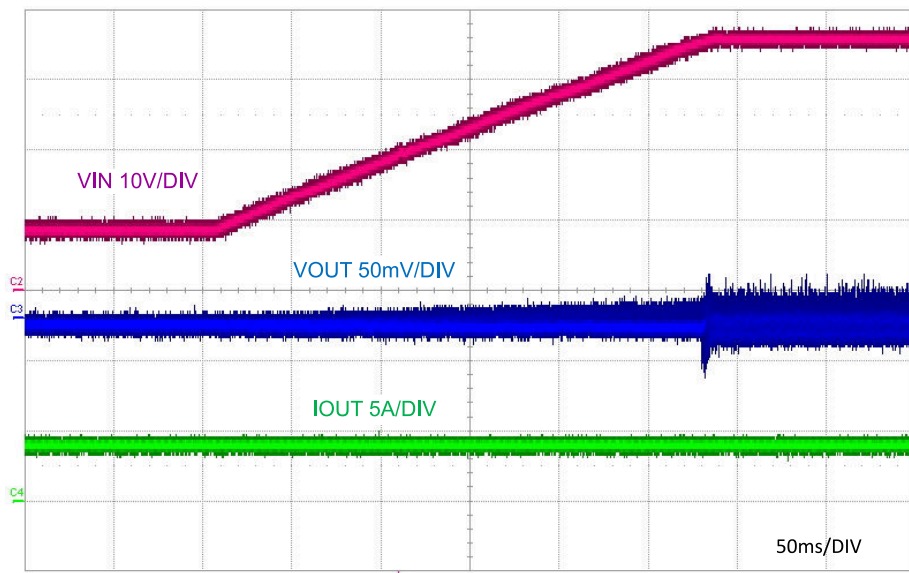
Figure 6-8. Line Transient Response to V$_{IN}$ = 8 V to 36 V, I$_{OUT}$ = 4 A
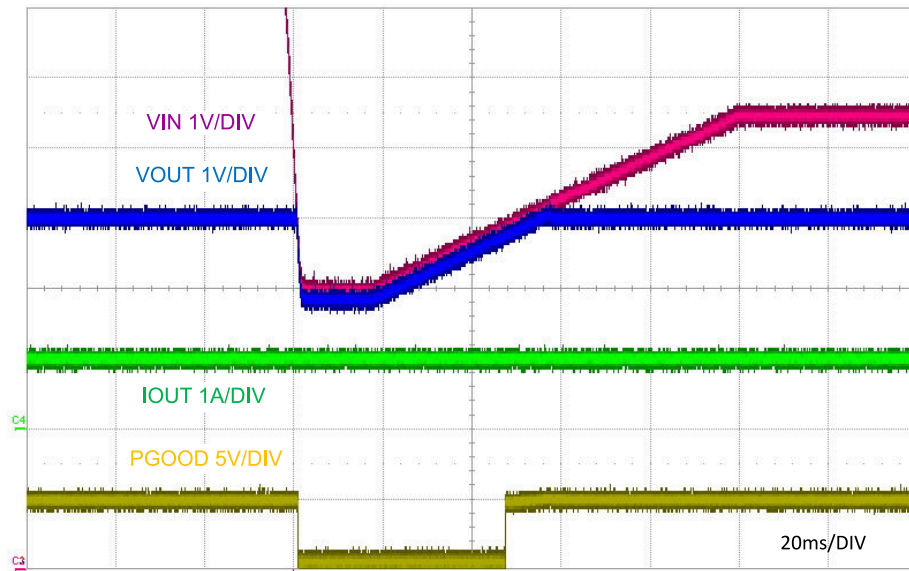
Figure 6-9. Cold-Crank Response to V$_{IN}$ = 3.8 V, I$_{OUT}$ = 1 A CC, EN tied to VIN

6.2.4 Start-Up and Shutdown With ENABLE ON and OFF
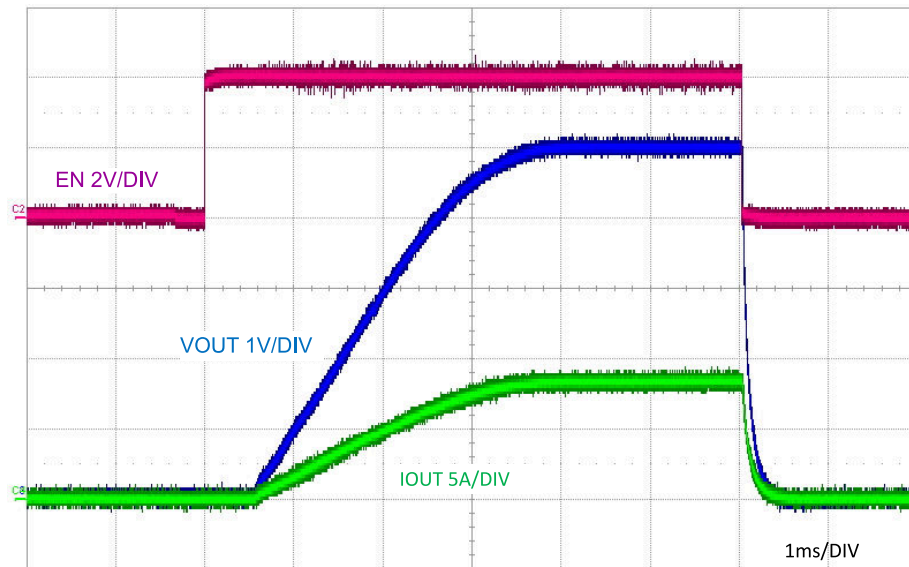
Figure 6-10. ENABLE ON and OFF, V$_{IN}$ = 12 V, I$_{OUT}$ = 8 A

6.2.5 Start-Up and Shutdown with EN Tied to VIN
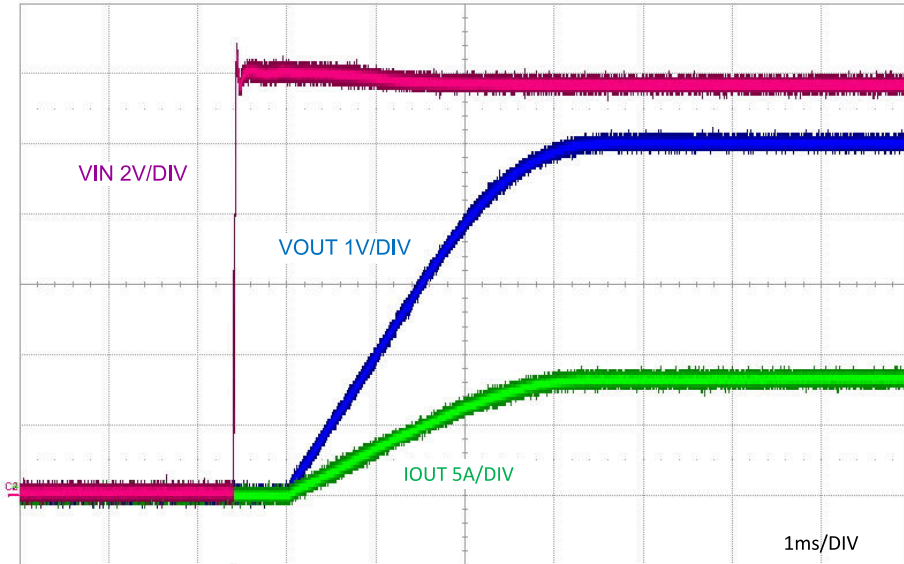
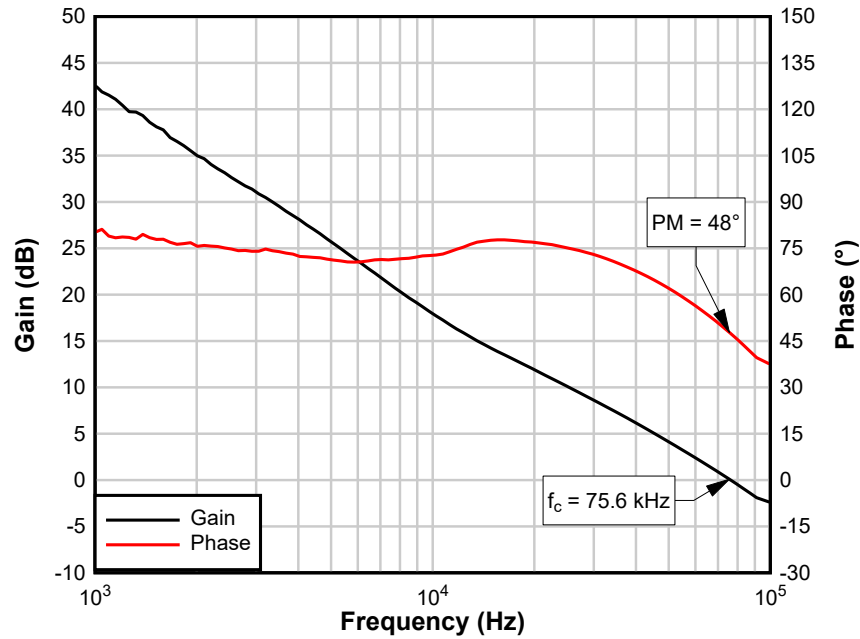**Figure 6-11. Start-Up, V$_{IN}$ = 12 V, I$_{OUT}$ = 8-A Resistive Load**
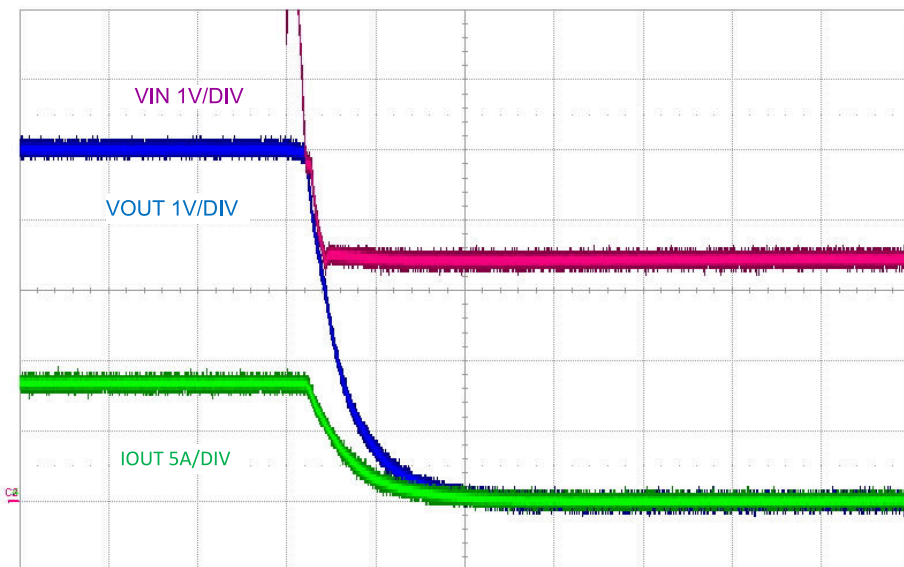
Figure 6-12. Shutdown, V$_{IN}$ = 12 V, I$_{OUT}$ = 8-A Resistive Load

6.3 Bode Plot


f_c = crossover frequency, PM = phase margin

Figure 6-13. Bode Plot, V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 8-A Resistive Load

6.4 CISPR 25 EMI Performance

Figure 6-14 presents the EMI performance of the LM25149-Q1 EVM at 12-V input with and without the EMI mitigation techniques enabled. Conducted emissions are measured over a frequency range of 150 kHz to 30 MHz using a 5-µH LISN according to the CISPR 25 low-frequency specification. CISPR 25 class 5 peak and average limit lines are denoted in red. The yellow and blue spectra are measured using peak and average detection, respectively.
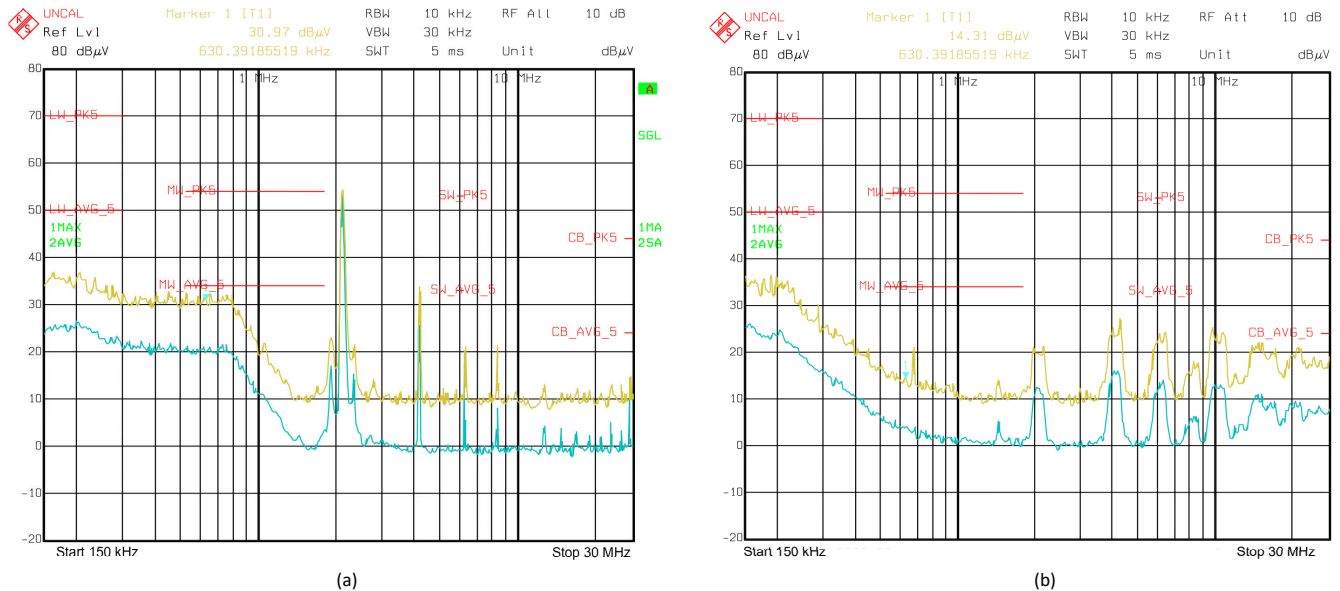
Figure 6-14. CISPR 25 Class 5 Conducted Emissions Plot, 150 kHz to 30 MHz, V_{IN} = 12 V, I_{OUT} = 8 A Resistive Load, (a) No EMI Mitigation, (b) Active EMI and Spread-Spectrum Enabled

6.5 Thermal Performance

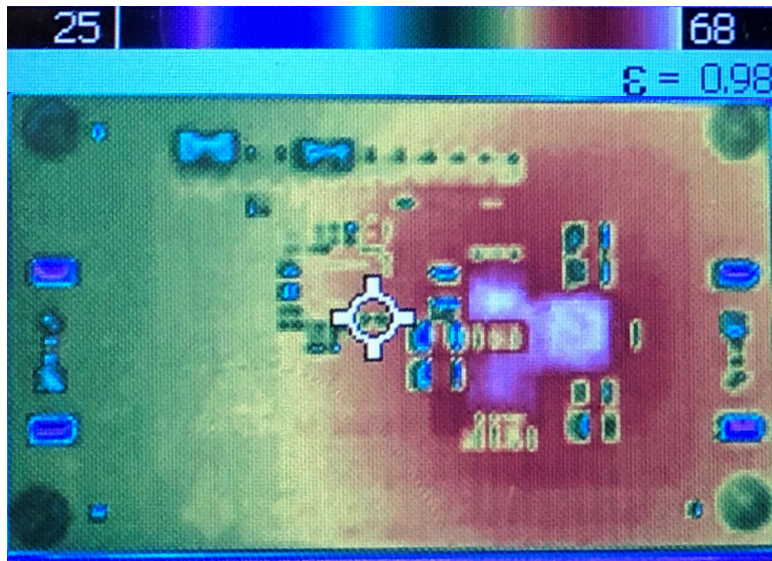Figure 6-15 shows the thermal performance image.

Figure 6-15. Thermal Performance, V_{IN} = 12 V, I_{OUT} = 8 A, T_{amb} = 25°C, Free Convection Airflow

7 EVM Documentation
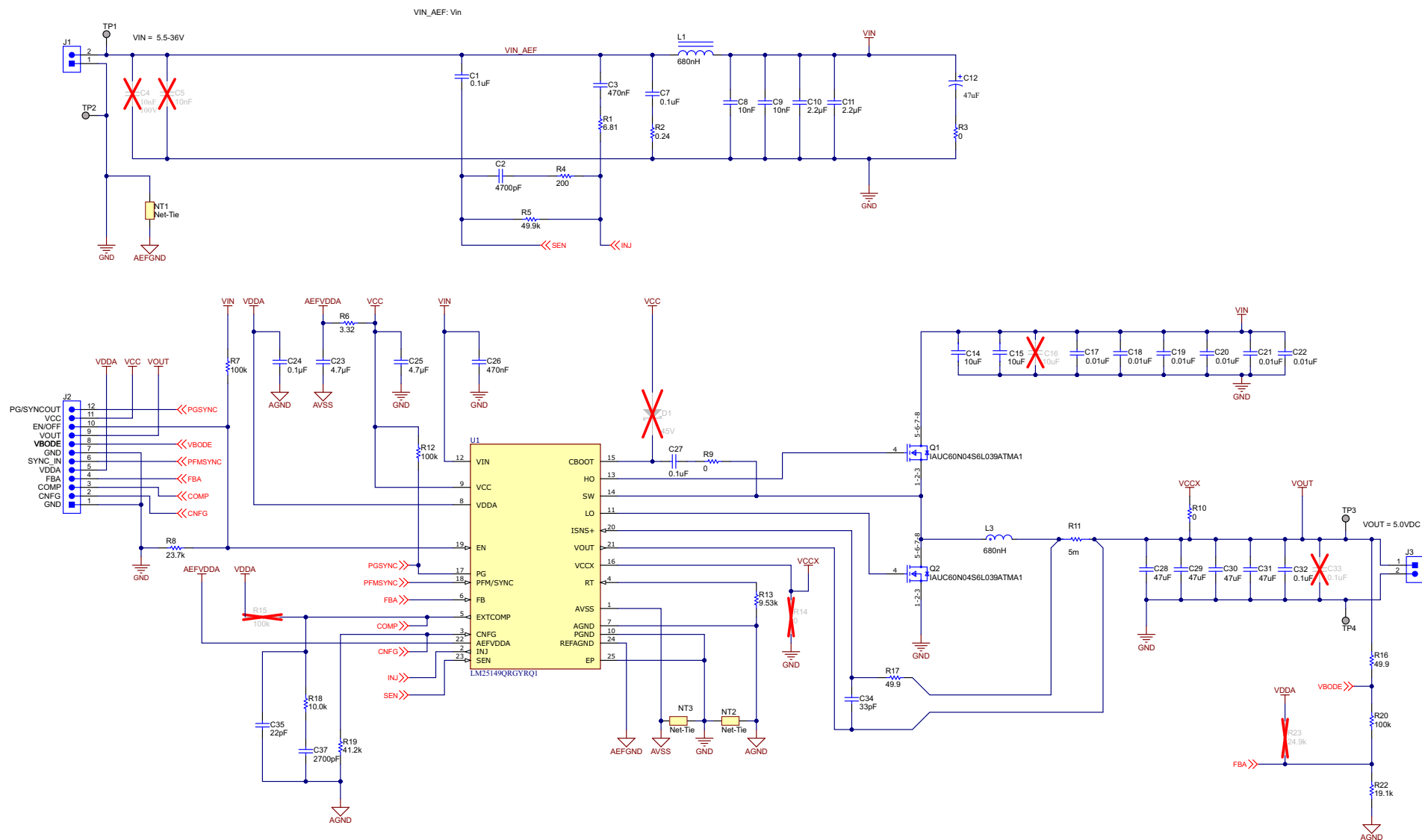
7.1 Schematic

Figure 7-1 shows the EVM schematic.

Figure 7-1. EVM Schematic

7.2 Bill of Materials

Table 7-1. Bill of Materials

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
3	C1, C7, C27	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 0402, AEC-Q200	CGA2B3X7R1H104K050BB	TDK
1	C2	Capacitor, Ceramic, 4700 pF, 50 V, X7R, 0402, AEC-Q200	CGA6P1X7S0J476M250AC	TDK
1	C3	Capacitor, Ceramic, 0.47 µF, 50 V, X7R, 0603	CGA3E3X7R1H474K080AB	TDK
2	C8, C9	Capacitor, Ceramic, 0.01 µF, 50 V, X7R, 0603	C1608X7R1H103K080AA	TDK
2	C10, C11	Capacitor, Ceramic, 2.2 µF, 50 V, X7R, 0805	UMK212BB7225KG-T	Taiyo Yuden
1	C12	Capacitor, Aluminum, 47 µF, 50 V, 0.68 Ω, AEC-Q200	EEE-FK1H470P	Panasonic
2	C14, C15	Capacitor, Ceramic, 10 µF, 50 V, X7R, 1210, AEC-Q200	12105C106K4Z2A	AVX
			CNA6P1X7R1H106K250AE	TDK
		Capacitor, Ceramic, 10 µF, 50 V, X7R, 1206, AEC-Q200	CGA5L1X7R1H106K160AC	TDK
6	C17, C18, C19, C20, C21, C22	Capacitor, Ceramic, 0.01 µF, 50 V, X7R, 0402 AEC-Q200	CGA2B3X7R1H103K050BB	TDK
1	C23	Capacitor, Ceramic, 4.7 µF, 25 V, X7R, 0805,AEC-Q200	CGA4J1X7R1E475K125AC	TDK
1	C24	Capacitor, Ceramic, 0.1 µF, 10 V, X7R, 0402, AEC-Q200	Std	Std
1	C25	Capacitor, Ceramic, 4.7 µF, 10 V, X7R, 0603	GRM188Z71A475ME15D	Murata
1	C26	Capacitor, Ceramic, 0.47 µF, 50 V, X7R, 0805 AEC-Q200	GCM21BR71H474KA55L	Murata
4	C28, C29, C30, C31	Capacitor, Ceramic, 47 µF, 10 V, X7R, 1210	GRM32ER71A476KE15L	Murata
1	C32, C33	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, 0603	C0603C104K5RAC-TU	KEMET
1	C34	Capacitor, Ceramic, 33 pF, 50 V, C0G/NP0, 0402, AEC-Q200	GCM1555C1H330JA16D	Murata
1	C35	Capacitor, Ceramic, 22 pF, 50 V, C0G/NP0, 0402, AEC-Q200	CGA2B2NP01H220J050BA	TDK
1	C37	Capacitor, Ceramic, 2700 pF, 50 V, X7R, 0402	CL05B272KB5NNNC	Samsung
4	H3, H4, H5, H6	Standoff, Hex, 0.5"L #4-40 Nylon	18K5088	
4	H7, H8, H9, H10	Screw, Pan Head , 4-40, 3/8", Nylon	H544-ND	
2	J1, J3	Terminal Block, 2 position, 5 mm, TH	Std	Std
1	J2	Header, 100 mil, 10×1, Au, TH	PBC12SABN	TSW-110-07-G-S
1	L1	Inductor, 0.68 µH, 9 mΩ typ, 8.2 A, 6 mm typ,	744383560068	Würth Electronik
1	L3	Inductor, 0.68 µH, 2.9 mΩ typ, 15.3 A, 3.1 mm typ, AEC-Q200	XGL6030-681MEB	Coilcraft
		Inductor, 0.56 µH, 3.6 mΩ typ, 13 A, 4.8 mm typ, AEC-Q200	744373490056	Würth Electronik
		Inductor, 0.68 µH, 5 mΩ typ, 15.5 A, 3 mm typ	IHLP2525CZERR68M01	Vishay
2	Q1, Q2	MOSFET, N-Channel, 40 V, 4 mΩ, AEC-Q101	IAUC60N04S6L039	Infineon
1	R1	Resistor, Chip, 6.81 Ω, 1/10W, 1%, 0603	Std	Std
1	R2	Resistor, Chip, 0.24 Ω, 1/4W, 5%, 0603	Std	Std
1	R3	Resistor, Chip, 0 Ω, 1/8W, 1%, 0805	Std	Std
1	R4	Resistor, Chip, 200 Ω, 1/16W, 1%, 0402	Std	Std
1	R5	Resistor, Chip, 49.9 kΩ, 1/8W, 1%, 0402	Std	Std
1	R6	Resistor, Chip, 3.32 Ω, 1/16W, 1%, 0402	Std	Std
3	R7, R12, R20	Resistor, Chip, 100 kΩ, 1/16W, 1%, 0402	Std	Std
1	R8	Resistor, Chip, 22.1 kΩ, 1/16W, 1%, 0402	Std	Std
3	R9, R10, R14	Resistor, Chip, 0 kΩ, 1/5W, 1%, 0603	Std	Std
1	R11	Resistor, Chip, 5 mΩ, 1W, 1%, 0508, AEC-Q200	KRL2012E-M-R005-F-T5	Susumu
1	R13	Resistor, Chip, 9.53 kΩ, 1/16W, 1%, 0402	Std	Std
2	R16, R17	Resistor, Chip, 49.9 Ω, 1/16W, 1%, 0402	Std	Std
1	R18	Resistor, Chip, 10 kΩ, 1/16W, 1%, 0402	Std	Std
1	R19	Resistor, Chip, 41.2 kΩ, 1/16W, 1%, 0402	Std	Std
1	R22	Resistor, Chip, 19.1 kΩ, 1/16 W, 1%, 0402	Std	Std
1	R23	Resistor, Chip, 24.9 kΩ, 1/16 W, 1%, 0402	Std	Std
4	TP1, TP2, TP3, TP4	Test Point, Miniature, SMT	5019	Keystone
1	U1	IC, LM25149-Q1, 42-V Synchronous Buck Controller, VQFN-24	LM25149QRGYRQ1	TI
1	PCB1	PCB, FR4, 6 layer, 2 oz, 70 mm × 40 mm	PCB	—

7.3 PCB Layout

Figure 7-2 through Figure 7-9 show the design of the LM25149-Q1 EVM using a six-layer PCB with 2-oz copper thickness. The power stage is essentially a single-sided design and the input filtering is located on the bottom side.
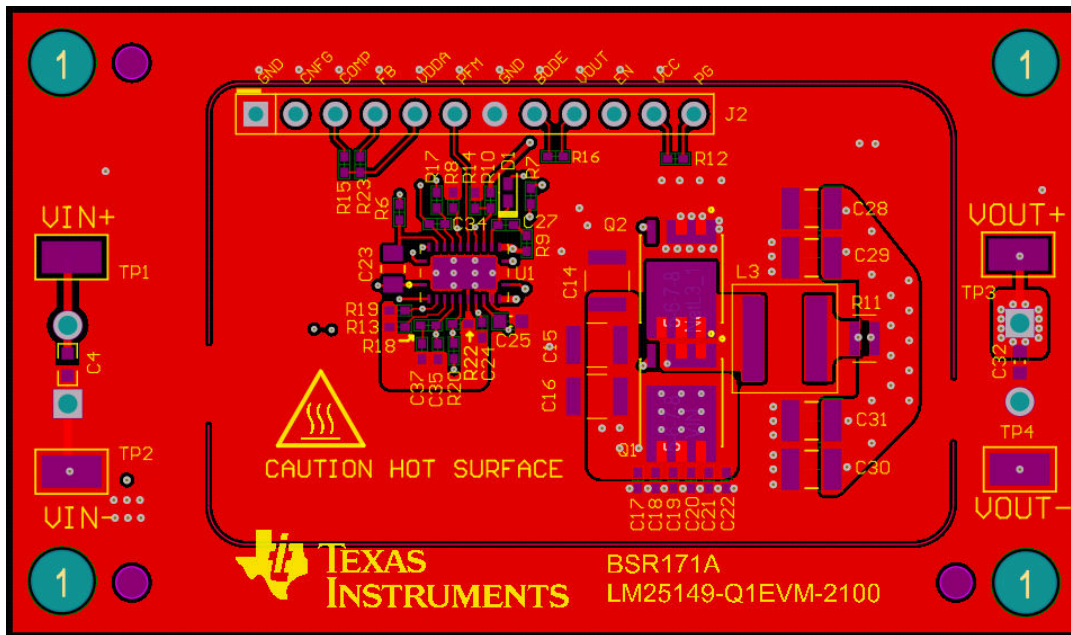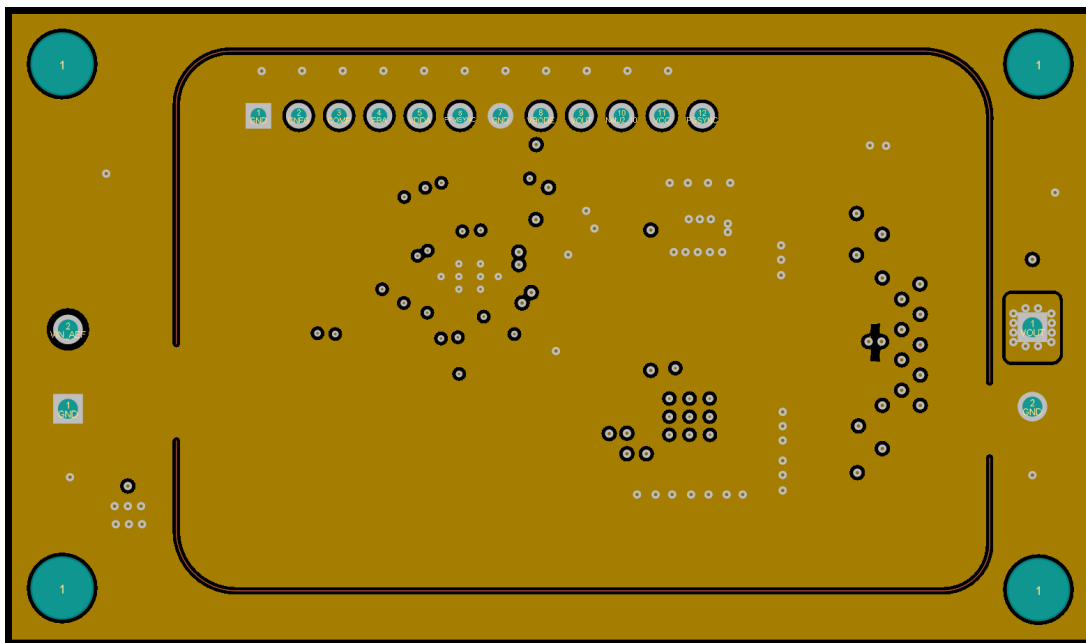

Figure 7-2. Top Copper (Top View)

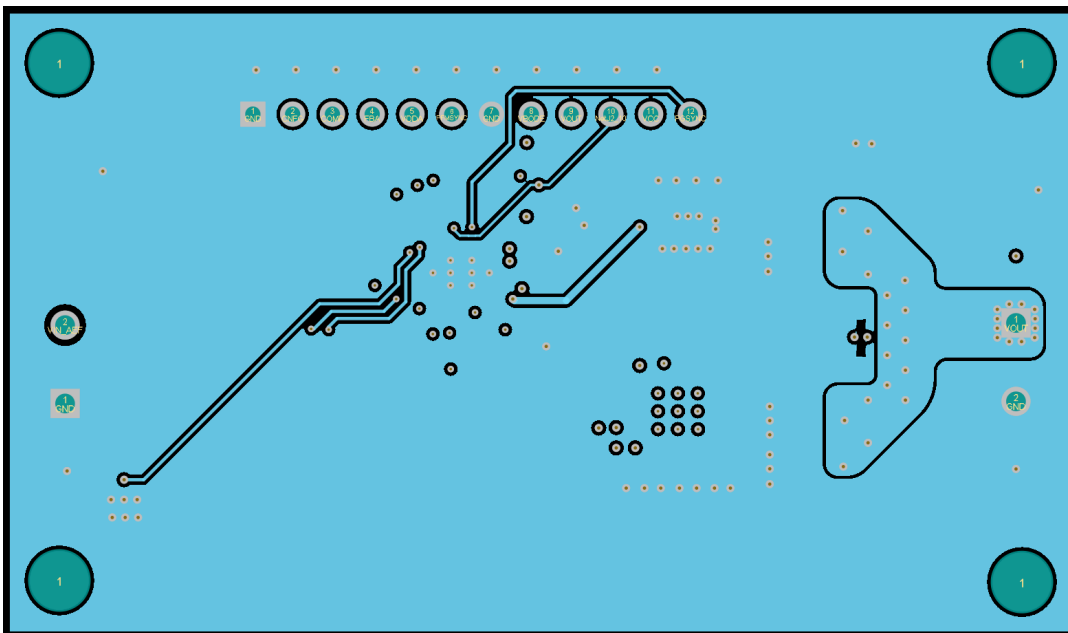
Figure 7-3. Layer 2 Copper (Top View)

Figure 7-4. Layer 3 Copper (Top View)
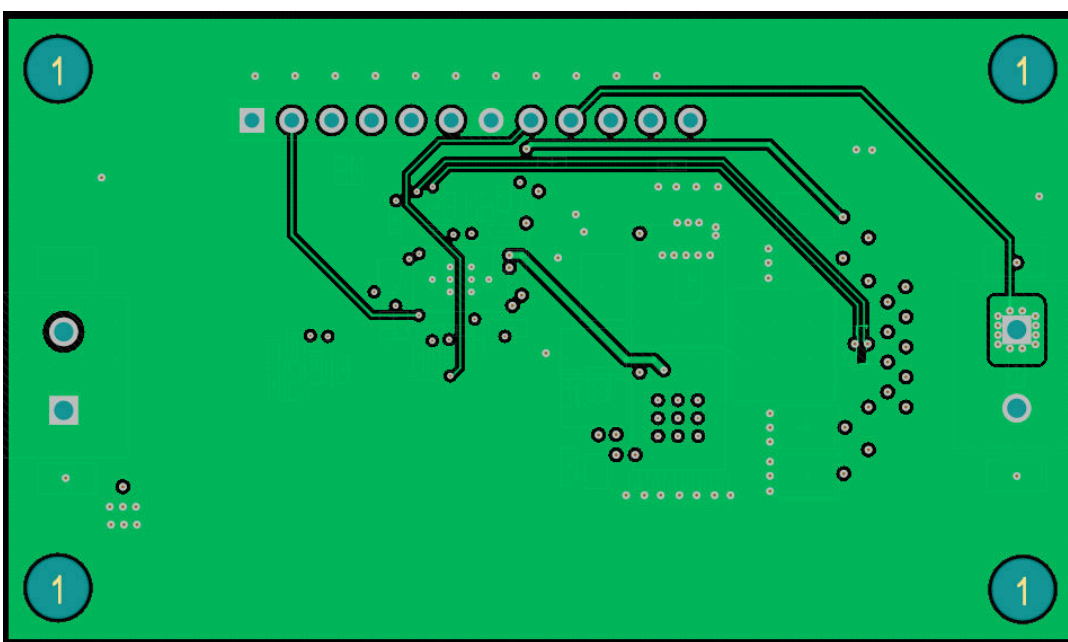
Figure 7-5. Layer 4 Copper (Top View)
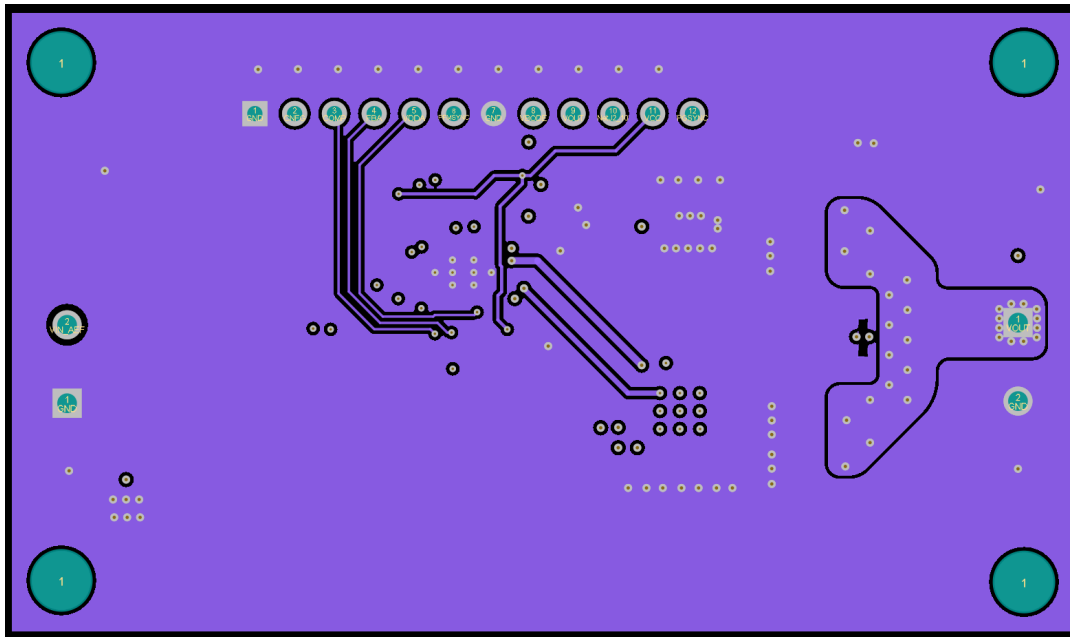
Figure 7-6. Layer 5 Copper (Top View)
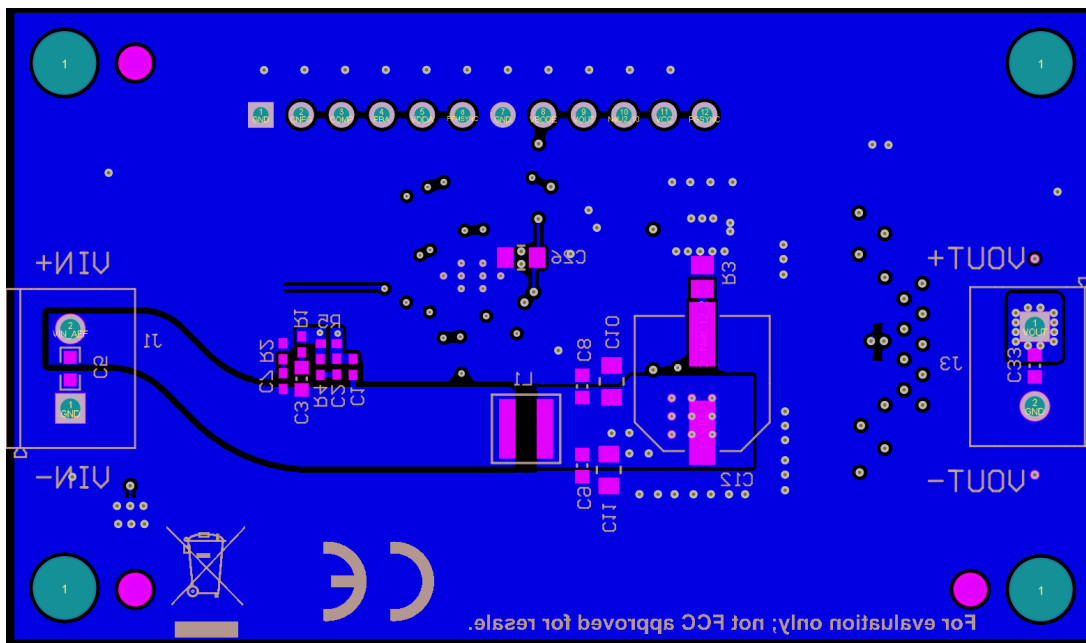
Figure 7-7. Bottom Copper (Top View)

7.4 Component Drawings
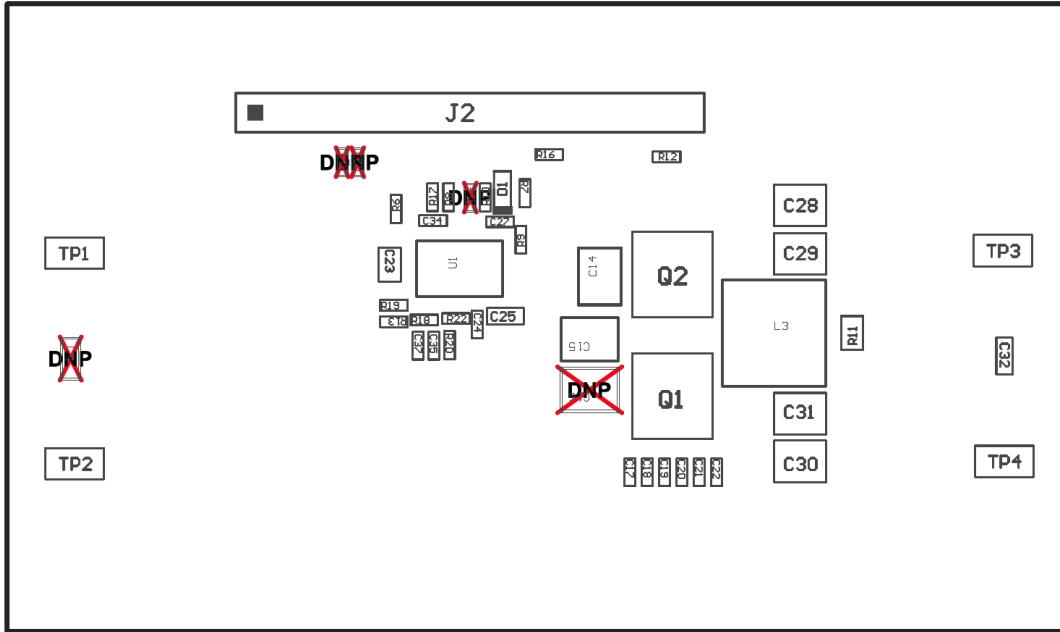
Figure 7-8. Top Component Drawing
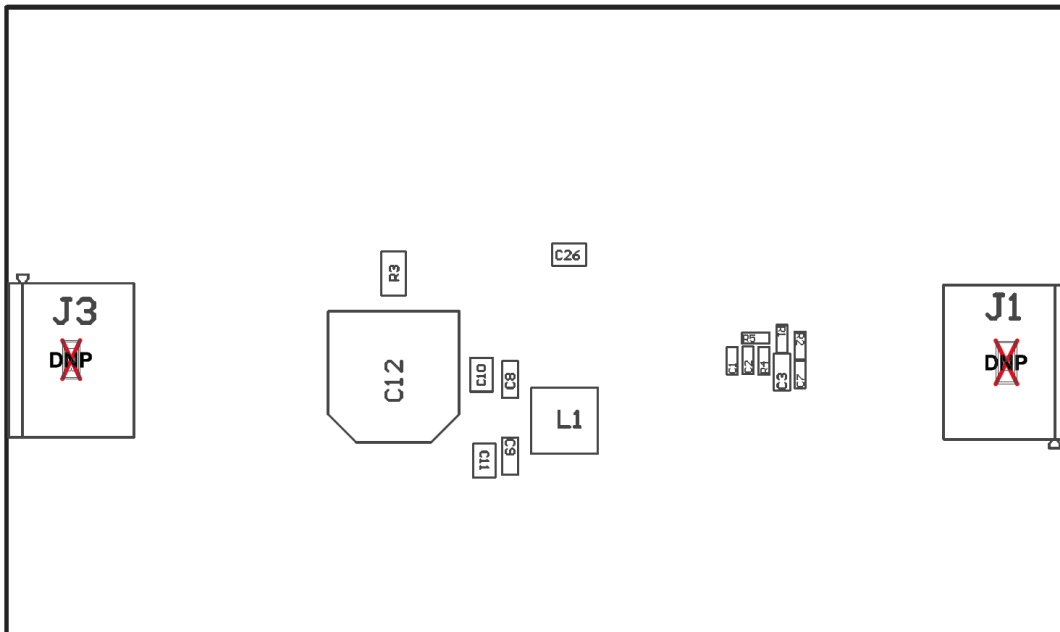
Figure 7-9. Bottom Component Drawing

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

For development support see the following:

- For TI's reference design library, visit TI reference designs
- For TI's WEBENCH Design Environments, visit the WEBENCH® Design Center
- LM25149-Q1 DC/DC Controller Quickstart Calculator

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- *LM25149-Q1 3.5-V to 42-V Synchronous Buck DC/DC Controller Data Sheet*
- *Improve High-current DC/DC Regulator Performance for Free with Optimized Power Stage Layout Application Brief*
- *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics Analog Applications Journal*
- *AN-2162 Simple Success with Conducted EMI from DC-DC Converters Application Report*
- White Papers:
  - *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*
  - *An Overview of Conducted EMI Specifications for Power Supplies*
  - *An Overview of Radiated EMI Specifications for Power Supplies*

8.2.1.1 PCB Layout Resources

- *AN-1149 Layout Guidelines for Switching Power Supplies Application Report*
- *AN-1229 Simple Switcher PCB Layout Guidelines Application Report*
- *Constructing Your Power Supply – Layout Considerations Power Supply Design Seminar*
- *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x Application Report*
- Power House Blogs:
  - *High-Density PCB Layout of DC-DC Converters*

8.2.1.2 Thermal Design Resources

- *AN-2020 Thermal Design by Insight, Not Hindsight Application Report*
- *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- *Semiconductor and IC Package Thermal Metrics Application Report*
- *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- *PowerPAD Thermally Enhanced Package Application Report*
- *PowerPAD Made Easy Application Brief*
- *Using New Thermal Metrics Application Report*

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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