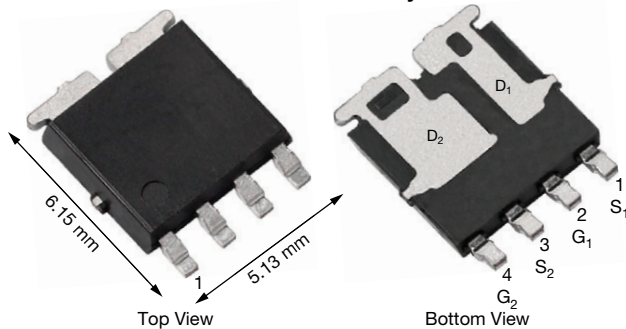


# Automotive Dual N-Channel 12 V (D-S) 175 °C MOSFETs

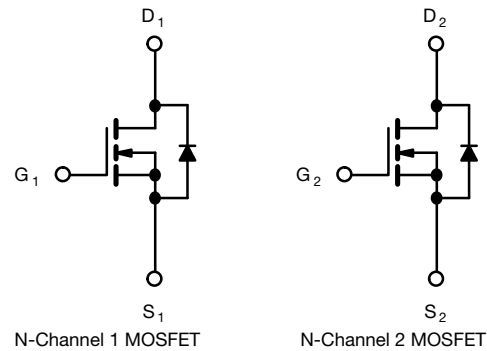
**PowerPAK® SO-8L Dual Asymmetric**

**FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>g</sub> and UIS tested
- Optimized for synchronous buck applications
- Material categorization:  
for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

 AUTOMOTIVE  
GRADE

**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

PRODUCT SUMMARY		
	N-CHANNEL 1	N-CHANNEL 2
V <sub>DS</sub> (V)	12	12
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 10 V	0.0083	0.0030
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 4.5 V	0.0093	0.0035
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 3.3 V	0.0103	0.0041
I <sub>D</sub> (A)	20	60
Configuration	Dual	
Package	PowerPAK SO-8L Dual Asymmetric	



ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT
Drain-source voltage	V <sub>DS</sub>	12	12	V
Gate-source voltage	V <sub>GS</sub>	± 12		
Continuous drain current	I <sub>D</sub>	T <sub>C</sub> = 25 °C	20 <sup>a</sup>	A
		T <sub>C</sub> = 125 °C	20 <sup>a</sup>	
Continuous source current (diode conduction)	I <sub>S</sub>	20 <sup>a</sup>	44	A
Pulsed drain current <sup>b</sup>	I <sub>DM</sub>	80	175	
Single pulse avalanche current	I <sub>AS</sub>	25	50	mJ
Single pulse avalanche energy	E <sub>AS</sub>	31.2	125	
Maximum power dissipation <sup>b</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	27	W
		T <sub>C</sub> = 125 °C	9	
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175		°C
Soldering recommendations (peak temperature) <sup>d, e</sup>		260		

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT
Junction-to-ambient	R <sub>thJA</sub>	85	85	°C/W
Junction-to-case (drain)	R <sub>thJC</sub>	5.5	3.1	

**Notes**

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



<b>SPECIFICATIONS</b> ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		N-Ch 1	12	-	-
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		N-Ch 2	12	-	-
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		N-Ch 1	0.5	1	1.5
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		N-Ch 2	0.5	1	1.5
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		N-Ch 1	-	-	$\pm 100$
				N-Ch 2	-	-	$\pm 100$
Zero gate voltage drain current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 12\text{ V}$	N-Ch 1	-	-	1
		$V_{GS} = 0\text{ V}$	$V_{DS} = 12\text{ V}$	N-Ch 2	-	-	1
		$V_{GS} = 0\text{ V}$	$V_{DS} = 12\text{ V}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 1	-	-	50
		$V_{GS} = 0\text{ V}$	$V_{DS} = 12\text{ V}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 2	-	-	50
		$V_{GS} = 0\text{ V}$	$V_{DS} = 12\text{ V}, T_J = 175\text{ }^\circ\text{C}$	N-Ch 1	-	-	300
		$V_{GS} = 0\text{ V}$	$V_{DS} = 12\text{ V}, T_J = 175\text{ }^\circ\text{C}$	N-Ch 2	-	-	300
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	N-Ch 1	15	-	-
		$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	N-Ch 2	30	-	-
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 4\text{ A}$	N-Ch 1	-	0.00675	0.00830
		$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}$	N-Ch 2	-	0.00246	0.00300
		$V_{GS} = 10\text{ V}$	$I_D = 4\text{ A}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 1	-	-	0.01250
		$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}, T_J = 125\text{ }^\circ\text{C}$	N-Ch 2	-	-	0.00470
		$V_{GS} = 10\text{ V}$	$I_D = 4\text{ A}, T_J = 175\text{ }^\circ\text{C}$	N-Ch 1	-	-	0.01460
		$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}, T_J = 175\text{ }^\circ\text{C}$	N-Ch 2	-	-	0.00560
		$V_{GS} = 4.5\text{ V}$	$I_D = 3\text{ A}$	N-Ch 1	-	0.00755	0.00930
		$V_{GS} = 4.5\text{ V}$	$I_D = 8\text{ A}$	N-Ch 2	-	0.00285	0.00350
		$V_{GS} = 3.3\text{ V}$	$I_D = 2\text{ A}$	N-Ch 1	-	0.00835	0.01030
		$V_{GS} = 3.3\text{ V}$	$I_D = 5\text{ A}$	N-Ch 2	-	0.00335	0.00410
Forward transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 4\text{ A}$		N-Ch 1	-	38	-
		$V_{DS} = 10\text{ V}, I_D = 10\text{ A}$		N-Ch 2	-	66	-
<b>Dynamic <sup>b</sup></b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 6\text{ V}, f = 1\text{ MHz}$	N-Ch 1	-	995	1400
		$V_{GS} = 0\text{ V}$	$V_{DS} = 6\text{ V}, f = 1\text{ MHz}$	N-Ch 2	-	2687	3700
Output capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 6\text{ V}, f = 1\text{ MHz}$	N-Ch 1	-	469	700
		$V_{GS} = 0\text{ V}$	$V_{DS} = 6\text{ V}, f = 1\text{ MHz}$	N-Ch 2	-	1240	1700
Reverse transfer capacitance	$C_{rss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 6\text{ V}, f = 1\text{ MHz}$	N-Ch 1	-	233	400
		$V_{GS} = 0\text{ V}$	$V_{DS} = 6\text{ V}, f = 1\text{ MHz}$	N-Ch 2	-	619	900
Total gate charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = 6\text{ V}, I_D = 2\text{ A}$	N-Ch 1	-	12.3	20
		$V_{GS} = 10\text{ V}$	$V_{DS} = 6\text{ V}, I_D = 4\text{ A}$	N-Ch 2	-	32.3	50
Gate-source charge <sup>c</sup>	$Q_{gs}$	$V_{GS} = 10\text{ V}$	$V_{DS} = 6\text{ V}, I_D = 2\text{ A}$	N-Ch 1	-	1.8	-
		$V_{GS} = 10\text{ V}$	$V_{DS} = 6\text{ V}, I_D = 4\text{ A}$	N-Ch 2	-	4.9	-
Gate-drain charge <sup>c</sup>	$Q_{gd}$	$V_{GS} = 10\text{ V}$	$V_{DS} = 6\text{ V}, I_D = 2\text{ A}$	N-Ch 1	-	2.4	-
		$V_{GS} = 10\text{ V}$	$V_{DS} = 6\text{ V}, I_D = 4\text{ A}$	N-Ch 2	-	6.6	-
Gate resistance	$R_g$	$f = 1\text{ MHz}$		N-Ch 1	1.05	2.15	3.3
				N-Ch 2	0.4	0.88	1.4



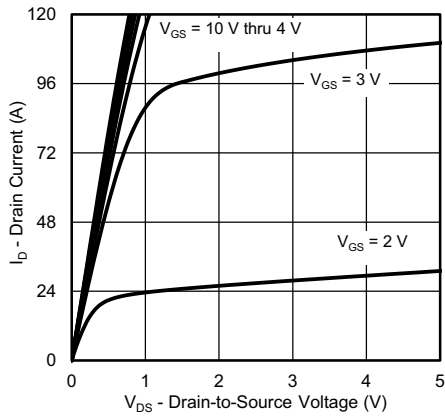
<b>SPECIFICATIONS</b> ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Dynamic <sup>b</sup></b>							
Turn-on delay time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 6\text{ V}$ , $R_L = 3\ \Omega$ , $I_D \cong 2\text{ A}$ , $V_{GEN} = 6\text{ V}$ , $R_g = 1\ \Omega$	N-Ch 1	-	10	15	ns
		$V_{DD} = 6\text{ V}$ , $R_L = 1.5\ \Omega$ , $I_D \cong 4\text{ A}$ , $V_{GEN} = 6\text{ V}$ , $R_g = 1\ \Omega$	N-Ch 2	-	17	30	
Rise time <sup>c</sup>	$t_r$	$V_{DD} = 6\text{ V}$ , $R_L = 3\ \Omega$ , $I_D \cong 2\text{ A}$ , $V_{GEN} = 6\text{ V}$ , $R_g = 1\ \Omega$	N-Ch 1	-	5	10	
		$V_{DD} = 6\text{ V}$ , $R_L = 1.5\ \Omega$ , $I_D \cong 4\text{ A}$ , $V_{GEN} = 6\text{ V}$ , $R_g = 1\ \Omega$	N-Ch 2	-	27	45	
Turn-off delay time <sup>c</sup>	$t_{d(off)}$	$V_{DD} = 6\text{ V}$ , $R_L = 3\ \Omega$ , $I_D \cong 2\text{ A}$ , $V_{GEN} = 6\text{ V}$ , $R_g = 1\ \Omega$	N-Ch 1	-	22	35	
		$V_{DD} = 6\text{ V}$ , $R_L = 1.5\ \Omega$ , $I_D \cong 4\text{ A}$ , $V_{GEN} = 6\text{ V}$ , $R_g = 1\ \Omega$	N-Ch 2	-	34	55	
Fall time <sup>c</sup>	$t_f$	$V_{DD} = 6\text{ V}$ , $R_L = 3\ \Omega$ , $I_D \cong 2\text{ A}$ , $V_{GEN} = 6\text{ V}$ , $R_g = 1\ \Omega$	N-Ch 1	-	5	10	
		$V_{DD} = 6\text{ V}$ , $R_L = 1.5\ \Omega$ , $I_D \cong 4\text{ A}$ , $V_{GEN} = 6\text{ V}$ , $R_g = 1\ \Omega$	N-Ch 2	-	5	10	
<b>Source-Drain Diode Ratings and Characteristics <sup>b</sup></b>							
Pulsed current <sup>a</sup>	$I_{SM}$		N-Ch 1	-	-	80	A
			N-Ch 2	-	-	175	
Forward voltage	$V_{SD}$	$I_F = 4\text{ A}$ , $V_{GS} = 0\text{ V}$	N-Ch 1	-	0.72	1.2	V
		$I_F = 10\text{ A}$ , $V_{GS} = 0\text{ V}$	N-Ch 2	-	0.73	1.2	
Body diode reverse recovery time	$t_{rr}$	$I_F = 4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	N-Ch 1	-	20	40	ns
		$I_F = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	N-Ch 2	-	34	70	
Body diode reverse recovery charge	$Q_{rr}$	$I_F = 4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	N-Ch 1	-	7.5	15	nC
		$I_F = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	N-Ch 2	-	22	50	
Reverse recovery fall time	$t_a$	$I_F = 4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	N-Ch 1	-	8	-	ns
		$I_F = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	N-Ch 2	-	15	-	
Reverse recovery rise time	$t_b$	$I_F = 4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	N-Ch 1	-	12	-	ns
		$I_F = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	N-Ch 2	-	19	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$	$I_F = 4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	N-Ch 1	-	-0.7	-	A
		$I_F = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	N-Ch 2	-	-1.2	-	

**Notes**

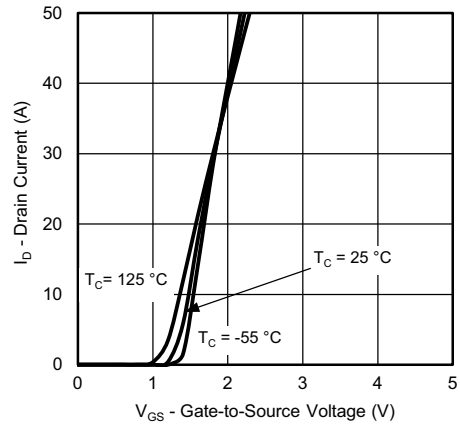
- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

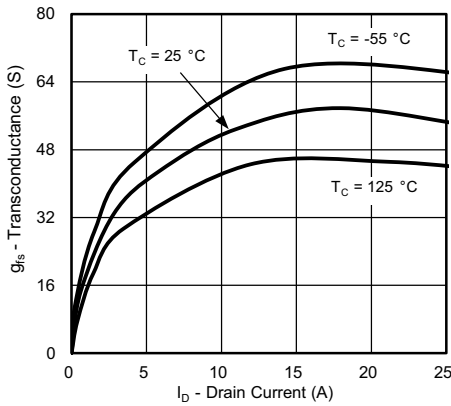
**N-CHANNEL 1 TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



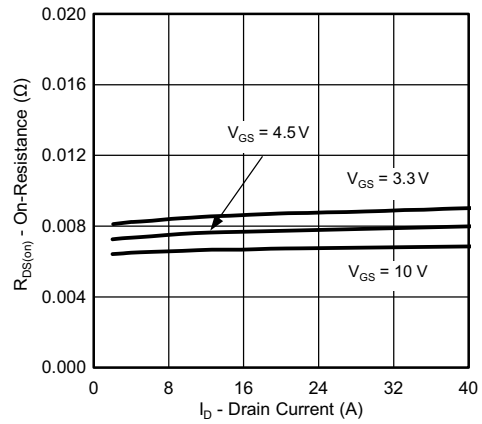
**Output Characteristics**



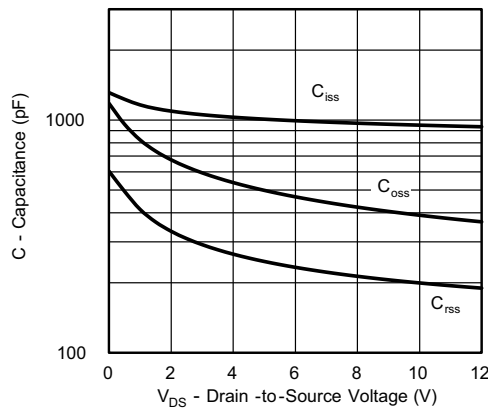
**Transfer Characteristics**



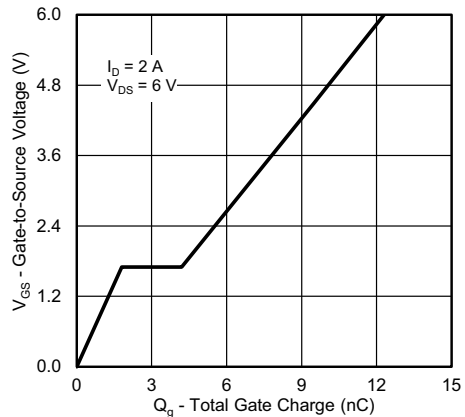
**Transconductance**



**On-Resistance vs. Drain Current**



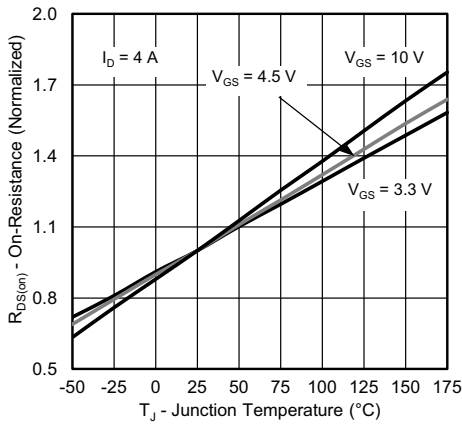
**Capacitance**



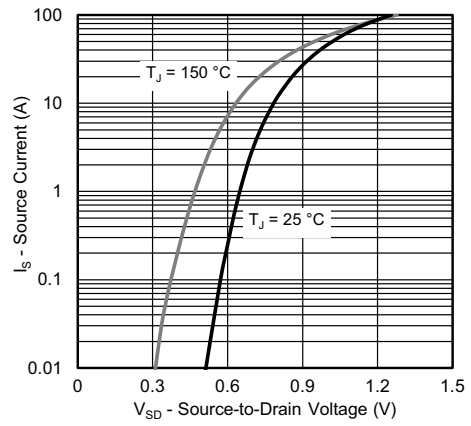
**Gate Charge**



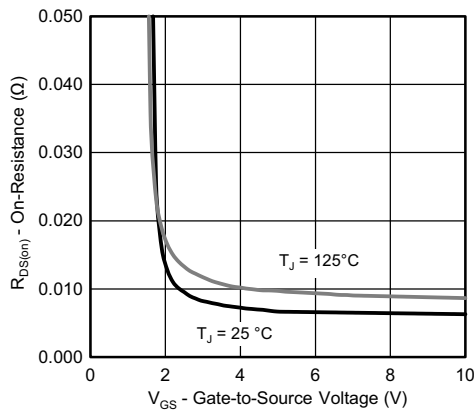
**N-CHANNEL 1 TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



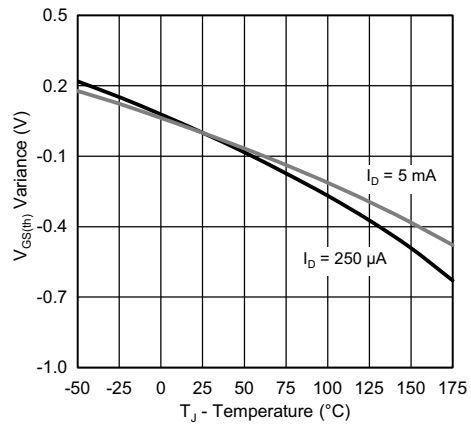
**On-Resistance vs. Junction Temperature**



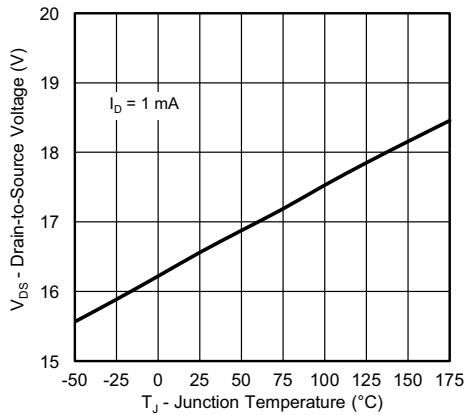
**Source Drain Diode Forward Voltage**



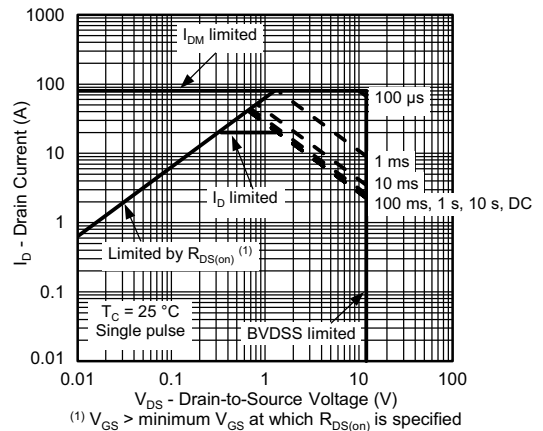
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



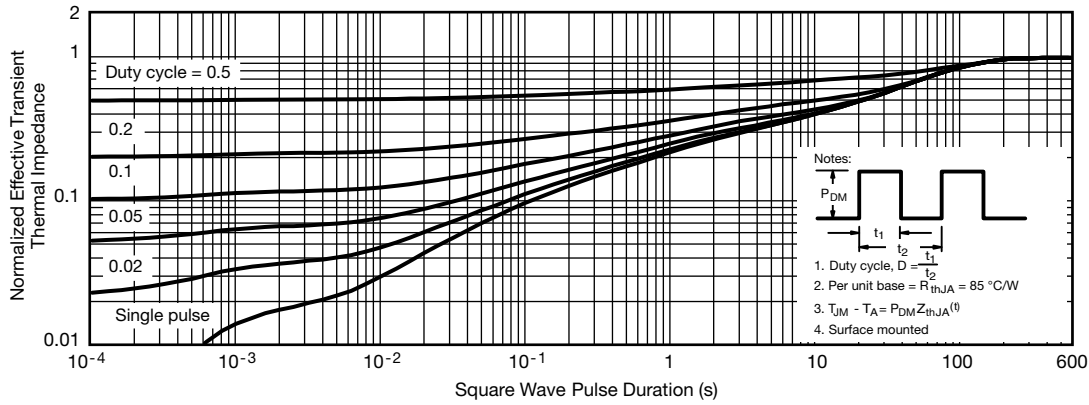
**Drain Source Breakdown vs. Junction Temperature**



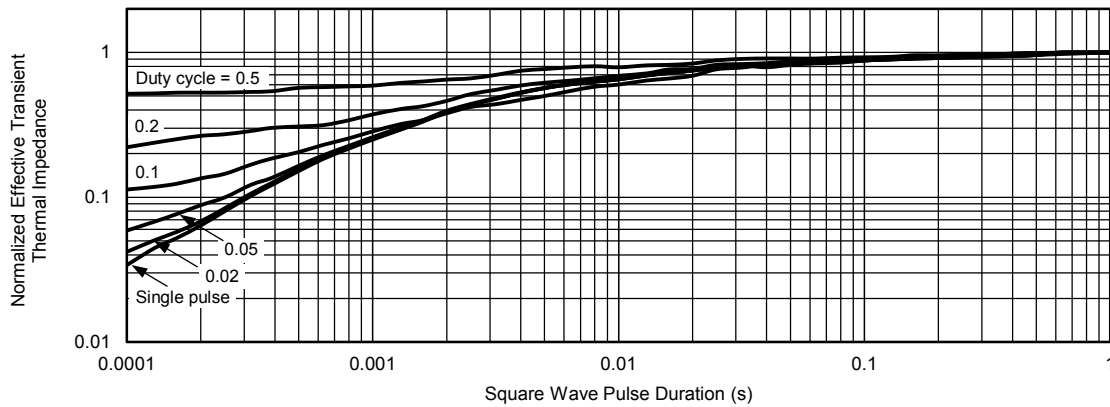
**Safe Operating Area**



**N-CHANNEL 1 TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

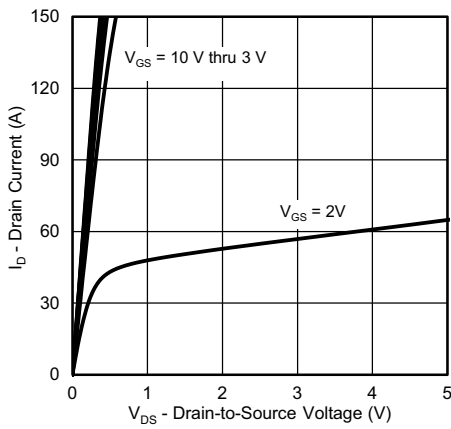


**Normalized Thermal Transient Impedance, Junction-to-Case**

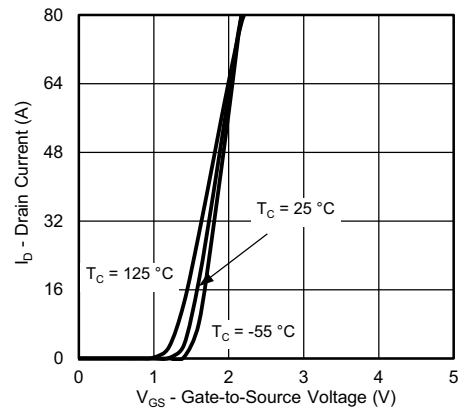
**Note**

- The characteristics shown in the graph:
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^\circ\text{C}$ ) is given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size  $1\text{ }^\prime \times 1\text{ }^\prime \times 0.062\text{ }^\prime$ , double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

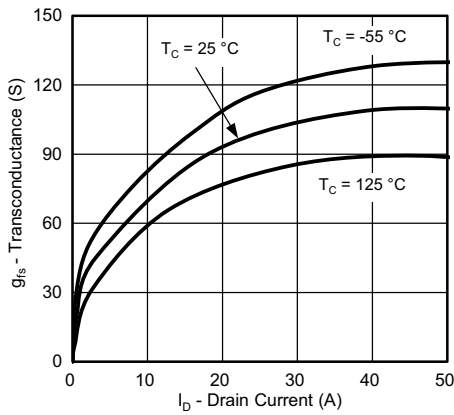
**N-CHANNEL 2 TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



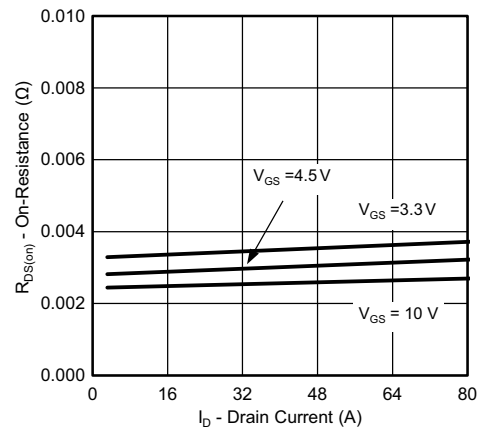
**Output Characteristics**



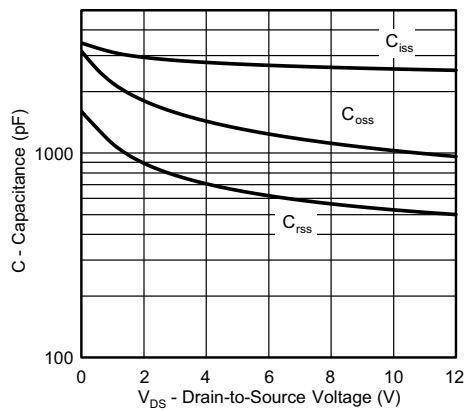
**Transfer Characteristics**



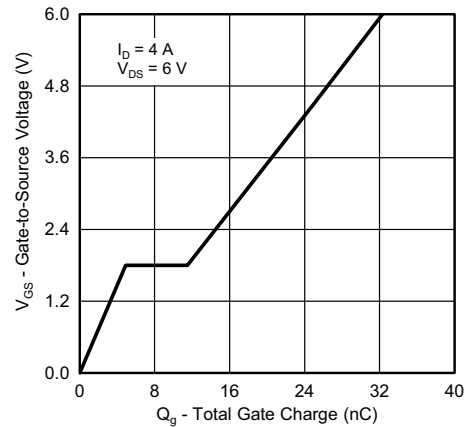
**Transconductance**



**On-Resistance vs. Drain Current**

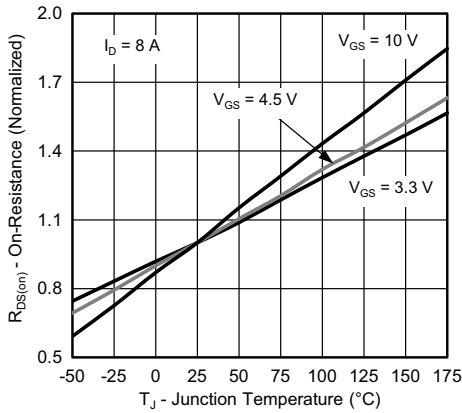


**Capacitance**

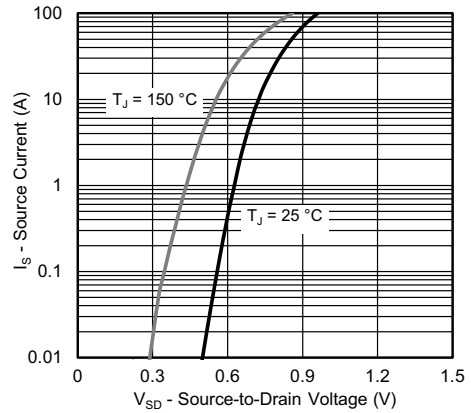


**Gate Charge**

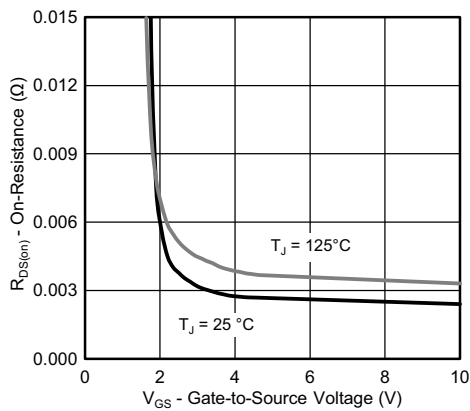
**N-CHANNEL 2 TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



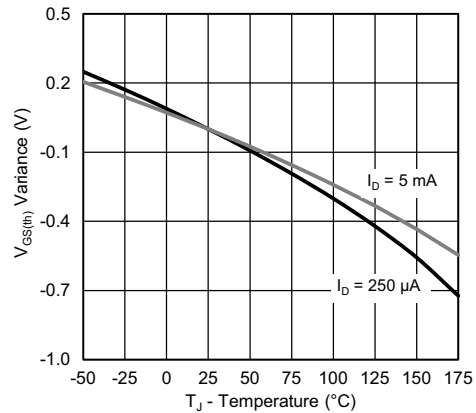
**On-Resistance vs. Junction Temperature**



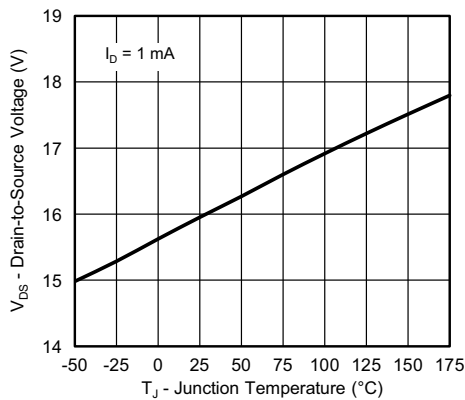
**Source Drain Diode Forward Voltage**



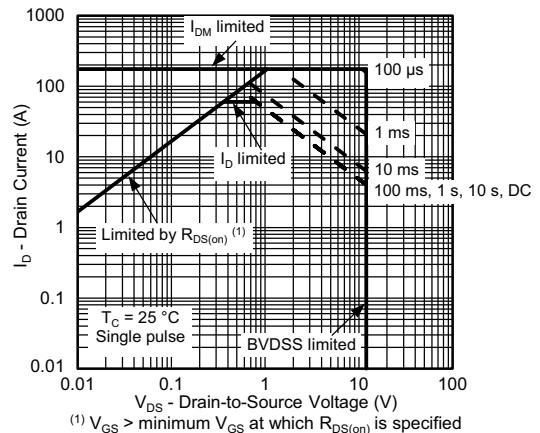
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Drain Source Breakdown vs. Junction Temperature**

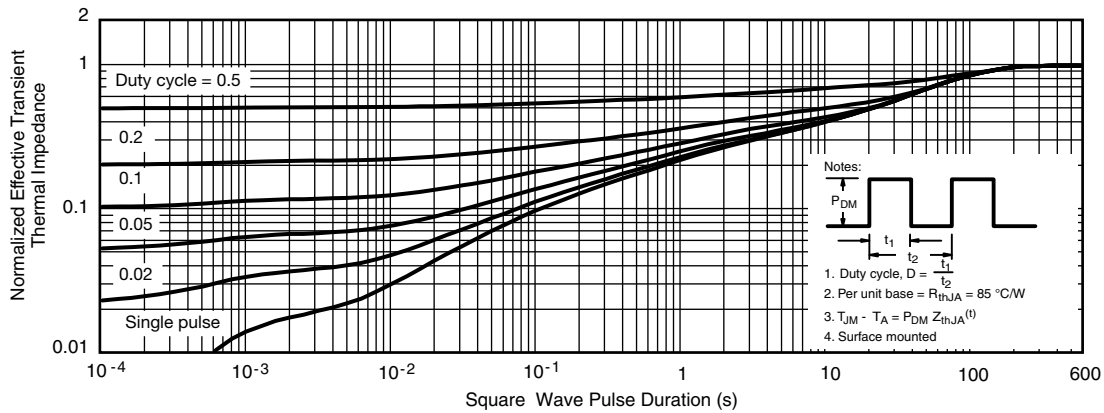


**Safe Operating Area**

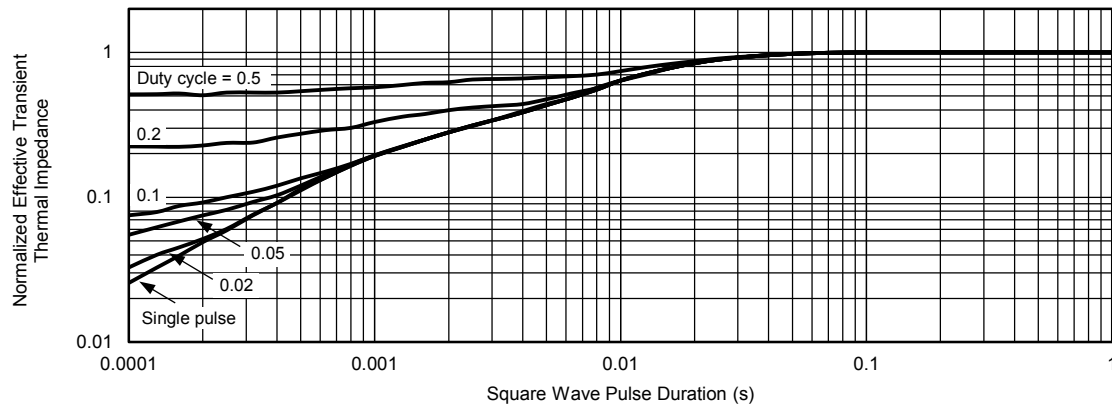




**N-CHANNEL 2 TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the graph:
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^\circ\text{C}$ ) is given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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