Product Change Notification - SYST-15JVTD747

Date:

16 Jul 2019

Product Category:

Ethernet Switches

Affected CPNs:

Notification subject:

Data Sheet - KSZ9897S 7-Port Gigabit Ethernet Switch with SGMII and RGMII/MII/RMII Interface Datasheet Document Revision

Notification text:

SYST-15JVTD747

Microchip has released a new DeviceDoc for the KSZ9897S 7-Port Gigabit Ethernet Switch with SGMII and RGMII/MII/RMII Interface of devices. If you are using one of these devices please read the document located at KSZ9897S 7-Port Gigabit Ethernet Switch with SGMII and RGMII/MII/RMII Interface .

Notification Status: Final

Description of Change:

1) Table 4-14, Transmit Tail Tag Format (from Host to Switch): Bit 7 changed to 15:00, description changed to Reserved.
2) Section 5.5.1, SGMII Control Register: Bit 12, Auto-Negotiation Enable - Applies to the SGMII Mode Port only
3) Section 2.1, General Description, on page 8: Updated first bullet to indicate the non-blocking wire-speed Ethernet switch fabric supports 1 Gbpson RGMII.
4) Table 3-1, Table 3-2, Table 3-3: Updated INTRP_N and CLKO_25_125 pin listings to indicate configuration strap functions.
5) Section 4.1.5, Pair-Swap, Alignment, and Polarity Check, on page 20: Updated first bullet description.
6) Section 4.3.3, Back-Off Algorithm, on page 26: Updated second sentence.
7) Section 4.3.5, Legal Packet Size, on page 26: Simplified paragraph for clarity.
8) Section 4.3.6, Flow Control, on page 26: Simplified last sentence of third paragraph.
9) Table 4-10, Hashed(SA)+FID Lookup in VLAN Mode: Updated Action description for the Yes entry.
10) Section 4.4.3.2.1, Tag Insertion and Removal, on page 34: Updated last paragraph of section.
11) Section 4.4.8, Multiple Spanning Tree Support, on page 38: Updated second sentence.
12) Table 4-17, ACL Matching Rule Parameters for MD = 01: Corrected ENB[1:0] 01 and 10 definitions to match those in Table 4-16, Matching Rule Options.
13) Section 4.10, In-Band Management, on page 57:
a) Added to last sentence of first paragraph.
b) Added additional sentence to end of second paragraph.
c) Added additional sentence to end of sixth paragraph.
14) Section 5.2.1.7, Port Operation Control 0 Register, on page 110: Updated bit 6 and 7 descriptions to include references to the MAC and additional clarification.
15) Section 5.2.2.15, PHY Remote Loopback Register, on page 123: Simplified bit 8 description.
16) Section 5.2.3, Port N: Port SGMII Control Registers (0xN200 - 0xN2FF), on page 128: Added new note to end of section.
17) Section 5.2.5.1, Port MAC Control 0 Register, on page 131: Bit 0 made reserved.
18) Section 6.4.7, Power-up and Reset Timing
a) Updated Note 1.
b) Updated Figure 6-12 to include SGMII power supplies (VDDHS, VDDLS).
19)Table 6-11 Added new trw entry to table.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 16 July 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

KSZ9897S 7-Port Gigabit Ethernet Switch with SGMII and RGMII/MII/RMII Interface

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

KSZ9897STXC
KSZ9897STXC-TR
KSZ9897STXI
KSZ9897STXI-TR