TSL2572

Light-to-Digital Converter

General Description

The TSL2572 device family provides ambient light sensing (ALS) that approximates human eye response to light intensity under a variety of lighting conditions and through a variety of attenuation materials. Accurate ALS measurements are the result of **ams**' patented dual-diode technology and the UV rejection filter incorporated in the package. In addition, the operating range is extended to 60,000 lux in sunlight when the low-gain mode is used.

While useful for general purpose light sensing, the TSL2572 device is particularly useful for display management to provide optimum viewing in diverse lighting conditions while extending battery life. The TSL2572 device family is ideally suited for use in mobile handsets, TVs, tablets, monitors, and portable media players where the display backlight may account for 50% to 70% of the system power consumption.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TSL2572, Light-to-Digital Converter are listed below:

Figure 1:
Added Value Of Using TSL2572

Benefits	Features
• Enables Operation in IR Light Environments	• Patented Dual-Diode Architecture
• Enables Dark Room to 60K Lux Sunlight Operation	• 8M:1 Dynamic Range
• Reduces Micro-Processor Interrupt Overhead	• Programmable Interrupt Function
• Improves Lux Accuracy Across Various Light Sources	• UV-Rejection Package
• Reduces Board Space Requirements While Simplifying Designs	• Area Efficient 2mm x 2mm Dual Flat No-Lead (FN) Package

- Ambient Light Sensing (ALS)
  - Approximates Human Eye Response
  - Programmable Analog Gain and Integration Time
  - 45,000,000:1 Dynamic Range
  - Operation to 60,000 lux in Sunlight
  - Very High Sensitivity — Ideally Suited for Operation Behind Dark Glass
  - Package UV Rejection Filter

- Maskable Interrupt
  - Programmable Upper and Lower Thresholds with Persistence Filter
- Wait Timer and Power Management
  - Low Power 2.2 mA Sleep State with User- Selectable Sleep-After-Interrupt Mode
  - 90 mA Wait State with Programmable Wait Time from 2.7 ms to > 8 seconds
- I^2C Fast Mode Compatible Interface
  - Data Rates up to 400 kbit/s
  - Input Voltage Levels Compatible with VDD or 1.8-V Bus
- Register Set- and Pin-Compatible with the TSL2x71 Series

Applications

TSL2572, Light-to-Digital Converter is ideal for:

- Display Backlight Control
- Keyboard Illumination Control
- Solid State Lighting Control for Daylight Harvesting
- Printer Paper Detection

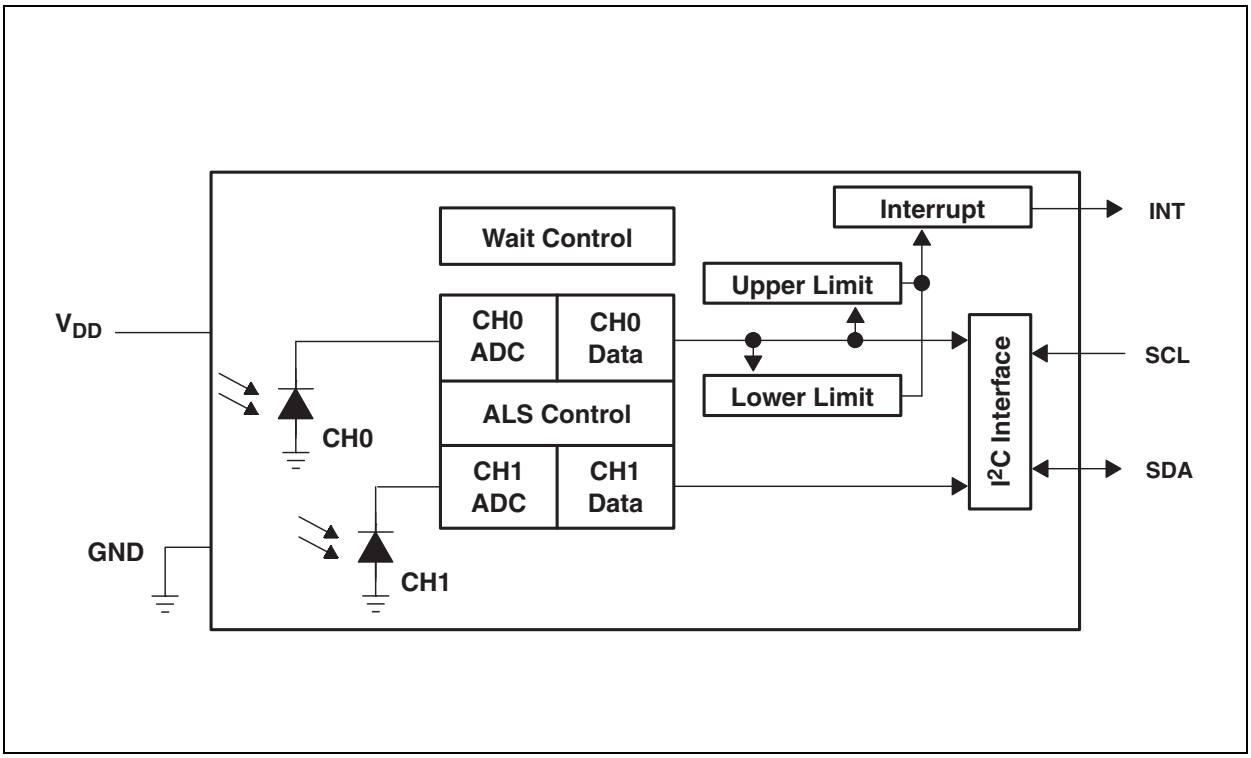
End Products and Market Segments

- Mobile Handsets, Tablets, Laptops, Monitors and TVs, Portable Media Players
- Medical and Industrial Instrumentation
- White Goods
- Toys
- Industrial/Commercial Lighting
- Digital Signage
- Printers

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TSL2572 Block Diagram



Pin Assignments

Figure 3:
Package FN Dual Flat No-Lead (Top View)

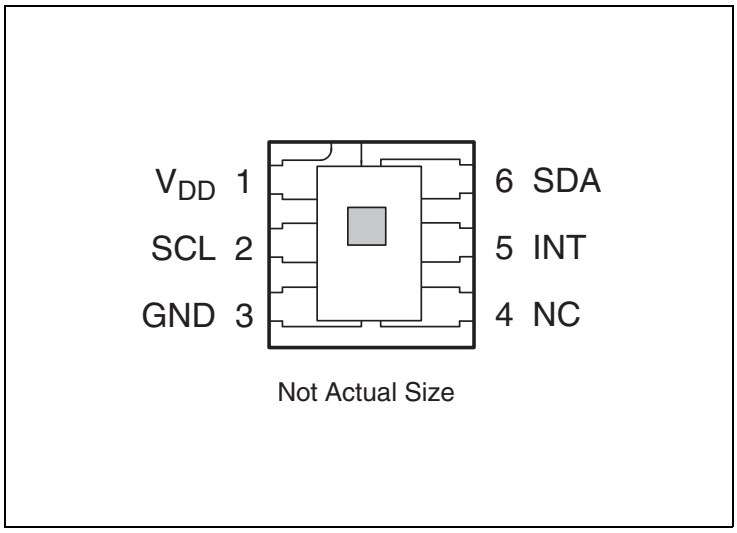


Figure 4:
Terminal Functions

Terminal		Type	Description
Name	No		
V_{DD}	1		Supply voltage
SCL	2	I	I^2C serial clock input terminal — clock signal for I^2C serial data
GND	3		Power supply ground. All voltages are referenced to GND
NC	4		Do not connect
INT	5	O	Interrupt — open drain (active low)
SDA	6	I/O	I^2C serial data I/O terminal — serial data I/O for I^2C

Detailed Description

The TSL2572 light-to-digital device provides on-chip photodiodes, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine, and an I^2C interface. Each device combines a Channel 0 photodiode (CH0), which is responsive to both visible and infrared light, and a channel 1 photodiode (CH1), which is responsive primarily to infrared light. Two integrating ADCs simultaneously convert the amplified photodiode currents into a digital value providing up to 16 bits of resolution. Upon completion of the conversion cycle, the conversion result is transferred to the data registers. This digital output can be read by a microprocessor through which the illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human eye response.

Communication to the device is accomplished through a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller. The digital output of the device is inherently more immune to noise when compared to an analog interface.

The device provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. An interrupt is generated when the value of an ALS conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Min	Max	Units
V_{DD} (1)	Supply voltage		3.8	V
	Input terminal voltage	-0.5	3.8	V
	Output terminal voltage	-0.5	3.8	V
	Output terminal current	-1	+20	mA
T_{strg}	Storage temperature range	-40	85	°C
ESD_{HBM}	ESD tolerance, human body model	±2000		V

Note(s):

1. All voltages are with respect to GND.

Electrical Characteristics

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Units
V_{DD}	Supply voltage	TSL25721, I^2C $V_{bus} = V_{DD}$	2.4	3	3.6	V
		TSL25723 , I^2C $V_{bus} = 1.8V$	2.7	3	3.6	V
T_A	Operating free-air temperature		-30		70	°C

Figure 7:
Operating Characteristics; V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Active		200	250	µA
		Wait mode		90		
		Sleep mode — no I^2C activity		2.2	4	
V_{OL}	INT, SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		–5		5	µA
V_{IH}	SCL, SDA input high voltage	TSL25721	0.7 V_{DD}			V
		TSL25723	1.25			
V_{IL}	SCL, SDA input low voltage	TSL25721			0.3 V_{DD}	V
		TSL25723			0.54	

Figure 8:
ALS Characteristics; V_{DD} = 3 V, T_A = 25°C, AGAIN = 16x; AEN = 1 (unless otherwise noted) (1) (2) (3)

Parameter	Test Conditions	Channel	Min	Typ	Max	Unit
Dark ADC count value	E_e = 0, AGAIN = 120× ATIME = 0xDB (100 ms)	CH0	0	1	5	counts
		CH1	0	1	5	
ADC integration time step size	ATIME = 0xFF		2.58	2.73	2.9	ms
ADC Number of integration steps (4)			1		256	steps
ADC counts per step (4)	ATIME = 0xFF		0		1024	counts
ADC count value (4)	ATIME = 0xC0		0		65535	counts
ADC count value	White light, E_e = 263.9 µW/cm^2 ATIME = 0xF6 (27 ms) (2)	CH0	4000	5000	6000	counts
		CH1		680		
	λ_p = 850 nm, E_e = 263.4 µW/cm^2 ATIME = 0xF6 (27 ms) (3)	CH0	4000	5000	6000	
		CH1		2850		
ADC count value ratio: CH1/CH0	White light, ATIME 0xF6 (27 ms) (2)		0.086	0.136	0.186	
	λ_p = 850 nm ATIME 0xF6 (27 ms) (3)		0.456	0.570	0.684	
R_e Irradiance responsivity	White light, ATIME = 0xF6 (27 ms) (2)	CH0		18.9		counts/ (µW/ cm^2)
		CH1		2.58		
	λ_p = 850 nm, ATIME = 0xF6 (27 ms) (3)	CH0		19.0		
		CH1		10.8		
Gain scaling, relative to 1× gain setting	AGAIN = 1× and AGL = 1		0.128	0.16	0.192	×
	AGAIN = 8× and AGL = 0		7.2	8.0	8.8	
	AGAIN 16× and AGL = 0		14.4	16.0	17.6	
	AGAIN = 120× and AGL = 0		108	120	132	

Note(s):

1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible white LEDs and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production.
2. The white LED irradiance is supplied by a white light-emitting diode with a nominal color temperature of 4000 K.
3. The 850 nm irradiance E_e is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength λ_p = 850 nm and spectral halfwidth $\Delta\lambda$½ = 42 nm.
4. Parameter ensured by design and is not tested.

Figure 9:
Wait Characteristics; V_{DD} = 3 V, T_A = 25°C, WEN = 1 (unless otherwise noted)

Parameter	Test Conditions	Channel	Min	Typ	Max	Unit
Wait step size	WTIME = 0xFF		2.58	2.73	2.9	ms
Wait number of integration steps (1)			1		256	steps

Note(s):

1. Parameter ensured by design and is not tested.

Figure 10:
AC Electrical Characteristics; V_{DD} = 3 V, T_A = 25°C, (unless otherwise noted)

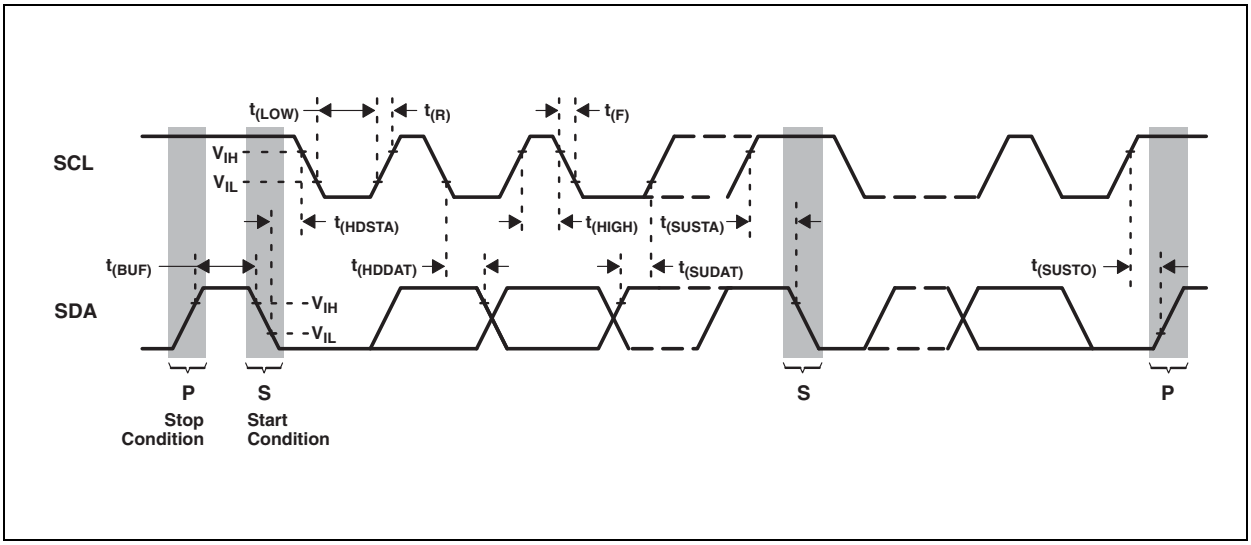
Symbol	Parameter(1)	Test Conditions	Min	Typ	Max	Unit
$f_{(SCL)}$	Clock frequency (I^2C only)		0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			µs
$t_{(SUSTO)}$	Stop condition setup time		0.6			µs
$t_{(HDDAT)}$	Data hold time		0			µs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			µs
$t_{(HIGH)}$	SCL clock high period		0.6			µs
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Parameter Measurement Information

Figure 11:
Timing Diagrams



Typical Characteristics

Figure 12:
Spectral Responsivity

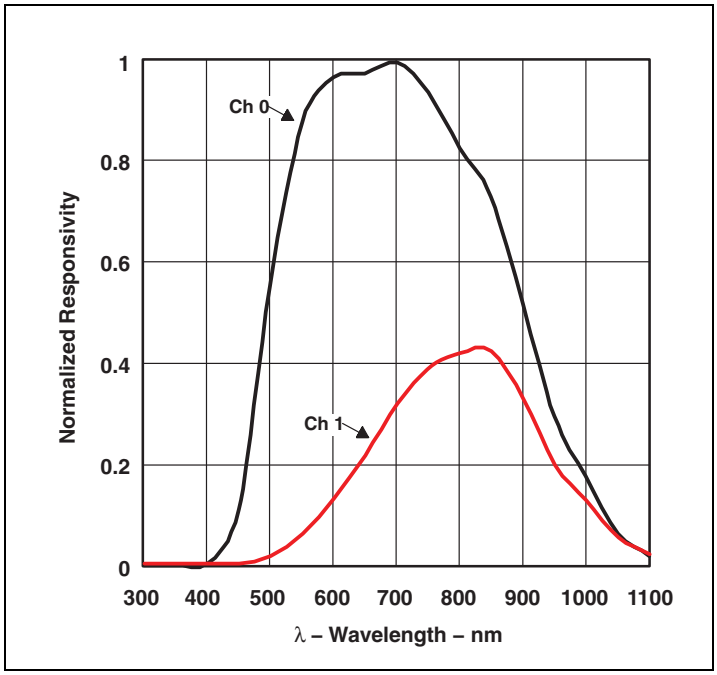


Figure 13:
Normalized Responsivity vs. Angular Displacement

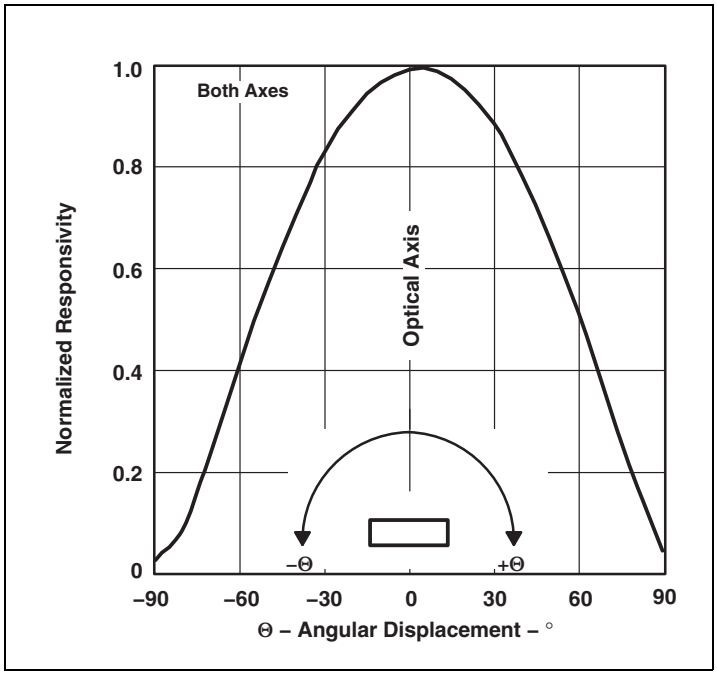


Figure 14:
Normalized I_{DD} vs.V_{DD} and Temperature

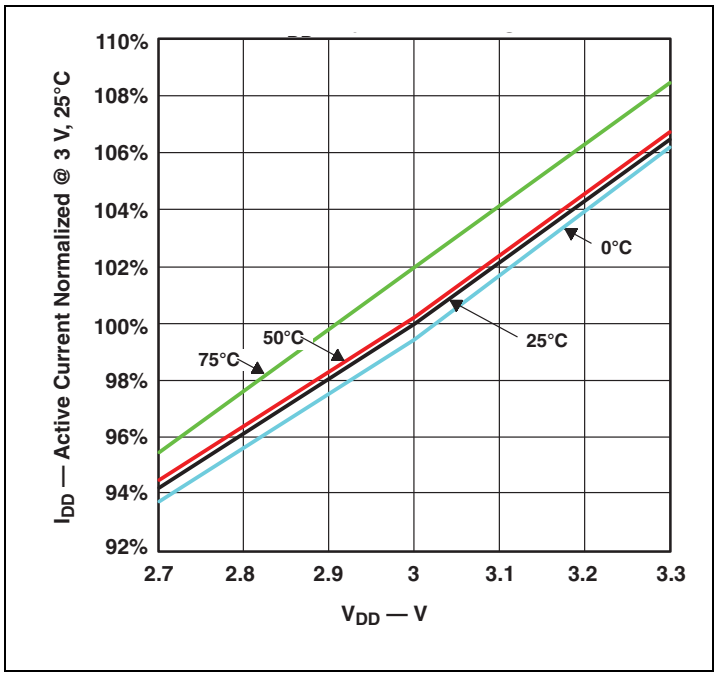
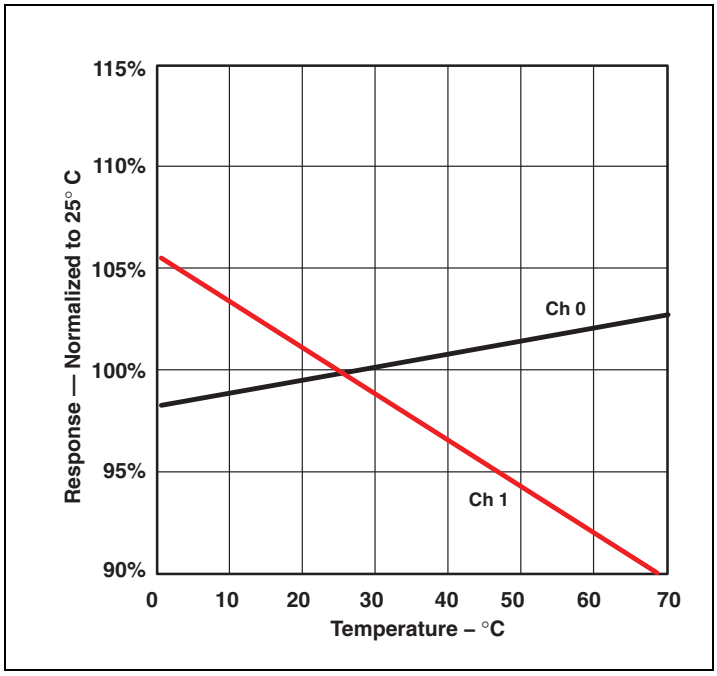


Figure 15:
Response to White LED vs.Temperature



Principles Of Operation

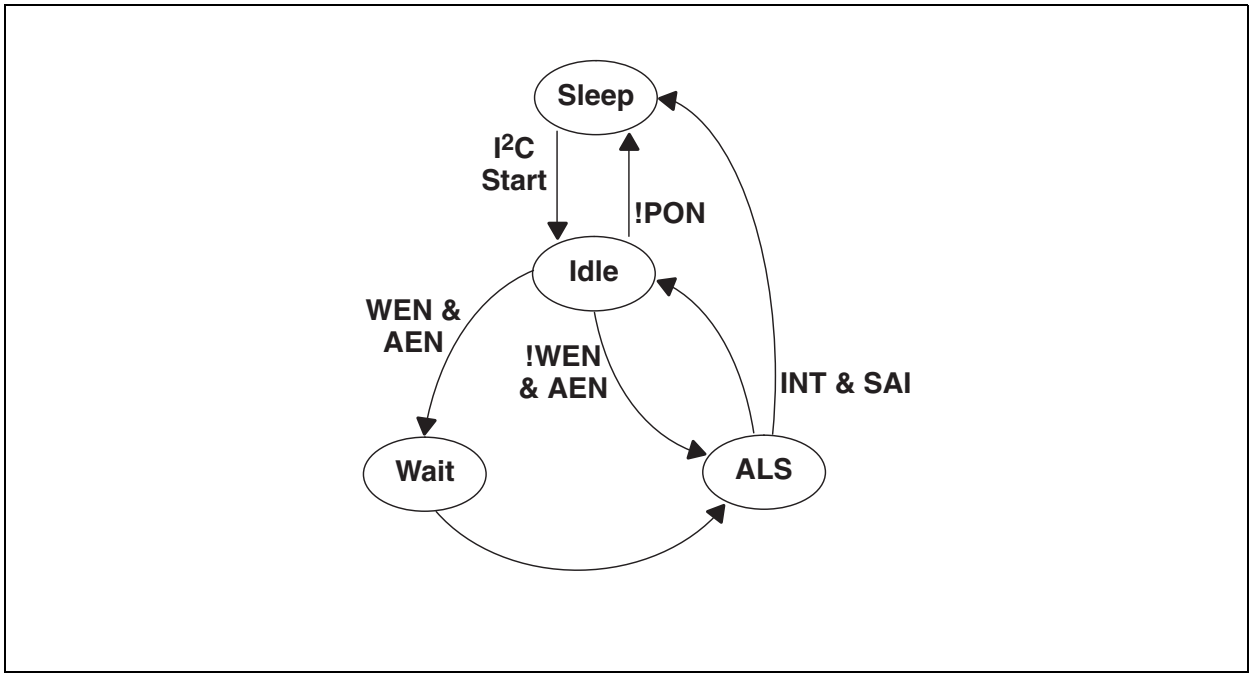
System State Machine

An internal state machine provides system control of the ALS and wait timer features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low-power Sleep state.

When a start condition is detected on the I²C bus, the device transitions to the Idle state where it checks the Enable register (0x00) PON bit. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until the ALS function is enabled. Once enabled, the device will execute the Wait and ALS states in sequence as indicated in Figure 16. Upon completion and return to Idle, the device will automatically begin a new Wait-ALS cycle as long as PON and AEN remain enabled.

If the ALS function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled, the device will transition to the Sleep state and remain in a low-power mode until an I²C command is received. See the Interrupts section for additional information.

Figure 16:
Simplified State Diagram



Photodiodes

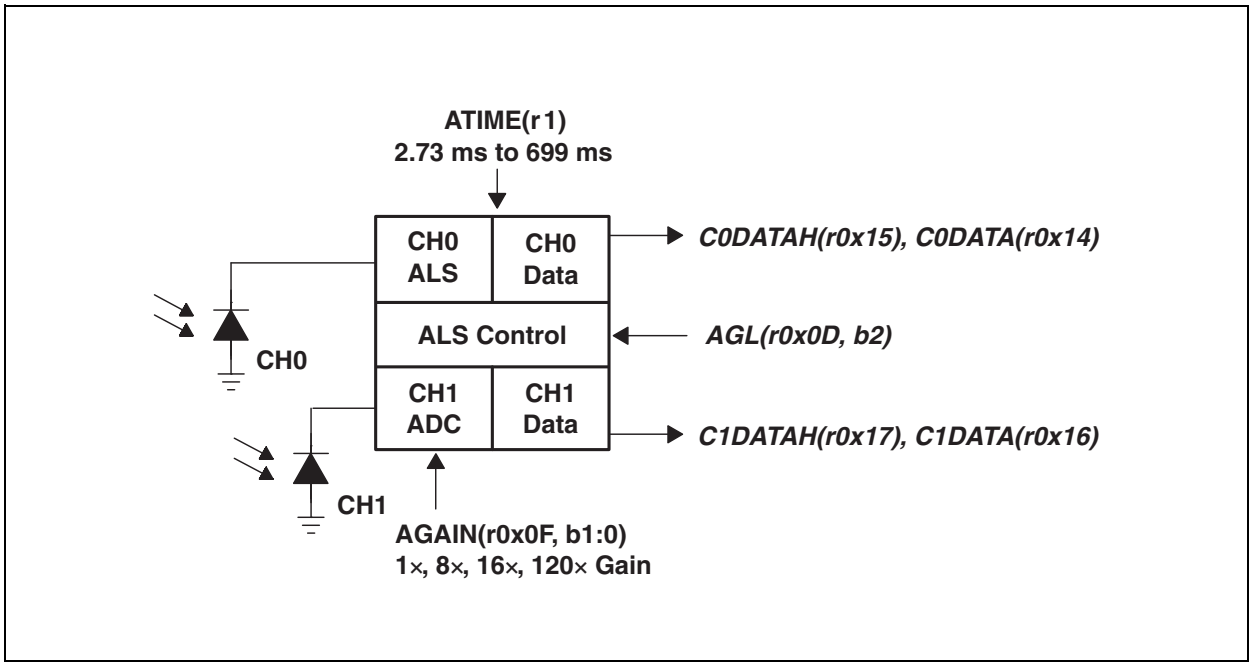
Conventional ALS detectors respond strongly to infrared light, which the human eye does not see. This can lead to significant error when the infrared content of the ambient light is high (such as with incandescent lighting).

This problem is overcome through the use of two photodiodes. The Channel 0 photodiode, referred to as the CH0 channel, is sensitive to both visible and infrared light, while the Channel 1 photodiode, referred to as CH1, is sensitive primarily to infrared light. Two integrating ADCs convert the photodiode currents to digital outputs.The ADC digital outputs from the two channels are used in a formula to obtain a value that approximates the human eye response in units of lux.

ALS Operation

The ALS engine contains ALS gain control (AGAIN) and two integrating analog-to-digital converters (ADC), one for the CH0 and one for the CH1 photodiodes. The ALS integration time (ATIME) impacts both the resolution and the sensitivity of the ALS reading. Integration of both channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the data registers (C0DATA and C1DATA). This data is also referred to as channel *count*. The transfers are double-buffered to ensure data integrity.

Figure 17:
ALS Operation



The registers for programming the integration and wait times are a 2's compliment values. The actual time can be calculated as follows:

ATIME = 256 - Integration Time / 2.73 ms

Inversely, the time can be calculated from the register value as follows:
Integration Time = 2.73 ms × (256 - ATIME)

In order to reject the 50/60-Hz ripple present in fluorescent lighting, the integration time needs to be programmed in multiples of 10 / 8.3 ms or the half cycle time. Both frequencies can be rejected with a programmed value of
50 ms (ATIME = 0xED) or multiples of 50 ms (i.e. 100, 150, 200, 400, 600).

AGAIN can be programmed to 1×, 8×, 16×, or 120× with the 2-bit AGAIN field in the Control register (0x0F). The gain, in terms of amount of gain, will be represented by the value AGAINx, i.e. AGAINx = 1, 8, 16, or 120. With the AGL bit set, the 1× and 8× gains are lowered to 1/6× and 8/6×, respectively, to allow for operation up to 60k lux. Do not enable AGL when AGAIN is 16× or 120×.

Lux Equation

The lux calculation is a function of CH0 channel count (C0DATA), CH1 channel count (C1DATA), ALS gain (AGAINx), and ALS integration time in milliseconds (ATIME_ms). If an aperture, glass/plastic, or a light pipe attenuates the light equally across the spectrum (300 nm to 1100 nm), then a scaling factor referred to as glass attenuation (GA) can be used to compensate for attenuation. For a device in open air with no aperture or glass/plastic above the device, GA = 1. If it is not spectrally flat, then a custom lux equation with new coefficients should be generated. (See **ams** application note).

Counts per Lux (CPL) needs to be calculated only when ATIME or AGAIN is changed, otherwise it remains a constant. The first segment of the equation (Lux1) covers fluorescent and incandescent light. The second segment (Lux2) covers dimmed incandescent light. The final lux is the maximum of Lux1, Lux2, or 0.

CPL = (ATIME_ms × AGAINx) / (GA × 60)

Lux1 = (1 × C0DATA - 1.87 × C1DATA) / CPL

Lux2 = (0.63 × C0DATA - 1 × C1DATA) / CPL

Lux = MAX(Lux1, Lux2, 0)

Interrupts

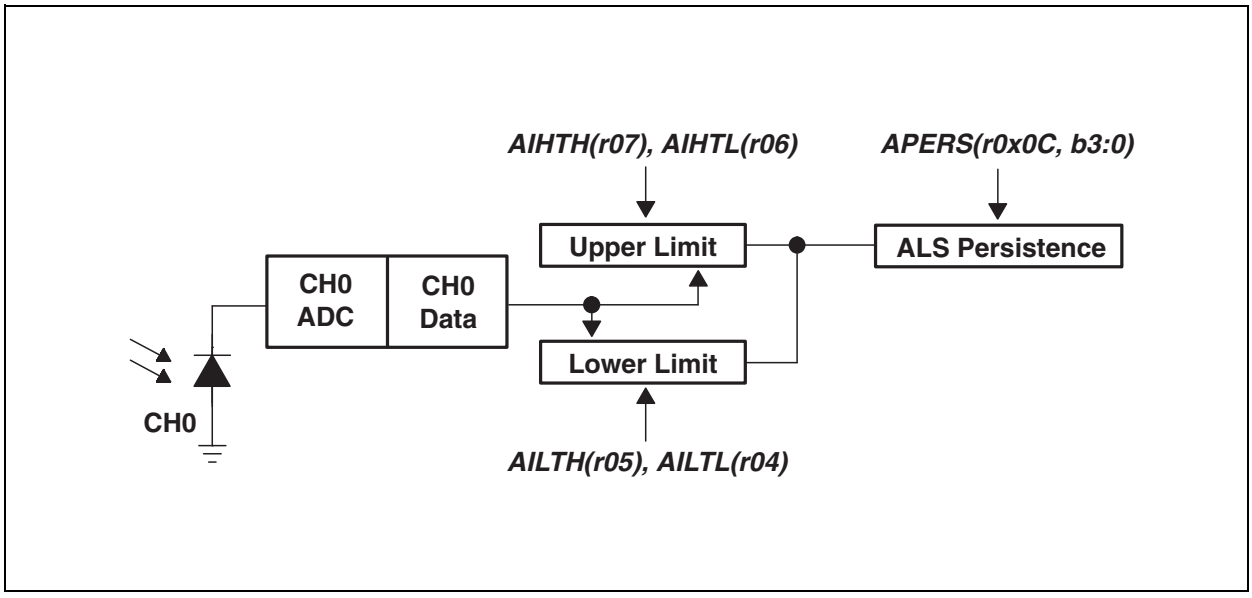
The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for light intensity values outside of a user-defined range. While the interrupt function is always enabled and it's status is available in the status register (0x13), the output of the interrupt state can be enabled using the ALS interrupt enable (AIEN) fields in the enable register (0x00).

Two 16-bit interrupt threshold registers allow the user to set limits below and above a desired light level. An interrupt can be generated when the ALS CH0 data (C0DATA) falls outside of the desired light level range, as determined by the values in the ALS interrupt low threshold registers (AILTx) and ALS interrupt high threshold registers (AIHTx).

It is important to note that the thresholds are evaluated in sequence, first the low threshold, then the high threshold. As a result, if the low threshold is set above the high threshold, the high threshold is ignored and only the low threshold is evaluated.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range ALS occurrences before an interrupt is generated. The persistence filter register (0x0C) allows the user to set the ALS persistence filter (APERS) value. See the persistence filter register for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see Command Register).

Figure 18:
Programmable Interrupt



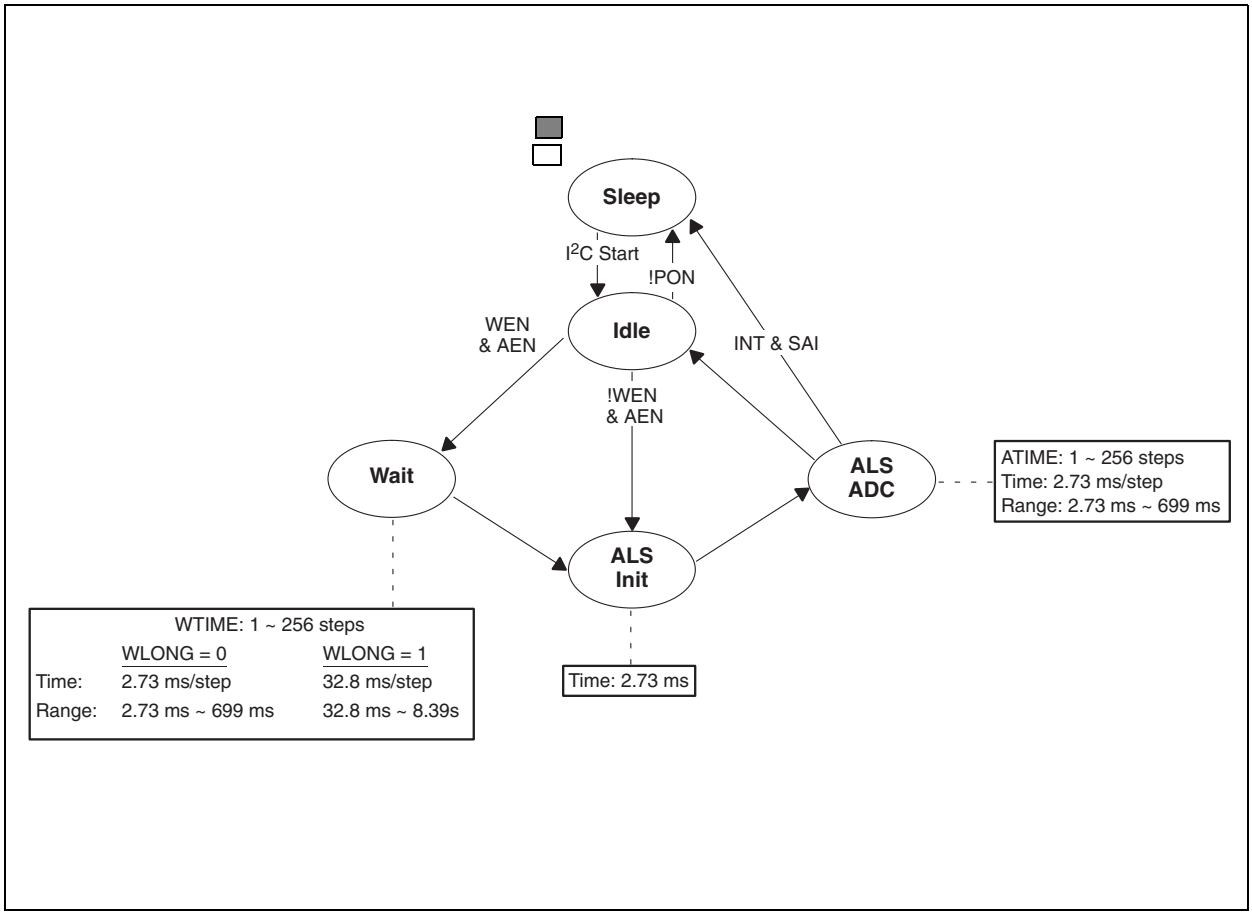
System State Machine Timing

The system state machine shown in Figure 16 provides an overview of the states and state transitions that provide system control of the device. This section highlights the programmable features, which affect the state machine cycle time, and provides details to determine system level timing.

When the power management feature is enabled (WEN), the state machine will transition in turn to the Wait state. The wait time is determined by WLONG, which extends normal operation by 12× when asserted, and WTIME. The formula to determine the wait time is given in the box associated with the Wait state in Figure 19.

When the ALS feature is enabled (AEN), the state machine will transition through the ALS Init and ALS ADC states. The ALS Init state takes 2.73 ms, while the ALS ADC time is dependent on the integration time (ATIME). The formula to determine ALS ADC time is given in the associated box in Figure 19. If an interrupt is generated as a result of the ALS cycle, it will be asserted at the end of the ALS ADC state and transition to the Sleep state if SAI is enabled.

Figure 19:
Detailed State Diagram



Note(s):

1. PON, WEN, AEN, and SAI are fields in the Enable register (0x00).

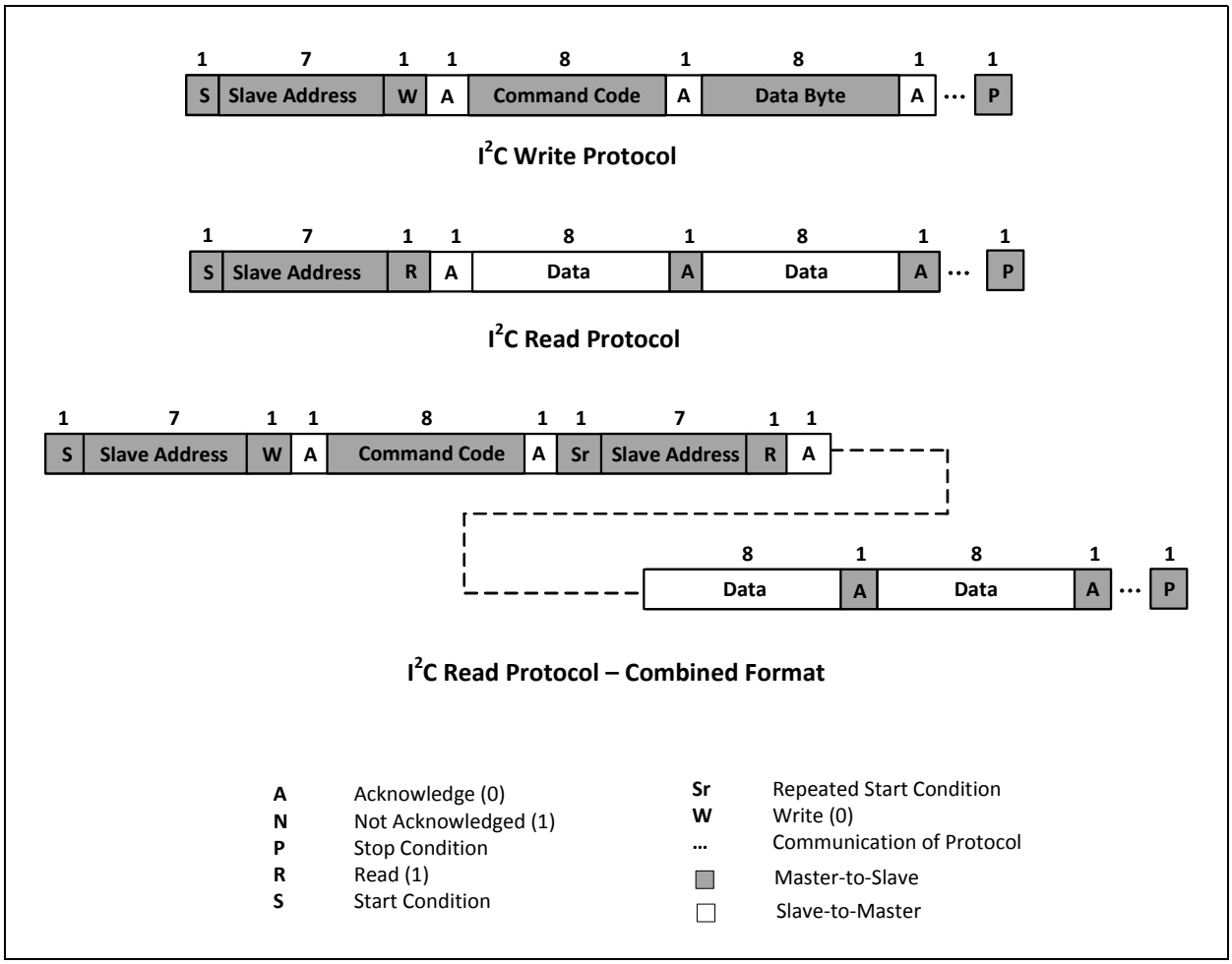
I²C Protocol

Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (see Figure 20). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.i2c-bus.org/references/.

Figure 20:
I²C Protocols



Register Overview

Register Set

The device is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure 21.

Figure 21:
Register Address

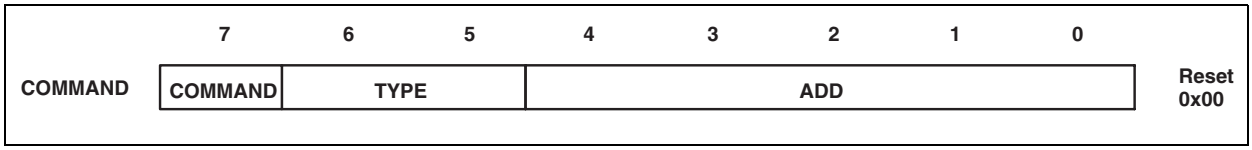
Address	Register Name	R/W	Register Function	Reset Value
––	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	ATIME	R/W	ALS time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x04	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x05	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x06	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x07	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filters	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0F	CONTROL	R/W	Control register	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x14	C0DATA	R	CH0 ADC low data register	0x00
0x15	C0DATAH	R	CH0 ADC high data register	0x00
0x16	C1DATA	R	CH1 ADC low data register	0x00
0x17	C1DATAH	R	CH1 ADC high data register	0x00

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I^2C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The command registers specifies the address of the target register for future write and read operations.

Figure 22:
Command Register

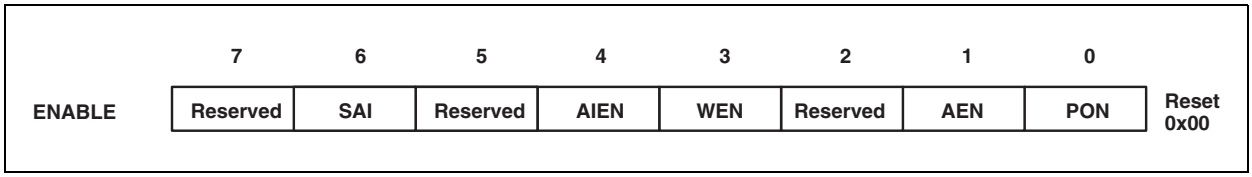


Field	Bits	Description	
COMMAND	7	Select Command Register. Must write as 1 when addressing COMMAND register.	
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:	
		FIELD VALUE	**DESCRIPTION**
		00	Repeated byte protocol transaction
		01	Auto-increment protocol transaction
		10	Reserved — Do not use
		11	Special function — See description below
		Transaction type 00 will repeatedly read the same register with each data access. Transaction type 01 will provide an auto-increment function to read successive register bytes.	
ADD	4:0	Address field/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for following write and read transactions. The field values listed below apply only to special function commands:	
		FIELD VALUE	**DESCRIPTION**
		00000	Normal — no action
		00110	ALS interrupt clear
		other	Reserved — do not write
		The ALS interrupt clear special function clears any pending ALS interrupt and is self clearing.	

Enable Register (0x00)

The ENABLE register is used to power the device ON/OFF, enable functions, and interrupts.

Figure 23:
Enable Register



Field	Bits	Description
Reserved	7	Reserved. Write as 0.
SAI	6	Sleep after interrupt. When asserted, the device will power down at the end of an ALS cycle if an interrupt has been generated
Reserved	5	Reserved. Write as 0.
AIEN	4	ALS interrupt mask. When asserted, permits ALS interrupts to be generated.
WEN	3	Wait enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
Reserved	2	Reserved. Write as 0.
AEN	1	ALS Enable. This bit actives the two channel ADC. Writing a 1 activates the ALS. Writing a 0 disables the ALS.
PON	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

ALS Timing Register (0x01)

The ALS timing register controls the internal integration time of the ALS ADCs in 2.73-ms increments. Upon power up, the ALS time register is set to 0xFF.

Figure 24:
ALS Timing Register

Field	Bits	Description			
		Value	INTEG_CYCLES	Time	Max Count
ATIME	7:0	0xFF	1	2.73 ms	1024
		0xF6	10	27.3 ms	10240
		0xDB	37	101 ms	37888
		0xC0	64	175 ms	65535
		0x00	256	699 ms	65535

Wait Time Register (0x03)

Wait time is set 2.73 ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number. Upon power up, the wait time register is set to 0xFF.

Figure 25:
Wait Time Register

Field	Bits	Description			
		Register Value	Wait Time	Time (WLONG = 0)	Time (WLONG = 1)
WTIME	7:0	0xFF	1	2.73 ms	0.033 s
		0xB6	74	202 ms	2.4 s
		0x00	256	699 ms	8.4 s

Note(s):

1. The Wait Time Register should be configured before AEN is asserted.

ALS Interrupt Threshold Registers (0x04 - 0x07)

The ALS interrupt threshold registers provides the values to be used as the high and low trigger points for the comparison function for interrupt generation. If C0DATA crosses below the low threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

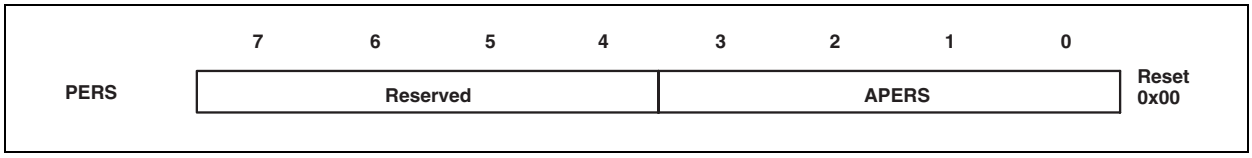
Figure 26:
ALS Interrupt Threshold Registers

Register	Address	Bits	Description
AILTL	0x04	7:0	ALS low threshold lower byte
AILTH	0x05	7:0	ALS low threshold upper byte
AIHTL	0x06	7:0	ALS high threshold lower byte
AIHTH	0x07	7:0	ALS high threshold upper byte

Persistence Register (0x0C)

The persistence register controls the filter interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after every ADC cycle or if the ADC cycle has produced a result that is outside of the values specified by threshold register for some specified amount of time. ALS interrupts are generated using C0DATA.

Figure 27:
Persistence Filter Register

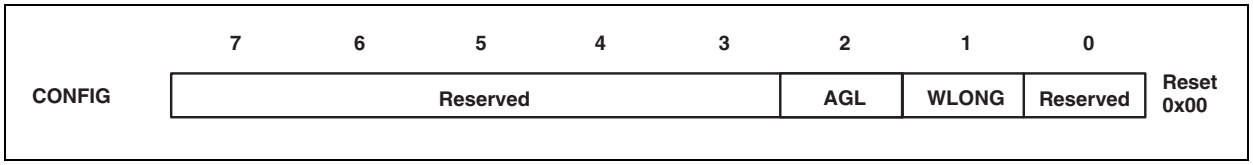


Field	Bits	Description		
Reserved	7:4	Reserved. Write as 0.		
APERS	3:0	ALS Interrupt persistence filter. Controls rate of ALS interrupt to the host processor		
		FIELD VALUE	**MEANING**	**INTERRUPT PERSISTENCE FUNCTION**
		0000	Every	Every ALS cycle generates an interrupt
		0001	1	1 value outside of threshold range
		0010	2	2 consecutive values out of range
		0011	3	3 consecutive values out of range
		0100	5	5 consecutive values out of range
		0101	10	10 consecutive values out of range
		0110	15	15 consecutive values out of range
		0111	20	20 consecutive values out of range
		1000	25	25 consecutive values out of range
		1001	30	30 consecutive values out of range
		1010	35	35 consecutive values out of range
		1011	40	40 consecutive values out of range
		1100	45	45 consecutive values out of range
		1101	50	50 consecutive values out of range
		1110	55	55 consecutive values out of range
		1111	60	60 consecutive values out of range

Configuration Register (0x0D)

The configuration register sets the wait long time and ALS gain level.

Figure 28:
Configuration Register

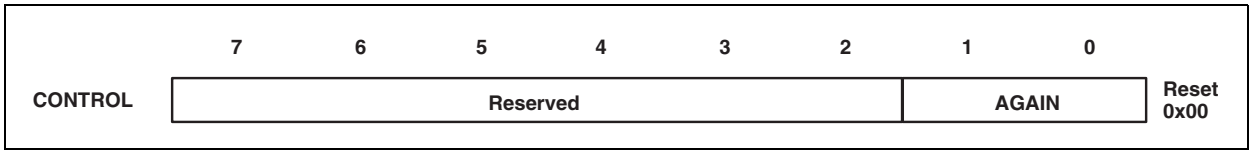


Field	Bits	Description
Reserved	7:3	Reserved. Write as 0.
AGL	2	ALS gain level. When asserted, the 1× and 8× ALS gain (AGAIN) modes are scaled by 0.16. Otherwise, AGAIN is scaled by 1. Do not use with AGAIN greater than 8×.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.
Reserved	0	Reserved. Write as 0.

Control Register (0x0F)

The Control register provides ALS gain control to the analog block.

Figure 29:
Control Register

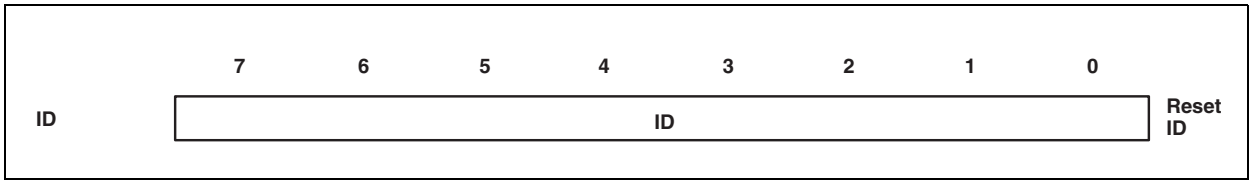


Field	Bits	Description	
Reserved	7:2	Reserved. Write as 0.	
AGAIN	1:0	ALS Gain.	
		FIELD VALUE	**ALS GAIN VALUE**
		00	1× gain
		01	8× gain
		10	16× gain
		11	120× gain

ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

Figure 30:
ID Register

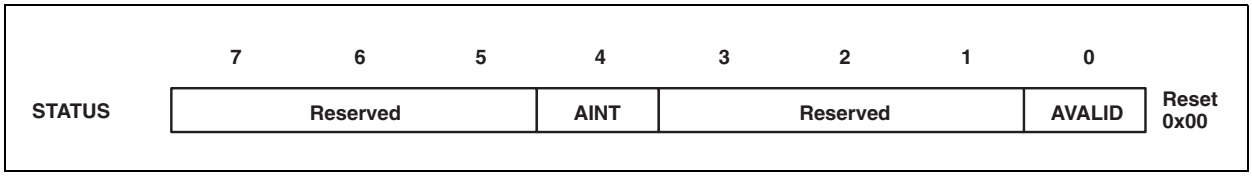


Field	Bits	Description	
ID	7:0	Part number identification	0x34 = TSL25721
			0x3D = TSL25723

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Figure 31:
Status Register



Field	Bit	Description
Reserved	7:5	Reserved. Bits read as 0.
AINT	4	ALS Interrupt. Indicates that the device is asserting an ALS interrupt.
Reserved	3:1	Reserved. Bits read as 0.
AVALID	0	ALS Valid. Indicates that the ALS channels have completed an integration cycle after AEN has been asserted.

ADC Channel Data Registers (0x14 - 0x17)

ALS data is stored as two 16-bit values. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored in a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Figure 32:
ADC Channel Data Registers

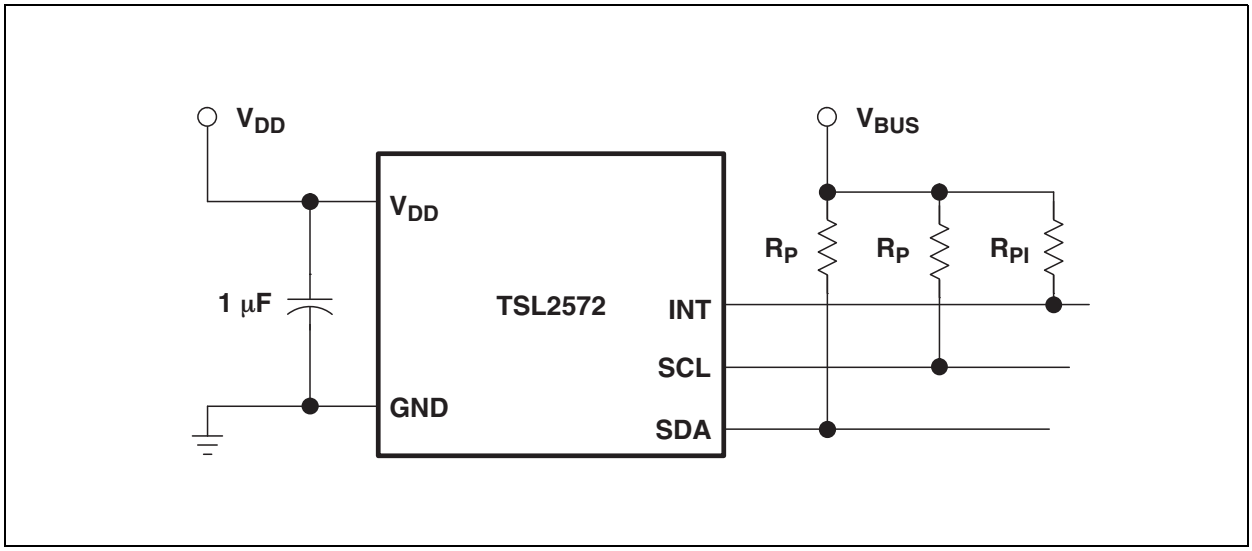
Register	Address	Bits	Description
C0DATA	0x14	7:0	ALS CH0 data low byte
C0DATAH	0x15	7:0	ALS CH0 data high byte
C1DATA	0x16	7:0	ALS CH1 data low byte
C1DATAH	0x17	7:0	ALS CH1 data high byte

Application Information: Hardware

Typical Hardware Application

A typical hardware application circuit is shown in Figure 33. A 1-µF low-ESR decoupling capacitor should be placed as close as possible to the V_{DD} pin.

Figure 33:
Typical Application Hardware Circuit



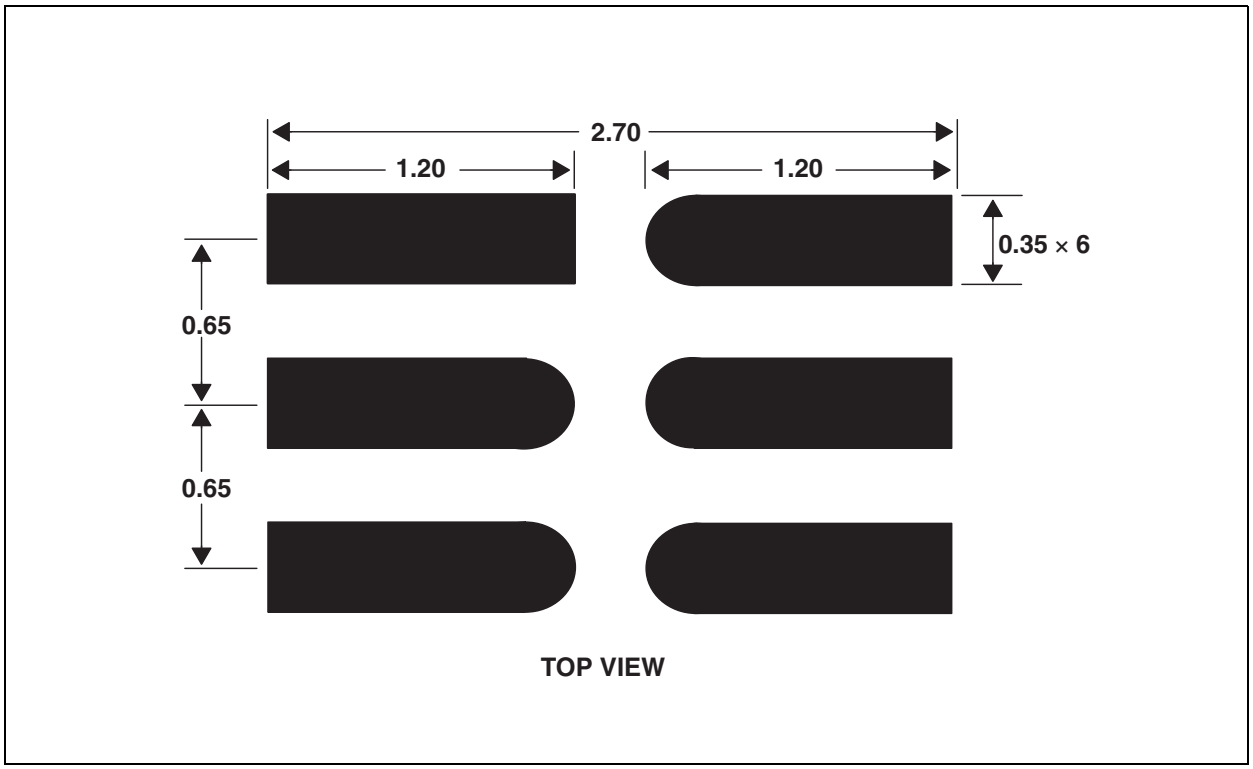
V_{BUS} in Figure 33 refers to the I^2C bus voltage, which is either V_{DD} or 1.8 V. Be sure to apply the specified I^2C bus voltage shown in the Available Options table for the specific device being used.

The I^2C signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (R_P) value is a function of the I^2C bus speed, the I^2C bus voltage, and the capacitive load. The **ams** EVM running at 400 kbps, uses 1.5-kΩ resistors. A 10-kΩ pull-up resistor (R_{PI}) can be used for the interrupt line.

PCB Pad Layout

Suggested land pattern based on the IPC-7351B Generic Requirements for Surface Mount Design and Land Pattern Standard (2010) for the small outline no-lead (SON) package is shown in Figure 34.

Figure 34:
Suggested FN Package PCB Layout

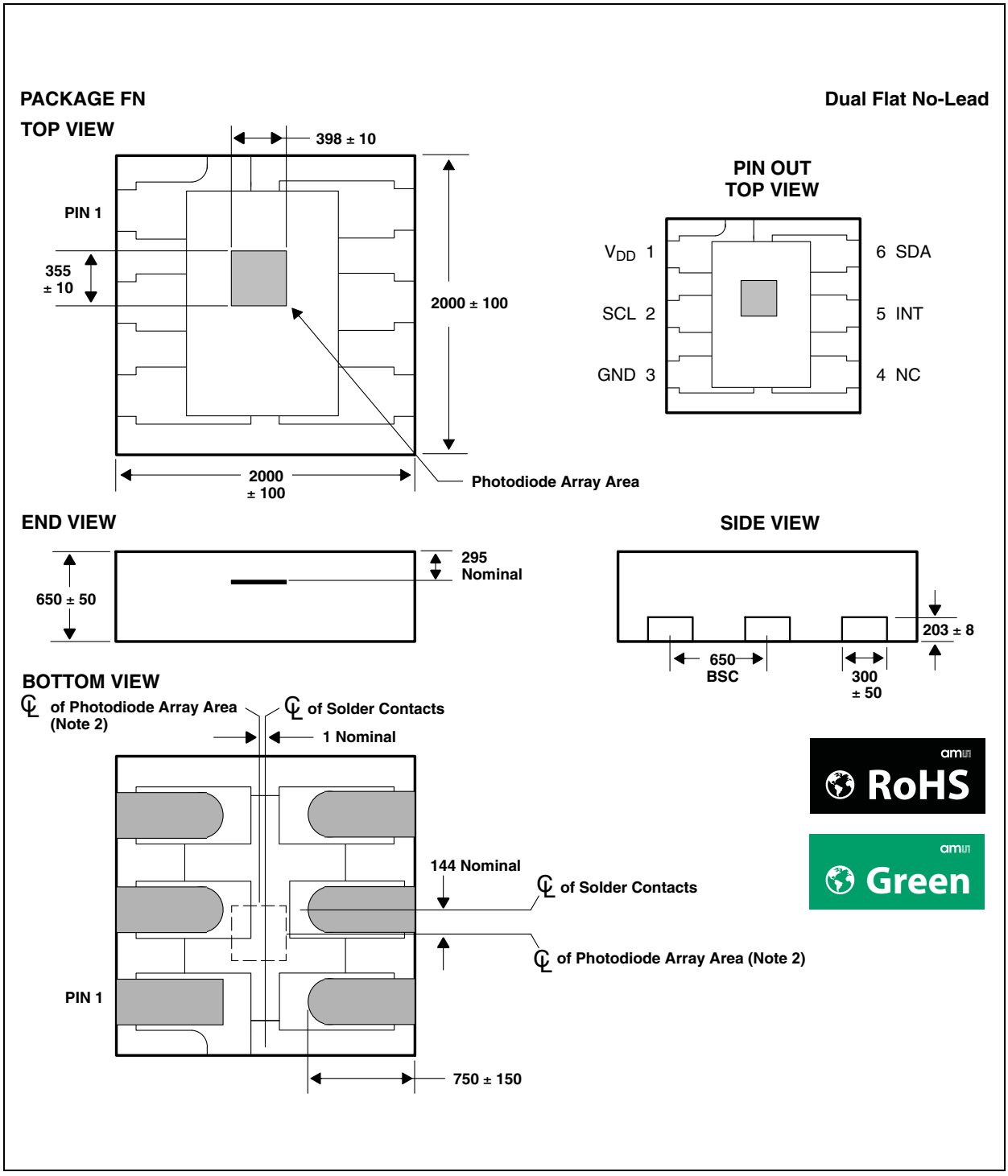


Note(s):

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Package Information

Figure 35:
Package FN — Dual Flat No-Lead Packaging Configuration

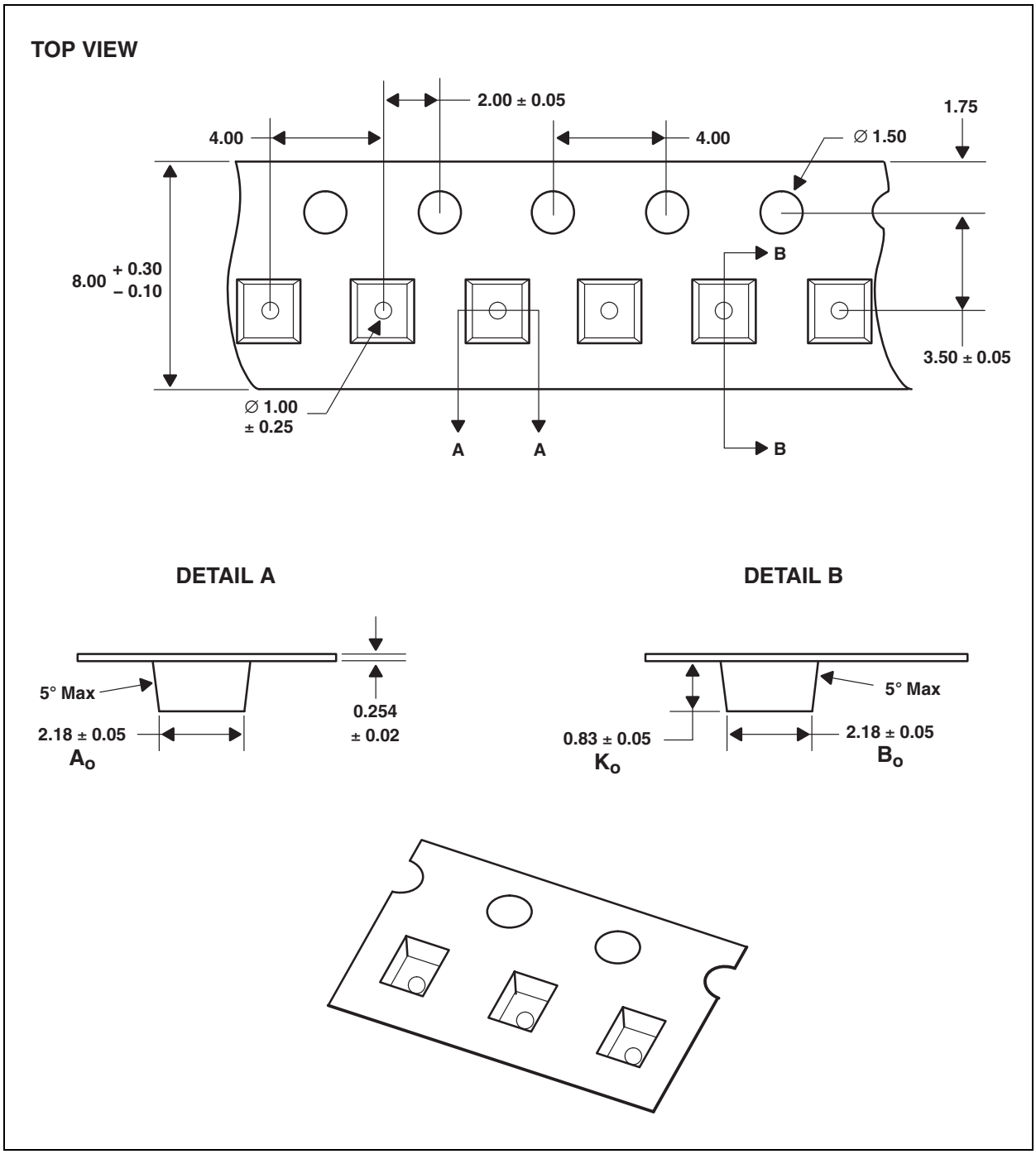


Note(s):

1. All linear dimensions are in micrometers.
2. The die is centered within the package within a tolerance of ± 75 µm.
3. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

Carrier Tape & Reel Information

Figure 36:
Package FN Carrier Tape



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 178 millimeters in diameter and contains 3500 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481-B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Soldering Information

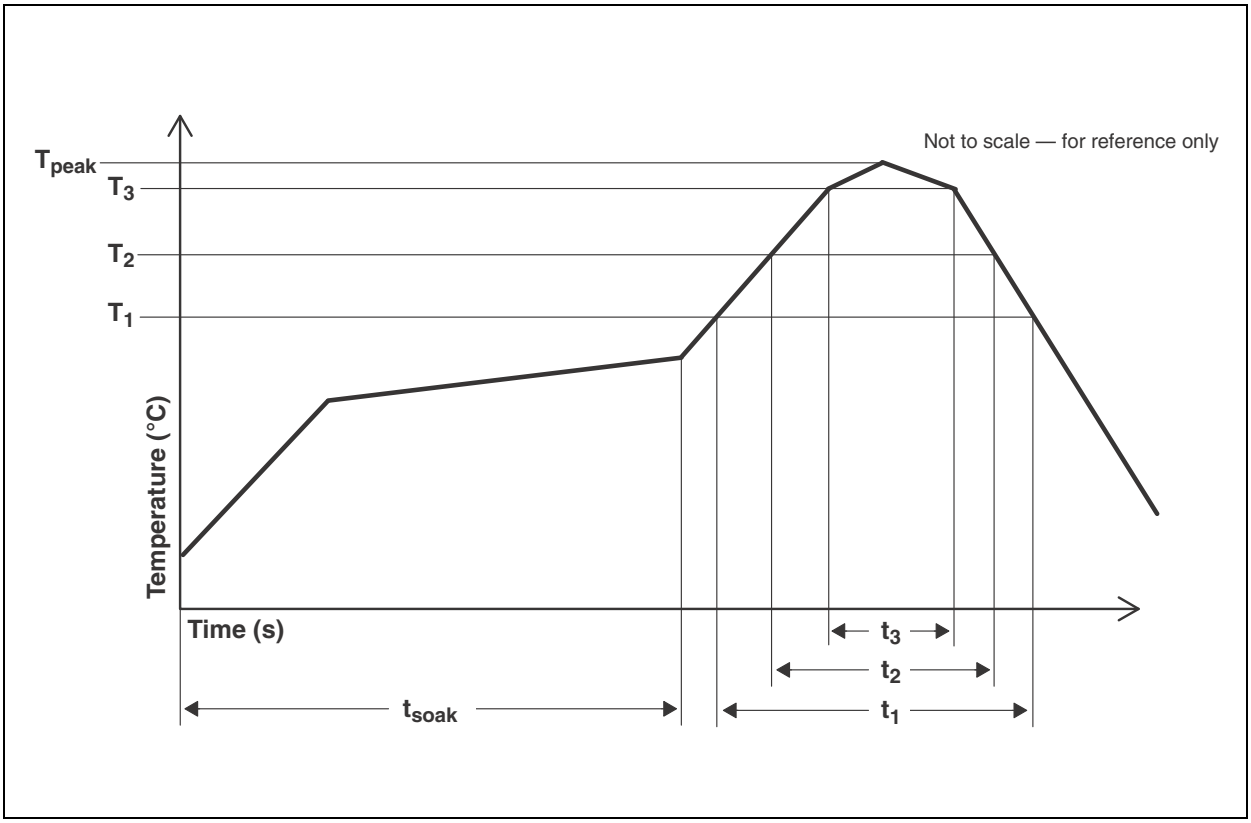
The FN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 37:
Soldier Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T_1)	t_1	Max 60 s
Time above 230°C (T_2)	t_2	Max 50 s
Time above T_{peak} –10°C (T_3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max –5°C/s

Figure 38:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping.
Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: < 40°C
- Relative Humidity: < 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The FN package has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: < 30°C
- Relative Humidity: < 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 39:
Ordering Information

Ordering Code	Device	Address	Package - Leads	Interface Description
TSL25721FN	TSL25721	0x39	FN–6	I^2C Vbus = V_{DD} Interface
TSL25723FN	TSL25723	0x39	FN–6	I^2C Vbus = 1.8 V Interface

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Revision Information

Changes from 1-00 (2016-Apr-01) to current revision 1-01 (2018-Mar-27)	Page
Updated Figure 6	7
Updated Figure 7	7
Updated Figure 30	26
Updated Figure 39	34

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide