42V/2A + 3× 8V/1A, 2MHz Quad Monolithic Synchronous Step-Down Regulator

FEATURES

- Flexible Power Supply System Providing Four Outputs with a Wide Input Range
- One High Voltage Synchronous Buck Regulator
  - 3V to 42V Input Voltage Range
  - Continuous Output Current Up to 2A
  - High Efficiency Up to 93%
- Three Low Voltage Synchronous Buck Regulators
  - 1.2V to 8V Input Voltage Range
  - Continuous Output Currents Up to 1A
  - High Efficiency Up to 95%
- Silent Switcher® Architecture
  - Ultralow EMI/EMC Emissions
  - Spread Spectrum Frequency Modulation
- Ultralow Quiescent Current Burst Mode® Operation
  - 9.6µA I_Q Regulating $12V_{IN1}$ to $5V/3.3V/1.8V/1.2V_{OUT1-4}$
  - Output Ripple <$10mV_{PK-PK}$
- External Synchronization Capability
- Forced Continuous Mode Capability
- Small Thermally Enhanced 4mm × 3mm 20-Lead LQFN Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Camera Modules
- Automotive Systems
- Industrial Controls and Power Supplies

DESCRIPTION

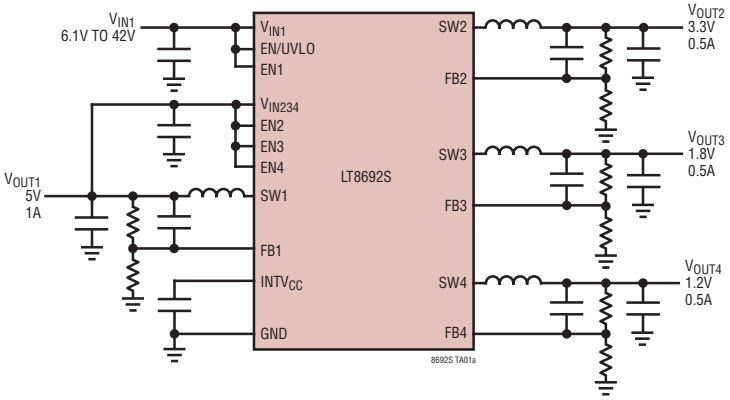
The LT®8692S is a quad channel step-down, current mode, monolithic buck switching regulator. All regulators are synchronized to a single oscillator with a fixed frequency of 2MHz. The "S" at the end of the part number refers to the second-generation Silent Switcher® technology which includes integrated bypass capacitor to deliver a high frequency and small solution size with excellent EMI performance. The integrated capacitors also make it easier to achieve the advertised EMI performance by reducing layout sensitivity. This performance makes the LT8692S ideal for noise sensitive applications and environments. The highly integrated four-channel solution saves space and simplifies the design of compact boards.

Burst Mode operation enables ultralow standby current consumption, forced continuous mode can be used to control frequency harmonics across the entire output load range or spread spectrum operation can further reduce EMI emissions.

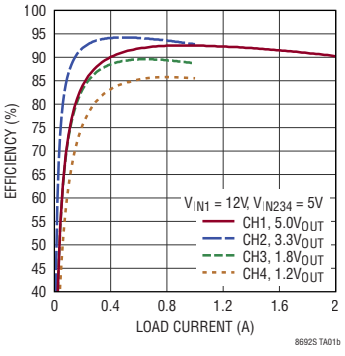
The fast, clean, low overshoot switching edges enable high efficiency operation at high switching frequencies, leading to a small solution size with wide control loop bandwidth for fast transient response.

TYPICAL APPLICATION

5V/1A, 3.3V/0.5A, 1.8V/0.5A, 1.2V/0.5A, 2MHz Step-Down Converter



Efficiency, FCM

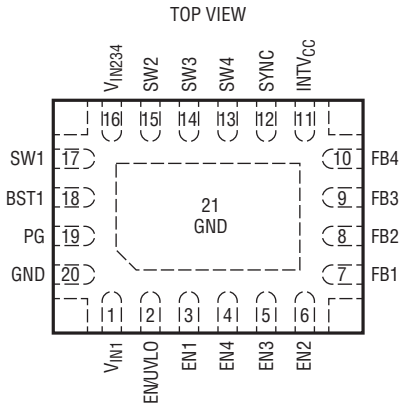


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, EN/UVLO, EN1 ..... 42V
PG 25V
EN2, EN3, EN4, V_{IN234} 8V
SYNC 6V
FB1, FB2, FB3, FB4 ..... 4V
$INTV_{CC}$, BST1 ..... (Note 2)
Operating Junction Temperature (Notes 3, 4)
LT8692SI ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Peak Package Body temperature ..... 260°C

PIN CONFIGURATION



LQFN PACKAGE
20-LEAD (4mm × 3mm × 0.94mm) PLASTIC LQFN

T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB GND

ORDER INFORMATION

PART NUMBER	TAPE AND REEL PART NUMBER	PART MARKING	FINISH CODE	PAD FINISH	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
LT8692SIV#PBF	LT8692SIV#TRPBF	8692S	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C
AUTOMOTIVE PRODUCTS*							
LT8692SIV#WPBF	LT8692SIV#WTRPBF	8692S	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C

- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Tape and reel specifications.
- Parts ending with PBF are RoHS and WEEE compliant.
- Recommended BGA PCB Assembly and Manufacturing Procedures.
- BGA Package and Tray Drawings

* Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1} Quiescent Current in Shutdown	$V_{EN/UVLO}$ = V_{EN1-4} = 0V, V_{SYNC} = 0V	●		2.3	5.4 11	µA µA
V_{IN1} + V_{CC} Quiescent Current in Sleep	$V_{EN/UVLO}$ = V_{EN1-4} = 2V, V_{FB1-4} > 0.8V, V_{SYNC} = 0V	●		5.8	12.5 25	µA µA
Oscillator Frequency		●	1.8	2	2.2	MHz
PG Upper Threshold Offset from V_{FB1} to V_{FB4}	V_{FB1} to V_{FB4} Rising	●	6	7.5	9	%
PG Lower Threshold Offset from V_{FB1} to V_{FB4}	V_{FB1} to V_{FB4} Falling	●	–9	–7.5	–6	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PG Hysteresis				0.15		%
PG Leakage	V_{PG} = 12V		–50		50	nA
PG Pull-Down Resistance	V_{PG} = 0.1V	●		200	500	Ω
SYNC Threshold	SYNC DC and Clock Low Level Voltage SYNC Clock High Level Voltage SYNC DC High Level Voltage		0.4		 1.5 2.8	V V V
SYNC Frequency			1.6		2.5	MHz
SYNC Current	V_{SYNC} = 6V			15		µA
EN/UVLO Threshold	EN/UVLO Falling	●	0.7	0.74	0.78	V
EN/UVLO Hysteresis				20		mV
EN/UVLO Input Current	$V_{EN/UVLO}$ = 2V		–50		50	nA
Channel 1						
Minimum Input Voltage V_{IN1}		●		2.4	3	V
Feedback Reference Voltage		●	0.79	0.8	0.81	V
Feedback Input Current		●	–50		50	nA
Feedback Voltage Line Regulation			–0.02	0.003	0.02	%/V
Minimum On-Time	I_{LOAD} = 1.5A, FCM	●		20	50	ns
Top Power NMOS Current Limit			3.2	4.2	5.2	A
Bottom Power NMOS Current Limit			2.2	2.9	3.6	A
SW Leakage Current			–5		5	µA
Power FET On-Resistance Main Switch (Top) Synchronous Switch (Bottom)	 I_{SW1} = 1A I_{SW1} = 1A			 250 120		 mΩ mΩ
EN1 Threshold	EN1 Falling	●	0.64	0.68	0.72	V
EN1 Hysteresis				20		mV
EN1 Input Current	V_{EN1} = 2V	●	–50		50	nA
Channel 2 to Channel 4						
Minimum Input Voltage V_{IN234}		●		1	1.2	V
Feedback Reference Voltage		●	0.79	0.8	0.81	V
Feedback Input Current		●	–50		50	nA
Feedback Voltage Line Regulation			–0.025	0.005	0.025	%/V
Minimum On-Time	I_{LOAD} = 0.1A, FCM	●		20	50	ns
Top Power NMOS Current Limit			1.8	2.4	3	A
Bottom Power NMOS Current Limit			0.9	1.3	1.7	A
SW Leakage Current			–5		5	µA
Power FET On-Resistance Main Switch (Top) Synchronous Switch (Bottom)	 I_{SW2-4} = 0.8A I_{SW2-4} = 0.8A			 170 65		 mΩ mΩ
EN2 to EN4 Threshold	EN2 to EN4 Falling	●	0.64	0.68	0.72	V
EN2 to EN4 Hysteresis				20		mV
EN2 to EN4 Input Current	V_{EN2-4} = 2V	●	–50		50	nA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

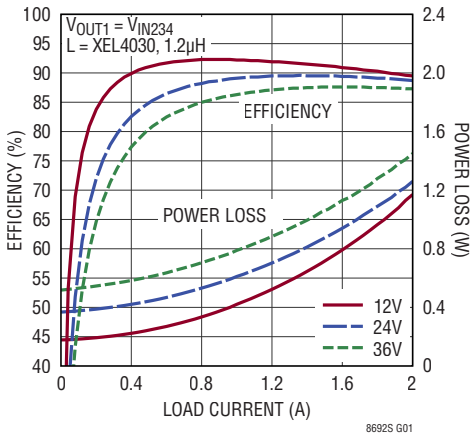
Note 2: Do not apply a positive or negative source voltage to these pins, or a permanent damage may occur

Note 3: The LT8692SI is specified over the –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

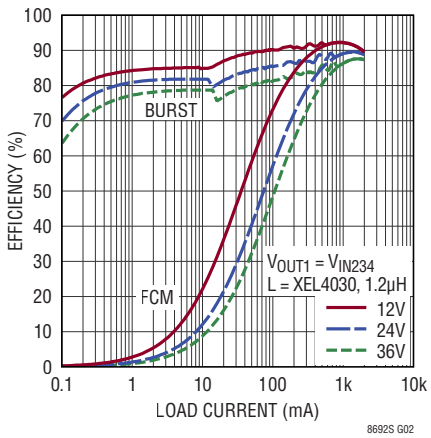
Note 4: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

TYPICAL PERFORMANCE CHARACTERISTICS

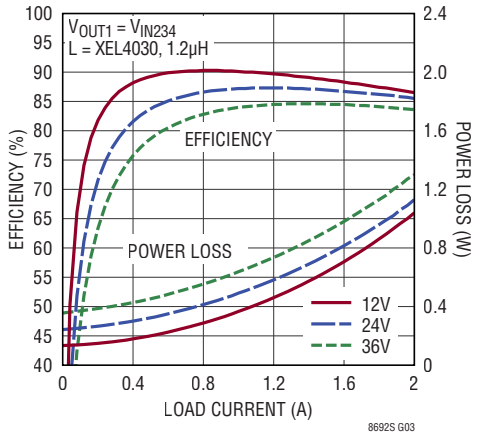
CH1, $5V_{OUT}$ Efficiency and Power Loss, FCM



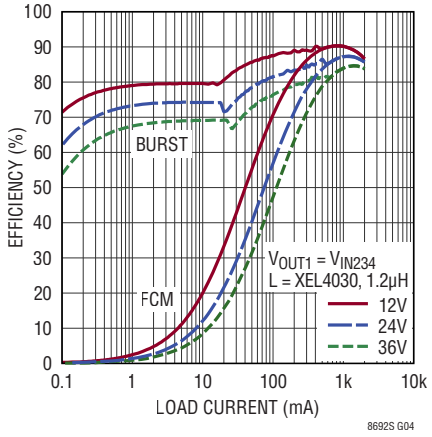
CH1, $5V_{OUT}$ Efficiency



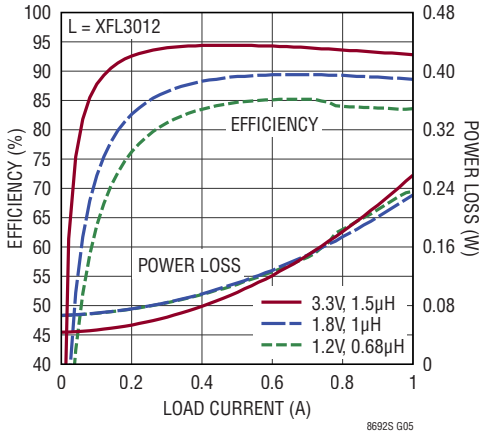
CH1 $3.3V_{OUT}$ Efficiency and Power Loss, FCM



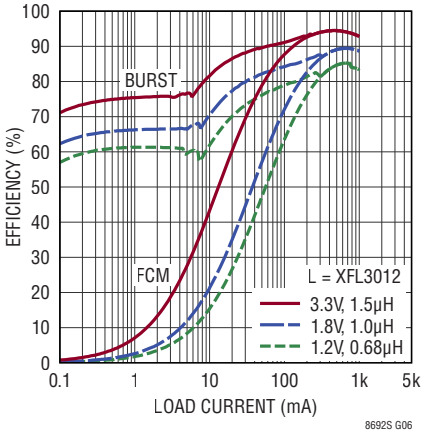
CH1 $3.3V_{OUT}$ Efficiency



CH2 to CH4 $5V_{IN}$ Efficiency and Power Loss, FCM

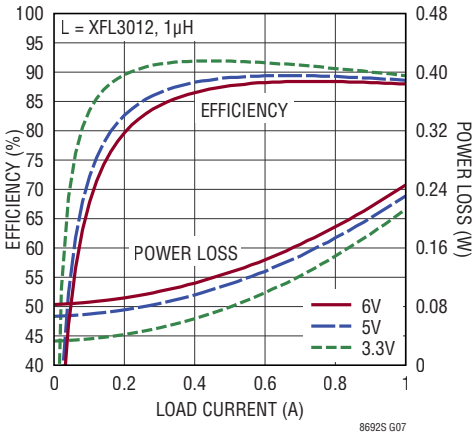


CH2 to CH4 $5V_{IN}$ Efficiency

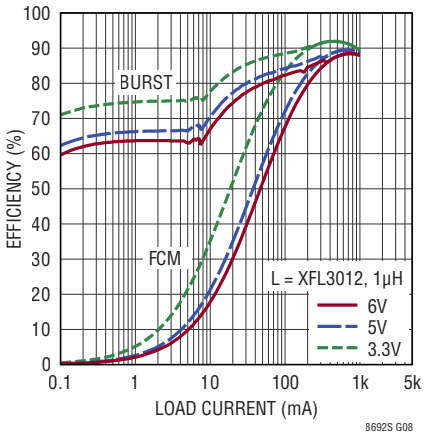


TYPICAL PERFORMANCE CHARACTERISTICS

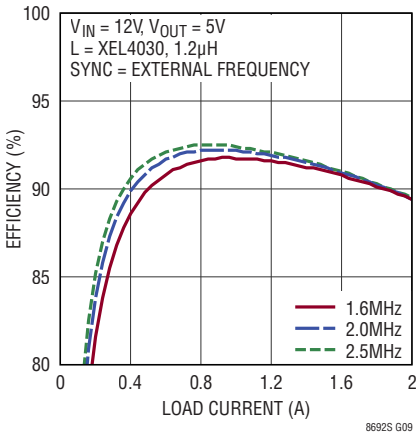
CH2 to CH4 1.8V_{OUT} Efficiency and Power Loss, FCM



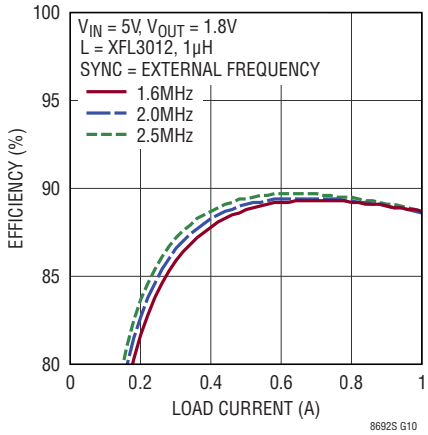
CH2 to CH4 1.8V_{OUT} Efficiency



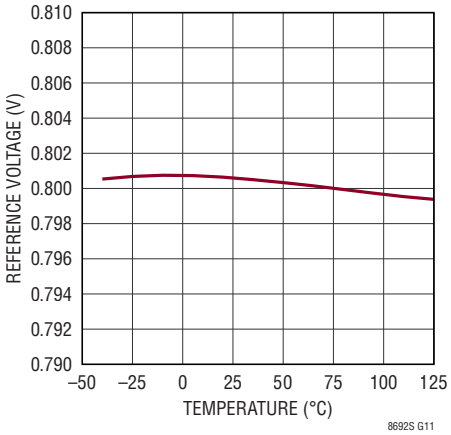
CH1 Efficiency at Different f_{SW}



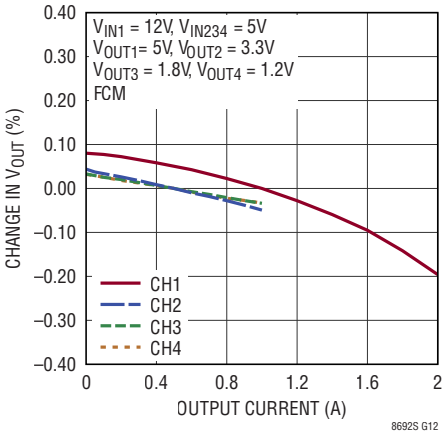
CH2 to CH4 Efficiency at Different f_{SW}



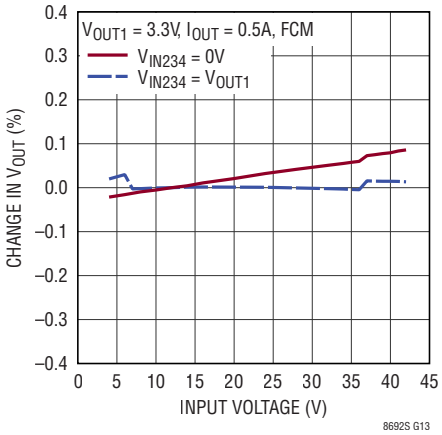
FB Reference Voltage



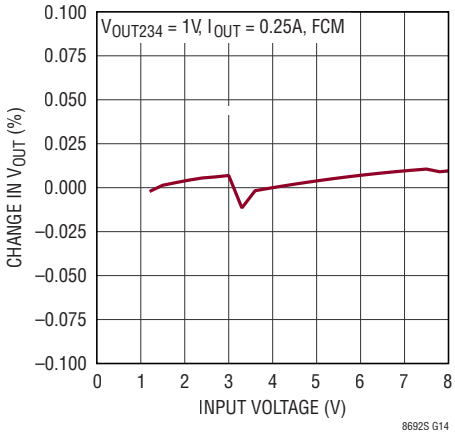
Load Regulation, FCM



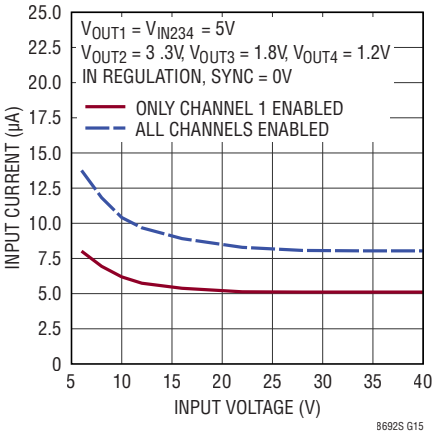
CH1 Line Regulation, FCM



CH2 to CH4 Line Regulation, FCM

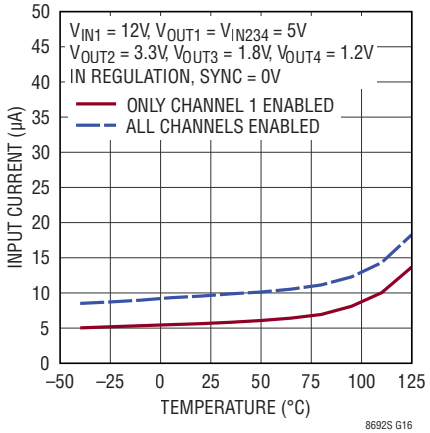


No Load Supply Current

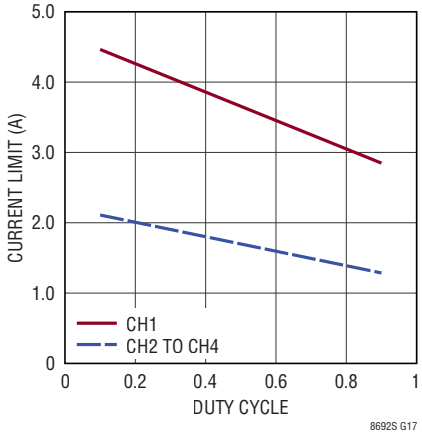


TYPICAL PERFORMANCE CHARACTERISTICS

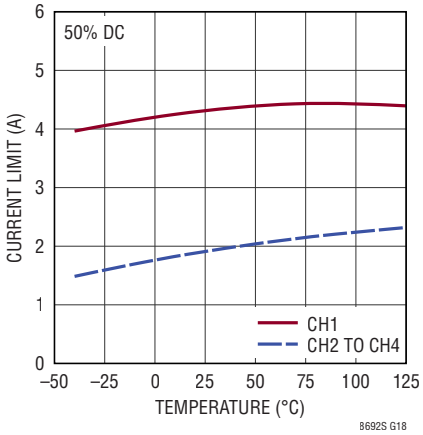
No Load Supply Current



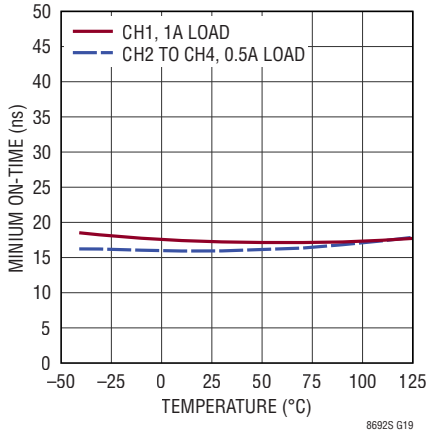
Top MOSFET Current Limit



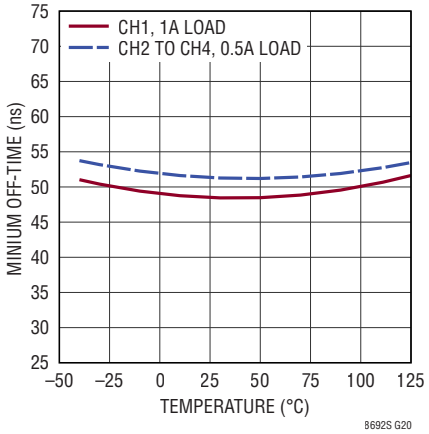
Top MOSFET Current Limit



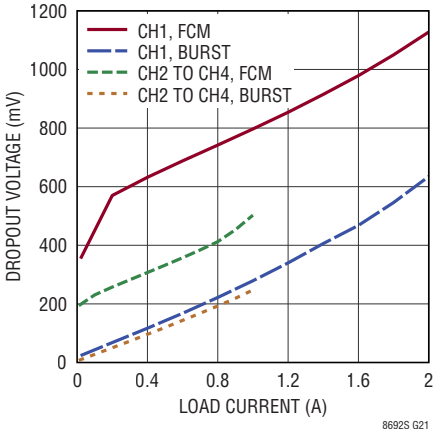
Minimum On-Time, FCM



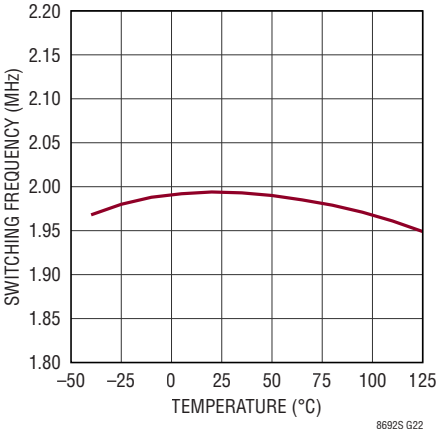
Minimum Off-Time, FCM



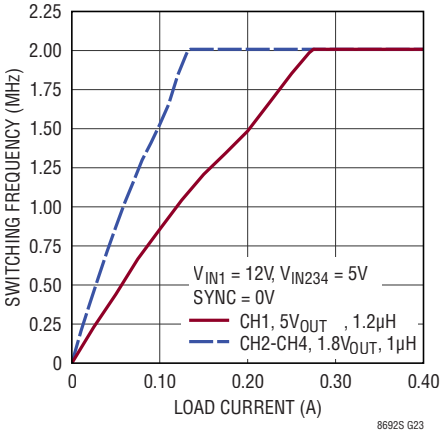
Dropout Voltage



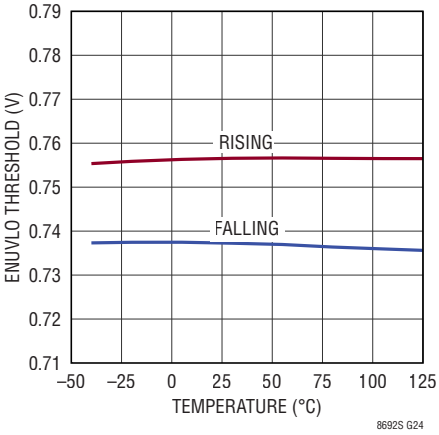
Switching Frequency



Burst Mode Frequency

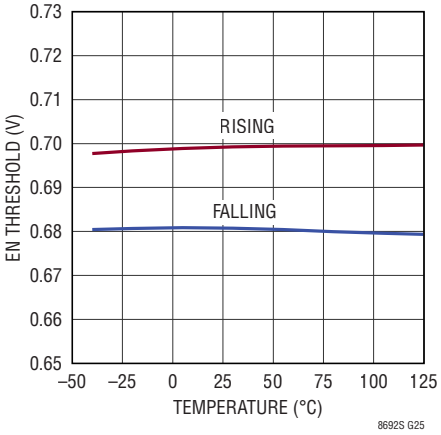


EN/UVLO Pin Threshold

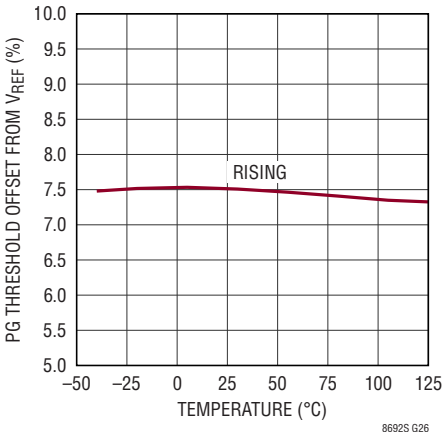


TYPICAL PERFORMANCE CHARACTERISTICS

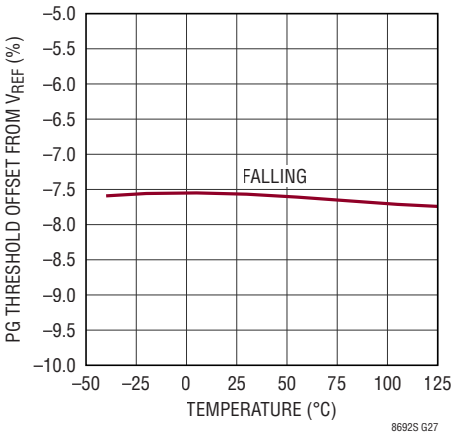
EN Pin Threshold



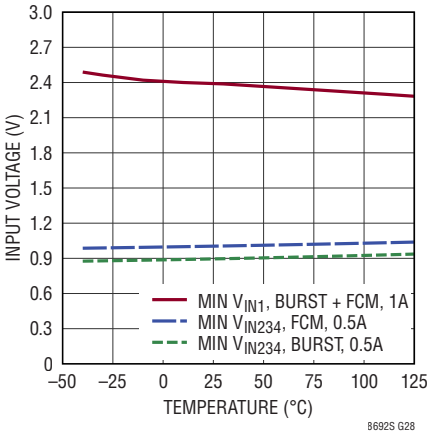
PG High Threshold



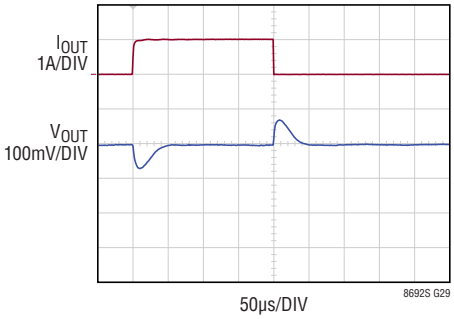
PG Low Threshold



Minimum Input Voltage

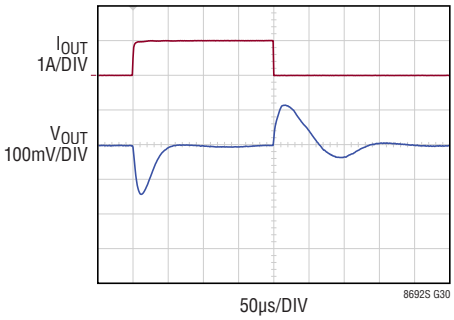


CH1 Transient Response, FCM



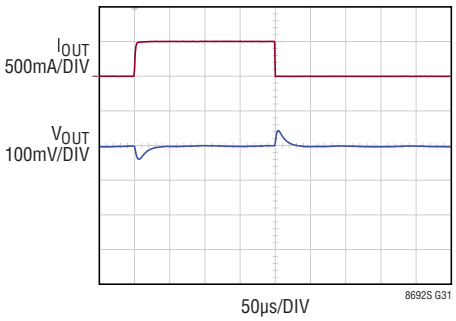
0A TO 1A TRANSIENT, FCM
$5V_{OUT}$, Ra = 100k, Rb = 19.1k
C_{OUT} = 47µF ×2, C_{PL} = 100pF

CH1 Transient Response, Burst Mode Operation



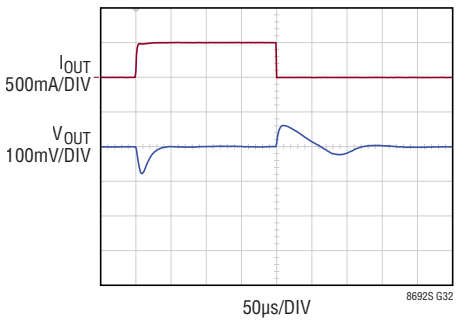
0A TO 1A TRANSIENTATION, Burst Mode OPERATION
$5V_{OUT}$, Ra = 100k, Rb =19.1k
C_{OUT} = 47µF ×2, C_{PL} = 100pF

CH2 to CH4 Transient Response, FCM



0A TO 0.5A TRANSIENT, FCM
$1.8V_{OUT}$, Ra = 100k, Rb = 80k
C_{OUT} = 47µF, C_{PL} = 100pF

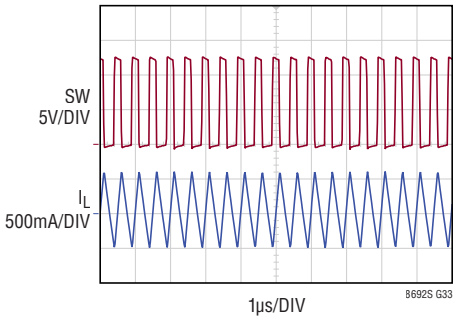
CH2 to CH4 Transient Response, Burst Mode Operation



0A TO 0.5A TRANSIENT, Burst Mode OPERATION
$1.8V_{OUT}$, Ra = 100k, Rb = 80k
C_{OUT} = 47µF, C_{PL} = 100pF

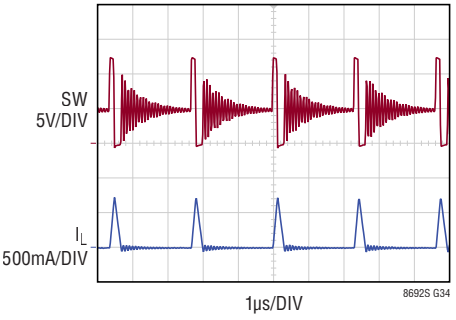
TYPICAL PERFORMANCE CHARACTERISTICS

CH1 FCM Operation



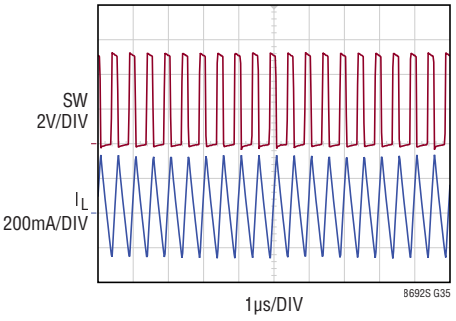
$12V_{IN}$ TO $5V_{OUT}$ AT 50mA
SYNC = FLOAT

CH1 Burst Mode Operation



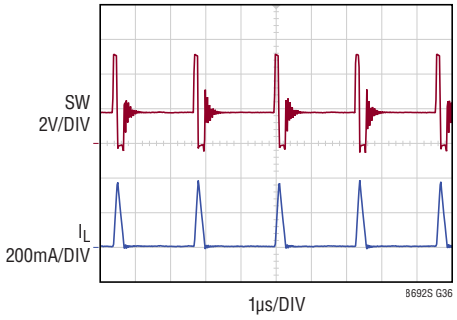
$12V_{IN}$ TO $5V_{OUT}$ AT 50mA
SYNC = 0V

CH2 to CH4 FCM Operation



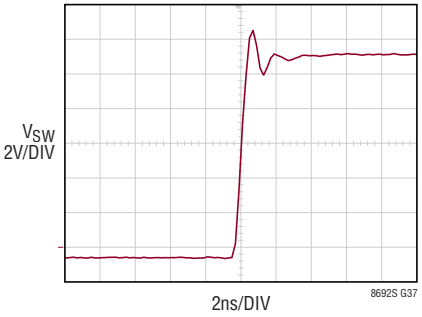
$5V_{IN}$ TO $1.8V_{OUT}$ AT 25mA
SYNC = FLOAT

CH2 to CH4 Burst Mode Operation

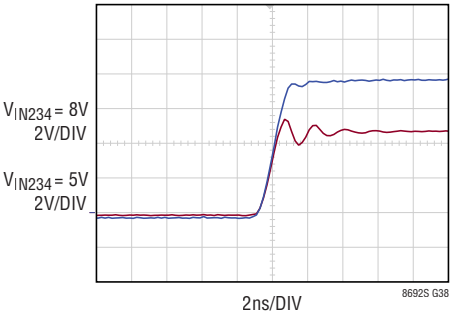


$5V_{IN}$ TO $1.8V_{OUT}$ AT 25mA
SYNC = 0V

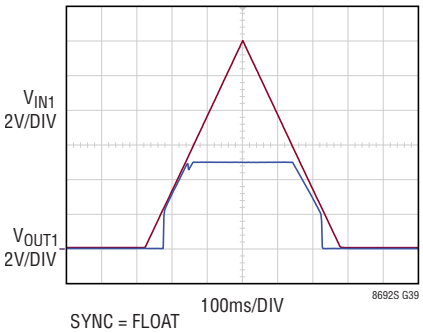
SW1 Rising Edge



SW2 to SW4 Rising Edge

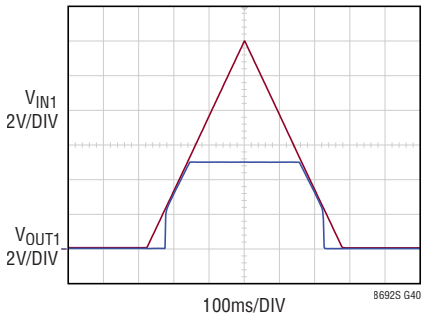


CH1 Start-Up Dropout Performance



SYNC = FLOAT
EN1 = V_{IN1}
5Ω LOAD
(1A IN REGULATION)

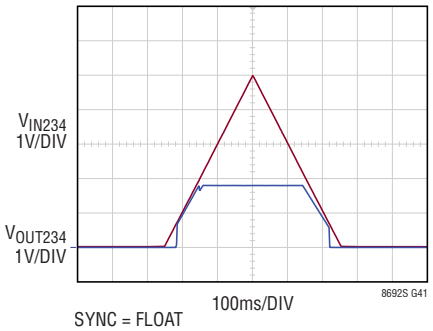
CH1 Start-Up Dropout Performance



SYNC = 0V
EN1 = V_{IN1}
5Ω LOAD
(1A IN REGULATION)

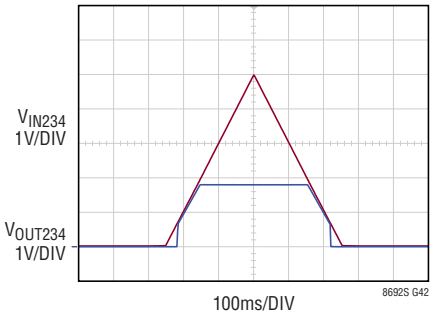
TYPICAL PERFORMANCE CHARACTERISTICS

CH2 to CH4 Start-Up Dropout Performance



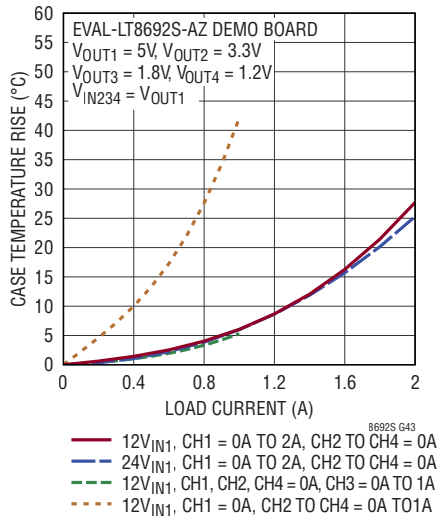
SYNC = FLOAT
EN2 TO EN4 = V_{IN234}
3.6Ω LOAD
(0.5A IN REGULATION)

CH2 to CH4 Start-Up Dropout Performance

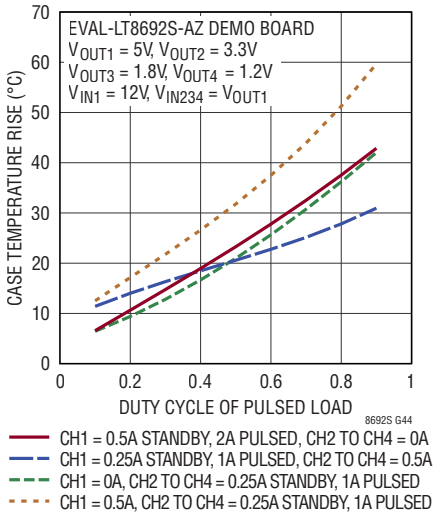


SYNC = 0V
EN2 TO EN4 = V_{IN234}
3.6Ω LOAD
(0.5A IN REGULATION)

Case Temperature Rise

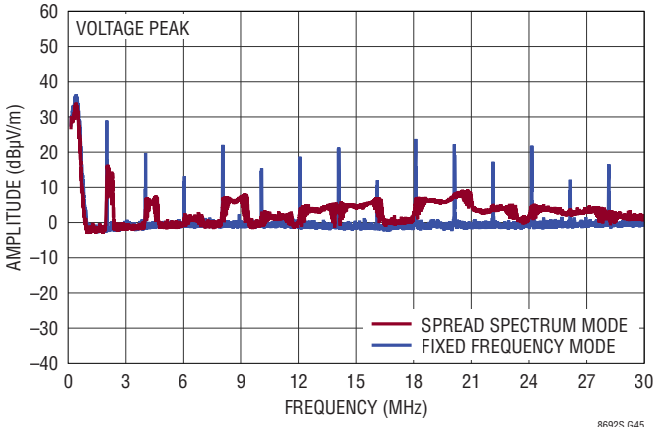


Case Temperature Rise



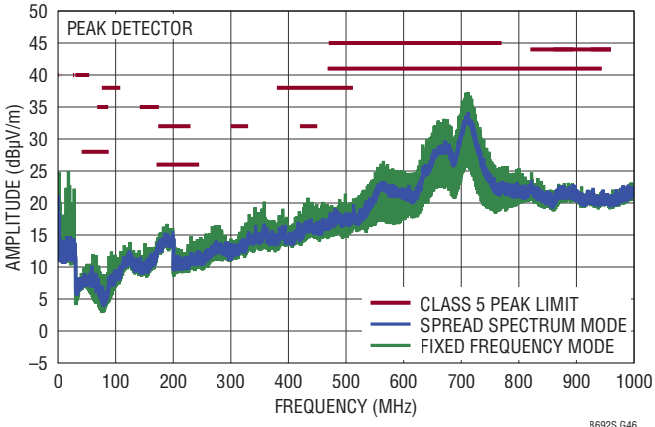
TYPICAL PERFORMANCE CHARACTERISTICS

Conducted EMI Performance



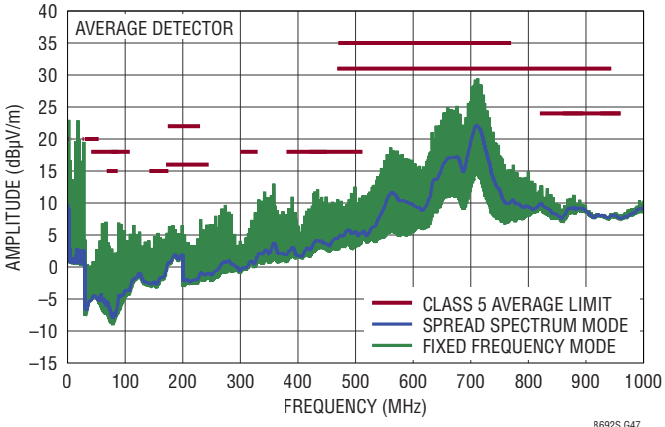
EVAL-LT8692S-AZ DEMO BOARD (WITH EMI FILTER INSTALLED)
14V INPUT TO 5V_{OUT1}/0.7A, 3.3V_{OUT2}/0.3A, 1.8V_{OUT3}/0.6A, 1.2V_{OUT4}/0.5A

Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)



EVAL-LT8692S-AZ DEMO BOARD (WITH EMI FILTER INSTALLED)
14V INPUT TO 5V_{OUT1}/0.7A, 3.3V_{OUT2}/0.3A, 1.8V_{OUT3}/0.6A, 1.2V_{OUT4}/0.5A

Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)



EVAL-LT8692S-AZ DEMO BOARD (WITH EMI FILTER INSTALLED)
14V INPUT TO 5V_{OUT1}/0.7A, 3.3V_{OUT2}/0.3A, 1.8V_{OUT3}/0.6A, 1.2V_{OUT4}/0.5A

PIN FUNCTIONS

V_{IN1} (Pin 1): Channel 1 Power Supply Input and internal circuitry power supply. This pin should be closely decoupled to the nearest ground pin with a low ESR capacitor of value 1µF or greater. See the Applications Information section for more details

EN/UVLO (Pin 2): Chip Enable Input. LT8692S is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 0.76V going up and 0.74V going down. Tie to V_{IN1} if the shutdown feature is not used. An external resistor divider from V_{IN1} can be used to program a V_{IN1} threshold below which the LT8692S will shut down. Do not float this pin.

EN1 (Pin 3): Channel 1 Enable Input Pin. The channel is active when the voltage on its corresponding enable pin is above 0.68V (within 15% of FB pin reference voltage). A precision threshold allows each enable pin to act as a programmable undervoltage lockout by connecting a resistor divider between the corresponding input supply and ground. If the channel is not used, tie EN1 pin to ground. If the enable function is not used, tie the EN1 pin to EN/UVLO.

EN2, EN3, EN4 (Pin 6, Pin 5, Pin 4): Channel 2 to channel 4 Enable Input Pins. Each channel is active when the voltage on its corresponding enable pin is above 0.68V (within 15% of FB pin reference voltage). A precision threshold allows each enable pin to act as a programmable undervoltage lockout by connecting a resistor divider between the corresponding input supply and ground. If a channel is not used, tie the respective EN pin to ground. These pins can also be used for sequencing, i.e., connect EN2 pin to FB1 pin in order for channel 2 to turn on after channel 1 is within 15% of its regulation voltage. If sequencing is not used, tie the EN pin to the $INTV_{CC}$ pin or to the V_{IN234} pin. If channel is not used, connect corresponding EN pin to GND.

FB1, FB2, FB3, FB4 (Pin 7, Pin 8, Pin 9, Pin 10): Output Voltage Feedback Inputs. Each channel regulates its respective pin to a precision, internal, 0.8V reference voltage. Connect these pins to the appropriate resistor divider networks to program the desired output voltage.

$INTV_{CC}$ (Pin 11): Internal Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. $INTV_{CC}$ current will be supplied from V_{IN234} if $V_{IN234} > 3.1V$, otherwise current will be drawn from V_{IN1}. Voltage on V_{INTVCC} will vary between 2.8V and 3.3V when V_{IN234} is between 3.0V and 3.5V. Do not load $INTV_{CC}$ pin with external circuitry.

SYNC (Pin 12): External Clock Synchronization Input. Ground this pin for low ripple Burst Mode operation at low output loads. Apply a DC voltage of 2.8V or higher or tie to $INTV_{CC}$ for forced continuous mode with spread spectrum modulation. Float the SYNC pin for forced continuous mode without spread spectrum modulation. When in forced continuous mode, the I_Q will increase to several mA. Apply a clock source to the SYNC pin for synchronization to an external frequency (1.6MHz to 2.5MHz). The LT8692S will be in forced continuous mode when an external frequency is applied.

SW2, SW3, SW4 (Pin 15, Pin 14, Pin 13): Channel 2 to channel 4 Switch Pins. These pins are the outputs of each corresponding channel's internal power switches. Connect each SW pin to the corresponding channel's inductor. SW traces on the PCB should be kept short for best efficiency and EMI performance.

V_{IN234} (Pin 16): Channel 2 to channel 4 Power Supply Input. This pin should be closely decoupled to the nearest ground with a low ESR capacitor of value 1µF or greater. See the Applications Information section for more details.

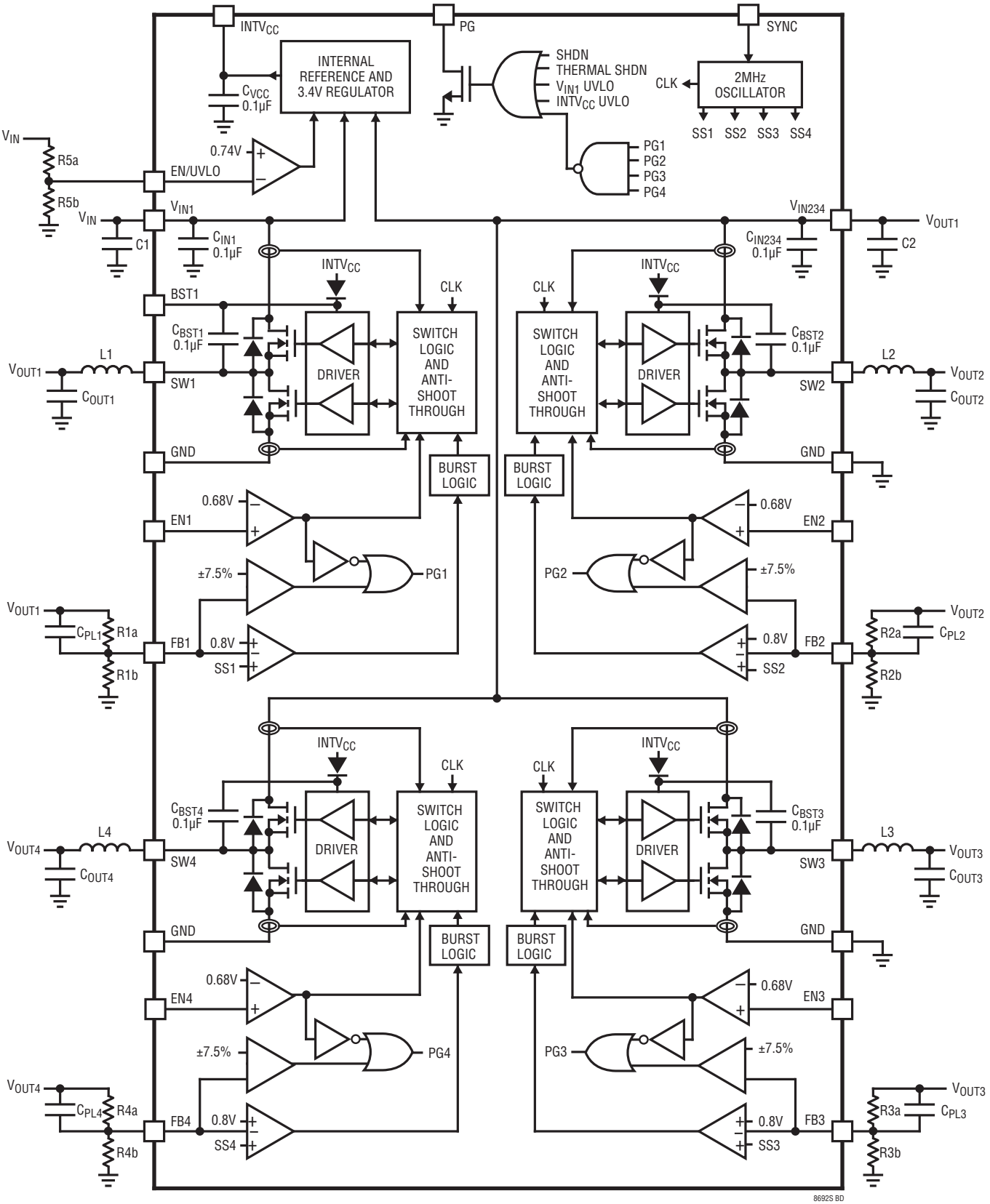
SW1 (Pin 17): Channel 1 Switch Pin. This pin is the output of the channel 1 internal power switches. The SW1 trace on the PCB should be kept short for best efficiency and EMI performance.

BST1 (Pin 18): Channel 1 connection to an external boost capacitor that is used for turning on the top switch. A 0.22µF capacitor between BST1 and SW1 pins may be used, but not required.

PG (Pin 19): Power Good Output. The PG pin is the open-drain output of an internal comparator. PG remains open until all FB pins of the enabled channels are within ±7.5% of the final regulation voltage and there are no fault conditions. PG is pulled low during V_{IN1} UVLO, V_{CC} UVLO, thermal shutdown or when the EN/UVLO pin is low.

GND (Exposed Pad, Pin 20): Ground Pins. These pins must be soldered to the PCB to provide low impedance electrical contact to ground and good thermal contact to the PCB.

BLOCK DIAGRAM



OPERATION

The LT8692S is a quad channel, constant frequency, current mode, monolithic step-down regulator. All channels are synchronized to a single oscillator. One of the channels is high voltage (up to 42V input) while the other three are low voltage (up to 8V input) and are typically powered from the output of the high voltage channel. The "S" in LT8692S refers to the second generation Silent Switcher technology. This technology allows fast switching edges for high efficiency at high switching frequencies, while simultaneously achieving good EMI/EMC performance. This includes the integration of ceramic capacitors into the package for V_{IN1}, driver boost capacitor for channel 1 to channel 4, V_{IN234}, and $INTV_{CC}$. These capacitors keep all the fast AC current loops small, which improves EMI/EMC performance.

Start-Up

When enabled by setting the EN/UVLO voltage above its threshold, the LT8692S starts charging the $INTV_{CC}$ capacitor from V_{IN1}. If V_{IN234} is higher than 3.1V, the current to the internal $INTV_{CC}$ regulator is supplied from V_{IN234} to reduce V_{IN1} quiescent current.

High Voltage Buck Regulator

The high voltage channel is a synchronous buck regulator that operates from an independent V_{IN} pin. The internal top power MOSFET is turned on at the beginning of each oscillator cycle and turned off when the current flowing through the top MOSFET reaches a level determined by the error amplifier. The error amplifier measures the output voltage through an external resistor divider tied to the FB pin to control the peak current in the top switch. The reference of the error amplifier is determined by the lower of the internal 0.8V reference and the voltage provided by the soft-start circuitry output SS1. The SS1 is reset during shutdown, V_{IN1} undervoltage or thermal shutdown.

While the top MOSFET is off, the bottom MOSFET is turned on for the remainder of the oscillator cycle (in FCM mode) or until inductor current falls to zero (not in FCM mode). If overload conditions result in more than the bottom N-channel MOSFET current limit flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

Low Voltage Buck Regulators

Each low voltage channel is a synchronous buck regulator that operates from a common V_{IN234} pin. Each internal top power MOSFET is turned on at the beginning of each oscillator cycle, and turned off when the current flowing through the top MOSFET reaches a level determined by the error amplifier. The error amplifier measures the output voltage through an external resistor divider tied to the FB pin to control the peak current in the top switch. The reference of the error amplifier is determined by the lower of the internal 0.8V reference and the voltage provided by the soft start circuitry output SS2 to SS4. SS2 to SS4 are reset during shutdown, V_{IN1} undervoltage or thermal shutdown.

While the top MOSFET is off, the bottom MOSFET is turned on for the remainder of the oscillator cycle (in FCM mode) or until inductor current falls to zero (not in FCM mode). If overload conditions result in more than the bottom N-channel current limit flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

Light Load Operation

If the SYNC pin is low, at light load, the regulators operate in low ripple Burst Mode operation. Low ripple Burst Mode operation shuts down most internal circuitry between switch on cycles to conserve power while still retaining low ripple at the output. If the SYNC pin left floating, FCM mode will be active. If the SYNC pin pulled high, FCM mode with spread spectrum (SSM) will be active. In case of FCM or FCM with SSM, internal circuitry is always on and the power switches activate every cycle, providing a predictable switching frequency, but lower efficiency at light loads.

OPERATION

Undervoltage Lockout

The EN/UVLO pin is used to put the LT8692S in shutdown, reducing the input to several microamps. The accurate 0.74V threshold of the EN/UVLO pin allows a programmable V_{IN1} undervoltage lockout through an external resistor divider tied to the EN/UVLO pin. A 20mV (typical) hysteresis voltage in the EN/UVLO pin protects against noise inadvertently shutting down the LT8692S.

Overvoltage Protection

If V_{IN1} rises higher than 37V or V_{IN234} is higher than 7.5V the corresponding channels will disable FCM mode in order to avoid input overvoltage due to the energy flow from the output to the input.

Power Good Comparators

Each channel has a power good comparator that trips when the feedback pin is within 7.5% of the final regulated value. The power good comparators outputs are combined into a single open drain output PG pin that is pulled low when an output of an enabled channel is out of regulation or a fault condition is present.

APPLICATIONS INFORMATION

Achieving Ultralow Quiescent Current

To enhance efficiency at light loads, the LT8692S can operate in low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and minimizing output voltage ripple. 2.3µA is supplied by V_{IN1} to common bias circuits. In Burst Mode operation the LT8692S delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode all channels consume a combined 5.8µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT8692S is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter quiescent current approaches 5.8µA for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.

While in Burst Mode operation the current limit of the top switch is approximately 0.7A for channel 1 and 0.4A for channel 2 to channel 4 resulting in output voltage ripple shown in Figure 2. Increasing the output capacitance will decrease the output voltage ripple proportionally. As load ramps upward from zero the switching frequency will increase but only up to the internal clock frequency of 2MHz as shown in Figure 1. The output load at which the LT8692S reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice. For some applications it is desirable to select forced continuous mode (FCM) to maintain full switching frequency down to zero output load. See Forced Continuous Mode section.

FB Resistor Network

The output voltage is programmed with a resistor between the output and the FB pin (R1a for channel 1, R2a for channel 2, R3a for channel 3, R4a for channel 4) and a resistor between FB pin and ground (R1b for channel 1, $R2_b$ for channel 2, R3b for channel 3, R4b for channel 4). Choose the resistor values according to Equation 1.

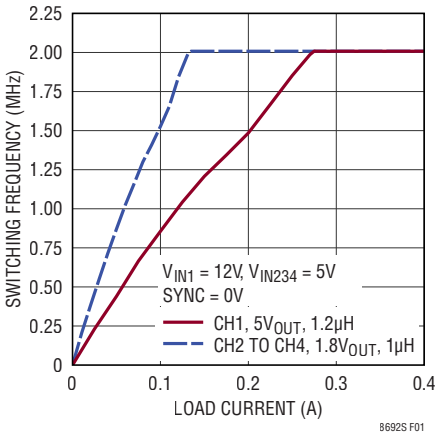


Figure 1. Burst Frequency

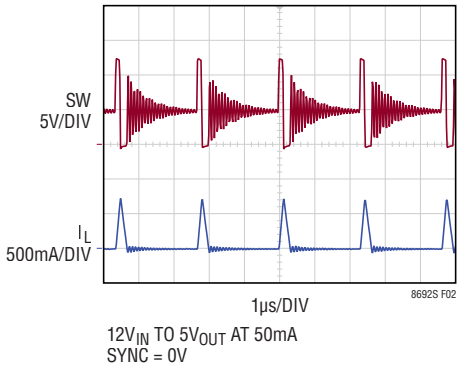


Figure 2. Burst Mode Operation

$$Ra = Rb\left(\frac{V_{OUT}}{0.8V} - 1\right) \quad (1)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

If low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a

APPLICATIONS INFORMATION

load current, and will increase the no-load input current to the converter, which is given approximately by Equation 2.

$$I_Q = 3.5\mu A + \left(\frac{V_{OUT1}}{Ra + Rb}\right)\left(\frac{V_{OUT1}}{V_{IN1}}\right)\left(\frac{1}{\eta}\right) \quad (2)$$

where 3.5µA is the quiescent current of channel 1 and common circuitry, the second term is the current in the feedback divider reflected to the input of channel 1 operating at its light load efficiency η. For a 5V application with R1 = 1M and R2 = 191k, the feedback divider draws 4.2µA. With V_{IN1} = 12V and η = 80%, this adds 2.2µA to the 3.5µA quiescent current resulting in 5.7µA no-load current from the 12V supply. Note that this equation implies that the no-load current is a function of V_{IN1}; this is plotted in the Typical Performance Characteristics section.

Each enabled channel draws extra 0.76µA from V_{IN1}. If V_{IN234} is connected to V_{OUT1}, then the current for channel 2 to channel 4 feedback dividers should be adjusted for conversion ratio and efficiency and added to the contribution of channel 1 feedback divider.

A similar calculation can be done to determine the input current contribution from the channel 2 to channel 4 feedback resistors.

For a typical FB resistor of 1M, a 4.7pF to 10pF phase-lead capacitor should be connected from V_{OUT} to FB.

Inductor Selection and Maximum Output Current

The LT8692S is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions the LT8692S safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is given by Equation 3.

$$L = k\frac{V_{OUT}}{f_{SW}} \quad (3)$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, k is 0.5 for channel 1 and 1 for channel 2 to channel 4, and L is the inductor value in µH. For channel 1, independent of the result of Equation 3, the minimum allowed inductor value is 0.8µH. To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of inductor ripple current (Equation 4)

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (4)$$

where ΔI_L is the inductor ripple current as calculated in Equation 4 and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 1A output should use an inductor with an RMS rating of greater than 1A and an I_{SAT} of greater than 1.3A. During long duration overload or short-circuit conditions, the inductor RMS rating requirement must be greater to avoid overheating of the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 0.04Ω, and the core material should be intended for high frequency applications.

The LT8692S limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) for channel 1 is approximately 4.6A at low duty cycles and decreases linearly to 3.0A at DC = 0.8. The top switch current limit (I_{LIM}) for channel 2 to channel 4 is approximately 2.2A at low duty cycles and decreases linearly to 1.4A at DC = 0.8. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current (Equation 5).

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} \quad (5)$$

APPLICATIONS INFORMATION

The peak-to-peak ripple current in the inductor can be calculated with Equation 6.

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (6)$$

where f_{SW} is the switching frequency of the LT8692S, and L is the value of the inductor. Therefore, the maximum output current that the LT8692S will deliver depends on the switch current limit, the inductor value, and the input and output voltages.

Each channel has a secondary bottom switch current limit. After the top switch has turned off, the bottom switch carries the inductor current. If for any reason the inductor current is too high, the bottom switch will remain on, delaying the top switch turning on until the inductor current returns to a safe level. This level is specified as the bottom N-channel MOSFET current limit, and is independent of duty cycle. Maximum output current in the application circuit is limited to this valley current plus one half of the inductor ripple current.

In most cases current limit is enforced by the top switch. The bottom switch limit controls the inductor current when the minimum on-time condition is violated (high input voltage, high frequency or saturated inductor).

For more information about maximum output current and discontinuous operation, see Analog Devices Application Note 44.

Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillation. The minimum inductance for such duty cycles is equal to the 60% of the value recommended earlier in this section.

Table 1. Inductor Manufacturers

VENDOR	URL
Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Toko	www.toko.com
Wurth Elektronik	www.we-online.com
Vishay	www.vishay.com

Input Capacitor

Bypass the input of the LT8692S circuit with a ceramic capacitor of X7R or X5R type placed as close as possible to the V_{IN} and GND pins. Y5V types have poor performance over temperature and applied voltage and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT8692S and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT8692S and to force this very high frequency switching current into a tight local loop, minimizing EMI. Typically, a 0.1µF capacitor in a small 0402 case size is placed as close as possible to the LT8692S and a larger bulk ceramic is added for more capacitance (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT8692S. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8692S circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8692S's voltage rating. This situation is easily avoided (see Analog Devices Application Note 88).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8692S to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8692S's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Applications section.

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Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and the addition of a phase-lead capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. See the Typical Applications section in this data sheet for suggested capacitor values.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8692S due to their piezoelectric nature. When in Burst Mode operation, the LT8692S's switching frequency depends on the load current, and at very light loads the LT8692S can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8692S operates at a lower current limit during Burst Mode operation, the noise is typically very quiet. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

Table 2. Ceramic Capacitor Manufacturers

MANUFACTURER	URL
Taiyo Yuden	www.t-yuden.com
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com

Enable Pins

The LT8692S is in shutdown when EN/UVLO pin is low and active when it is high. The rising threshold of the EN/UVLO comparator is 0.76V, with 20mV of hysteresis. The EN/UVLO pin can be tied to V_{IN1} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN1} to EN/UVLO programs the LT8692S to operate only when V_{IN1} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values of the resistor $R5_a$ from V_{IN1} pin to EN/UVLO pin and $R5_b$ from EN/UVLO pin to ground such that they satisfy Equation 7.

$$R5a = \left(\frac{V_{IN(EN)}}{0.74V} - 1 \right) R5b \quad (7)$$

where the corresponding channel will remain off until V_{IN1} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

When operating in Burst Mode operation for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT8692S. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

Each of the channels is enabled by its relative EN pin. The rising threshold of the EN comparators is 0.7V, with 20mV hysteresis. The comparator threshold is 15% lower than the regulated voltage of FB pins which can be used to sequence channels, if it is required for some channels to be on after others.

V_{CC} Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from V_{IN1} that powers the drivers and the internal bias circuitry. For this reason, V_{IN1} must be

APPLICATIONS INFORMATION

present and valid to use the other channels. The $INTV_{CC}$ regulator can supply enough current for the LT8692S's circuitry and must be bypassed to ground with a 1µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. To improve efficiency the internal LDO can also draw current from the V_{IN234} pin when the V_{IN234} pin is at 3.1V or higher. If the V_{IN234} pin is below 3.0V, the internal LDO will consume current from V_{IN1}.

Applications with high input voltage and high switching frequency where the internal LDO pulls current from V_{IN1} will increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the $INTV_{CC}$ pin.

Soft-Start

The LT8692S implements an internal soft-start function to prevent a current surge on the input supply. During the soft-start ramp the output voltage will linearly rise to its regulation voltage with a typical rise time of 0.5ms (see Figure 3).

In the case of fault conditions the soft-start is reset and will ramp when the faults are cleared. Fault conditions that restart the soft-start are the EN/UVLO pin below 0.74V, V_{IN1} falling below its undervoltage lockout threshold, or thermal shutdown.

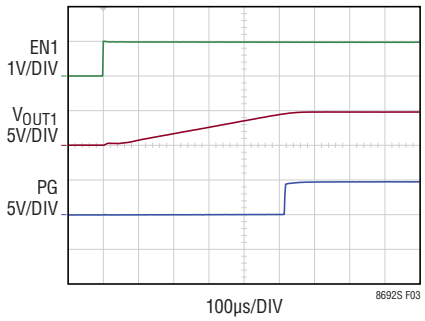

Figure 3. Soft-Start and Power Good Functions

Output Power Good

When the LT8692S's output voltage of the enabled channels is within the ±7.5% window of the regulation point, which is a FB voltage in the range of 0.74V to 0.86V (typical), the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor (see Figure 3). Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching both the upper and lower thresholds include 0.15% of hysteresis.

The PG pin is also actively pulled low during several fault conditions: EN/UVLO pin below 0.74V, $INTV_{CC}$ or V_{IN1} falling below their respective undervoltage lockout thresholds, or thermal shutdown.

Sequencing

Start-up sequencing can be configured in several ways with the LT8692S. One channel can be required to be valid before enabling the other channel to sequence their start-up order. This can be done by connecting the EN pin of the second channel to the FB pin of the first channel (see Figure 4).

Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below 0.4V (this can be ground or a logic low output). To select forced continuous mode (FCM), float the SYNC pin. To select FCM with spread spectrum modulation (SSM), tie the SYNC pin above 2.8V (SYNC can be tied to $INTV_{CC}$). To synchronize the LT8692S oscillator to an external frequency connect a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V (up to 6V). When synchronized to an external clock the LT8692S will use FCM.

LT8692S will synchronize its positive switch edge transitions to the positive edge of the SYNC signal.

APPLICATIONS INFORMATION

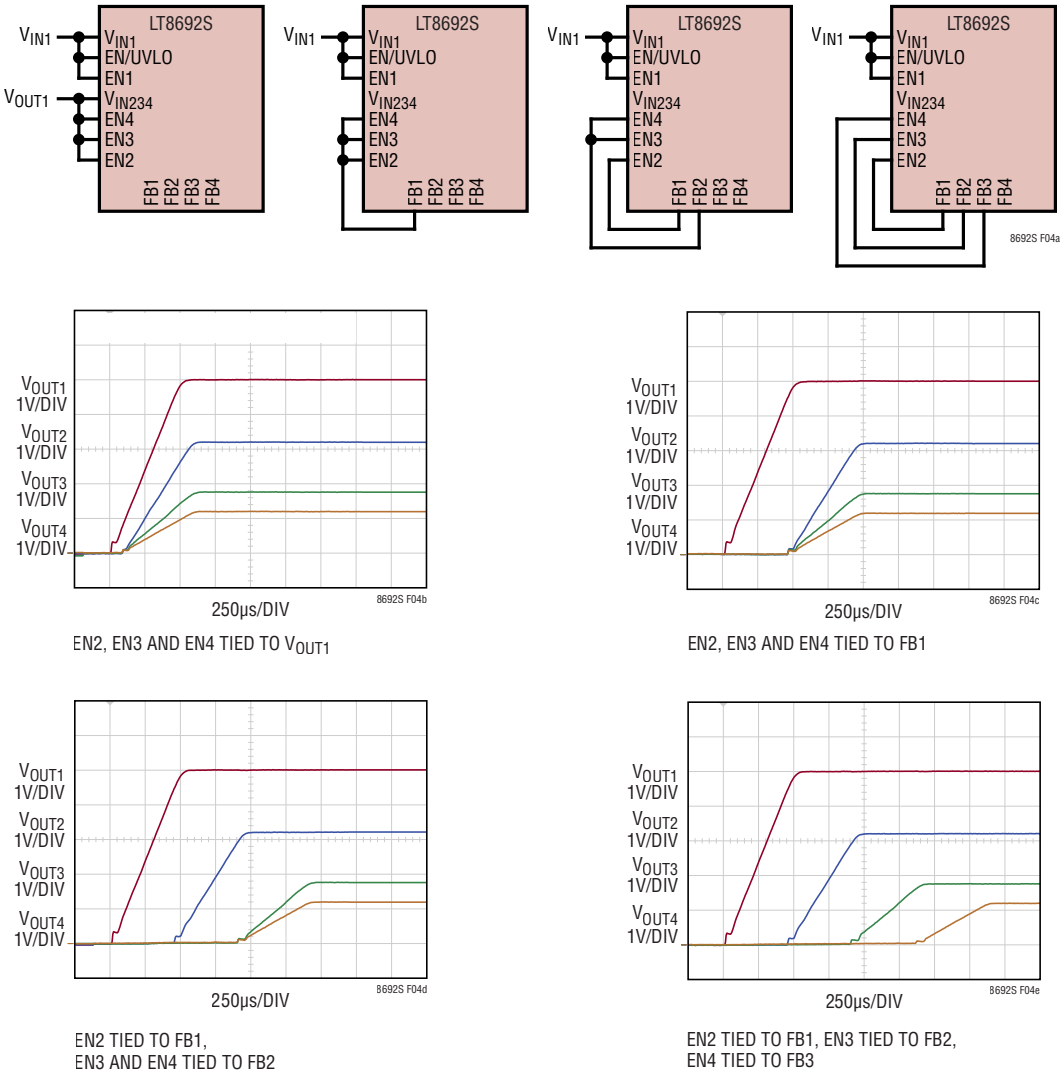

Figure 4. Sequencing and Start-Up Configurations

APPLICATIONS INFORMATION

The LT8692S may be synchronized over a 1.6MHz to 2.5MHz range.

A synchronizing signal that incorporates spread spectrum may reduce EMI.

Forced Continuous Mode

Forced continuous mode (FCM) is activated by either floating the SYNC pin, tying the SYNC pin to V_{CC}, applying a DC voltage above 2.8V to the SYNC pin or applying an external clock to the SYNC pin.

While in FCM, discontinuous mode operation is disabled and the inductor current is allowed to go negative so that the regulator can switch at the programmed frequency all the way down to zero output current. This has the advantage of maintaining the programmed switching frequency across the entire load range so that the switch harmonics and EMI are consistent and predictable. The disadvantage of FCM is that the light load efficiency will be low compared to Burst Mode operation.

The negative inductor current of channel 1 is limited to a maximum of about –2.5A, so the LT8692S can only sink a maximum of about –1.3A. This prevents boosting an excessive amount of current back from the output to the input. FCM is disabled if the input voltage is greater than 37V and 7.5V for channel 1 and channel 2 to channel 4 respectively to prevent overvoltaging the LT8692S if the input capacitor is charged when sinking current from the output. Additional safety features include disabling FCM during soft-start to prevent discharging the output when starting up into a pre-biased output, and a bottom MOSFET current limit to prevent over charging the output if the minimum on time is violated.

Spread Spectrum Modulation

Spread spectrum modulation (SSM) is activated by applying a DC voltage above 2.8V to the SYNC pin. SSM reduces the EMI/EMC emissions by modulating the switching frequency between the internal oscillator frequency to approximately 20% higher than that value. The switching frequency is modulated linearly up and then linearly down at a 6kHz rate. This is an analog function, so each switching period will be different than the previous one. For example, when the LT8692S is programmed to 2MHz and the SSM feature is enabled, the switching frequency will vary from 2MHz to 2.4MHz at a 6kHz rate. When in SSM, the part will also operate in forced continuous mode.

Temperature Monitor Function

As a safeguard, the LT8692S has an additional thermal shutdown set at a typical value of 165°C. If the thermal shutdown is exceeded, all channels of the LT8692S will be shut down until the thermal overload event expires.

Shorted and Reversed Input Protection

The LT8692S will tolerate a shorted output. The bottom switch current is monitored such that if inductor current is beyond safe levels switching of the top switch will be delayed until such time as the inductor current falls to safe levels. A shorted output fault condition at one of the low voltage channels does not affect operation of other channels.

There is another situation to consider in systems where the output will be held high when the input to the LT8692S is absent. This may occur in battery charging applications or in battery-backup systems where a battery or some other supply is OR-ed with channel 1's output. If the V_{IN1} pin is allowed to float and EN/UVLO pin is held high (either by a logic signal or because it is tied to V_{IN1}), then the LT8692S's internal circuitry will pull its quiescent current through its SW1 pin. This is acceptable if the system can tolerate current draw in this state. If the EN/UVLO pin is grounded the V_{IN1} pin current will drop to near 2.3µA. However, if the V_{IN1} pin is grounded while the channel 1 output is held high, parasitic body diodes inside the LT8692S can pull current from the output through the SW1 pin and the V_{IN1} pin, damaging the IC.

V_{IN234} is also connected to the shared internal supply and will pull its quiescent current if left floating and its voltage pulled higher that 3V. If the V_{IN234} pin is grounded while either of channel 2 to channel 4 output is held high,

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parasitic body diodes inside the LT8692S can pull current from the output through the SW2 to SW4 pins and the V_{IN234} pin, damaging the IC.

Figure 5 shows a connection of the V_{IN1} and and EN/UVLO pin that will allow the LT8692S to run only when the input voltage is present and that protects against a shorted or reversed input.

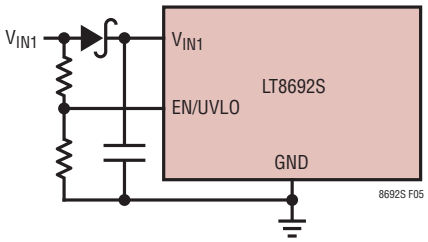


Figure 5. Reverse V_{IN1} Protection

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 6 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT8692S's V_{IN} pins, GND pins, and the input capacitors. The loop formed by the input capacitor should be as small as possible by placing the capacitor adjacent to the V_{IN} and GND pins. When using a physically large input capacitor the resulting loop may become too large in which case using a small case/value capacitor placed close to the V_{IN} and GND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local,

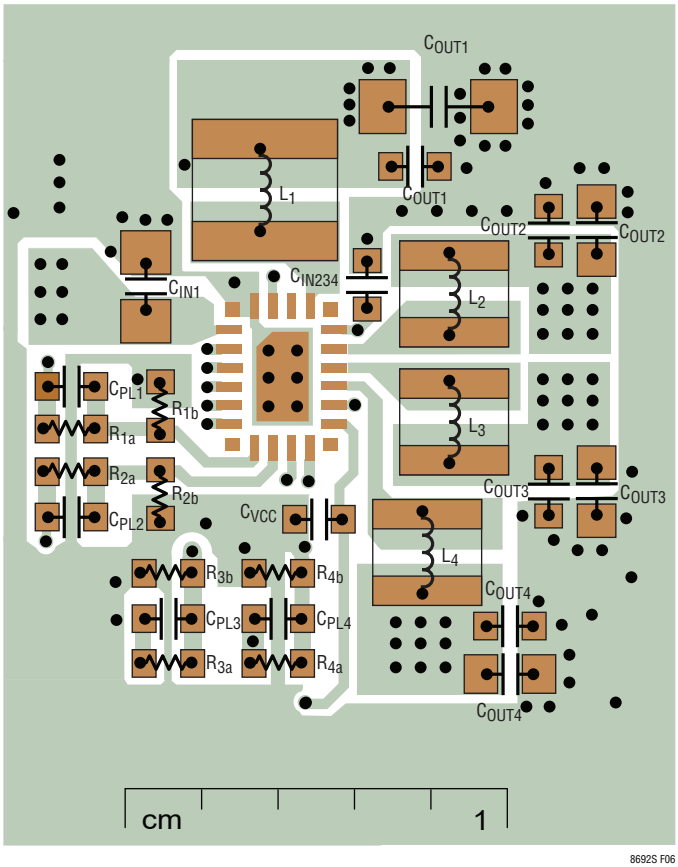


Figure 6. Recommended Layout

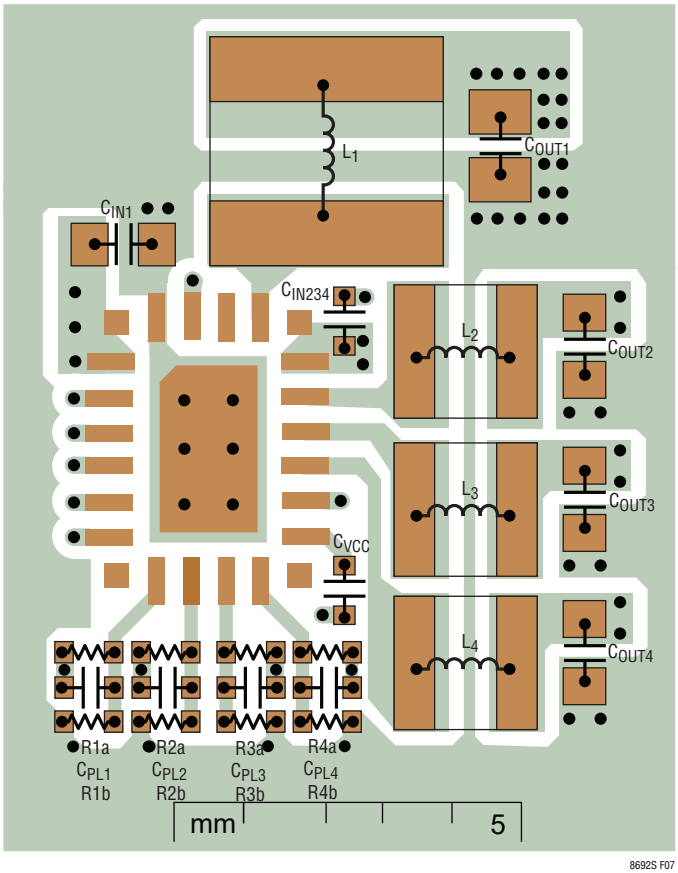


Figure 7. Smallest Layout

APPLICATIONS INFORMATION

unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BST nodes should be as small as possible. Finally, keep the FB nodes small so that the ground traces will shield them from the SW and BST nodes. The exposed pad acts as a heat sink and is connected electrically to ground. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT8692S to additional ground planes within the circuit board and on the bottom side. See Figure 6 for an example PCB layout.

If smallest solution is the priority, then smallest footprint capacitors and inductors that satisfy voltage and current requirements of the circuit should be selected (Figure 7).

High Temperature Considerations

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8692S. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8692S. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8692S can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8692S power dissipation by the thermal resistance from junction to ambient.

The internal thermal shutdown protection of LT8692S will stop switching and indicate a fault condition if junction temperature exceeds 165°C. The fault condition will clear and switching resume when the temperature drops back below 160°C.

Temperature rise of the LT8692S is worst when operating at high load, high V_{IN}, and high switching frequency. If the case temperature is too high for a given application, then either V_{IN}, switching frequency, or load current can be decreased to reduce the temperature to an acceptable level. Figure 8 shows examples case temperature rise vs load current load.

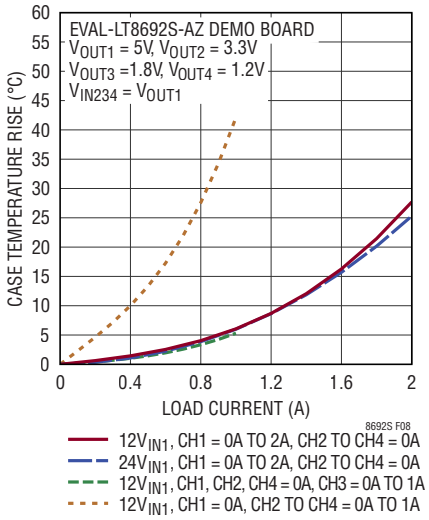
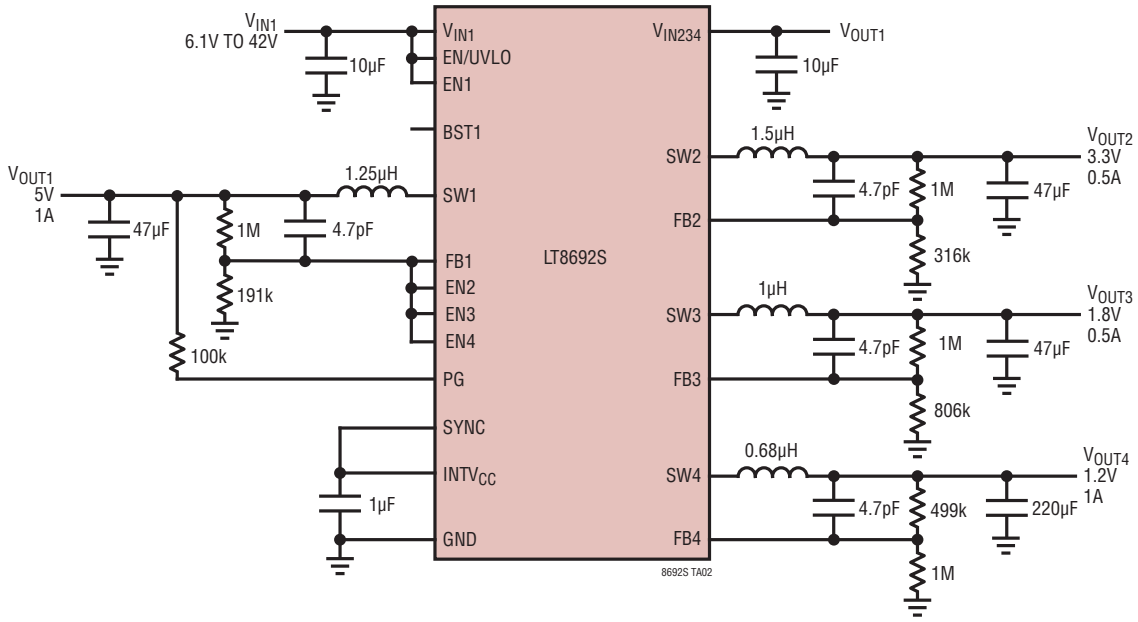


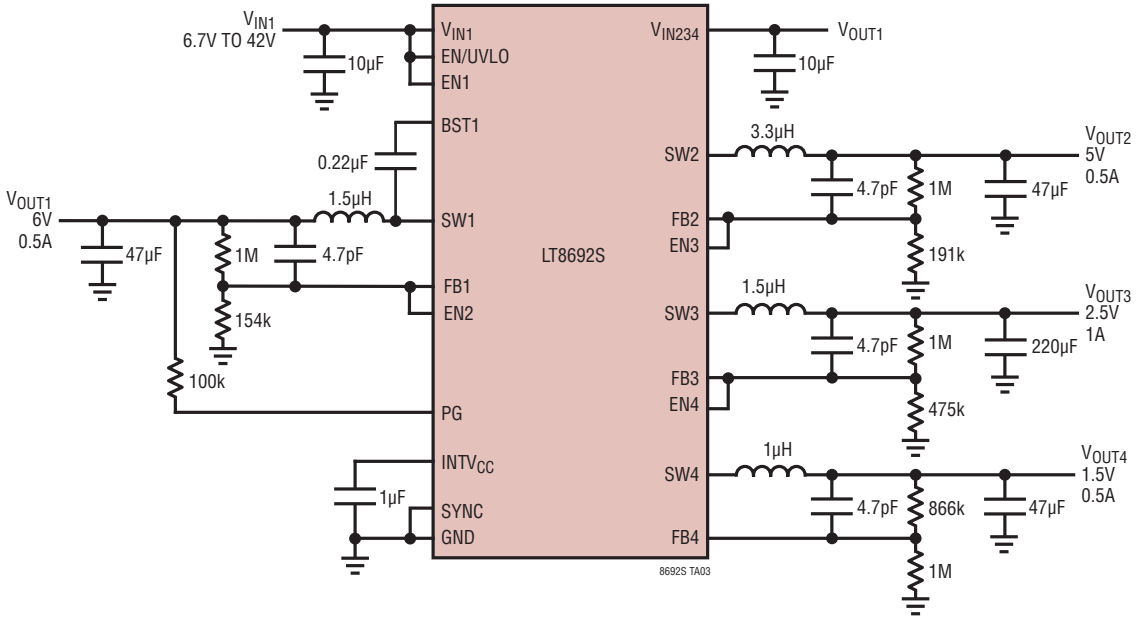
Figure 8. Case Temperature Rise

TYPICAL APPLICATIONS

5V, 3.3V, 1.8V, 1.2V, 2MHz Step-Down Converter with Spread Spectrum Frequency Modulation and Single Voltage Source

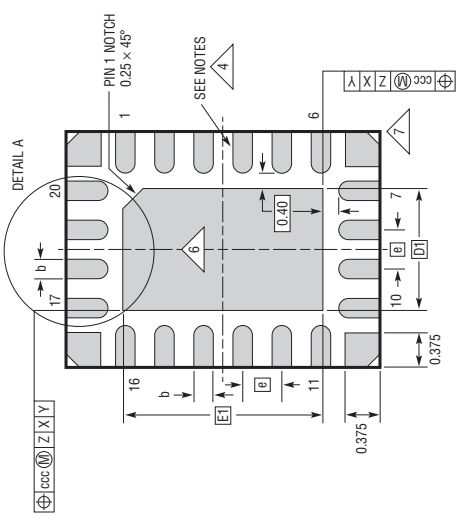


6V, 5V, 2.5V, 1.5V, 2MHz Step-Down Converter with Burst Mode and Turn-On Sequence

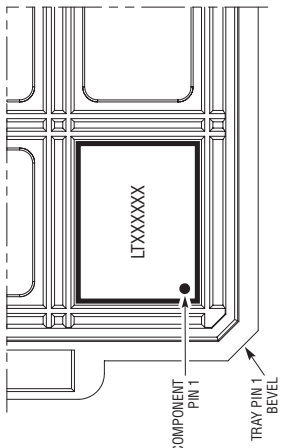


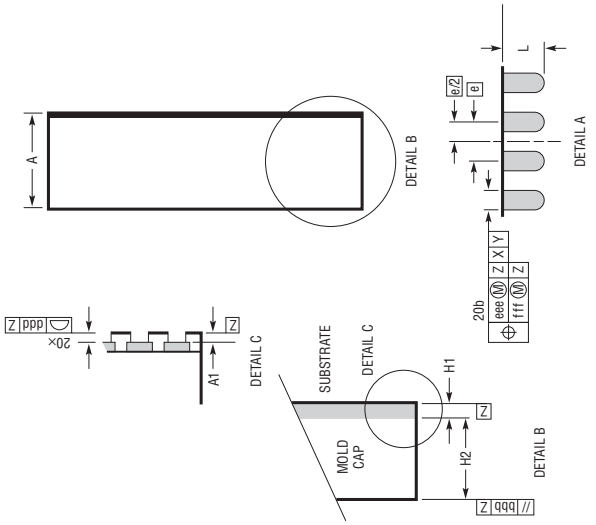
PACKAGE DESCRIPTION

LQFN Package
20-Lead (3mm × 4mm × 0.94mm)
(Reference LTC DWG # 05-08-1716 Rev Ø)

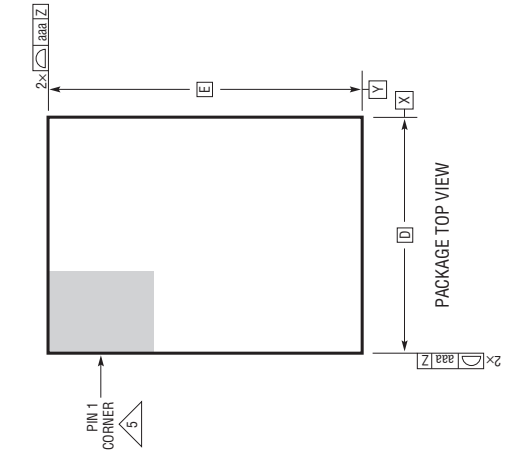


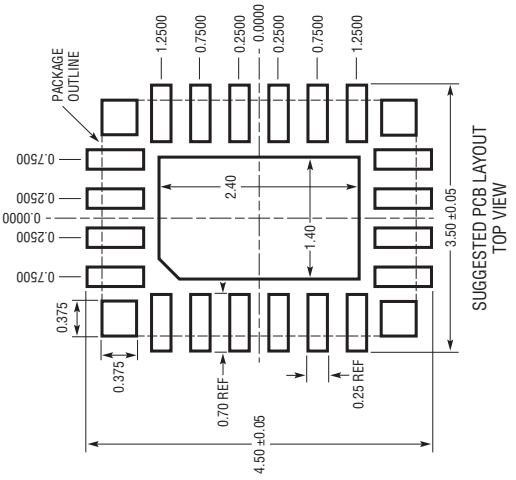
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.95	1.05	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		3.00		
E		4.00		
D1		1.40		
E1		2.40		
e		0.50		
H1		0.25		
H2		0.70		
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	





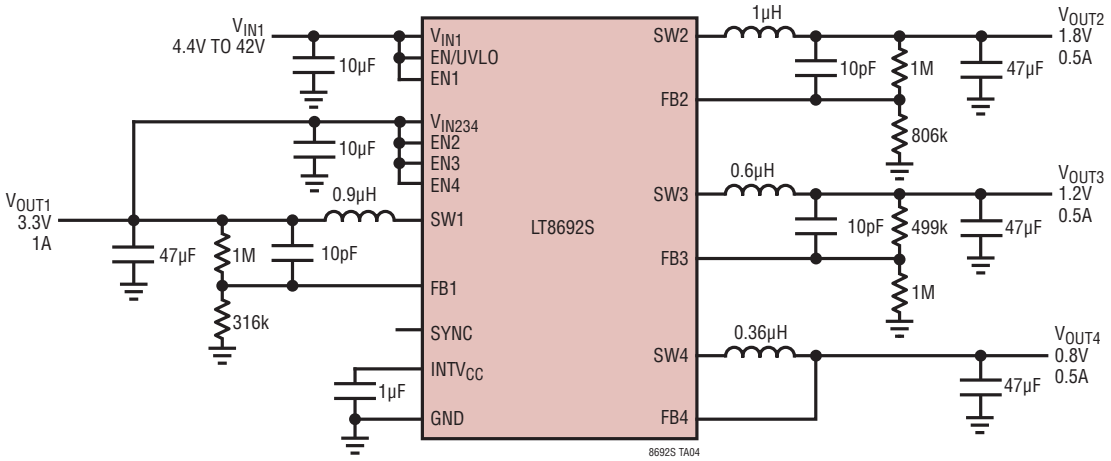
Rev. A

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/22	Updated Figures 6 and 7	22
		Updated Package Description	26

TYPICAL APPLICATION

3.3V/1A, 1.8V/0.5A, 1.2V/0.5A, 0.8V/0.5A 2MHz Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3370/LTC3371	2.25V to 5.5V_{IN}, 4-Channel 8A Configurable 1A Buck DC/DCs	Four Synchronous Buck Regulators with 8× 1A Power Stages; Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Max) with a Single Inductor; Eight Configurations Possible, Precision PGOOD Indication; 800mV FB Regulation; LTC3371 Has a Watchdog Timer; Buck 1 Accuracy ±1%, others ±2.5%
LTC3374/LTC3375	2.25V to 5.5V_{IN}, 8-Channel Parallelable 1A Buck DC/DCs	Eight 1A Synchronous Buck Regulators; Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Max) with a Single Inductor; 15 Configurations Possible; 800mV FB Regulation; All Bucks ±2.5% Accuracy; LTC3375 Has I^2C Programming with a Watchdog Timer and Pushbutton
LTC3374A	2.25V to 5.5V_{IN}, High Accuracy 8-Channel Parallelable 1A Buck DC/DC	Eight 1A Synchronous Buck Regulators; Can Connect Up to Four Power Stages in Parallel to Make a High Current Output (4A Max) with a Single Inductor; 15 Configurations Possible; 800mV FB Regulation; Buck 1 Accuracy ±1%, Others ±2%; Overvoltage Monitor Included in PGOOD
LTC3376	3V to 20V_{IN}, 4-Channel Buck DC/DC with 8 Configurable 1.5A Power Stages	8× 1.5A Buck Power Stages Configurable as 1 to 4 Output Channels; 15 Unique Pin Selectable Output Configurations (1.5A to 12A per Channel); 1% V_{OUT} Accuracy on All Channels
LTC3644/LTC3644-2	Quad 2.7V to 17V_{IN}, 1.25A Parallelable Synchronous Buck DC/DC with Ultralow Quiescent Current	Can Be Configured for Quad 1.25A Outputs, Triple 2.5A/1.25A/1.25A Outputs, Dual 2.5A Outputs, or Dual 3.75A/1.25A Output; 1MHz (LTC3644) or 2.3MHz (LTC3644-2) Fixed Frequency Operation; Integrated 300mΩ P-Channel/80mΩ N-Channel MOSFETs Provide Up to 93% Efficiency
LT8602	Quad 3V to 42V, 1× 2.5A + 3× 1.5A Synchronous Buck Converter	1× 2.5A + 3× 1.5A Buck power Stages, 25µA Quiescent Current, 1000mV (CH1 and CH2) and 800mV (CH3 and CH4) FB Regulation, 1.25% V_{OUT} Accuracy on All Channels, Up to 95% Efficiency, 6mm × 6mm 40-Lead QFN
LT8650S	Dual 3V to 42V, 4A Synchronous Silent Switcher 2 Buck Converter with Ultralow Quiescent Current	2× 4A Buck Power Stages, 6.2µA Quiescent Current, 800mV FB Regulation, 1.25% V_{OUT} Accuracy on All Channels, Up to 95% Efficiency, 4mm × 6mm 32-Lead LQFN
LT8653S	Dual 3V to 42V, 2A Synchronous Silent Switcher 2 Buck Converter with Ultralow Quiescent Current	2× 2A Buck Power Stages, 6.2µA Quiescent Current, 800mV FB Regulation, 1.25% V_{OUT} Accuracy on All Channels, Up to 45% Efficiency, 3mm × 4mm 20-Lead LQFN