Product Update

Errata for ZLP12840

UP007303-0307

ZLP12840 MCU with All Date Codes

Table 1 lists the errata for ZiLOG's ZLP12840 MCU with all package date codes except those marked with '2179'. The issues are already fixed for IC with '2179' marking. When reviewing the following errata, it is recommended that you refer the recent version of the product specification, *ZLP12840 OTP MCU with Learning Amplification Product Specification (PS0244)*, available for download at www.zilog.com.

Table 1. Errata to the ZLP12840 Device

No.	Issue	Detailed Description
1	Changing the register pointer causes corruption in locations FC, FD, FE, and FF of banks 1, 2, and 3.	When the bank location within the RP register of the device, bits 3 through 0 of the device's RP register, is rewritten with a different bank value, certain RAM locations (01FC through 01FF, 02FC through 02FF, and 03FC through 03FF) can be corrupted. The data residing at address locations FC through FF of the new bank value represented by the RP register are rewritten with the values at FC through FF of the previous RP register bank setting. **Workarounds** There are two workarounds: • Do not use locations FC–FF of banks 1, 2, or 3. • Do not switch the RP register, and use the LDX and LDXI instructions to access other banks that are not part of the RP register.
2	Location 04 in bank 0 of the RAM is not accessible using the LDX or LDXI instructions.	The LDX or LDXI instructions will not access location 04 of bank 0 of the RAM. **Workaround** Do not use the LDX instructions to access location 04 of Bank 0.
3	When using the UART's baud rate generator as a general-purpose timer, the time-out period of the timer is too short to be useful to some applications.	If the baud rate generator is used as a general-purpose timer, the time-out period of the current silicon is: $\text{Time-Out Period}\ (\mu s) = \frac{\text{UART Baud Rate Divisor Value (BCNST)}}{\text{System Clock Frequency (MHz)}}$ The next silicon will have the following time-out period: $\text{Time-Out Period}\ (\mu s) = \frac{(16 \times \text{UART Baud Rate Divisor Value (BCNST)})}{\text{System Clock Frequency (MHz)}}$ **Workaround** No workaround is available.

Warning: DO NOT USE IN LIFE SUPPORT

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As used herein

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