74ABT823

9-bit D-type flip-flop with reset and enable; 3-state

Rev. 4 — 7 November 2011 Product data sheet

1. General description

The 74ABT823 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT823 is a 9-bit wide buffered register with clock enable input ($\overline{CE}$) and master reset input ($\overline{MR}$) which are ideal for parity bus interfacing in systems using many microprocessors.

The 74ABT823 is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data and address paths of buses carrying parity.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output Q of the flip-flop.

2. Features and benefits

- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64 mA and −32 mA
- Power-on 3-state
- Power-on reset
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT823D	−40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74ABT823DB	−40 °C to +85 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74ABT823PW	−40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

4. Functional diagram

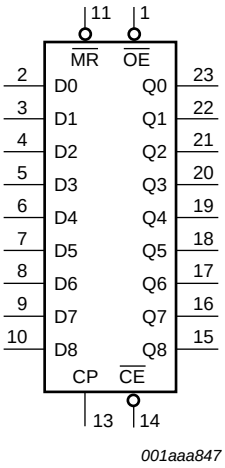

Fig 1. Logic symbol

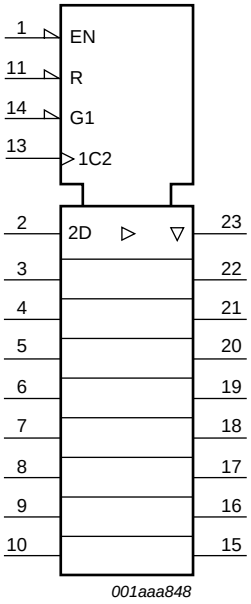

Fig 2. IEC logic symbol

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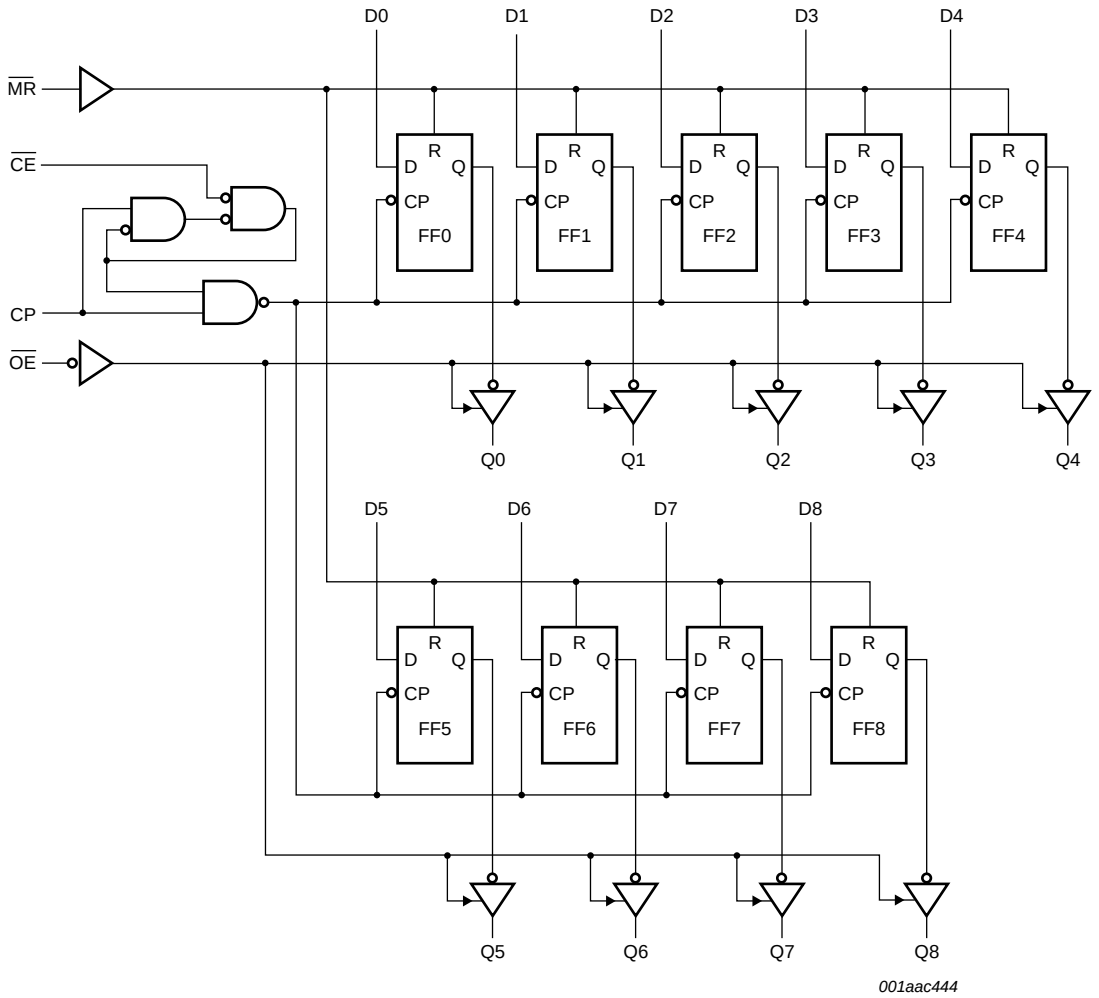

Fig 3. Logic diagram

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5. Pinning information

5.1 Pinning

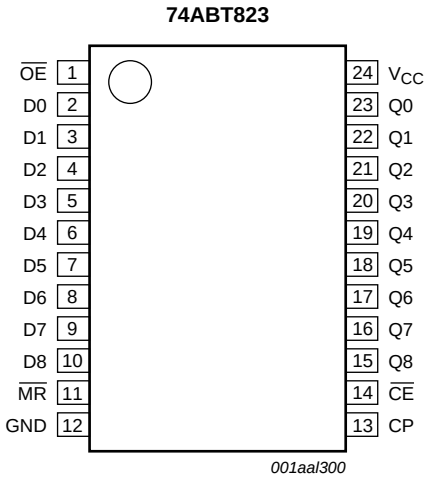

Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	output enable input (active LOW)
D0, D1, D2, D3, D4, D5, D6, D7, D8	2, 3, 4, 5, 6, 7, 8, 9, 10	data input
$\overline{MR}$	11	master reset input (active LOW)
GND	12	ground (0 V)
CP	13	clock pulse input (active rising edge)
$\overline{CE}$	14	clock enable input (active LOW)
Q8, Q7, Q6, Q5, Q4, Q3, Q3, Q2, Q1, Q0	15, 16, 17, 18, 19, 20, 21, 22, 23	data output
V_{CC}	24	positive supply voltage

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6. Functional description

6.1 Function table

Table 3. Function table[1]

Input					Output	Operating mode
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	Dn	Qn	
L	L	X	X	X	L	clear
L	H	L	↑	h	H	load and read data
L	H	L	↑	l	L	
L	H	H	NC	X	NC	hold
H	X	X	X	X	Z	high-impedance

[1] H = HIGH voltage level;
L = LOW voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
↑ = LOW-to-HIGH clock transition;
NC = no change;
X = don't care;
Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7.0	V
V_I	input voltage		[1]	−1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	−0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V		−18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		−50	-	mA
I_O	output current	output in LOW-state		-	128	mA
T_j	junction temperature		[2]	-	150	°C
T_{stg}	storage temperature			−65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

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8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level Input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		–32	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		–1.2	–0.9	-	–1.2	-	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IL}$ or V_{IH}							
		V_{CC} = 4.5 V; I_{OH} = –3 mA		2.5	2.9	-	2.5	-	V
		V_{CC} = 5.0 V; I_{OH} = –3 mA		3.0	3.4	-	3.0	-	V
		V_{CC} = 4.5 V; I_{OH} = –32 mA		2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; $V_I = V_{IL}$ or V_{IH}		-	0.42	0.55	-	0.55	V
$V_{OL(pu)}$	power-up LOW-level output voltage	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}	[1]	-	0.13	0.55	-	0.55	V
I_I	input leakage current	V_{CC} = 5.5 V; $V_I = V_{CC}$ or GND		-	±0.01	±1.0	-	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or $V_O \leq$ 4.5 V		-	±5.0	±100	-	±100	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} = 2.0 V; V_O = 0.5 V; V_I = GND or V_{CC}; $\overline{OE}$ HIGH	[2]	-	±5.0	±50	-	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; $V_I = V_{IL}$ or V_{IH}							
		V_O = 2.7 V		-	5.0	50	-	50	µA
		V_O = 0.5 V		-	–5.0	–50	-	–50	µA
I_{LO}	output leakage current	HIGH-state; V_O = 5.5 V; V_{CC} = 5.5 V; V_I = GND or V_{CC}		-	5.0	50	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[3]	–180	–50	–50	–180	–50	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}							
		outputs HIGH-state		-	0.5	250	-	250	µA
		outputs LOW-state		-	27	34	-	34	mA
		outputs disabled		-	0.5	250	-	250	µA

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Table 6. Static characteristics *...continued*

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND	[4]	-	0.5	1.5	-	1.5	mA
C_I	input capacitance	V_I = 0 V or V_{CC}		-	4	-	-	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or V_{CC}		-	7	-	-	-	pF

[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 % a transition time of up to 100 μs is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Figure 9.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			–40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
f_{max}	maximum frequency	see Figure 5	125	200	-	125	-	MHz
t_{PLH}	LOW to HIGH propagation delay	CP to Qn, see Figure 5	2.1	4.3	5.9	2.1	6.8	ns
t_{PHL}	HIGH to LOW propagation delay	CP to Qn, see Figure 5	2.2	4.4	6.1	2.2	6.7	ns
		$\overline{MR}$ to Qn, see Figure 6	2.0	4.1	6.3	2.0	7.1	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$ to Qn; see Figure 8	1.0	3.0	4.5	1.0	5.3	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to Qn; see Figure 8	2.2	4.1	5.6	2.2	6.3	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to Qn; see Figure 8	2.7	4.8	6.2	2.7	6.9	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to Qn; see Figure 8	2.5	5.0	6.4	2.5	6.9	ns
$t_{su(H)}$	set-up time HIGH	Dn to CP; see Figure 7	2.1	0.5	-	2.1	-	ns
		$\overline{CE}$ to CP; see Figure 7	+2.0	–0.5	-	+2.0	-	ns
$t_{su(L)}$	set-up time LOW	Dn to CP; see Figure 7	2.1	0.2	-	2.1	-	ns
		$\overline{CE}$ to CP; see Figure 7	3.3	1.5	-	3.3	-	ns
$t_{h(H)}$	hold time HIGH	CP to Dn; see Figure 7	1.3	0.0	-	1.3	-	ns
		CP to $\overline{CE}$; see Figure 7	+1.0	–1.4	-	+1.0	-	ns
$t_{h(L)}$	hold time LOW	CP to Dn; see Figure 7	+1.3	–0.3	-	+1.3	-	ns
		CP to $\overline{CE}$; see Figure 7	2.0	0.7	-	2.0	-	ns
t_{WH}	pulse width HIGH	CP; see Figure 5	2.9	1.9	-	2.9	-	ns

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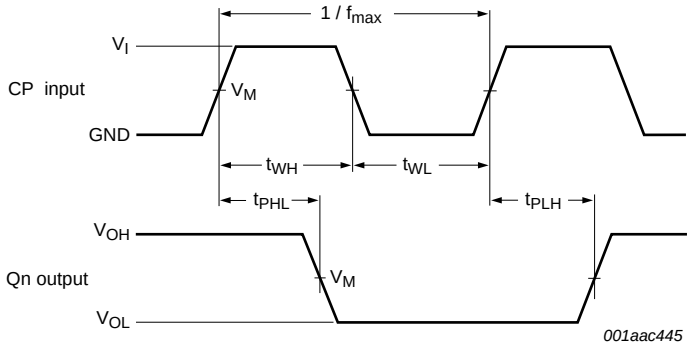
Table 7. Dynamic characteristics *...continued*

GND = 0 V; for test circuit, see Figure 9.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			–40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t_{WL}	pulse width LOW	CP; see Figure 5	3.8	2.8	-	3.8	-	ns
		$\overline{MR}$; see Figure 6	5.5	4.0	-	5.5	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Figure 6	2.5	0.6	-	2.5	-	ns

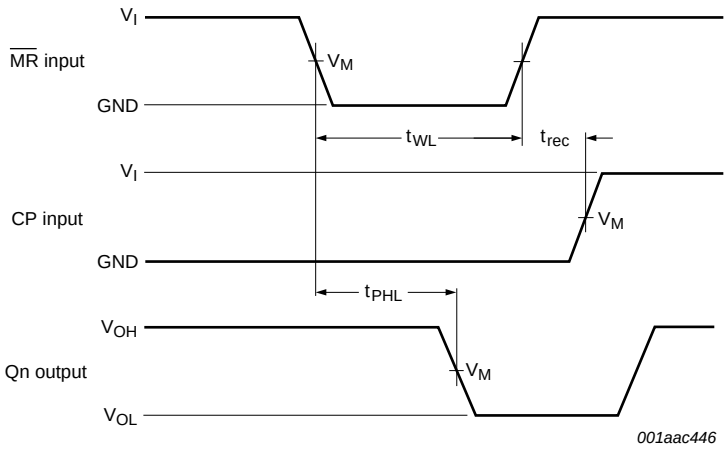
11. Waveforms



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Propagation delay clock input (CP) to output (Qn), clock pulse (CP) width and maximum clock (CP) frequency



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Master reset ($\overline{MR}$) pulse width, propagation delay master reset ($\overline{MR}$) to output (Qn) and recovery time master reset (MR) to clock (CP)

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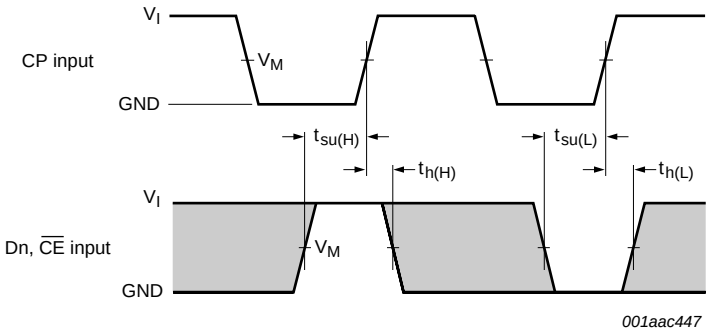
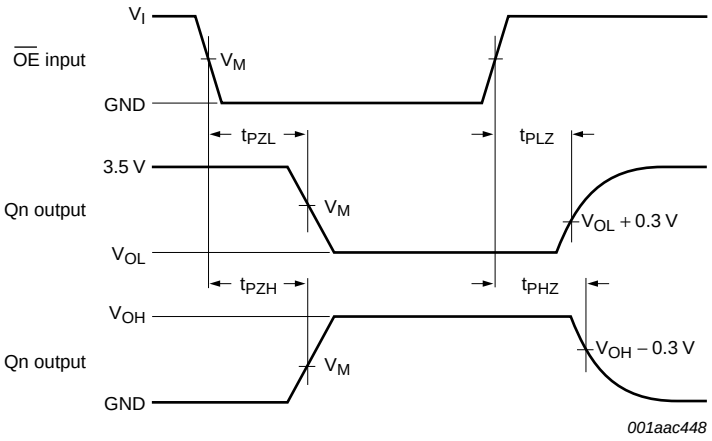


V_M = 1.5 V

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 7. Set-up and hold times data output (Dn) to clock (CP) and clock enable input ($\overline{CE}$) to clock (CP)



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load

Fig 8. 3-state output (Qn) enable and disable times

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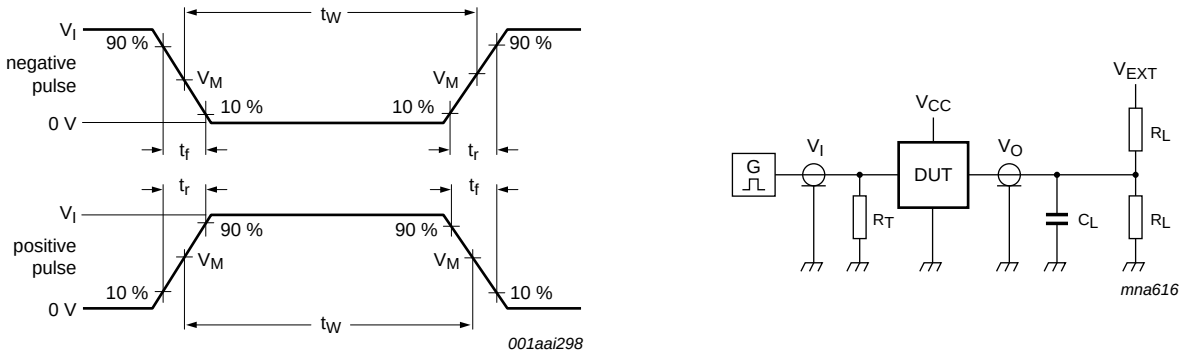

a. Input pulse definition

b. Test circuit

Test data is given in Table 8.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 9. Load circuitry for switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

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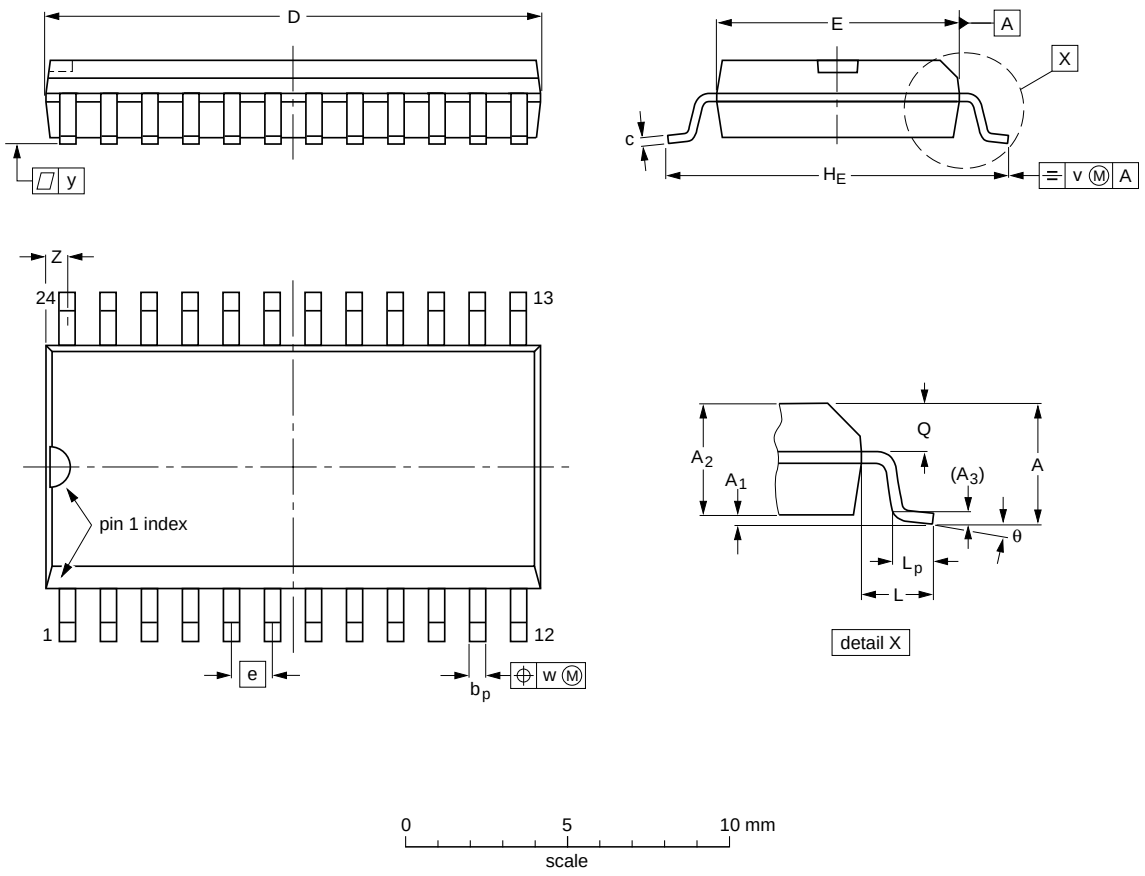
12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT137-1 (SO24)

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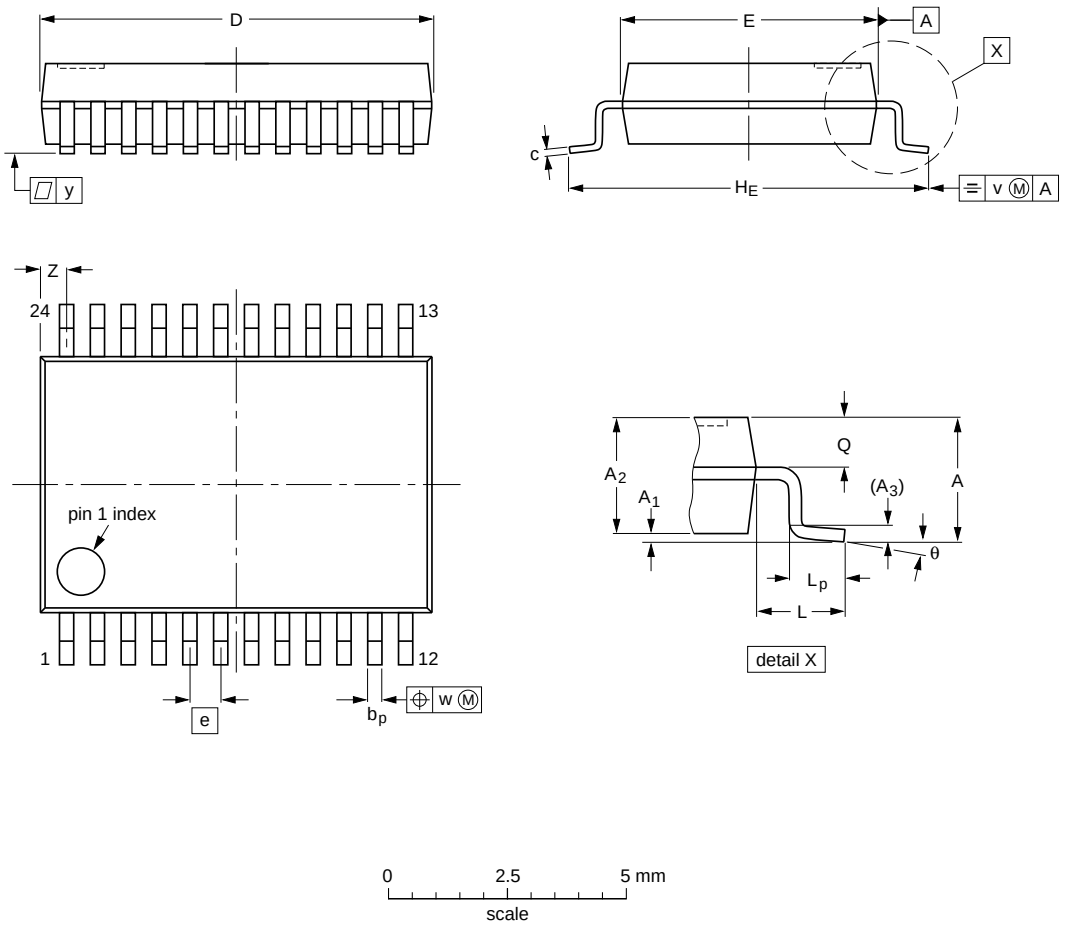
SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT340-1 (SSOP24)

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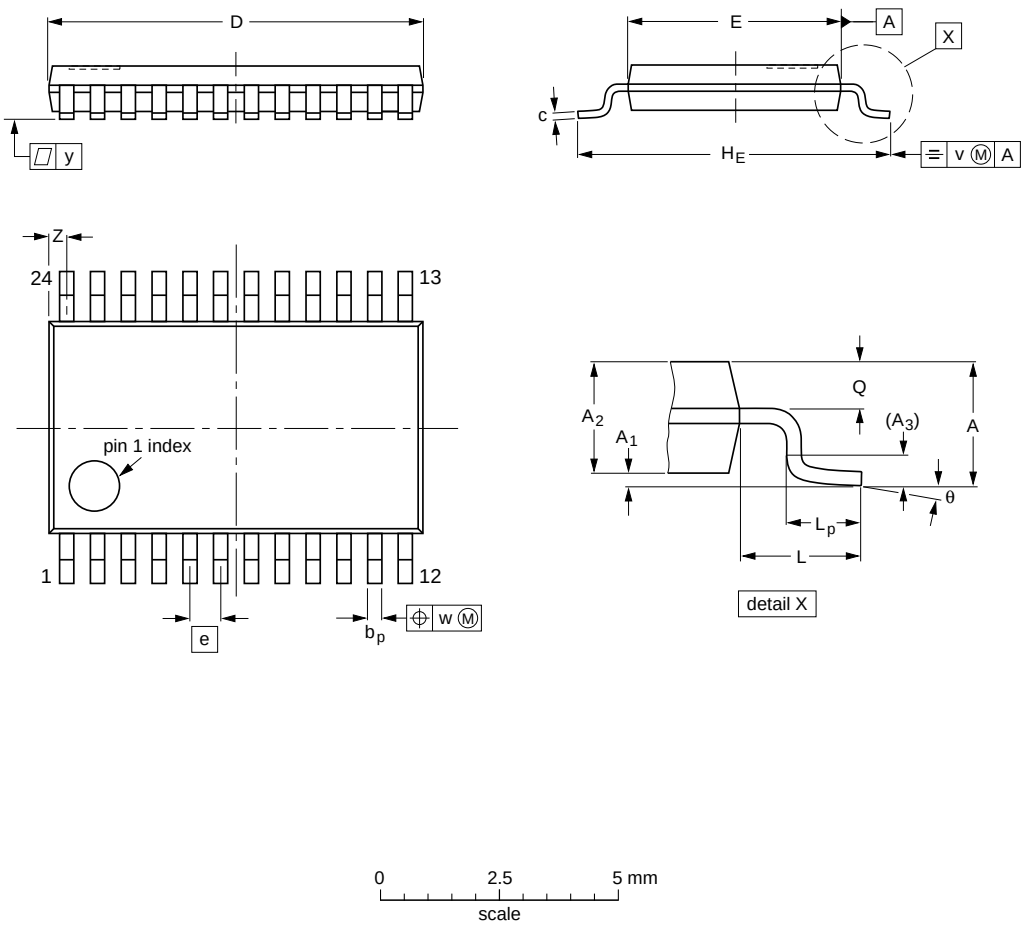
TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT355-1 (TSSOP24)

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13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT823 v.4	20111107	Product data sheet	-	74ABT823 v.3
Modifications:	• Legal pages updated.			
74ABT823 v.3	20100323	Product data sheet	-	74ABT823 v.2
74ABT823 v.2	20050207	Product specification	-	74ABT823 v.1
74ABT823 v.1	19960314	Product specification	-	

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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