



Maxim > Design Support > Technical Documents > Application Notes > A/D and D/A Conversion/Sampling Circuits > APP 5477
Maxim > Design Support > Technical Documents > Application Notes > Amplifiers > APP 5477
Maxim > Design Support > Technical Documents > Application Notes > Audio Circuits > APP 5477

Keywords: jitter, time interval error, TIE, sampling jitter, jitter spectrum, audio, digital input, I2S, PCM, PDM, TDM, cycle-skip, wideband, broadband, sigma-delta, delta-sigma, single-bit, BCLK, LRCLK, d-to-a, d/a, DAC, single-bit, noise shaping, oversampled

APPLICATION NOTE 5477

Analyzing Audio DAC Jitter Sensitivity

By: Matt Felder, Senior Member of Technical Staff

Patrick Gallagher

Brian Donoghue

Oct 11, 2012

Abstract: This application note describes how sampling clock jitter (time interval error or "TIE jitter") affects the performance of delta-sigma digital-to-analog converters (DACs). New insights explain the importance of separately specifying low-frequency (< 2x passband frequency) and high-frequency or wideband (> 2x passband frequency) jitter tolerance in these devices. The article also provides an application example of a simple highly jittered cycle-skipped sampling clock and describes a method for generating a proper broadband jittered clock. The document then goes on to compare Maxim's audio DAC jitter tolerance to competitor audio DACs. Maxim's exceptionally high jitter tolerance allows very simple and low-cost sample clock implementations.

A similar version of this article appears on [EDN](#), October 4, 2012.

Introduction

High-performance audio digital-to-analog converters (DACs) traditionally require a very clean sample master clock (MCLK) to avoid degradations in the audio quality. The clock sources are often derived directly from crystal oscillators, which typically produce less than 100ps jitter. In some systems the audio oversampling frequency (usually a multiple of 3.072MHz or 2.8224MHz) is not a convenient fraction of the crystal oscillator reference frequency. Although these systems can implement a fractional-N divider PLL to create the desired audio MCLK frequency, such PLL-based frequency references usually have multiple reference frequency spurs and substantial low-frequency jitter. Moreover, these PLL-based frequency references often cannot get the jitter low enough for the application without exceeding desired pin count, area, or power consumption targets. There is, however, a solution to the dilemma. An audio DAC that can tolerate high jitter allows a simpler sampling clock reference to be used in such systems.



Attend this brief webcast by Maxim on TechOnline

Understanding Jitter Tolerance

High jitter tolerance is important because it:

1. Maximizes audio signal quality in the presence of jitter
2. Reduces system complexity or bill of materials (BOM) through the use of simpler jittery clock sources
3. Eliminates the need for a high-frequency MCLK, thus reducing power and electromagnetic interference (EMI)

There currently is no standard methodology for evaluating jitter tolerance. The Audio Precision 2700 (AP2700) audio analyzer can create a jittered clock, but it creates mostly low-frequency jitter (mostly below the Nyquist audio sample rate) as shown in **Figure 1**.

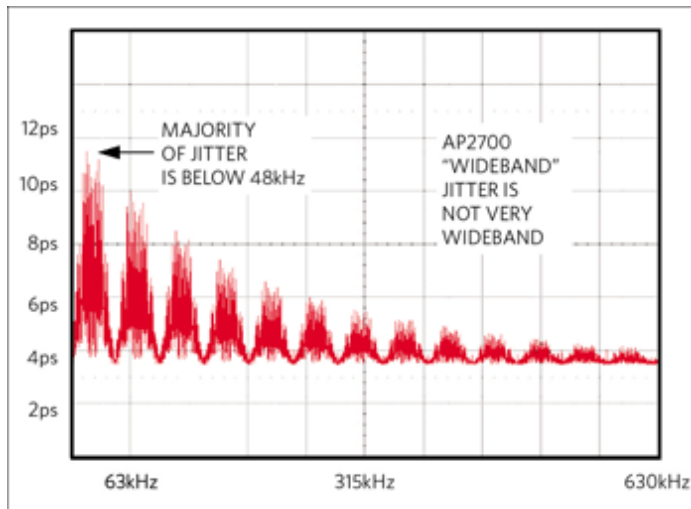


Figure 1. Spectrum of 5ns "wideband" jitter generated from an AP2700.

Jitter Tolerance Test Setup

Two different jittered clock sources were used to compare jitter sensitivity for multiple DACs. The first jittered clock was a 12.288MHz cycle-skipped clock from a 25MHz reference. This generated ~11ns of jitter above 40kHz and ~0.37ns of jitter below 40kHz. This clock was created using a National Instruments® PXI-5421 100MHz arbitrary waveform generator (ARB) that was fed the desired clock pattern.

A second jittered clock was a wideband, white jittered clock created with the same ARB. The ARB generated a 6.144MHz sine wave with white noise added, which was then fed through a [MAX999](#) comparator to create a square-wave clock with substantial wideband jitter.

The jitter was measured with a LeCroy WaveRunner® 104MXI-A 1GHz oscilloscope using the time interval error (TIE) jitter measurement. Both the rising and falling edges are jittered in both of the test files.

The wideband jittered clock created for this evaluation has a true wideband (white) jitter spectrum that is suited for evaluating sensitivity to broadband jitter. See **Figures 2, 3, and 4**. This truly white jitter spectrum is unlikely to be found in a real application; however, it is a good test for jitter tolerance because it will uncover sensitivities to jitter in any particular frequency range.

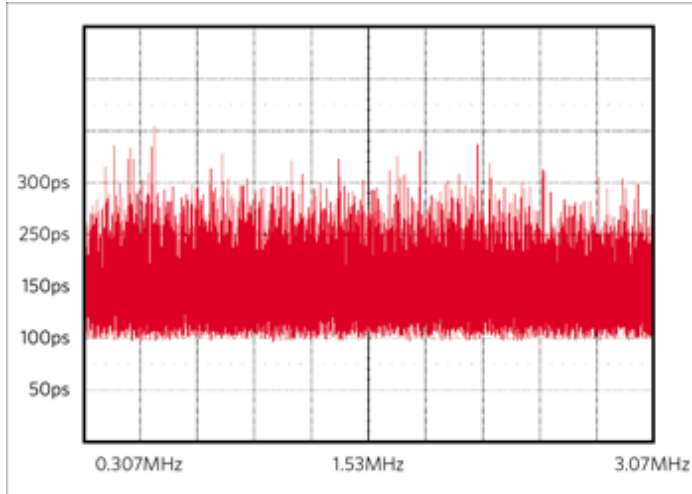


Figure 2. Wideband 5.9ns RMS white jitter spectrum used for this analysis.

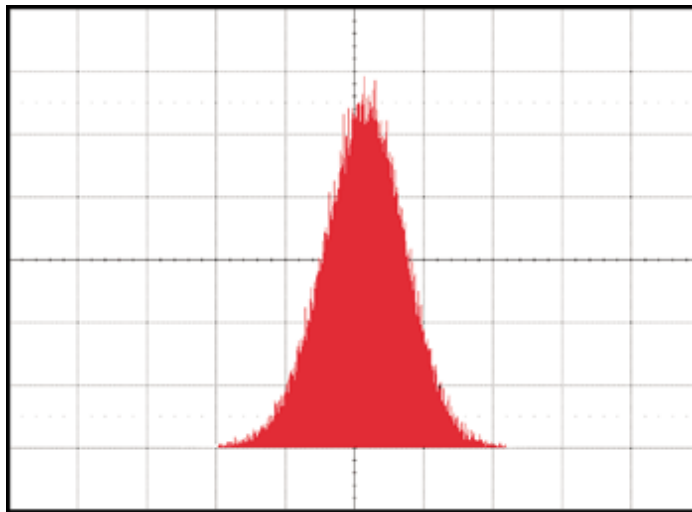


Figure 3. Histogram of 5.9ns wideband jitter.

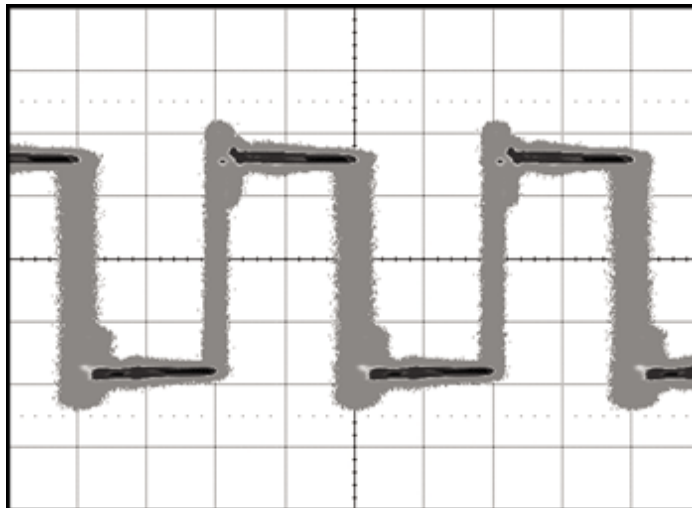


Figure 4. Scope capture of 3.072MHz clock with 5.9ns wideband white jitter.

The cycle-skipped clock used for this study is shown in **Figure 5** and the jitter spectrum of this clock is illustrated in **Figure 6** and **Figure 7**. This cycle-skipped clock test demonstrates that a very easily generated, extremely jittery clock can be tolerated by the DAC, without a PLL. Only a small amount of logic is required to skip clock cycles from any frequency reference to generate any (lower frequency) sample clock. There is no filtering or feedback loop required for this type of clock generation.

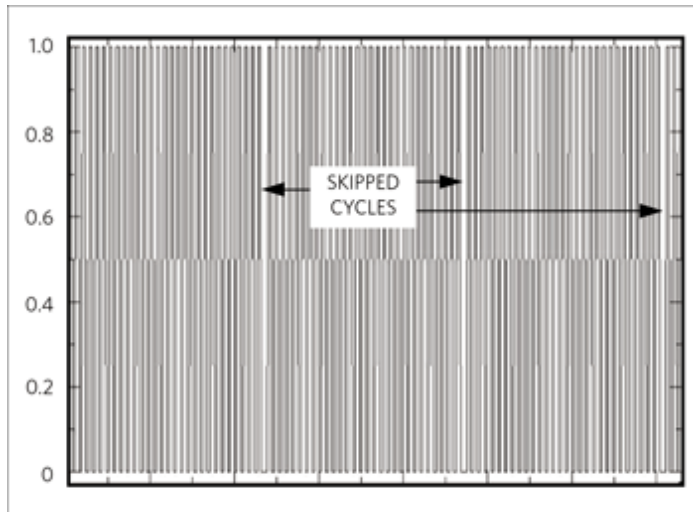


Figure 5. The transient plot of a 12.288MHz MCLK from a cycle-skipped 25MHz clock.

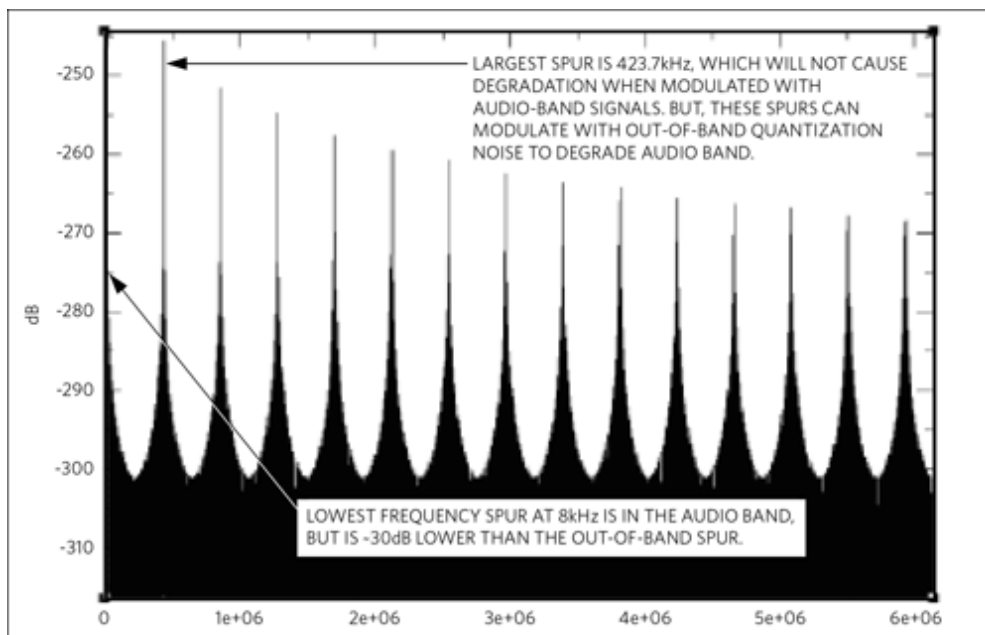


Figure 6. Spectrum of jitter for 12.288MHz MCLK cycle-skipped from 25MHz reference clock.

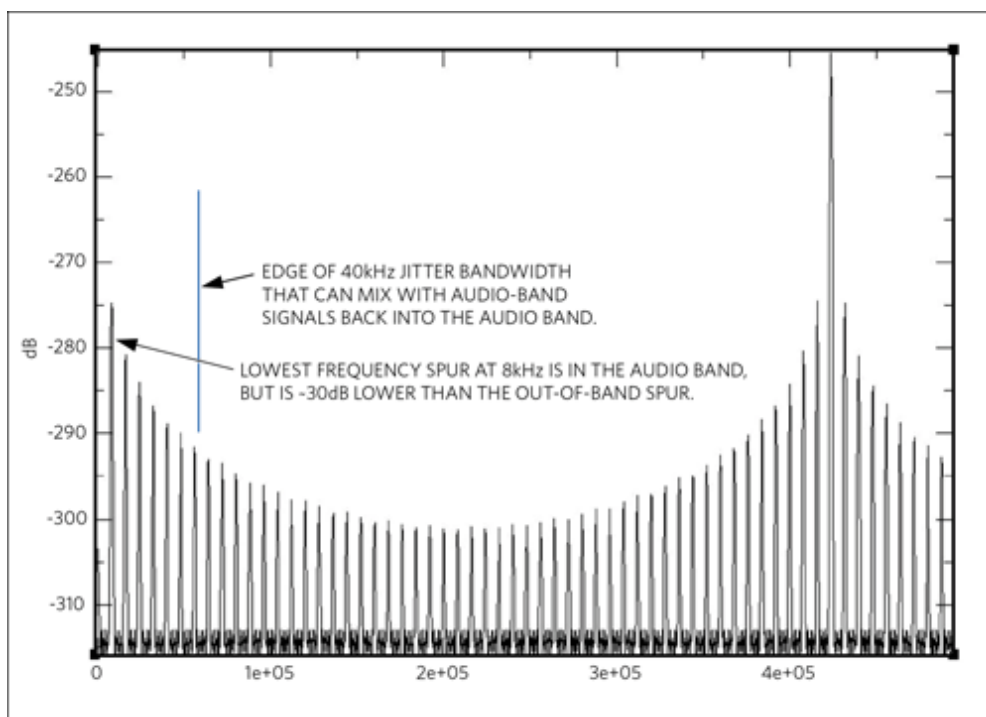


Figure 7. Low-frequency jitter spectrum for a cycle-skipped clock.

Several Maxim parts, including audio codecs ([MAX98089](#) and [MAX98096](#)) and the [MAX98355/MAX98356](#) power amplifiers, benefit from a highly jitter-tolerant DAC. The devices are specified to tolerate up to 0.5ns of jitter in the 0 to 40kHz band and 12ns of jitter above 40kHz. With this amount of jitter, these parts will show the following jitter-induced performance limits (with no circuit noise included):

- -108dB THD+N with a 1kHz full-scale tone
- -96.5dB THD+N with a 6kHz full-scale tone
- -87dB THD+N with a 20kHz full-scale tone
- 105dB dynamic range and signal-to-noise ratio (SNR)

The THD+N performance results are only affected by the low-frequency jitter (< 40kHz). While the dynamic range and SNR are only affected by the high-frequency jitter (> 40kHz).

Figures 8, 9, 10, and **11** show how audio performance measurements with highly jittered clock sources for Maxim's MAX98355 power amplifier compare with a group of competitive DACs. All of these competitor parts except for Competitor 2 claim that they are insensitive to clock jitter, but do not provide a jitter tolerance specification.

Jitter Tolerance Test Results

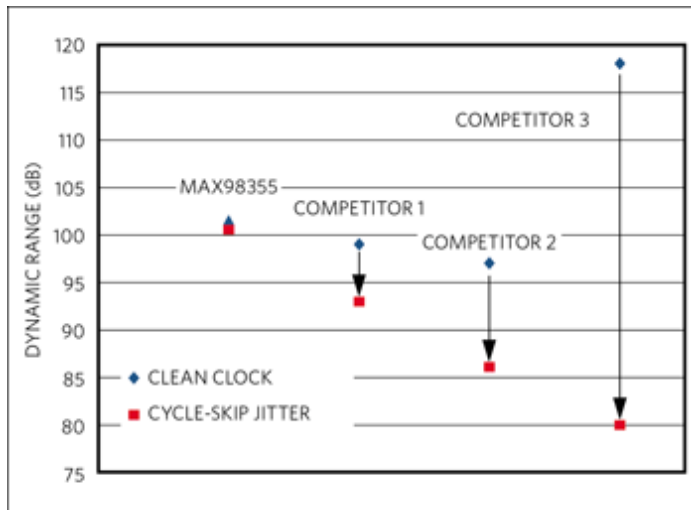


Figure 8. Dynamic range degradation with 11.5ns RMS cycle-skipped clock jitter.

Notice that the MAX98355 dynamic range does not degrade with the cycle-skipped jittered clock. The MAX98355 thus outperforms the "120dB DAC" by more than 20dB with the jittered clock.

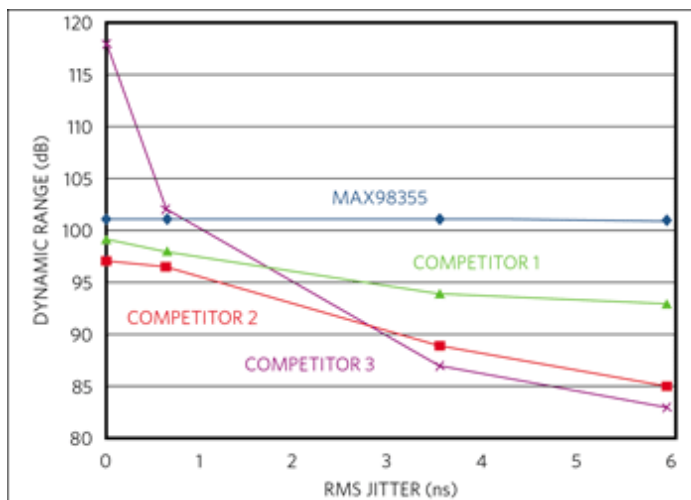


Figure 9. Dynamic range degradation with broadband white jitter.

The 3.5ns and 5.9ns jitter performance for Competitor 3 as well as the 5.9ns jitter for Competitor 2 are extrapolated because the part does not actually function properly with those jitter levels; they start dropping bits and the actual measured dynamic range is lower than shown in this plot.



Figure 10. 1kHz THD+N performance degradation with clock jitter.

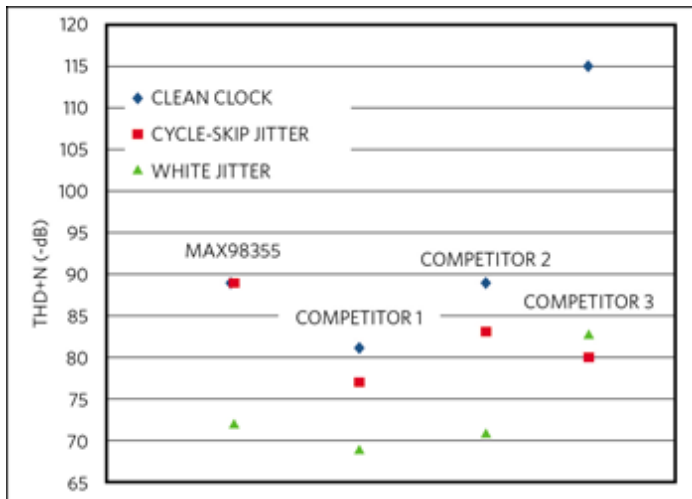


Figure 11. 20kHz THD+N performance degradation with clock jitter.

Conclusion

This application note has presented a methodology for testing audio DAC jitter tolerance. Audio DACs respond differently to jitter in the low-frequency and high-frequency bands, thus it helps to separately specify tolerance to these two bands of jitter spectrum. DACs that tolerate high levels of jitter allow simpler implementations of the sampling clocks without degrading audio quality.

National Instruments is a registered trademark of National Instruments Corporation.

WaveRunner is a registered trademark of LeCroy Corporation.

Related Parts

[MAX98095](#)

Audio Hub with FlexSound Processor

MAX98096	Audio Hub with Wideband FlexSound Processor	
MAX98355A	PCM Input Class D Audio Power Amplifiers	Free Samples
MAX98355B	PCM Input Class D Audio Power Amplifiers	Free Samples
MAX98356	PDM Input Class D Audio Power Amplifier	

More Information

For Technical Support: <http://www.maximintegrated.com/support>

For Samples: <http://www.maximintegrated.com/samples>

Other Questions and Comments: <http://www.maximintegrated.com/contact>

Application Note 5477: <http://www.maximintegrated.com/an5477>

APPLICATION NOTE 5477, AN5477, AN 5477, APP5477, Appnote5477, Appnote 5477

© 2013 Maxim Integrated Products, Inc.

Additional Legal Notices: <http://www.maximintegrated.com/legal>