DS92LV010A Bus LVDS 3.3/5.0V Single Transceiver

Check for Samples: DS92LV010A

FEATURES

- **Bus LVDS Signaling (BLVDS)**
- **Designed for Double Termination Applications**
- **Balanced Output Impedance**
- **Lite Bus Loading 5pF Typical**
- **Glitch Free Power Up/Down (Driver Disabled)**
- **3.3V or 5.0V Operation**
- **±1V Common Mode Range**
- **±100mV Receiver Sensitivity**
- **High Signaling Rate Capability (Above 100 Mbps)**
- **Low Power CMOS Design**
- **Product Offered in 8 Lead SOIC Package**
- **Industrial Temperature Range Operation**

DESCRIPTION

The DS92LV010A is one in a series of transceivers designed specifically for the high speed, low power proprietary bus backplane interfaces. The device operates from a single 3.3V or 5.0V power supply and includes one differential line driver and one receiver. To minimize bus loading the driver outputs and receiver inputs are internally connected. The logic interface provides maximum flexibility as 4 separate lines are provided (DIN, DE, $\overline{RE}$, and ROUT). The device also features flow through which allows easy PCB routing for short stubs between the bus pins and the connector. The driver has 10 mA drive capability, allowing it to drive heavily loaded backplanes, with impedance as low as 27 Ohms.

The driver translates between TTL levels (single-ended) to Low Voltage Differential Signaling levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition the differential signaling provides common mode noise rejection of ±1V.

The receiver threshold is ±100mV over a ±1V common mode range and translates the low voltage differential levels to standard (CMOS/TTL) levels.

CONNECTION DIAGRAM

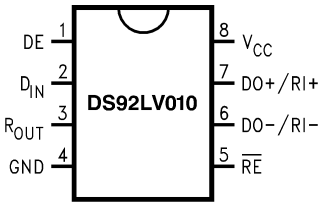


Figure 1. SOIC Package
See Package Number D0008A

BLOCK DIAGRAM

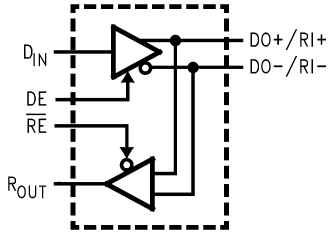


Figure 2.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)(3)

Supply Voltage (V_{CC})		6.0V
Enable Input Voltage (DE, $\overline{RE}$)		−0.3V to (V_{CC} + 0.3V)
Driver Input Voltage (DIN)		−0.3V to (V_{CC} + 0.3V)
Receiver Output Voltage (R_{OUT})		−0.3V to (V_{CC} + 0.3V)
Bus Pin Voltage (DO/RI±)		−0.3V to + 3.9V
Driver Short Circuit Current		Continuous
ESD (HBM 1.5 kΩ, 100 pF)		>2.0 kV
Maximum Package Power Dissipation at 25°C	SOIC	1025 mW
	Derate SOIC Package	8.2 mW/°C
Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)		260°C

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground except V_{OD}, V_{ID}, V_{TH} and V_{TL} unless otherwise specified.
(2) Absolute Maximum Ratings are these beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

	Min	Max	Units
Supply Voltage (V_{CC}), or	3.0	3.6	V
Supply Voltage (V_{CC})	4.5	5.5	V
Receiver Input Voltage	0.0	2.9	V
Operating Free Air Temperature	−40	+85	°C

3.3V DC ELECTRICAL CHARACTERISTICS (1)(2)

T_A = −40°C to +85°C unless otherwise noted, V_{CC} = 3.3V ± 0.3V

Parameter		Test Conditions		Pin	Min	Typ	Max	Units
V_{OD}	Output Differential Voltage	R_L = 27Ω, See Figure 3		DO+/RI+, DO−/RI−	140	250	360	mV
ΔV_{OD}	V_{OD} Magnitude Change					3	30	mV
V_{OS}	Offset Voltage				1	1.25	1.65	V
ΔV_{OS}	Offset Magnitude Change					5	50	mV
I_{OSD}	Output Short Circuit Current	V_O = 0V, DE = V_{CC}				−12	−20	mA
V_{OH}	Voltage Output High	V_{ID} = +100 mV	I_{OH} = −400 µA	R_{OUT}	2.8	3		V
		Inputs Open			2.8	3		V
		Inputs Shorted			2.8	3		V
		Inputs Terminated, R_L = 27Ω			2.8	3		V
V_{OL}	Voltage Output Low	I_{OL} = 2.0 mA, V_{ID} = −100 mV				0.1	0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, V_{ID} = +100 mV			−5	−35	−85	mA
V_{TH}	Input Threshold High	DE = 0V		DO+/RI+, DO−/RI−			+100	mV
V_{TL}	Input Threshold Low				−100			mV
I_{IN}	Input Current	DE = 0V, V_{IN} = +2.4V, or 0V			−20	±1	+20	µA
		V_{CC} = 0V, V_{IN} = +2.4V, or 0V			−20	±1	+20	µA
V_{IH}	Minimum Input High Voltage			DIN, DE, $\overline{RE}$	2.0		V_{CC}	V
V_{IL}	Maximum Input Low Voltage				GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V				±1	±10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V				±1	±10	µA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −18 mA			−1.5	−0.8		V
I_{CCD}	Power Supply Current	DE = $\overline{RE}$ = V_{CC} , R_L = 27Ω		V_{CC}		13	20	mA
I_{CCR}		DE = $\overline{RE}$ = 0V				5	8	mA
I_{CCZ}		DE = 0V, $\overline{RE}$ = V_{CC}				3	7.5	mA
I_{CC}		DE = V_{CC}, $\overline{RE}$ = 0V, R_L = 27Ω				16	22	mA
C_{output}	Capacitance @ BUS Pins			DO+/RI+, DO−/RI−		5		pF

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground except V_{OD}, V_{ID}, V_{TH} and V_{TL} unless otherwise specified.
(2) All typicals are given for V_{CC} = +3.3V or 5.0 V and T_A = +25°C, unless otherwise stated.

5V DC ELECTRICAL CHARACTERISTICS (1)(2)

T_A = −40°C to +85°C unless otherwise noted, V_{CC} = 5.0V ± 0.5V

Parameter		Test Conditions		Pin	Min	Typ	Max	Units
V_{OD}	Output Differential Voltage	R_L = 27Ω, See Figure 3		DO+/RI+, DO−/RI−	145	270	390	mV
ΔV_{OD}	V_{OD} Magnitude Change					3	30	mV
V_{OS}	Offset Voltage				1	1.35	1.65	V
ΔV_{OS}	Offset Magnitude Change					5	50	mV
I_{OSD}	Output Short Circuit Current	V_O = 0V, DE = V_{CC}				−12	−20	mA
V_{OH}	Voltage Output High	V_{ID} = +100 mV	I_{OH} = −400 µA	R_{OUT}	4.3	5.0		V
		Inputs Open			4.3	5.0		V
		Inputs Shorted			4.3	5.0		V
		Inputs Terminated, R_L = 27Ω			4.3	5.0		V
V_{OL}	Voltage Output Low	I_{OL} = 2.0 mA, V_{ID} = −100 mV				0.1	0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, V_{ID} = +100 mV			−35	−90	−130	mA
V_{TH}	Input Threshold High	DE = 0V		DO+/RI+, DO−/RI−			+100	mV
V_{TL}	Input Threshold Low				−100			mV
I_{IN}	Input Current	DE = 0V, V_{IN} = +2.4V, or 0V			−20	±1	+20	µA
		V_{CC} = 0V, V_{IN} = +2.4V, or 0V			−20	±1	+20	µA
V_{IH}	Minimum Input High Voltage			DIN, DE, $\overline{RE}$	2.0		V_{CC}	V
V_{IL}	Maximum Input Low Voltage				GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V				±1	±10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V				±1	±10	µA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −18 mA			−1.5	−0.8		V
I_{CCD}	Power Supply Current	DE = $\overline{RE}$ = V_{CC}, R_L = 27Ω		V_{CC}		17	25	mA
I_{CCR}		DE = $\overline{RE}$ = 0V				6	10	mA
I_{CCZ}		DE = 0V, $\overline{RE}$ = V_{CC}				3	8	mA
I_{CC}		DE = V_{CC}, $\overline{RE}$ = 0V, R_L = 27Ω				20	25	mA
C_{output}	Capacitance @ BUS Pins			DO+/RI+, DO−/RI−		5		pF

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground except V_{OD}, V_{ID}, V_{TH} and V_{TL} unless otherwise specified.
(2) All typicals are given for V_{CC} = +3.3V or 5.0 V and T_A = +25°C, unless otherwise stated.

3.3V AC ELECTRICAL CHARACTERISTICS (1)

T_A = −40°C to +85°C, V_{CC} = 3.3V ± 0.3V

Parameter		Test Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low	R_L = 27Ω, See Figure 4 and Figure 5 C_L = 10 pF	1.0	3.0	5.0	ns
t_{PLHD}	Differential Prop. Delay Low to High		1.0	2.8	5.0	ns
t_{SKD}	Differential SKEW |t_{PHLD} - t_{PLHD}|			0.2	1.0	ns
t_{TLH}	Transition Time Low to High			0.3	2.0	ns
t_{THL}	Transition Time High to Low			0.3	2.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 27Ω, See Figure 6 and Figure 7 C_L = 10 pF	0.5	4.5	9.0	ns
t_{PLZ}	Disable Time Low to Z		0.5	5.0	10.0	ns
t_{PZH}	Enable Time Z to High		2.0	5.0	7.0	ns
t_{PZL}	Enable Time Z to Low		1.0	4.5	9.0	ns
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low	See Figure 8 and Figure 9 C_L = 10 pF	2.5	5.0	12.0	ns
t_{PLHD}	Differential Prop. Delay Low to High		2.5	5.5	10.0	ns
t_{SKD}	Differential SKEW |t_{PHLD} - t_{PLHD}|			0.5	2.0	ns
t_r	Rise Time			1.5	4.0	ns
t_f	Fall Time			1.5	4.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 500Ω, See Figure 10 and Figure 11 C_L = 10 pF(2)	2.0	4.0	6.0	ns
t_{PLZ}	Disable Time Low to Z		2.0	5.0	7.0	ns
t_{PZH}	Enable Time Z to High		2.0	7.0	13.0	ns
t_{PZL}	Enable Time Z to Low		2.0	6.0	10.0	ns

(1) Generator waveforms for all tests unless otherwise specified: f = 1MHz, ZO = 50Ω, tr, tf ≤ 6.0ns (0%–100%) on control pins and ≤ 1.0ns for RI inputs.
(2) For receiver tri-state delays, the switch is set to V_{CC} for t_{PZL}, and t_{PLZ} and to GND for t_{PZH}, and t_{PHZ}.

5V AC ELECTRICAL CHARACTERISTICS (1)

T_A = −40°C to +85°C, V_{CC} = 5.0V ± 0.5V

Parameter		Test Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low	R_L = 27Ω, See Figure 4 and Figure 5 C_L = 10 pF	0.5	2.7	4.5	ns
t_{PLHD}	Differential Prop. Delay Low to High		0.5	2.5	4.5	ns
t_{SKD}	Differential SKEW |t_{PHLD} - t_{PLHD}|			0.2	1.0	ns
t_{TLH}	Transition Time Low to High			0.3	2.0	ns
t_{THL}	Transition Time High to Low			0.3	2.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 27Ω, See Figure 6 and Figure 7 C_L = 10 pF	0.5	3.0	7.0	ns
t_{PLZ}	Disable Time Low to Z		0.5	5.0	10.0	ns
t_{PZH}	Enable Time Z to High		2.0	4.0	7.0	ns
t_{PZL}	Enable Time Z to Low		1.0	4.0	9.0	ns
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low	See Figure 8 and Figure 9 C_L = 10 pF	2.5	5.0	12.0	ns
t_{PLHD}	Differential Prop. Delay Low to High		2.5	4.6	10.0	ns
t_{SKD}	Differential SKEW |t_{PHLD} - t_{PLHD}|			0.4	2.0	ns
t_r	Rise Time			1.2	2.5	ns
t_f	Fall Time			1.2	2.5	ns
t_{PHZ}	Disable Time High to Z	R_L = 500Ω, See Figure 10 and Figure 11 C_L = 10 pF(2)	2.0	4.0	6.0	ns
t_{PLZ}	Disable Time Low to Z		2.0	4.0	6.0	ns
t_{PZH}	Enable Time Z to High		2.0	5.0	9.0	ns
t_{PZL}	Enable Time Z to Low		2.0	5.0	7.0	ns

(1) Generator waveforms for all tests unless otherwise specified: f = 1MHz, ZO = 50Ω, tr, tf ≤ 6.0ns (0%–100%) on control pins and ≤ 1.0ns for RI inputs.
(2) For receiver tri-state delays, the switch is set to V_{CC} for t_{PZL}, and t_{PLZ} and to GND for t_{PZH}, and t_{PHZ}.

TEST CIRCUITS AND TIMING WAVEFORMS

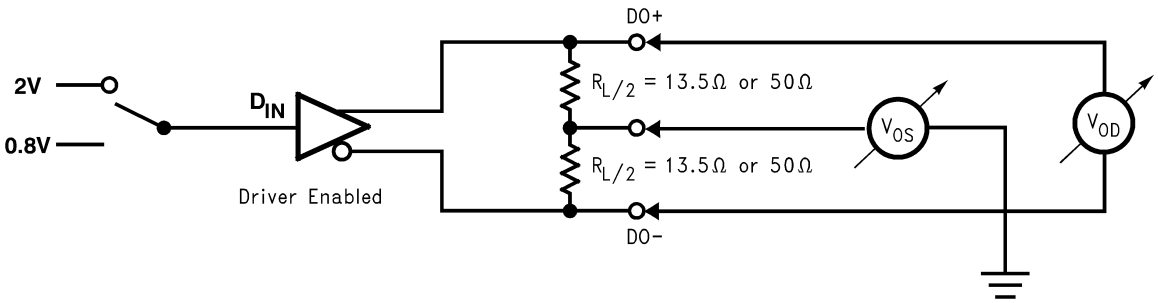


Figure 3. Differential Driver DC Test Circuit

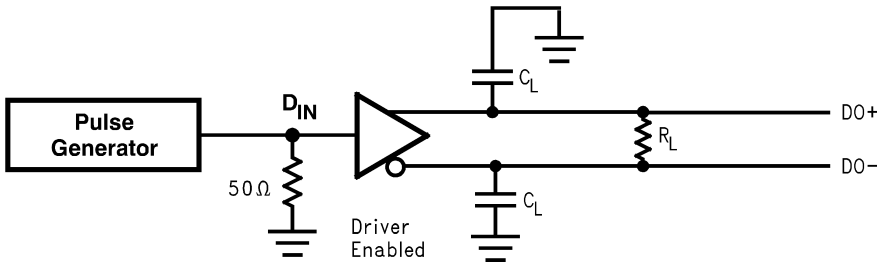


Figure 4. Differential Driver Propagation Delay and Transition Time Test Circuit

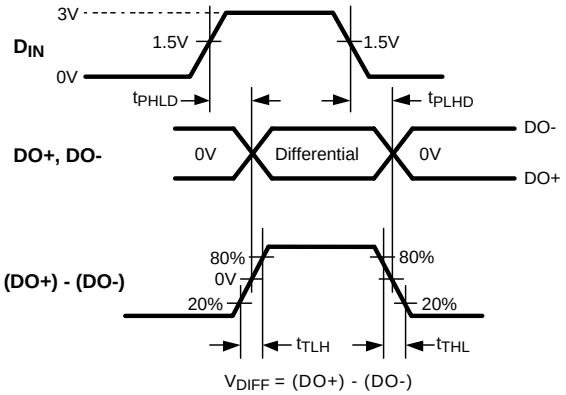


Figure 5. Differential Driver Propagation Delay and Transition Time Waveforms

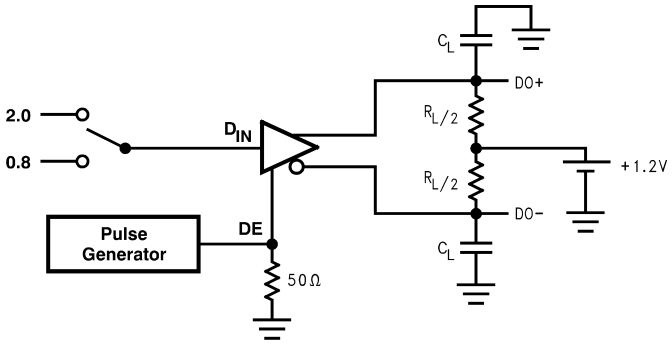


Figure 6. Driver TRI-STATE Delay Test Circuit

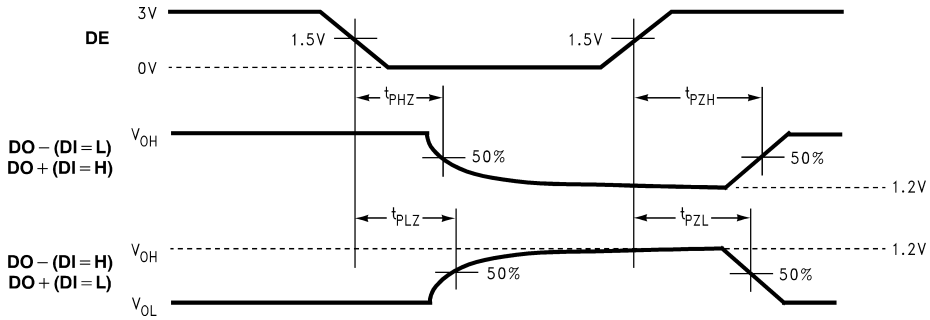


Figure 7. Driver TRI-STATE Delay Waveforms

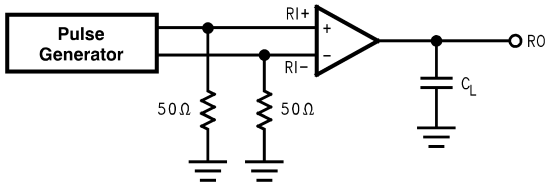


Figure 8. Receiver Propagation Delay and Transition Time Test Circuit

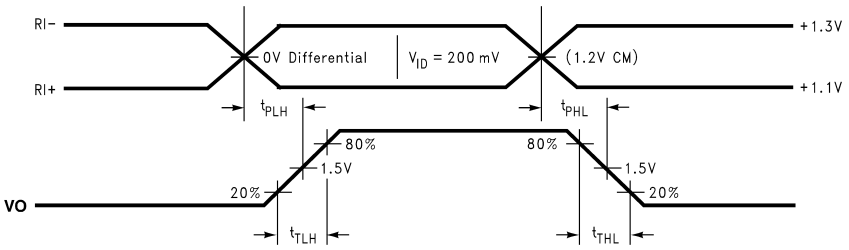


Figure 9. Receiver Propagation Delay and Transition Time Waveforms

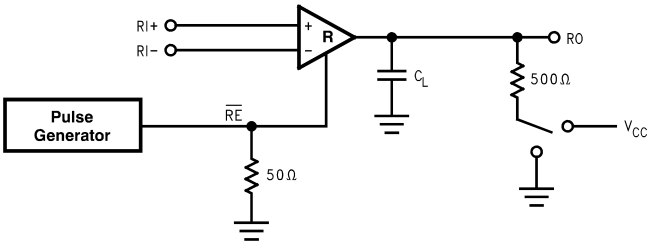


Figure 10. Receiver TRI-STATE Delay Test Circuit

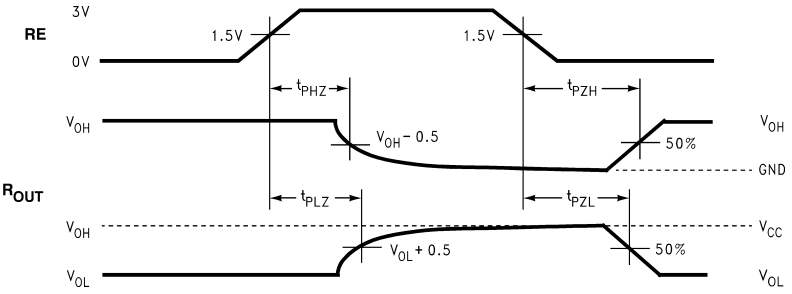


Figure 11. Receiver TRI-STATE Delay Waveforms TRI-STATE Delay Waveforms

TYPICAL BUS APPLICATION CONFIGURATIONS

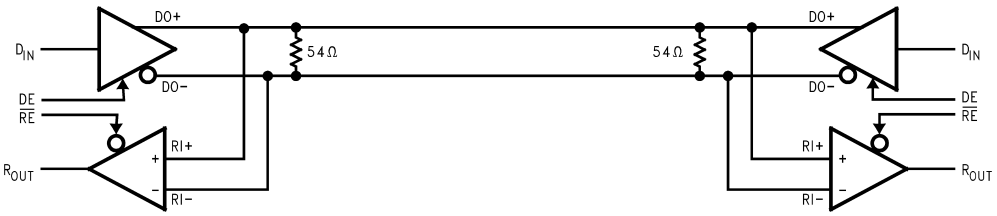


Figure 12. Bi-Directional Half-Duplex Point-to-Point Applications

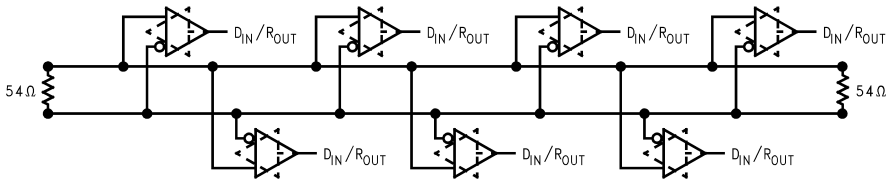


Figure 13. Multi-Point Bus Applications

APPLICATION INFORMATION

There are a few common practices which should be implied when designing PCB for BLVDS signaling. Recommended practices are:

- Use at least 4 layer PCB board (BLVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (BLVDS port side) connector as possible.
- Bypass each BLVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best. Two or three multi-layer ceramic (MLC) surface mount capacitors (0.1 µF, and 0.01 µF in parallel should be used between each V_{CC} and ground. The capacitors should be as close as possible to the V_{CC} pin.
- Use the termination resistor which best matches the differential impedance of your transmission line.
- Leave unused LVDS receiver inputs open (floating)

Table 1. Functional Table

MODE SELECTED	DE	$\overline{RE}$
DRIVER MODE	H	H
RECEIVER MODE	L	L
TRI-STATE MODE	L	H
LOOP BACK MODE	H	L

Table 2. Transmitter Mode(1)

INPUTS		OUTPUTS	
DE	DI	DO+	DO−
H	L	L	H
H	H	H	L
H	2 > & > 0.8	X	X
L	X	Z	Z

(1) L = Low state
H = High state

Table 3. Receiver Mode(1)

INPUTS		OUTPUT
$\overline{RE}$	(RI+)-(RI−)	
L	L (< −100 mV)	L
L	H (> +100 mV)	H
L	100 mV > & > −100 mV	X
H	X	Z

(1) X = High or Low logic state
Z = High impedance state
L = Low state
H = High state

Table 4. Device Pin Descriptions

Pin Name	Pin No.	Input/Output	Description
DIN	2	I	TTL Driver Input
DO±/RI±	6, 7	I/O	LVDS Driver Outputs/LVDS Receiver Inputs
R_{OUT}	3	O	TTL Receiver Output
$\overline{RE}$	5	I	Receiver Enable TTL Input (Active Low)
DE	1	I	Driver Enable TTL Input (Active High)
GND	4	NA	Ground
V_{CC}	8	NA	Power Supply

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS92LV010ATM	NRND	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LV010 ATM	
DS92LV010ATM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LV010 ATM	Samples
DS92LV010ATMX	NRND	SOIC	D	8	2500	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LV010 ATM	
DS92LV010ATMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LV010 ATM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

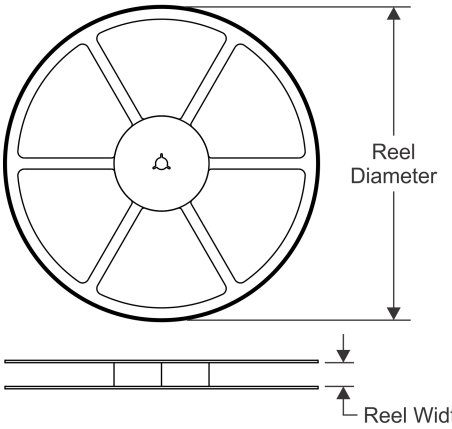
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

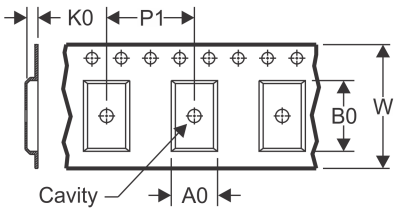
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

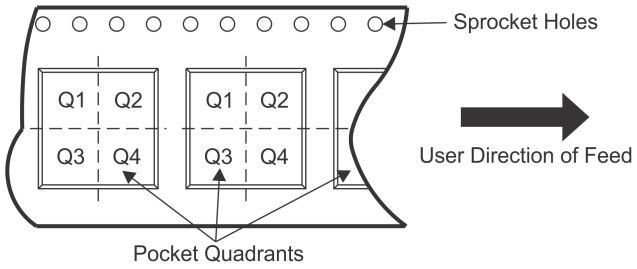


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

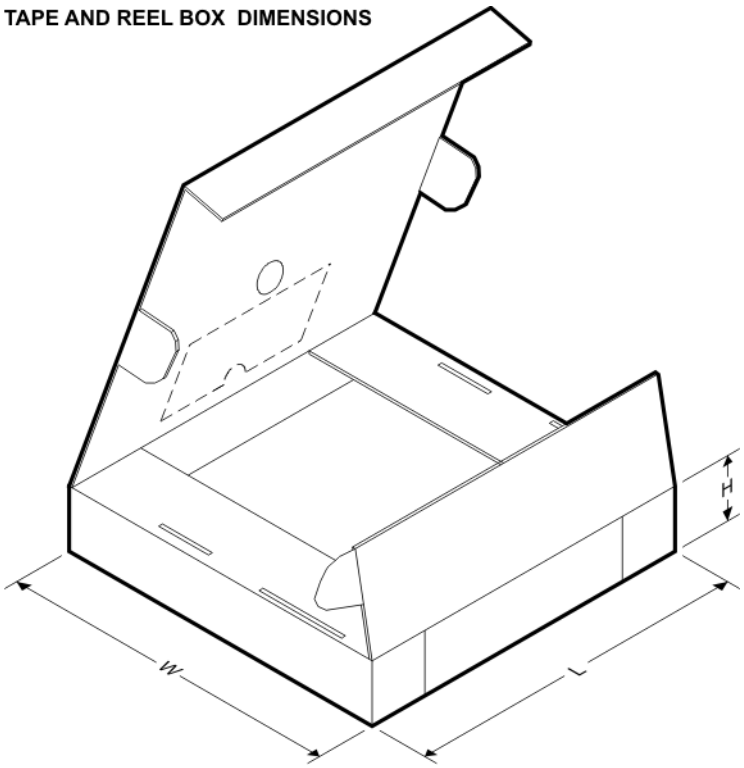
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS92LV010ATMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS92LV010ATMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

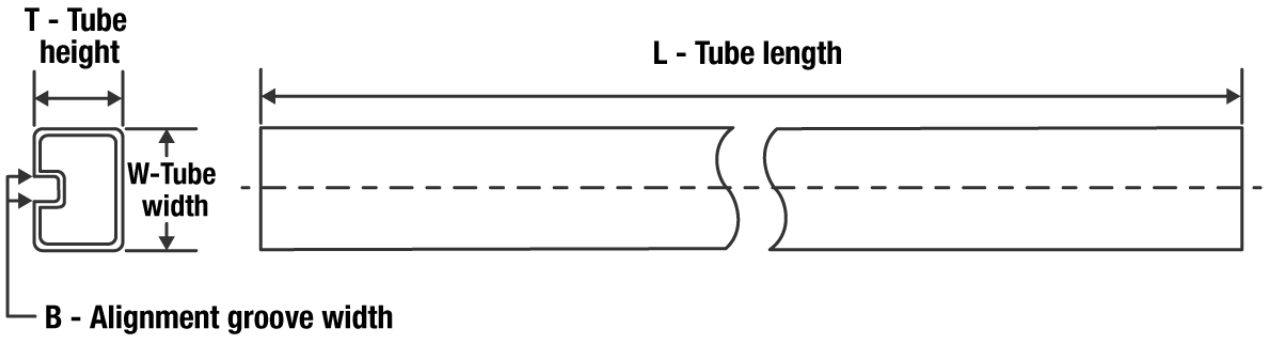
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

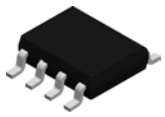
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS92LV010ATMX	SOIC	D	8	2500	367.0	367.0	35.0
DS92LV010ATMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS92LV010ATM	D	SOIC	8	95	495	8	4064	3.05
DS92LV010ATM	D	SOIC	8	95	495	8	4064	3.05
DS92LV010ATM/NOPB	D	SOIC	8	95	495	8	4064	3.05

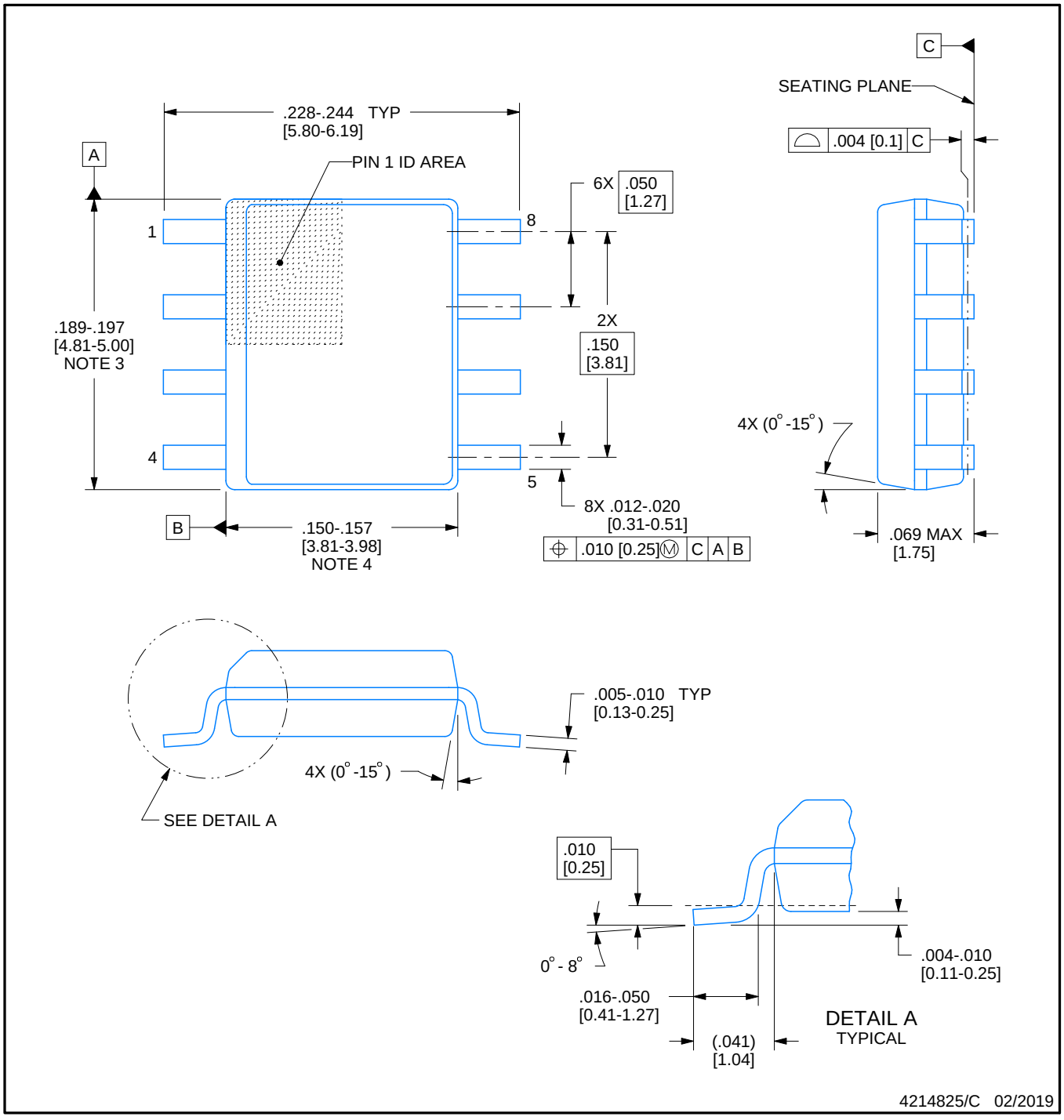


PACKAGE OUTLINE

D0008A

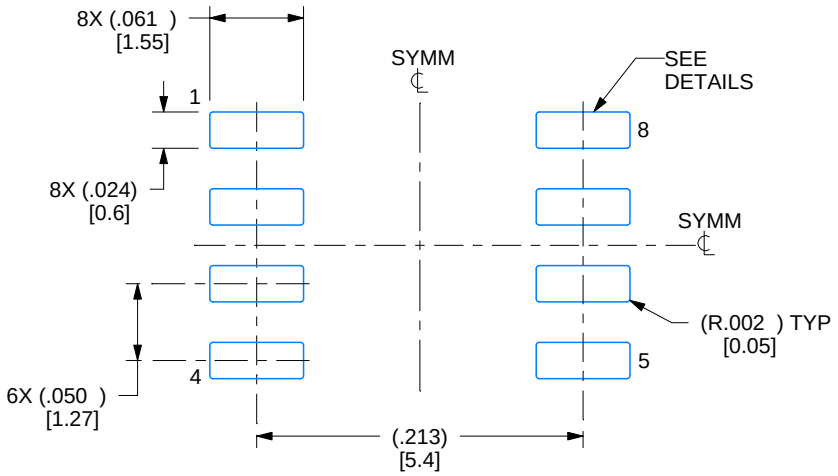
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

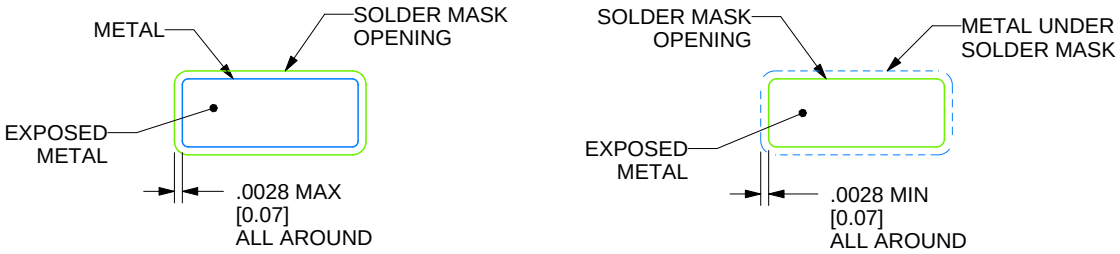


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

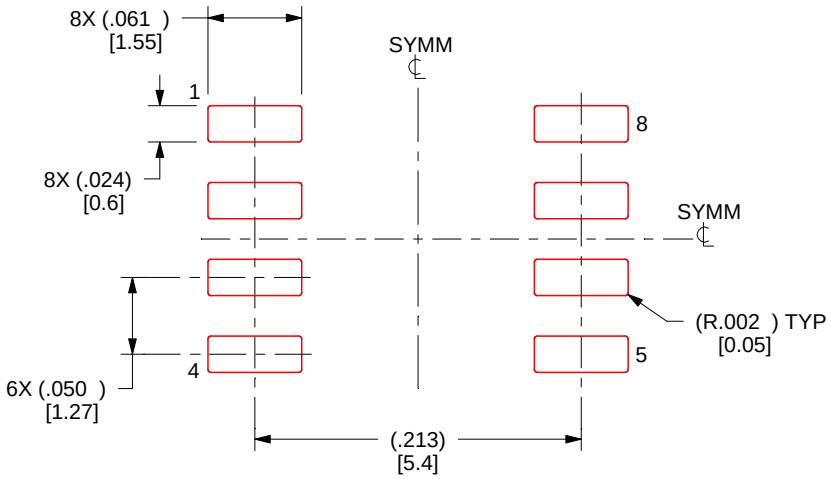
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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