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APPLICATION NOTE 6596

FIVE THINGS YOU SHOULD KNOW ABOUT LINEAR REGULATORS

Abstract: While linear regulators (LDOs) seem relatively simple, many situations occur in which LDOs perform contrary to your expectations. This application note explores five of those situations, including startup, quiescent current near dropout, load transient performance, PSRR and noise, and input protections. Understanding these situations will improve product selection and debug processes.

Introduction

When you're looking for a linear regulator these days, it's simple to navigate through the seemingly limitless offerings using parametric search tools and narrow your choices down to a handful of relevant candidates. What output voltage do I need? How much load current? Input voltage withstand? How close to dropout will the regulator run? What is the maximum operating input voltage? What about the package and external component sizes? Next comes the fine-tuning. What if the load is sensitive to supply fluctuations? You might need very low output noise and high PSRR. Maybe your design is a battery-powered device with an always-on supply. In that case, you'll need a regulator with ultra-low quiescent current.

Now you've got the field narrowed sufficiently to just the parts that are appropriate for your application. But you're not done yet. There are five things to consider before making your final choice.

How does the regulator deal with startup?

Is the quiescent current still low if I run into, or near, dropout?

How about the load transient performance with the actual load, rather than just the situation depicted in the data sheet?

Is my LDO output ripple dominated by feedthrough from the input due to low PSRR, or by the LDO output noise?

How does the part behave when I turn it off?

Why are these questions so important? They aren't. . .until there's a problem. Then, some functionality issue just turned your new favorite part into your most curious part. You probably feel a little betrayed, or at least underinformed. And, you need to spend extra time troubleshooting and possibly redesigning your board.

This application note sheds some light on these five LDO features. Hopefully, the insights are useful during your next selection and design-in of a linear regulator.

#1: Startup

Most regulators come with an enable input to control the regulator power-up and to save power when the output is turned off. Regulators with enable inputs generally also have a soft-start feature. Soft-start prevents the regulator from overloading the input when the output is turned on. Soft-start is generally implemented in one of two ways.

Current Soft-Start

The first method is current soft-start. Most regulators have a current limit; current soft-start works by ramping up or stepping up that current limit. Current soft-start causes the output voltage to rise slowly as the output capacitance charges up with something much less than the maximum load current. The benefit of current soft-start is that the regulator input current follows a consistent increasing pattern, without transferring startup load-current transients to the input.

When the load circuitry is enabled, you might notice a point where the output voltage ramp abruptly changes direction. This happens because the load circuitry is turning on and trying to operate from a regulator with limited output current capability. If the load current exceeds the soft-start current, the load pulls itself into undervoltage, resulting in an unwanted reset. This cycle continues as the load current turns on and off. Eventually the soft-start current limit becomes high enough to support the load, the reset circuitry releases for the last time, and the load circuitry wakes up with a hangover.

Voltage Soft-Start

The second method of soft-start is to ramp the regulation voltage. Ramping the regulation voltage produces a monotonic slope on the output voltage, absent of any voltage transients when downstream circuitry turns on. This should also prevent the load from multiple visits into the reset state, since the output voltage only crosses the load undervoltage threshold once.

The inrush current during voltage soft-start is determined by the output capacitance and the ramp rate of the output voltage, plus the current drawn by the load. Typically, the output voltage ramp rate is set to a level that creates an inrush current of approximately 1% to 10% of the maximum rated output current when using the recommended minimum output capacitor. Setting the inrush current to under 10% of the maximum load current leaves room for extra current from the load and any extra output capacitance. The downside is that input current is a function of the load and is not directly controlled. The benefit is that you avoid the multiple resets.

Figure 1 shows a comparison of the current soft-start and voltage soft-start behaviors.

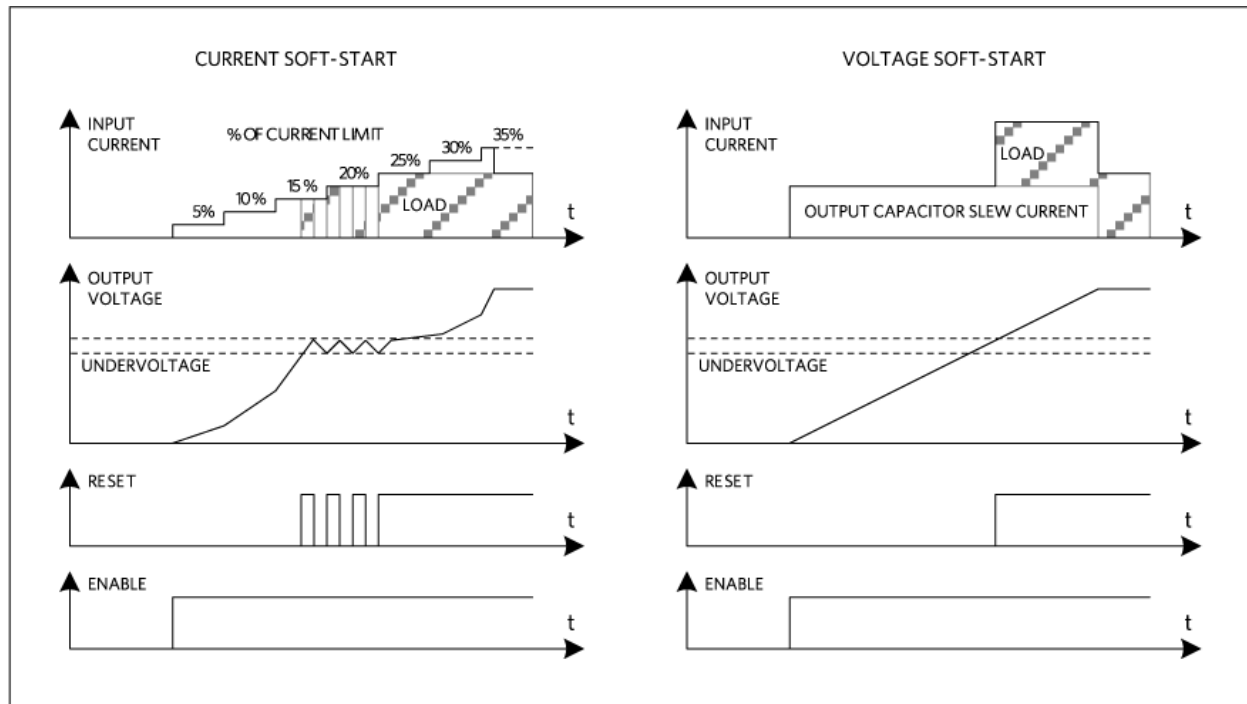


Figure 1. Behaviors of current soft-start and voltage soft-start.

#2: Dropout Supply Current

If your circuitry is powered from a battery, the regulator supply current can be important. The load circuitry could operate briefly, then remain in a standby state for long periods of time to save power. In this case, the battery life can, to a large extent, be determined by the quiescent supply current of the regulator and load. If so, you'll likely choose a linear regulator with the lowest possible quiescent current.

Now imagine your battery has been run down to the point where your input-to-output voltage is getting small. When running a linear regulator in dropout, even though the load current can be very small, the regulator forces the output FET to turn on hard to minimize the input-to-output voltage drop. The problem here is that driving an output FET on hard in dropout can consume a lot of current in the gate-drive circuitry (**Figure 2**). This has the effect of turning your "Standby Mode" into a "Fast Battery Discharging Mode."

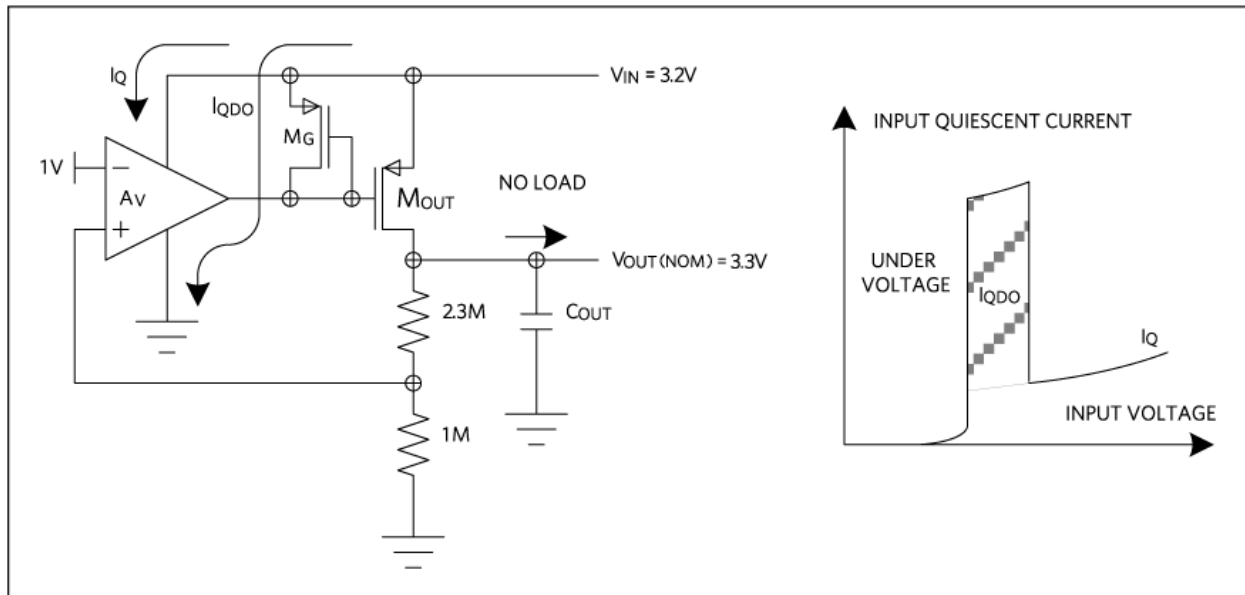


Figure 2. Increased quiescent current in dropout caused by M_G driver impedance.

Even on the better designs, it's not uncommon for the quiescent supply current to become elevated in dropout. Increases in dropout supply current of 2x are not uncommon, and some designs have increases of 10x or more. Occasionally dropout supply current is specified in the EC table or in a typical operating characteristics curve of quiescent current vs. input voltage. More often, though, the high dropout supply current information is left out of the data sheet.

If quiescent current in dropout is important in your application, look for an LDO with a data sheet that provides this information, or measure it yourself, to be certain the performance matches your expectations.

#3: Load-Transient Performance

Most regulators have some ability to hold the output in regulation during fast changes in load. As the load changes, the output FET gate drive needs to change. The time required for the gate drive to attain its new level usually determines the output transient undershoot or overshoot.

Usually a fast transition to full load results in the worst-case output transient undershoot. Before comparing regulators, always check the starting load current before the transient is applied. Starting from 10% of full load tends to give much better results than starting from 1%, since the output FET gate voltage starts much closer to its final value when prebiased with a 10% load vs. a 1% load. Much more difficult is achieving good load-transient performance when the load is changing from no load to full load.

You may think that maintaining a minimum load on your regulator output prevents large load transients. This should certainly help but is not always the solution. When a regulator is recovering from a load step from full load to light load, there is often an output overshoot. While the regulator is recovering from this overshoot, it resides its most vulnerable state—the situation where the output FET is completely debiased. In this state, if another load step is immediately applied, the output exhibits an undershoot that is much worse than the first.

If you have any situations where rapid on and off load pulses can occur, it's a good idea to check the load-transient performance of each regulator under similar conditions. **Figure 3** shows load-transient degradation during double-pulsed loads.

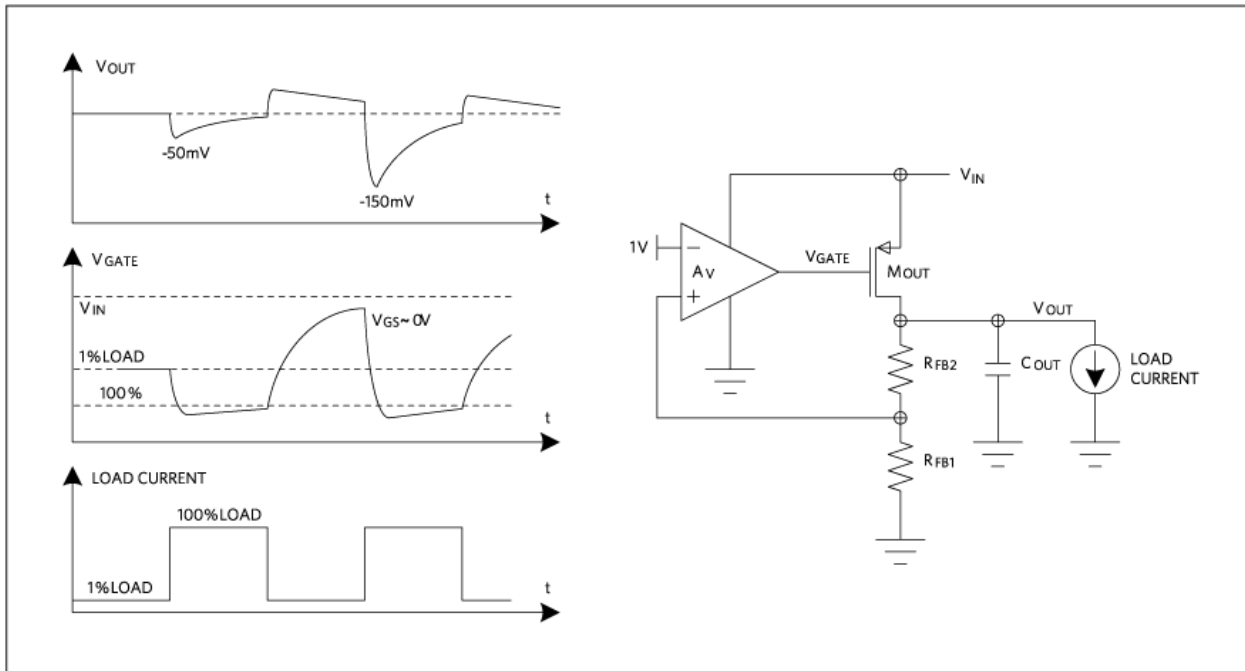


Figure 3. Load-transient undershoot degradation during double-pulsed loads.

#4: Noise vs. Power-Supply Rejection Ratio (PSRR)

Most regulators that are designed for low output noise also have excellent PSRR, for obvious reasons. The load is sensitive to supply ripple, regardless of the cause.

When running from a switching regulator, PSRR can be more of a problem than output noise. Take the case of a linear regulator with a step-down regulator at its input and a noise-sensitive load at its output. If the ripple from the step-down is $50\text{mV}_{\text{P-P}}$ at 100kHz , and at that same 100kHz the linear regulator has 60dB of PSRR, there is $50\text{mV}_{\text{P-P}}$ of ripple at the output, which is possibly equivalent to approximately 15mV_{RMS} of output noise. It might be that the total output noise of that same linear regulator is less than 5mV_{RMS} in a 10Hz to 100kHz bandwidth, but because of the PSRR and input ripple, the output ripple performance is no better than a regulator with 3x the noise, as shown in **Figure 4**.

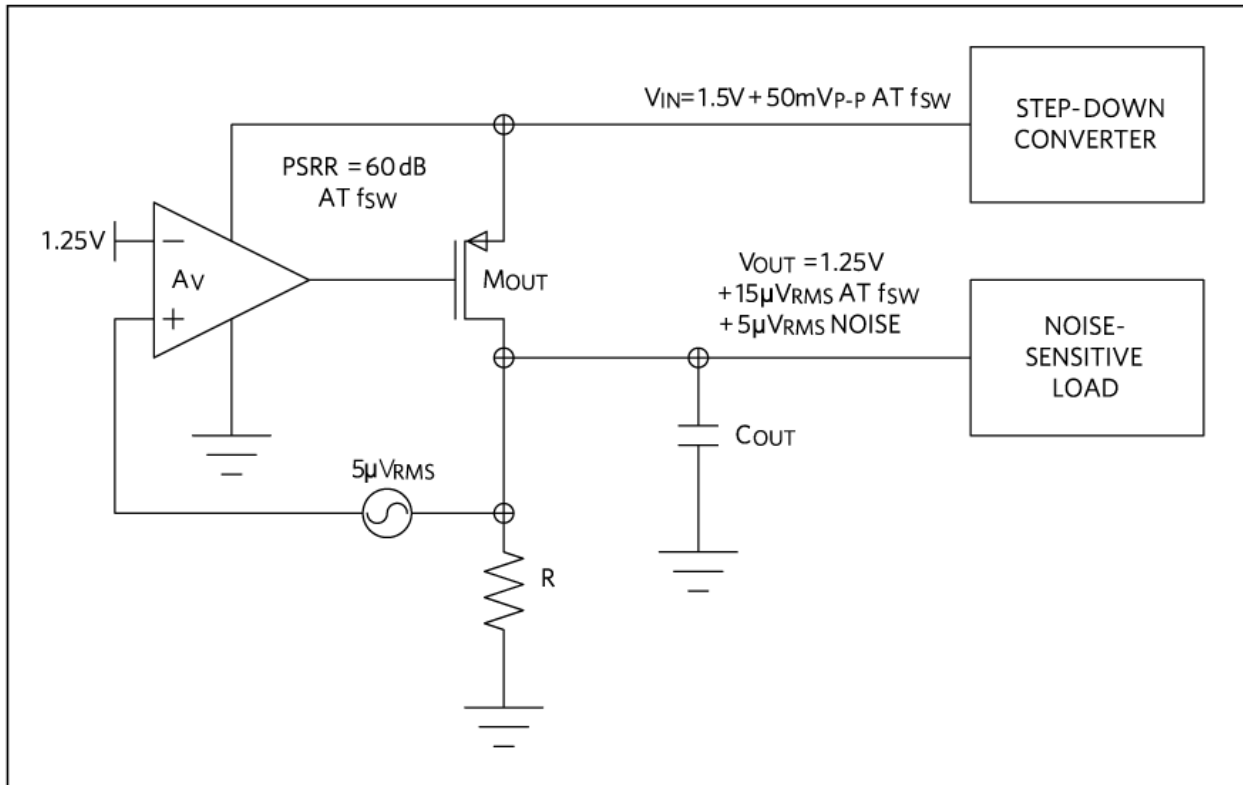


Figure 4. Output noise degradation dominated by PSRR.

For higher output voltages, the output noise of the linear regulator can become dominant of the PSRR performance. This is because the noise of the feedback input gets gained up by the feedback divider. Take the case of a linear regulator used to convert a noisy step-up converter output of 17V to a quiet 16V supply with less than 100mV of ripple. With a PSRR of 60dB at the switching frequency, a $50mV_{P-P}$ step-up converter ripple would be attenuated to $50mV_{P-P}$, or $15mV_{RMS}$, at the output. With a seemingly quiet $5mV_{RMS}$ reference and feedback amp input, you might think the feedback input noise wouldn't be a problem. But if the feedback input regulates to 1.25V and a resistor feedback string sets the output to 16V, the noise at the output grows to $5mV_{RMS} \times (16V/1.25V)$, or $64mV_{RMS}$, and is likely the dominant source of noise. **Figure 5** shows output noise degradation due to high output voltage.

When searching for a linear regulator, usually both output noise and PSRR need to be considered when powering a noise-sensitive load.

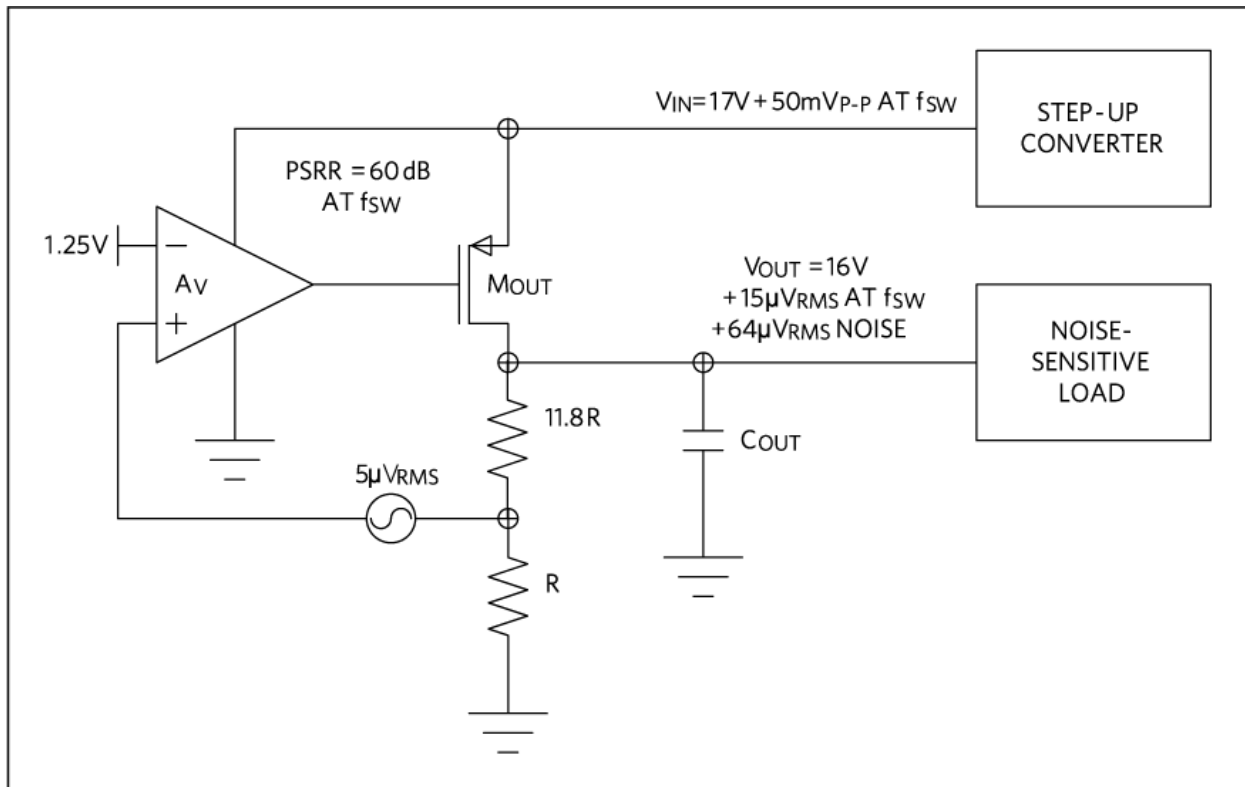


Figure 5. Output noise degradation due to high output voltage.

#5: Input Protection

It's common for linear regulators to have a body diode in their output FETs. This diode prevents the output from being more than 0.7V above the input. In most use cases this diode doesn't get in the way, but there are two cases where it can become a problem.

Reverse-Voltage Protection

There are situations where it is possible for the input voltage to be applied with the wrong polarity. Think of a 9V battery with its two metal contacts sitting side by side. Although the connector can prevent a permanent reverse connection to the battery, there can be several seconds or more of reverse voltage as the user replaces the battery.

Reverse-voltage protection allows the input pin to be below the ground pin without drawing any significant current. To accomplish this, the body diode of the output FET needs to be disconnected with a series switch. Most regulators include diodes that prevent any pin from going below ground to protect the pin from electrostatic discharge, or ESD. These diodes must also be removed and replaced with a different protection device to achieve reverse-voltage protection. See **Figure 6**.

An example of a device with reverse-voltage protection is the **MAX1725**, which allows its input to be 12V below ground without drawing significant input current.

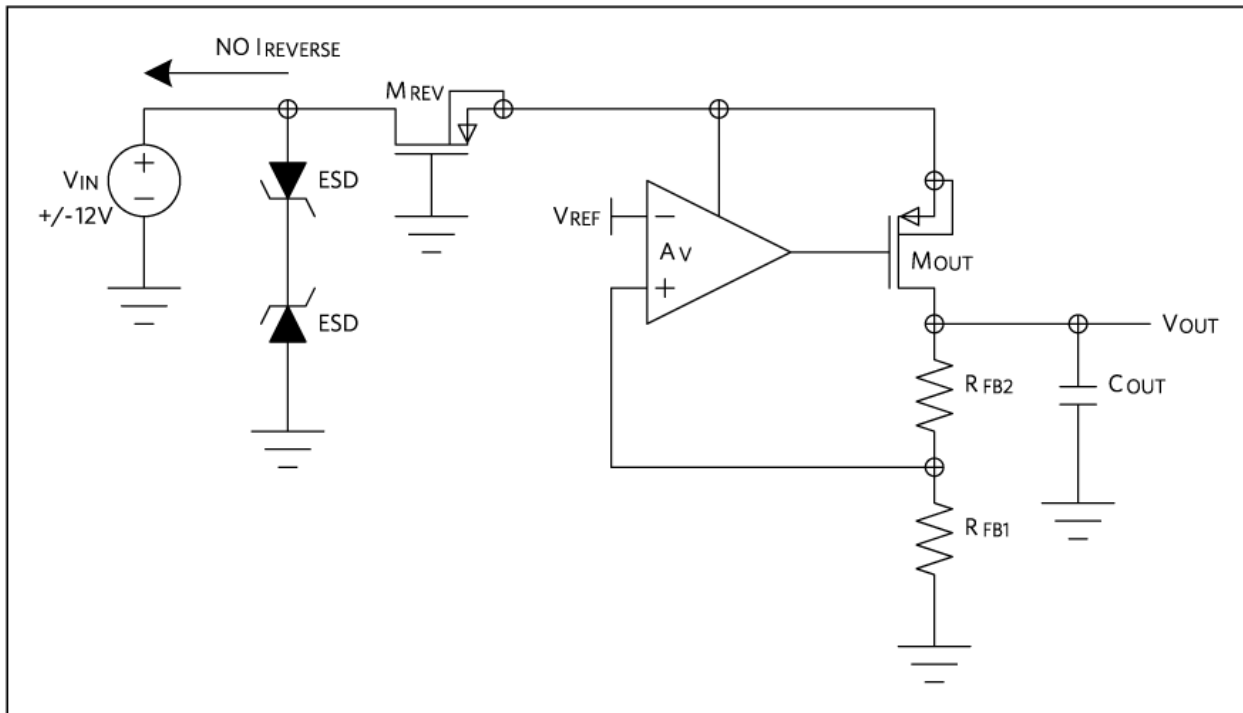


Figure 6. Reverse-voltage protection.

Reverse-Current Protection

Reverse-current protection in linear regulators is often confused with reverse-voltage protection. Although the effect is similar, to block reverse-current conduction in the body diode of the output FET, the control mechanism is quite different. **Figure 7** shows how reverse-current protection works.

Imagine the case where a highly capacitive load, like an audio circuit with many distributed supply decoupling capacitors, is powered from a linear regulator. Let's also assume this linear regulator is powered from a high-current step-down converter, and that in the shutdown state the converter shorts its output to ground. It wouldn't be surprising to find that, during the first shutdown event, the linear regulator gets damaged, as the network of load capacitors get discharged simultaneously through the body diode of the linear regulator.

Linear regulators with reverse-current protection avoid this problem by disconnecting the body diode when the input voltage drops below the output voltage. If the output was previously in regulation, the output FET would be on, and a small amount of reverse current would flow before tripping the protection circuitry. Notice that reverse-current protection simply eliminates current from output to input but makes no attempt to block current when the input pin voltage goes below ground, as in the case of reverse-voltage protection. An example of a device with reverse-current protection is the [MAX8902](#), which blocks reverse current from the load capacitors when the input is shorted to ground.

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