Using the VM1010 Wake-on-Sound Microphone and ZeroPower Listening™ Technology

Application Note
Rev2.0

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1 Introduction

1.1 Always-on voice-control is (almost) everywhere

Always-on voice-control is already a standard feature in PCs, smartphones and now voice controlled smart speakers which double as home automation hubs. Voice-control does not require a screen, physical contact or a user's full attention, and the only sensor is a microphone or mic array. The on-board processor must recognize a wake-word (Amazon's *Alexa*, Apple's *Hey Siri*, Google's *Hey Google* or Microsoft's *Cortana*, etc.) but all further voice-recognition can be performed in the cloud. By all appearances, it is the ideal way to interact with a new class of omnipresent, unobtrusive, connected devices that are almost everywhere.

Yet they are *almost everywhere* but why not *everywhere*?

Until now, the standby power-consumption of Always-on Voice-control has been too high – it has limited it to devices which are connected to power outlets, or at least frequently charged. This means the devices want to reside by a power outlet for too much of the time to be everywhere. If you examine the architecture of the voice processing, the reason for the high-power levels becomes clear.

The microphone and speech processor are always alert, always waiting for the wake-word - even when there is no sound to be heard, or a constant, unremarkable noise floor. This is wasteful and leaves a lot of room for power optimization. How do we put them to sleep when there is nothing of interest to hear? This type of optimization is needed to make battery power feasible for the Always on Voice device.

1.2 Introducing ZeroPower Listening

What is *ZeroPower Listening*™ (ZPL)? It is a new power optimized architecture for Always on Voice systems which uses the Vesper Piezoelectric MEMS to operate as an ultra-low power sound detector. When a soundwave hits a piezoelectric cantilever, and makes it move, the motion creates a voltage via the piezoelectric effect. This voltage is sensed by a low current comparator circuit which turns on the microphone circuit and sends a signal to the DSP to turn on. The first product to implement this ZPL architecture is Vesper's VM1010 which has a Wake on Sound (WoS) mode. This application note describes how to use the VM1010 microphone and its WoS mode.

In *Normal* (or "full power") mode, the microphone has a current consumption of 85µA, and acts as a full bandwidth high performance MEMS microphone with a single-ended output. As with all Vesper mics, it has high immunity to dust and water exposure.

In *Wake-on-Sound* mode, the microphone has a current consumption of only 10µA. The analog output is disabled, but the mic is still monitoring the ambient sound level. If a sound is heard which exceeds the (pre-configured) Wake on Sound loudness threshold, the microphone sets the digital output pin high. This single bit digital pin acts as a wake-up signal for a voice-processor, readying it to record and process the incoming sound.

The low current draw and threshold adjustment features of the VM1010 microphone create a configurable, ultra-low-power "acoustic watchdog". While it stays alert, the entire signal chain – voice-processor, preamplifiers & data converters – can go to sleep. And when a sound arrives, the system springs to action.

In many applications, the VM1010 provides this ability with virtually zero power drain. The battery in a smartphone or portable speaker naturally dissipates ~200µA[1], even with no load. A (much smaller) smartwatch battery will drain ~20µA with no load. This battery self-discharge represents the theoretical maximum battery life of a device with zero power consumption. The VM1010's 10µA supply current therefore has minimal impact on this in-built drain, making a "ZeroPower Listening" architecture in terms of product battery life.

Example applications for the VM1010 include:

1. As the only microphone in an always-on voice-control system – waking the Voice Processor and providing an analog audio signal.
2. As an "acoustic watchdog" only – waking up the Voice Processor, which then records audio using a separate microphone array.

[1] ~5%/month self-discharge of a 3000mAh Li-Ion battery (2% leakage + 3% protection-circuits drain)

2 Pinout & Pin Description

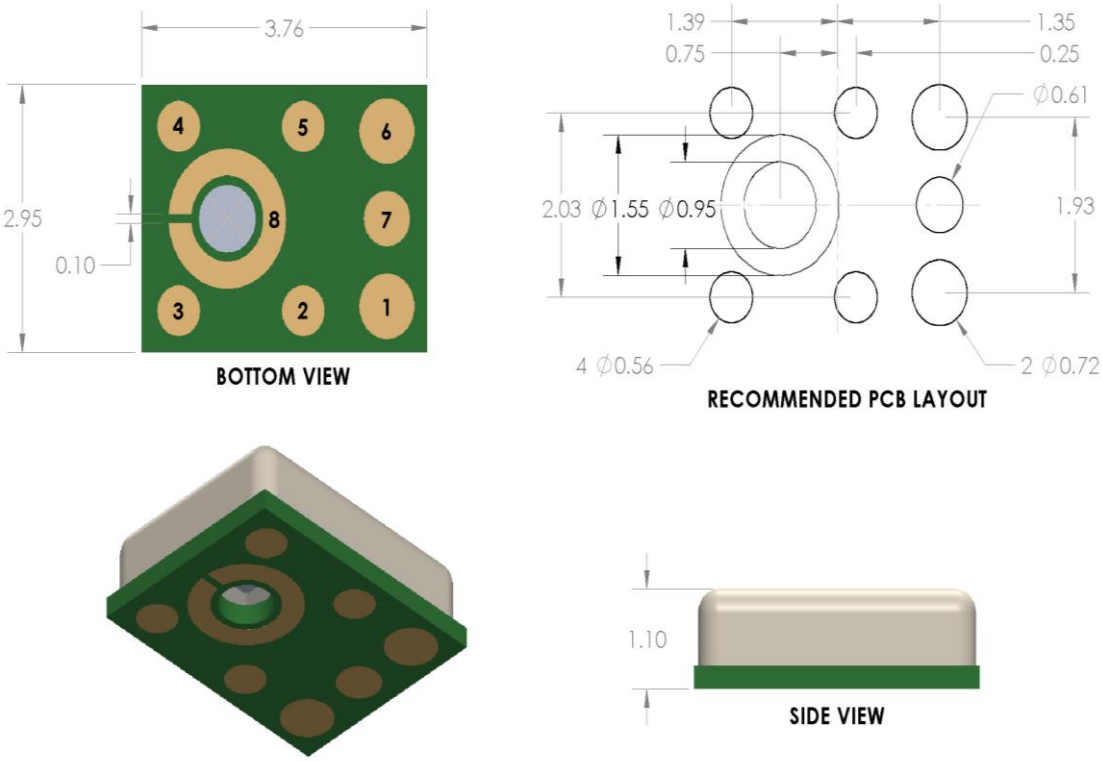


Figure 1: Mechanical drawing of VM1010 Microphone

Pin Number	Pin Name	Description
1	Vout	Analog Output Voltage
2	GA2	Wake-on-Sound Acoustic Threshold Adjust pin 2
3	GA1	Wake-on-Sound Acoustic Threshold Adjust pin 1
4	GND	Ground
5	mode	Mode control *(hi=Wake-on-Sound, lo=Normal-Power)*
6	Vdd	Power Supply *(1.6V to 3.6V)*

7	d_{out}	Digital output for Wake-on-Sound trigger
8	GND	Ground

Table 1: Pin Description for VM1010 Microphone

3 Microphone Modes

mode pin	**Mic mode**	Idd, **typ. (µA)**	**Vout pin**	**d_{out} pin**
high	Wake-on-Sound	10	GND	low, then latches high after first wake-up event
low or floating	Normal	85	audio output	Tied to GND through low impedance

Table 2: Effect of mode pin on microphone mode, supply current & output pins

The VM1010 microphone switches between two modes, depending on the *mode* digital input pin. All digital pins use standard CMOS logic levels, scaled to *Vdd*.

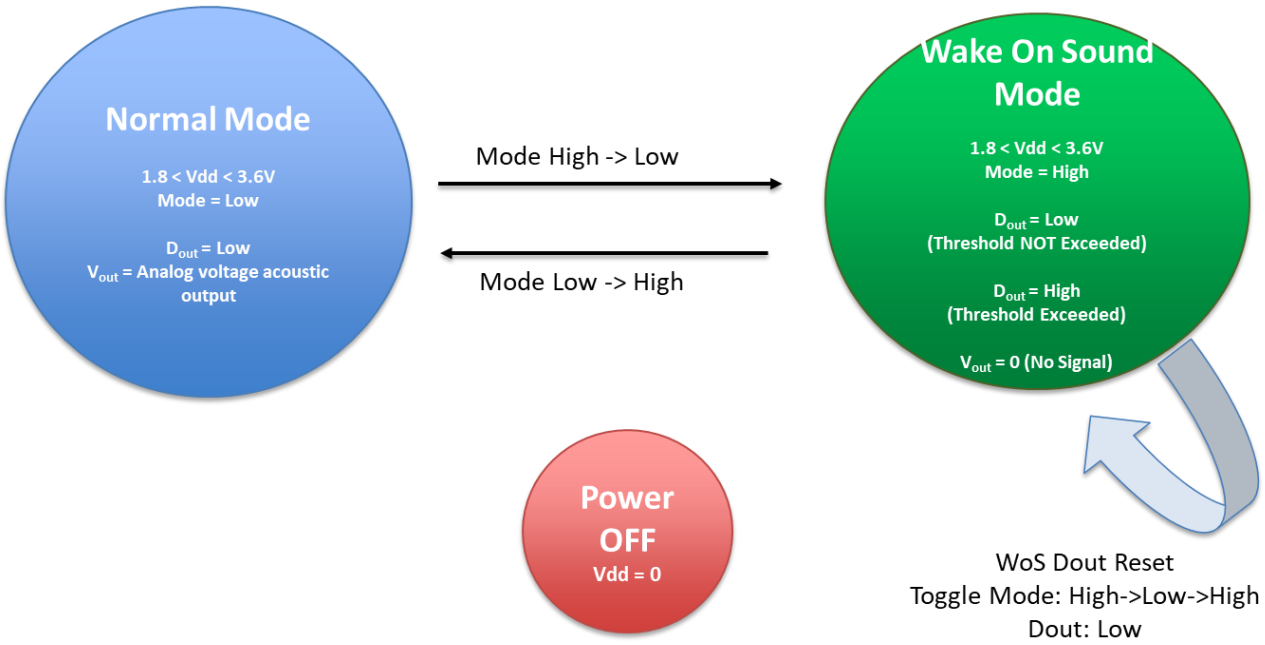


Figure 2: State diagram of VM1010 modes and relevant transitions

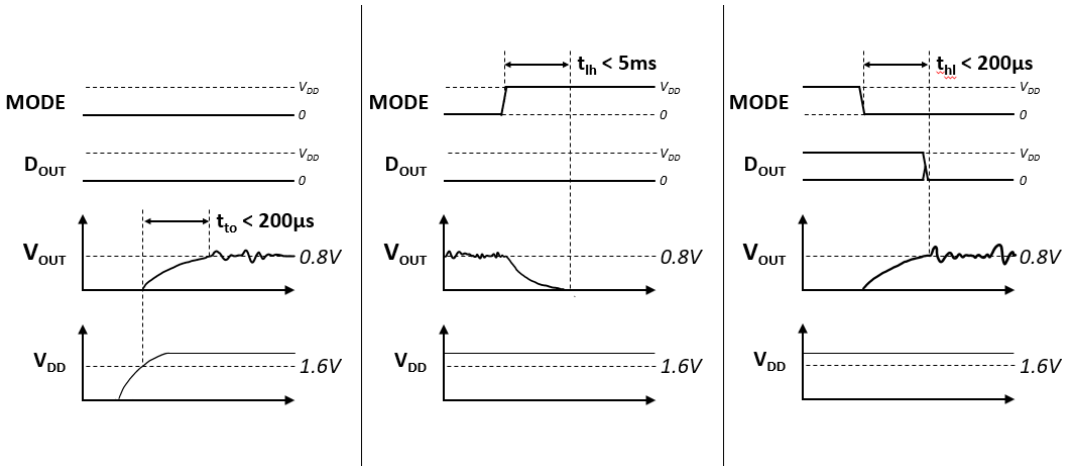


Figure 3: Vout DC and Vdd level timing diagrams showing turn-on time (left), transition time into Wake-on-Sound mode (center) & Full-Power mode (right)

We recommend powering up the microphone in Full-Power mode (*mode* pin low), and then entering WoS mode (raising *mode*) as needed.

3.1 Normal Mode

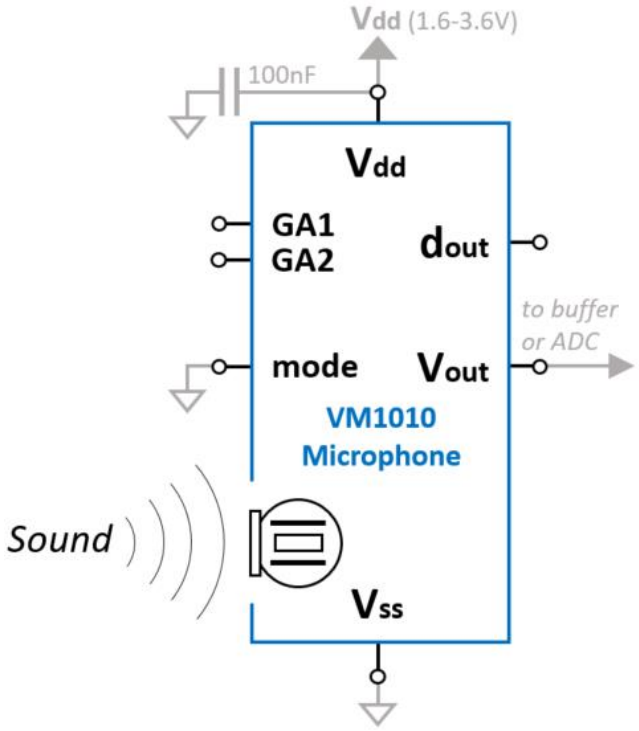


Figure 4: VM1010 Microphone example circuit in Full-Power mode

With the **mode** pin low, the microphone is in Full-Power mode. It can be used like any other single-ended MEMS microphone.

In Full-Power mode, **Vout** is biased at 0.8V. **Vout** swings from 0 to 1.5V at full output. In Wake-on-Sound mode, **Vout** is grounded. It is recommended to DC couple Vout to the input of the ADC or audio processor to avoid any audio artifacts when Vout goes from 0V to 0.8V.

Specification	Typical value	Units
Sensitivity	-38	dBV/Pa
Signal-to-Noise Ratio (20Hz-20kHz)	60.5	dB(A)
Acoustic Overload Point (10% THD)	126	dBSPL
Directivity	Omni	
Supply Voltage	1.6 to 3.6	V
Supply Current	85	µA
Output Impedance	1	kΩ
Output DC Offset	0.8	V

Table 3: Specifications of VM1010 in Normal mode

3.2 Wake-on-Sound Mode

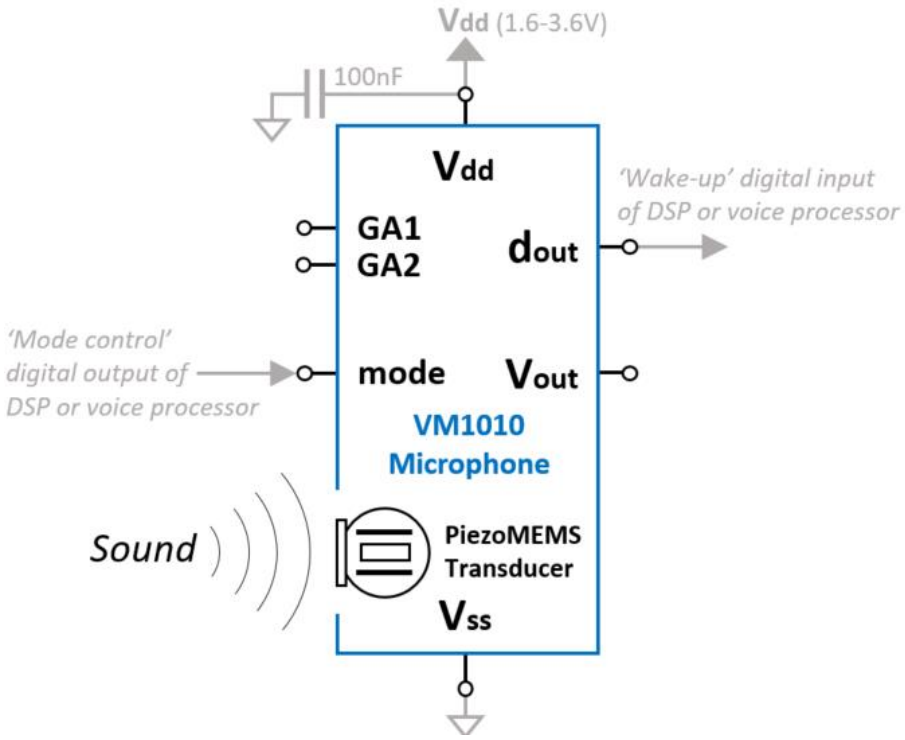


Figure 5: Minimal circuit for VM1010 microphone in Wake-on-Sound mode

With the *mode* pin high, the microphone is in Wake-on-Sound mode.

When first entering WoS mode, the d_{out} pin is set to logic low. If the microphone signal exceeds the WoS threshold, d_{out} latches to logic high.

After latching high, d_{out} remains high until the microphone leaves WoS mode. Hence, the latch can be reset by toggling the *mode* pin to leave and re-enter WoS mode.

Specification	Typical value	Units
Digital logic levels (*mode*, d_{out})	CMOS scaled to Vdd	
Directivity	Omni	
Supply Voltage	1.6 to 3.6	V
Supply Current	10	µA
Default WoS threshold High-Z (open) between *GA1* & *GA2*	89	dBA
WoS minimum threshold 18kΩ between *GA1* & *GA2*	65	dBA
Max load capacitance at *GA1*	5	pF
Max load capacitance at *GA2*	5	pF

Table 4: Specifications of VM1010 in WoS mode

In Wake on Sound mode, the microphone has a bandpass frequency response from 250Hz to 6kHz approximately. This allows the system to detect human voice successfully but reject wind noise, HVAC sounds, and other environmental signals and avoid false positives.

The WoS threshold is controlled by the resistance between pins *GA1* and *GA2*. If these pins are not connected (High-Z), the threshold defaults to 89dBSPL. Chapters 3.2.1 and 3.2.2 show how to adjust this threshold.

3.2.1 Note on Digital Logic Levels and Level Translation

The digital logic level of the VM1010 tracks Vdd where a Logic high is at least 0.65xVdd, and a logic low is a maximum of 0.35xVdd:

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Logic Input High			0.65*VDD		3.6	V
Logic Input Low			-0.3		0.35*VDD	V
Logic Output High		I_{Load} = 0.5mA	0.7*VDD	VDD		V
Logic Output Low		I_{Load} = 0.5mA		0	0.3*VDD	V
Driving Capability					100	pF

Table 5: Digital Electrical Interface specification table

If you wish to use VM1010 at a higher voltage such as 3.3V to be compatible with a DSP or microcontroller running at that digital logic level then there is no major power penalty, Idd remains low for both Wake on Sound mode and Normal Mode:

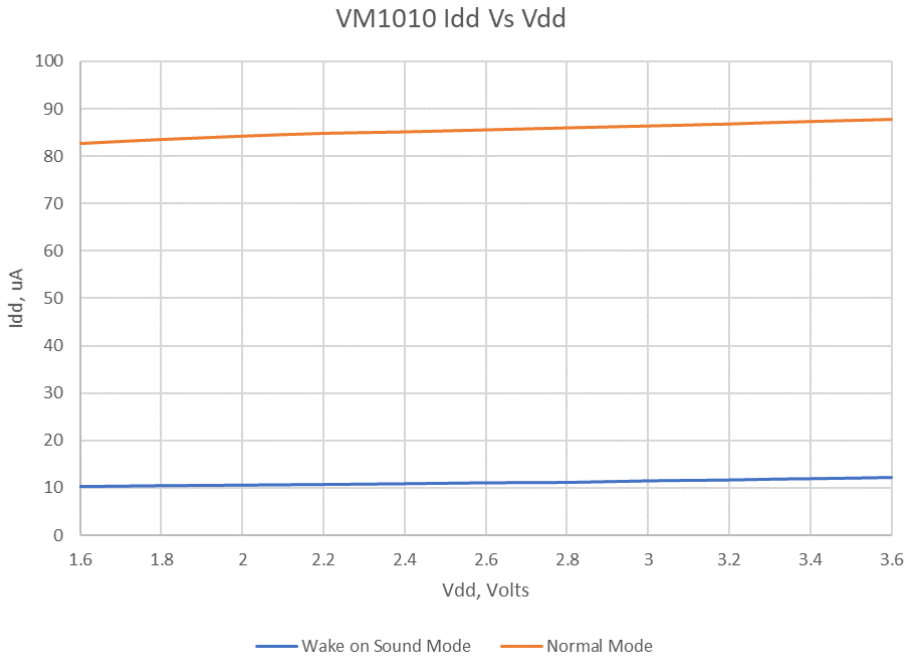


Figure 6: VM1010 Idd Vs Vdd

Correct logic level translation should be only done by using an active logic level translator. A resistor divider circuit to pull up or down voltage will not be a robust solution and may not activate Mode correctly or trigger a system correctly when Dout goes high.

3.2.2 Wake-on-Sound Threshold Configuration

The default WoS threshold is 89dBSPL and can adjusted by connecting a resistor between pins *GA1* and *GA2*. As can be seen in Figure 6, these pins provide access to the feedback network of an instrumentation amplifier in the WoS signal path. Note that the 331 kΩ resistor is internal to the VM1010 ASIC.

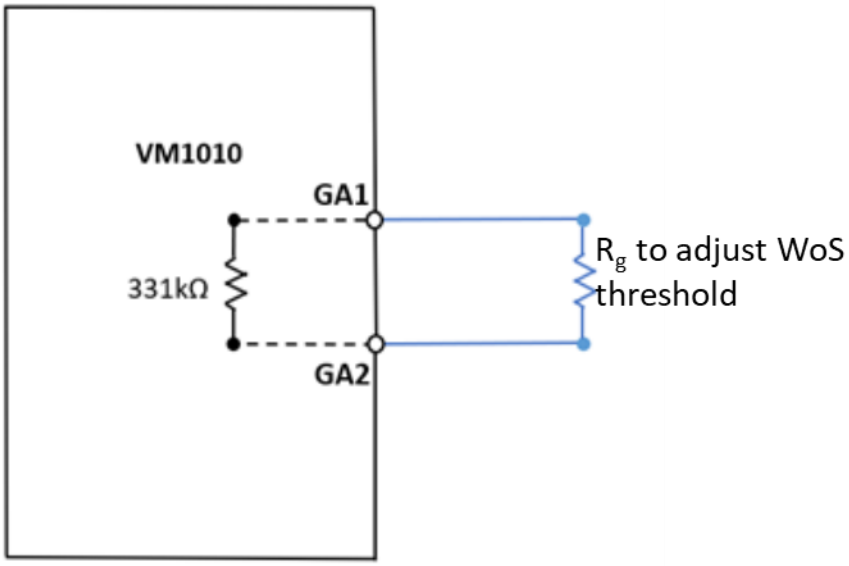


Figure 7: Fixed adjusted WoS threshold, implemented with external resistor (Rg) between GA1 and GA2 pins

The smaller the resistor between *GA1* and *GA2*, the higher the gain of the instrumentation amplifier. The resulting WoS threshold follows this formula:

$$WoS\ threshold = \left[89 - 20 \cdot \log_{10}(1 + \left(\frac{331k\Omega}{Rg}\right))\right] dBSPL$$

This formula holds true to a minimum threshold of 65dBSPL, as shown in Figure 7:

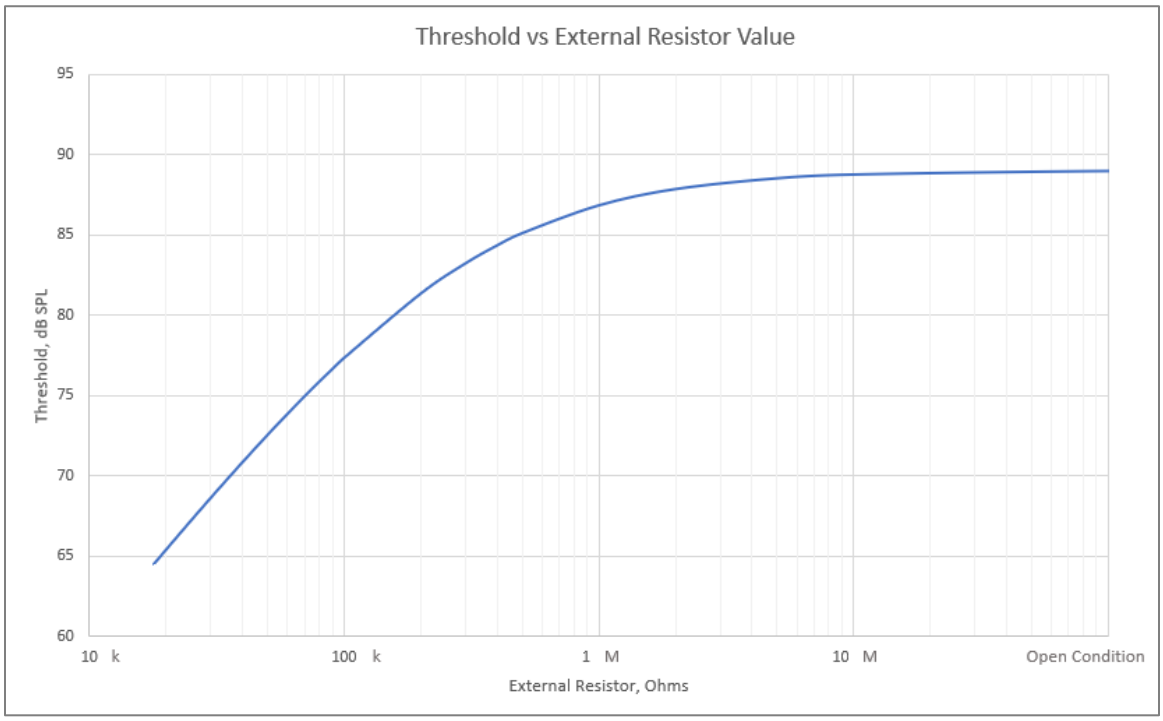


Figure 8: Graph of WoS threshold versus external gain resistor (Rg)

As stated in Table 4, the *GA1* and *GA2* pins can each tolerate a maximum load capacitance of 5pF to GND. Therefore, it is best practice to keep the wires connecting R_g to *GA1* and *GA2* as short as possible.

4 System architecture

4.1 Control Loop for Wake-on-Sound

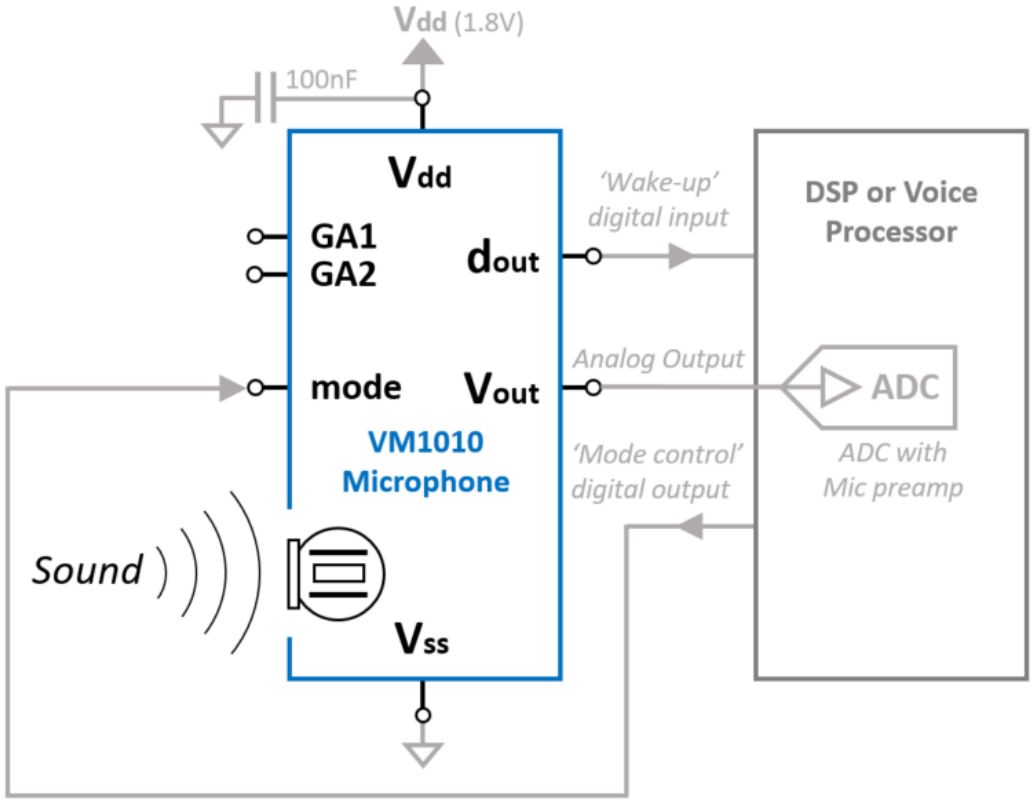
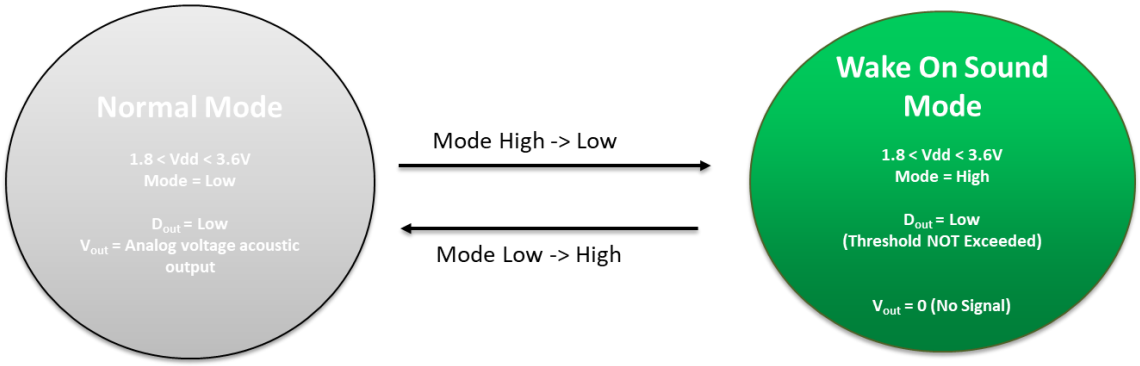


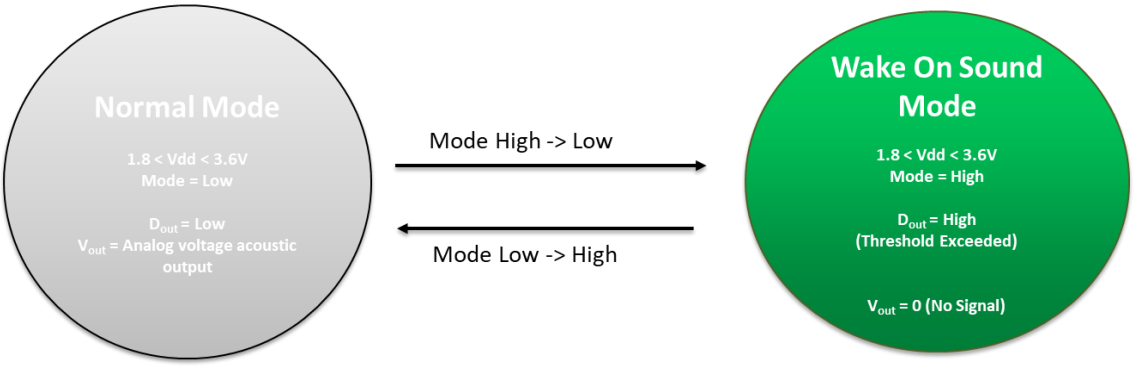
Figure 9: Block diagram of full-featured system built around VM1010 microphone

Figure 8 shows a full-featured system built around the WoS microphone. As the WoS microphone wakes up the system when triggered by sound, the DSP or Voice Processor can be kept in a low-power state when there is no sound to process.

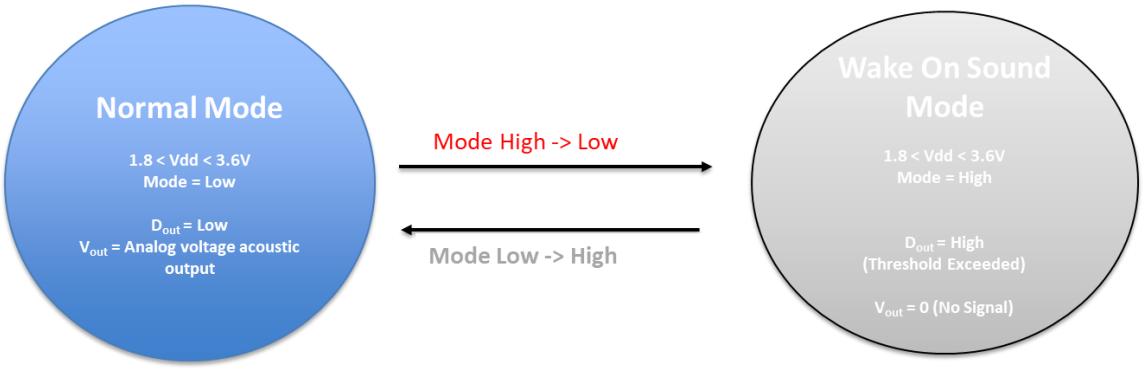
Here is an example control loop which can be built around this system architecture:



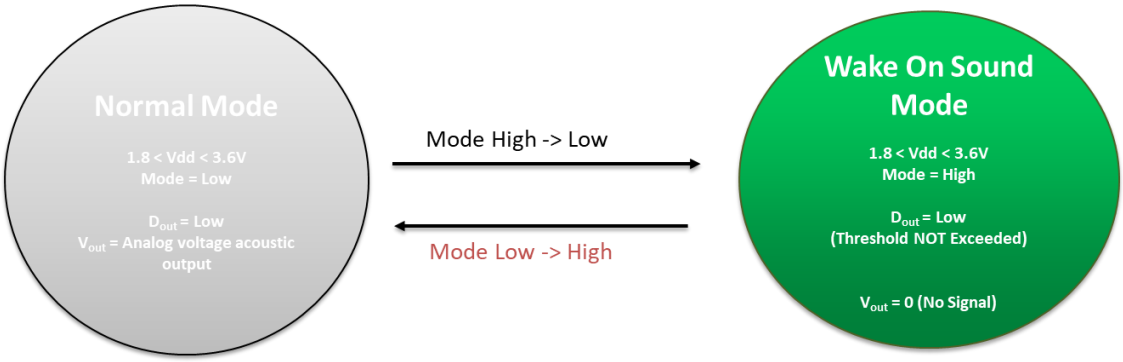
1. Microphone is in WoS mode with *mode* high. Voice Processor is in a low-power state, with d_{out} set up as a hardware interrupt pin.



2. A sound is heard above the threshold, $\mathbf{d_{out}}$ transitions from low-to-high, which wakes up the Voice Processor.



3. The Voice Processor pulls the **mode** pin low to enable Normal mode. **Vout** is enabled and it sends analog audio to the ADC. The Voice Processor captures & analyzes this audio for wake-words and responds appropriately.



4. The Voice Processor continues responding to sounds until the scene is quiet again. Then the Voice Processor sets the **mode** pin high (putting the mic back into WoS mode) and enters a low-power state.

In a quiet scene, the system will spend most of its time in Step 1, where the Voice Processor is in a low-power state and the microphone is only drawing 10µA. In louder scenes, the Voice Processor can place a larger resistor between **GA1** & **GA2** to raise the WoS threshold above the noise floor. Many use-cases do not require all the blocks in this architecture, such as an ADC with built-in mic preamplifier

The VM1010 can be used as an 'acoustic watchdog' next to an array of other microphones

- The other microphones are used for analog capture
- WoS microphone only used for waking from sleep

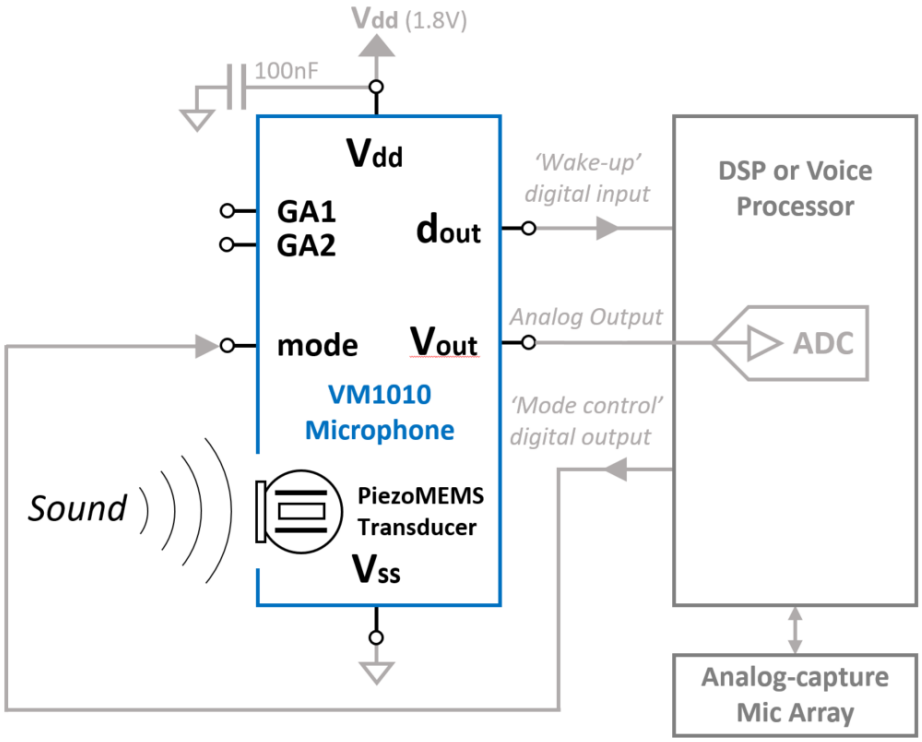


Figure 10: Block diagram of system using VM1010 microphone as 'acoustic watchdog' only

4.2 Vesper Wake on Sound Hardware

Vesper have designed hardware for customers to evaluate Zero Power Listening. There are two types:

- VM1010 Evaluation PCB
- VM1010 Zero Power Listening Development Kit

4.2.1 VM1010 Evaluation Board

The VM1010 Evaluation board provides the basic circuitry needed to evaluate Zero Power Listening. It has a current monitor chip to allow simple validation of current levels and has different solder options for threshold level.

Figure 11: Vesper's VM1010 Zero Power Evaluation Board (VM1010 microphone seen at the center)

4.2.2 VM1010 Zero Power Listening Development Kit

The VM1010 Zero Power Listening Development Kit is a board is built on a DSP Group DBMD6 development platform. It is designed to keep the VM1010 microphone in WoS mode, waiting for an acoustic trigger. Upon triggering, the DBMD6 sets the VM1010 into Normal mode and streams the audio into the processor. The DBMD6 carries out local keyword detect and then can go into a higher performance mode (which in turn can stream audio to the cloud for command processing) or else perform general tasks via the GPIO pins.

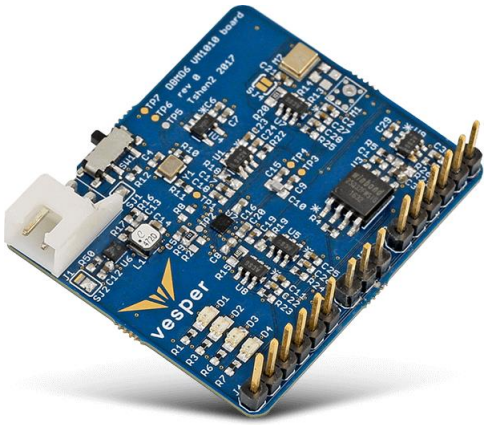


Figure 12: Vesper's VM1010 Zero Power Listening Development board (VM1010 Microphone seen at top right)

5 PCB layout recommendations

PCB footprint for VM1010 is provided in the datasheet. Below are a few recommendations for the layout of the components around the PCB

- The supply bypass cap should be as close to the device as possible to filter out any noise on the supply.
- GA1/GA2 CMOS switch circuit should be as close to the device as possible so there is minimal capacitive loading on the GA pins
- Output impedance of the Vout pin is around 1kohm, it is recommended to limit the cable length to match with this impedance.
- Any buffer or gain stage for Vout is recommended to be in close proximity to the device

6 Supporting hardware for Vesper WoS microphone

6.1 Analog to Digital Converter (ADC)

A 12-bit ADC is recommended to achieve optimum gain at the output of the front-end circuitry. In order to retain the ultra-low power and fast startup advantage of VM1010, ADC with low sleep mode current and fast startup is recommended.

For a DSP or SoC with 1-bit PDM digital interface, On Semi ADC Part number FAN3850D can be used. Key performance metrics of this microphone pre-amplifier with PDM output are given in Table 6 below –

Metric	FAN3850D Microphone pre-amp	VM1010
Gain	16 dB	N/A
Sleep mode current	1.5 µA	10 µA
Wake-up time	350 µsec	< 200 µsec
Supply current	470 µA	85 µA
Supply Voltage Range	1.64 – 3.63 V	1.62-3.6 V
Signal to Noise Ratio	62 dB	60 dB
CLK frequency range	1 – 4 MHZ	N/A

Table 6: FAN3850D Microphone pre-amp key specifications

6.2 Operational Amplifier

In the case of using 10-bit ADC, it is recommended to include an Op amp in the design to provide additional gain. Some of the metrics to consider in selection of an op amp is given below

- ✓ Choose an op amp with Shut down pin: This pin allows to disable the op amp when the VM1010 is in WoS mode.

An op-amp without shutdown pin could be used by connecting Vdd to an additional logic inverter. TI op amp OPA333 included in the spec comparison table above could be used in this case. Note that the bandwidth, turn-on time and noise are higher for OPA333 but provides a lower quiescent current. Therefore, OPA333 could be a good choice for applications where the noise can be traded off for low power. However, it is recommended to use a 12-bit ADC to minimize the impact of op amp noise on the output signal.

A comparison of the key metrics for the two Op amps is given in Table 7 below

Metric	TLV341/342	OPA333
Shut down current	10 pA/channel	N/A
Turn on time from shutdown	0.5 µsec	100 µsec
Supply voltage	1.8 – 5 V	1.8 – 5.5 V
Quiescent current	10 pA	17 µA
Slew rate	0.9 V/µs	0.16 V/µs
Bandwidth	2.3 MHz	350 kHz
Input referred voltage noise	20 nV/√Hz	55 nV/√Hz

Table 7: Op amp comparison

- ✓ Noise contribution of the front-end amplifier must be low enough to prevent degradation in overall system SNR
- ✓ Slew rate and Gain Bandwidth Product (GBP) must be high enough to ensure WoS operation throughout the entire frequency band of interest.

Example of an implementation with TLV341 TI op amp is shown in Figure 13 below.

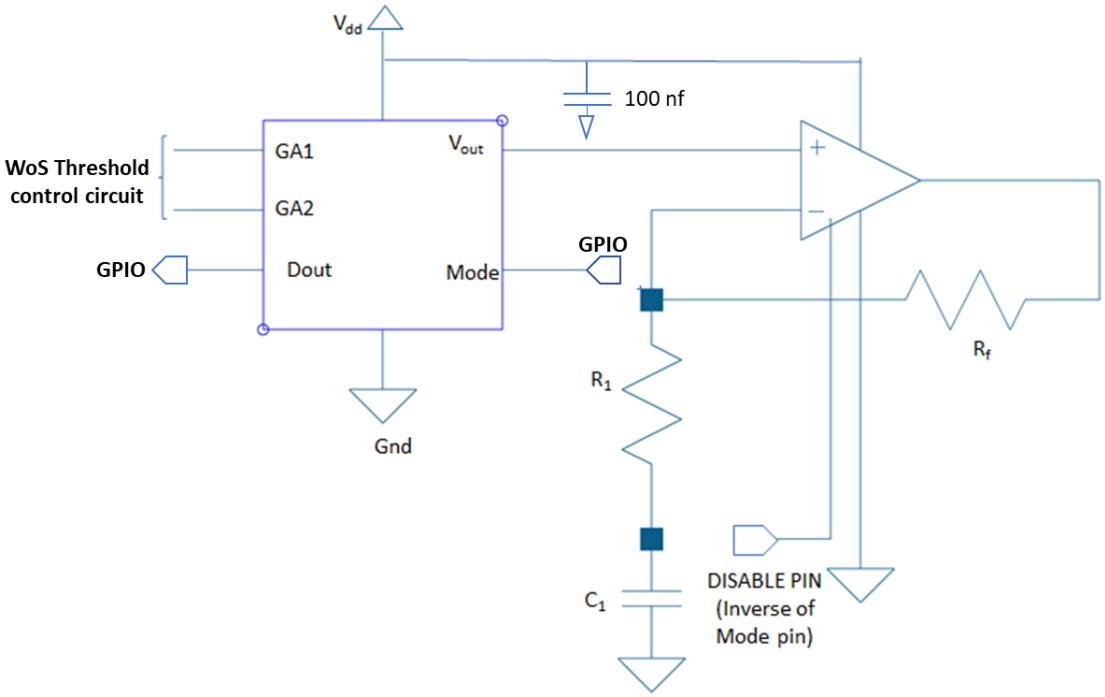


Figure 13: Example implementation of Op-amp circuit with ZPL Microphone

Note that the SHUTDOWN signal on the TLV341 (pin 5) needs to be the inverse of the VM1010's MODE signal. In other words, when MODE is high, SHUTDOWN is low. When MODE is low, SHUTDOWN is high. This can be implemented with a logic inverter IC, or by using an additional GPIO from the processor.

6.3 Voltage Regulator

VM1010 can operate within the voltage range 1.6 – 3.6 V. For devices operating at a voltage rail outside this range, a low quiescent current, Low-Dropout (LDO) regulator can be used to reduce the voltage rail to meet VM1010 rail.

TI TPS7A05 is an example of an ultra-low quiescent current LDO in a small package size with just 1 µA quiescent current.

6.4 Alternate techniques to control WoS Threshold

External resistor at the GA1/GA2 pins is the most simplistic and power optimized technique to control the WOS threshold. However, alternate methods such as Analog switch/resistor combination or digital potentiometer can be used to adjust the WoS threshold automatically, with a little tradeoff of power consumption. These details are provided in the Application Note "AN5 -Dynamic Threshold Adjustment on ZeroPower Listening™".

7 Using VM1010 with Vesper's PDM microphone, VM3000

For voice applications that require multiple microphone arrays, Vesper's digital microphone can be combined with ZPL microphone. This combination allows further power optimization and fast wakeup of the system and provide better wake word detection accuracy for voice wakeup applications. In this case, the CLK pin on VM3000 can be directly driven by the Dout pin on VM1010 to wake up the microphone from sleep mode. Additional details on combining digital microphone with ZPL can be found in AN6 – Using Vesper's VM3000 PDM microphone together with ZPL microphone.

For additional information on Vesper's latest roadmap of microphone products, reach out to info@vespermems.com.

8 Supporting documents

Application Note AN3 – Vesper piezoelectric MEMS microphone Assembly guidelines , https://vespermems.com/resources/

Application Note AN4 – Vesper piezoelectric MEMS microphone Assembly guidelines

Application Note AN5 – Dynamic Threshold adjustment on ZeroPower Listening Microphone

Application Note AN6 – Using Vesper's VM3000 PDM microphone together with ZPL microphone

On-Semi FAN3850D Microphone pre-amplifier with Digital output datasheet, https://www.onsemi.com/products/audio-video-assp/audio-assp/fan3852

Texas Instruments (TI) TLV341 CMOS Op amp datasheet, http://www.ti.com/product/TLV341

TI OPA333 Op-amp datasheet, http://www.ti.com/lit/ds/symlink/opa333.pdf

TI TPS7A05 Low-dropout (LDO) Regulator datasheet, http://www.ti.com/product/TPS7A05

9 Revision History

Version	Date	Comments
Rev1.0	Nov 2018	Initial version
Rev2.0	Sep 2019	Added sections 5 through 9 with information on system implementation of VM1010