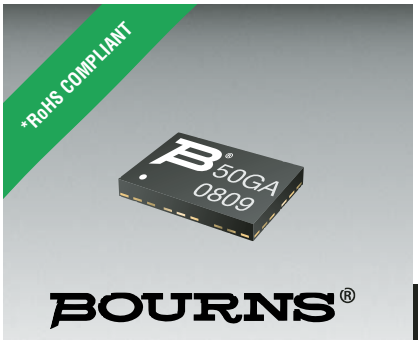


Features

- Formerly FulTec brand
- Extremely high speed performance
- Blocks high voltages and currents
- Two TBU™ protectors in one small package
- Simple, superior circuit protection
- Minimal PCB area
- RoHS compliant*, UL Recognized

Applications

- POTS linecards
- VoIP equipment
- Voice and data combo linecards
- ONU, ONT
- Gateways
- Cable and DSL modems

TBU™ P500-G and P850-G Protectors

Transient Blocking Units - TBU™ Devices

Bourns® Model P500-G and P850-G TBU™ products are high speed, surge protection components designed to protect Subscriber Line Interface Circuits (SLICs) against transients caused by AC power cross, induction and lightning surges.

The TBU™ device blocks surges and provides an effective barrier behind which sensitive electronics are not exposed to large voltages or currents during surge events.

Agency Approval

UL recognized component File # E315805.

Industry Standards

Description			Model
Telcordia	GR-1089	Port Type 2, 4	P500-G
		Port Type 3, 5	P850-G
ITU-T	K.20, K.20E, K.21, K.21E, K.45		P850-G

Absolute Maximum Ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{imp}	Maximum protection voltage for impulse faults with rise time ≥ 1 µsec	P500-Gxxx-WH P850-Gxxx-WH	500 850	V
V_{rms}	Maximum protection voltage for continuous V_{rms} faults	P500-Gxxx-WH P850-Gxxx-WH	300 425	V
T_{op}	Operating temperature range		-40 to +85	°C
T_{stg}	Storage temperature range		-65 to +150	°C

Electrical Characteristics (T_{amb} = 25 °C)

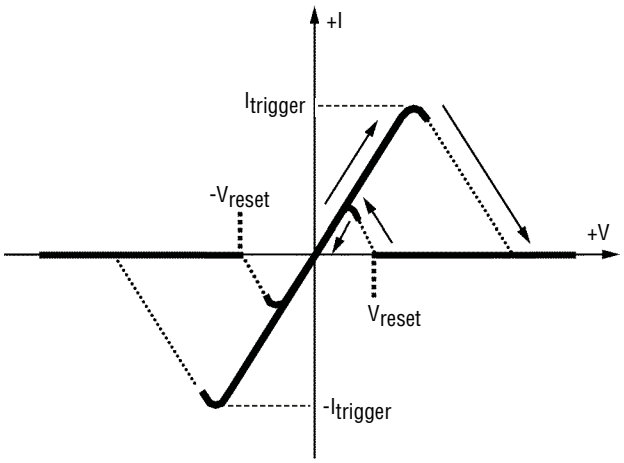
Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{op}	Maximum current through the device that will not cause current blocking	P500-G120-WH P500-G200-WH P850-G120-WH P850-G200-WH			100 200 100 200	mA
$I_{trigger}$	Typical current for the device to go from normal operating state to protected state	P500-G120-WH P500-G200-WH P850-G120-WH P850-G200-WH		150 275 150 275		mA
I_{out}	Maximum current through the device	P500-G120-WH P500-G200-WH P850-G120-WH P850-G200-WH			200 400 200 400	mA
R_{TBU}	Series resistance of the TBU™ device			50	55	Ω
R_{bal}	Line-to line series resistance difference between two TBU™ devices				2	Ω
t_{block}	Maximum time for the device to go from normal operating state to protected state				1	µs
$I_{quiescent}$	Current through the triggered TBU™ device with 50 Vdc circuit voltage			0.7		mA
V_{reset}	Voltage below which the triggered TBU™ device will transition to normal operating state			22		V

The P-G series TBU™ devices are bidirectional; specifications are valid in both directions.

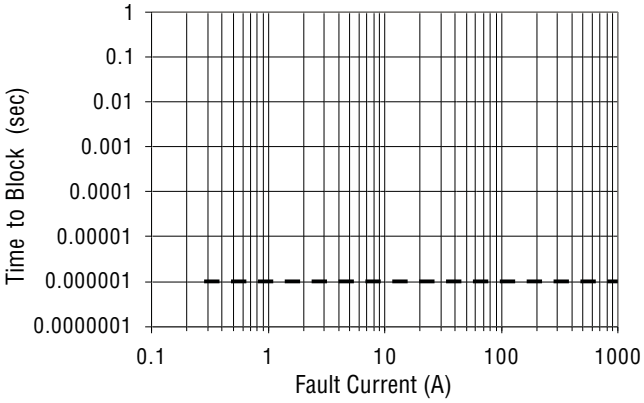
*RoHS Directive 2002/95/EC Jan 27 2003 including Annex.
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications

Typical Performance Characteristics

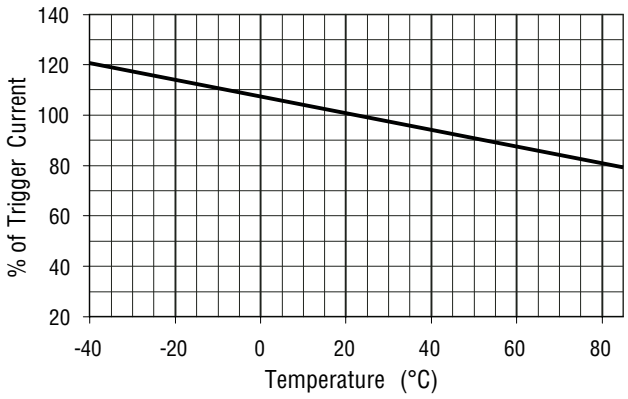
V-I Characteristics



Time to Block vs. Fault Current



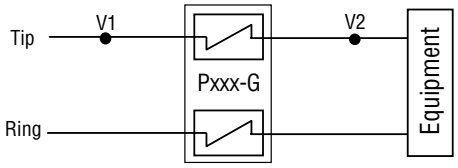
Trigger Current Temperature



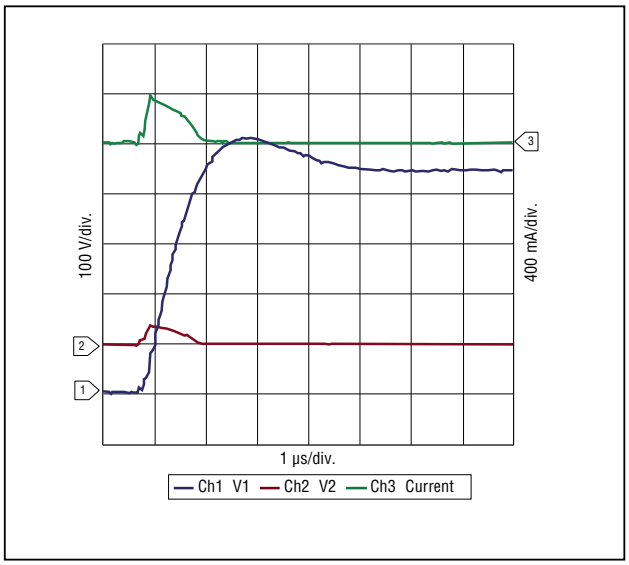
Operational Characteristics

The graphs below demonstrate the operational characteristics of the TBU™ device. For each graph the fault voltage, protected side voltage, and current is presented.

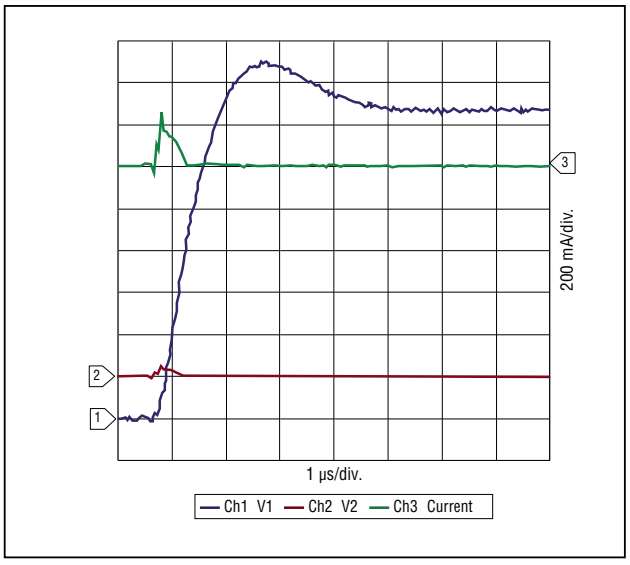
TEST CONFIGURATION DIAGRAM



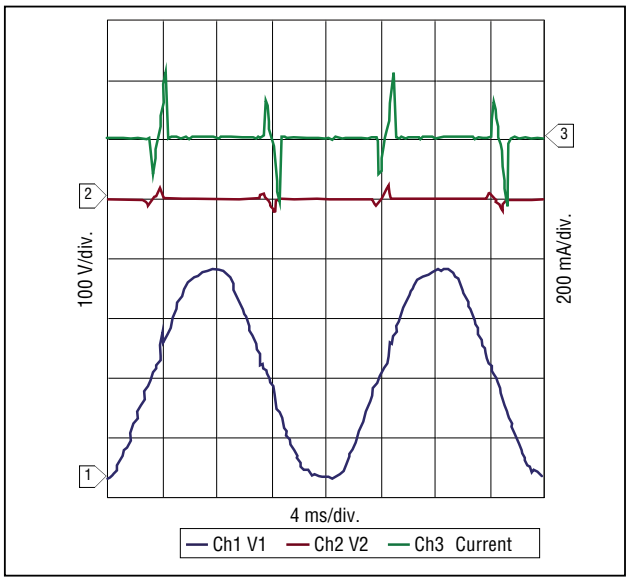
P500-G Lightning, 500 V



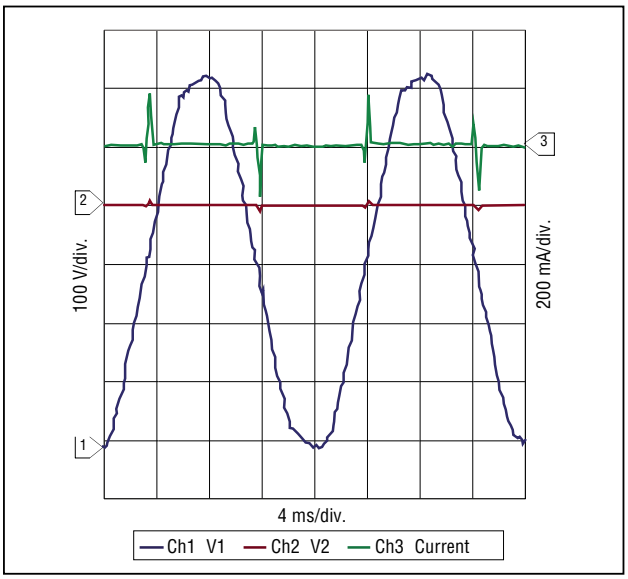
P850-G Lightning, 850 V



P500-G Power Fault, 120 Vrms, 25 A

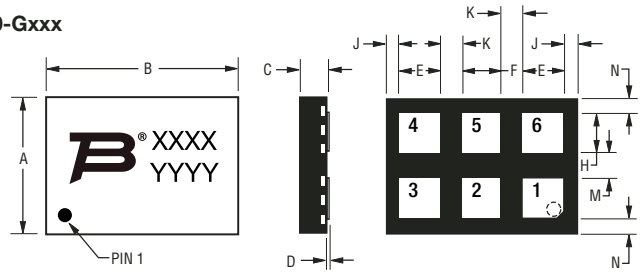


P850-G Power Fault, 230 Vrms, 25 A



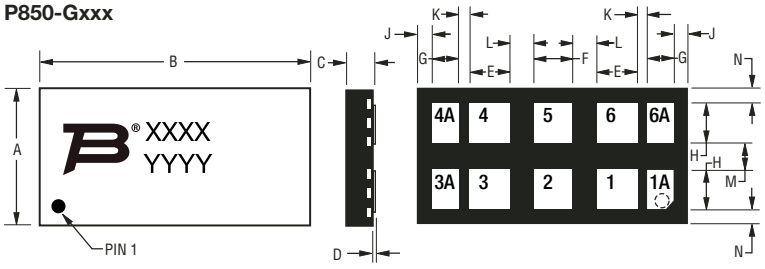
Product Dimensions

P500-Gxxx



TOP VIEW SIDE VIEW BOTTOM VIEW

P850-Gxxx



TOP VIEW SIDE VIEW BOTTOM VIEW

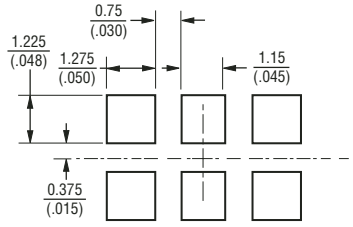
Pads 1A and 1 are internally connected; the same for pads 3A with 3, 4A with 4, and 6A with 6. This allows for one PCB layout to accommodate the P500 or P850.

Dim.	P500-G			P850-G		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.40 (.139)	4.00 (.157)	4.10 (.161)	3.40 (.139)	4.00 (.157)	4.10 (.161)
B	5.90 (.232)	6.00 (.236)	6.10 (.240)	8.15 (.321)	8.25 (.325)	8.35 (.329)
C	0.80 (.031)	0.85 (.033)	0.90 (.035)	0.80 (.031)	0.85 (.033)	0.90 (.035)
D	0.000 (.000)	0.025 (.001)	0.050 (.002)	0.000 (.000)	0.025 (.001)	0.050 (.002)
E	1.15 (.045)	1.25 (.049)	1.35 (.053)	1.15 (.045)	1.25 (.049)	1.35 (.053)
F	1.05 (.041)	1.15 (.045)	1.25 (.049)	1.05 (.041)	1.15 (.045)	1.25 (.049)
G	--	--	--	0.725 (.029)	0.825 (.032)	0.925 (.036)
H	1.10 (.043)	1.20 (.047)	1.30 (.051)	1.10 (.043)	1.20 (.047)	1.30 (.051)
J	0.375 (.015)	0.425 (.017)	0.475 (.019)	0.375 (.015)	0.425 (.017)	0.475 (.019)
K	0.70 (.028)	0.75 (.030)	0.80 (.031)	0.25 (.010)	0.30 (.012)	0.35 (.014)
L	--	--	--	0.70 (.028)	0.75 (.030)	0.80 (.031)
M	0.70 (.028)	0.75 (.030)	0.80 (.031)	0.70 (.028)	0.75 (.030)	0.80 (.031)
N	0.375 (.015)	0.425 (.017)	0.475 (.018)	0.375 (.015)	0.425 (.017)	0.475 (.018)

DIMENSIONS: MM (INCHES)

Recommended Pad Layout

P500-Gxxx

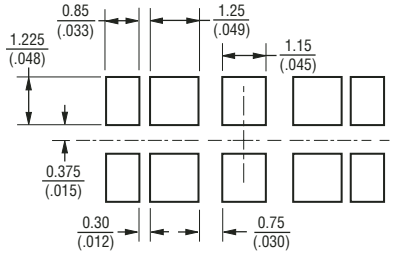


Pad Designation

Pad #	Apply
1	Tip In
2	NC
3	Tip Out
4	Ring Out
5	NC
6	Ring In

NC = Solder to PCB; do not make electrical connection, do not connect to ground.

P850-Gxxx



Pad Designation

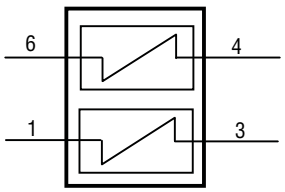
Pad #	Apply	Pad #	Apply
1A	Tip In	4A	Ring Out
1	Tip In	4	Ring Out
2	NC	5	NC
3	Tip Out	6	Ring In
3A	Tip Out	6A	Ring In

NC = Solder to PCB; do not make electrical connection, do not connect to ground.

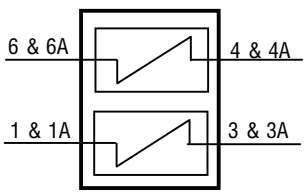
TBU™ devices have matte-tin termination finish. Suggested layout should use non-solder mask define (NSMD). Recommended stencil thickness is 0.10-0.12 mm (.004-.005 in.) with stencil opening size 0.025 mm (.0010 in.) less than the device pad size. As when heat sinking any power device, it is recommended that, wherever possible, extra PCB copper area is allowed. For minimum parasitic capacitance, do not allow any signal, ground or power signals beneath any of the pads of the device.

Block Diagram

P500-Gxxx



P850-Gxxx

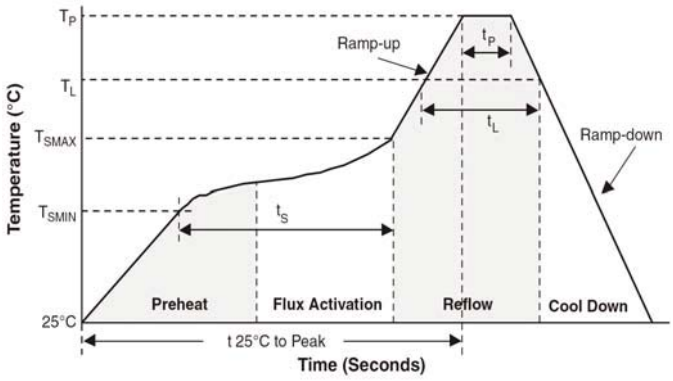


Thermal Resistances

Part #	Symbol	Parameter	Value	Unit
P500-G	$R_{th(j-a)}$	Junction to leads (package)	113	°C/W
		Junction to leads (per TBU™ device)	236	°C/W
P850-G	$R_{th(j-a)}$	Junction to leads (package)	119	°C/W
		Junction to leads (per TBU™ device)	215	°C/W

Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Tsmax to Tp)	3 °C/sec. max.
Preheat - Temperature Min. (Tsmin) - Temperature Max. (Tsmax) - Time (tsmin to tsmax)	 150 °C 200 °C 60-180 sec.
Time maintained above: - Temperature (TL) - Time (tL)	 217 °C 60-150 sec.
Peak/Classification Temperature (Tp)	260 °C
Time within 5 °C of Actual Peak Temp. (tp)	20-40 sec.
Ramp-Down Rate	6 °C/sec. max.
Time 25 °C to Peak Temperature	8 min. max.



TBU™ P500-G and P850-G Protectors

BOURNS®

How to Order

P 500 - G 120 - WH

Form Factor
P = Two TBU™ protectors in one device

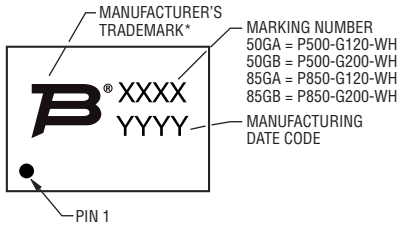
Impulse Voltage Rating
500 = 500 V
850 = 850 V

Directional Indication for Paired Devices
G = Bidirectional

Iop Indicator
120 = 100 mA
200 = 200 mA

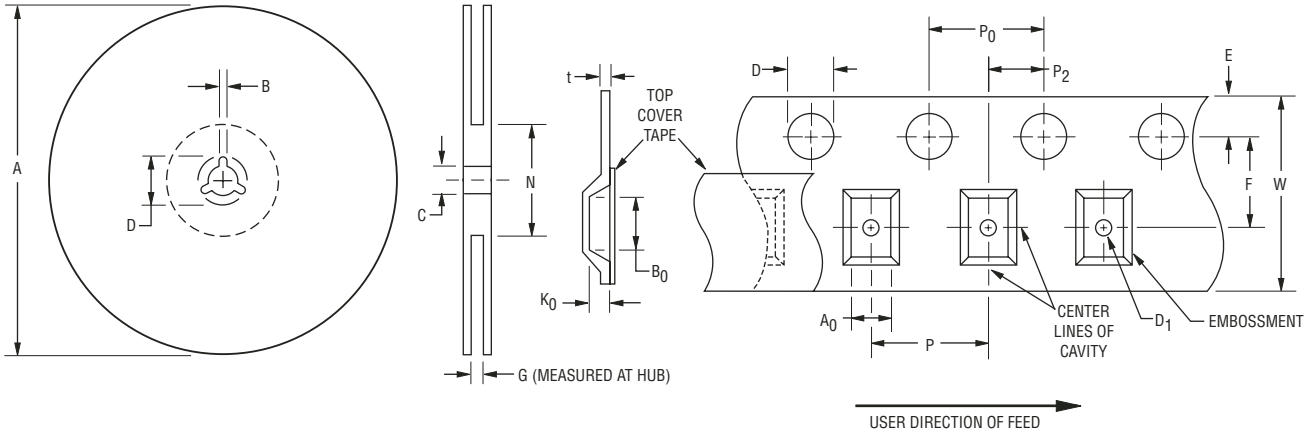
Packaging Indicator
Blank = Packaged in tape and reel (3000 pieces per reel)
X = Packaged in tubes

Typical Part Marking



*TRANSITION FROM FULTEC TRADEMARK TO BOURNS TRADEMARK IN 2009.

Packaging Specifications (per EIA468-B)



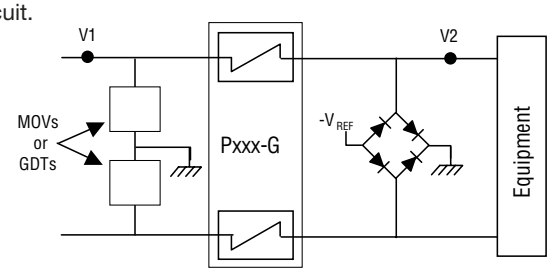
Device	A		B		C		D		G	N
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Ref.	Ref.
P500-G, P850-G	326 (12.835)	330.25 (13.002)	1.5 (.059)	2.5 (.098)	12.8 (.504)	13.5 (.531)	20.2 (.795)	-	16.5 (.650)	102 (4.016)

Device	A_0		B_0		D		D_1		E		F	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	max.
P500-G	4.2 (.165)	4.4 (.173)	6.2 (.244)	6.4 (.252)	1.5 (.059)	1.6 (.063)	1.5 (.059)	-	1.65 (.065)	1.85 (.073)	5.4 (.213)	5.6 (.220)
P850-G	4.2 (.165)	4.4 (.173)	8.45 (.333)	8.65 (.341)	1.5 (.059)	1.6 (.063)	1.5 (.059)	-	1.65 (.065)	1.85 (.073)	7.4 (.291)	7.6 (.299)
Device	**K_0**		**P**		**P_0**		**P_2**		**t**		**W**	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
P500-G	1.0 (.039)	1.2 (.047)	7.9 (.311)	8.1 (.319)	3.9 (.159)	4.1 (.161)	1.9 (.075)	2.1 (.083)	0.25 (.010)	0.35 (.014)	11.7 (.461)	12.3 (.484)
P850-G	1.1 (.043)	1.3 (.051)	7.9 (.311)	8.1 (.319)	3.9 (.159)	4.1 (.161)	1.9 (.075)	2.1 (.083)	0.25 (.010)	0.35 (.014)	15.7 (.618)	16.3 (.642)

DIMENSIONS: MM (INCHES)

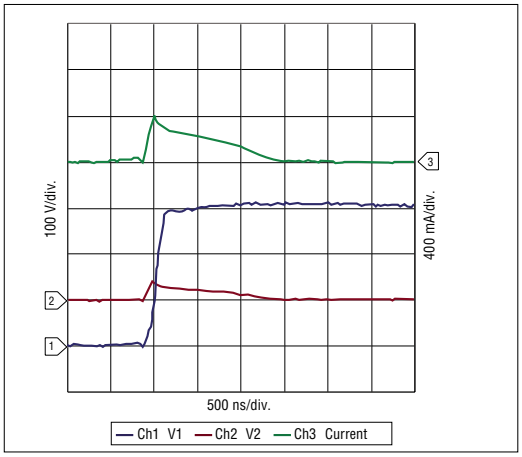
Reference Designs

A cost-effective protection solution combines the Bourns® TBU™ protection device with a pair of MOVs or Bourns® GDTs and a diode bridge. The diagram below illustrates a common configuration of these components. The graphs to the right demonstrate the operational characteristics of the circuit.



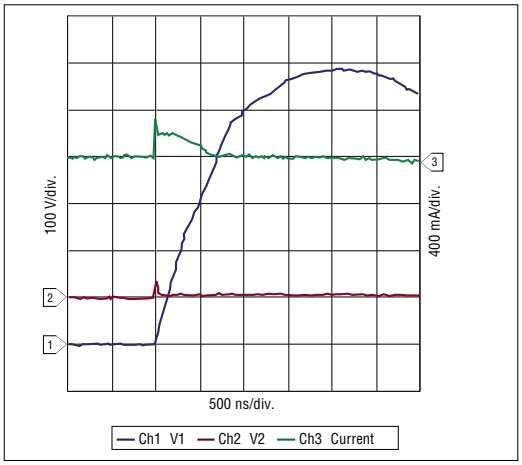
Common Configuration Diagram

P500-G Configuration (GR-1089 Intra-building and 5 kV Lightning)			
Product	**Qty.**	**Part Number**	**Source**
TBU™ Device	1	P500-Gxxx-WH	Bourns, Inc.
MOV	2	CNR-10D201K GNR10D201K	CNR Centra Science Ceramate Technical
Diode bridge	2	GSD2004S-V MMBD2004S	Vishay Diodes Inc.



P500-G Solution: 5000 V Lightning 2/10 µsec, 500 A

P850-G Configuration (ITU-T K.20, K.21, K.20E, K.21E, K.45)			
Product	**Qty.**	**Part Number**	**Source**
TBU™ Device	1	P850-G120-WH	Bourns, Inc.
MOV	2	CNR-10D361K GNR10D361K	CNR Centra Science Ceramate Technical
Diode bridge	2	GSD2004S-V MMBD2004S	Vishay Diodes Inc.



P850-G Solution: 4000 V Lightning 10/700 µsec, 100 A

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