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S1R72U16
Technical Manual

SEIKO EPSON CORPORATION

Rev.2.00

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Scope

This document applies to the S1R72U16 IDE device - USB 2.0 host bridge LSI.

Notice

Before using the S1R72U16, carefully read the sections “Special use case for S1R72U16” and “S1R72U16 Errata.”

Table of Contents

1. Terminology

Main CPU	The main CPU of the user's system.
FS	Full-speed mode in the USB standard. Theoretical maximum transfer rate is 12 Mbps.
HS	High-speed mode in the USB standard. Theoretical maximum transfer rate is 480 Mbps.
Mass Storage Class	Mass storage class in the USB standard
Hub Class	Hub class in the USB standard
Bulk Only Transport	Protocol for issuing storage commands using bulk transfer only as stipulated for mass storage class
CBI Transport	Protocol for issuing storage commands using control, bulk, or interrupt transfer as stipulated for mass storage class
Embedded Host Compliance	USB 2.0 logo certification for embedded hosts
TPL	Target peripheral list
LUN	Logical unit number
NSF	No silent failures
SUSPEND	USB device sleep state
RESUME	USB device wakeup
Port reset	Resetting the port to which the storage device is connected
Mass storage reset	Resetting of the storage device
CBW	Command block wrapper
CSW	Command status wrapper

2. Functions

This LSI is an IDE device - USB 2.0 host bridge that features three different mode settings for command system, number of connected devices, and interface, to suit specific systems. For detailed information on individual modes, see “2.1 Mode Settings”.

The device complies with the following standards in IDE mode.

- AT Attachment with Packet Interface - 4, 5, 6 (ATA/ATAPI - 4, 5, 6)
- Multi-Media Commands - 5 (MMC - 5) [CD/DVD support]
- INF - 8070i, 8090i [MO support]
- SFF - 8080 [CD support]
- Information technology - SCSI/ATA Translation (SAT) [16 byte command is unsupported]

CF+ and Compact Flash Specification Revision 3.0 I/O mode can be applied in CPU mode. However, this LSI has no CIS/CCR registers or attribute memory and does not meet CF standards.

2.1 Mode Settings

The LSI operating mode is set by the pins shown in Table 2.1.

Do not change the setting pins after switching on the power.

Table 2.1 Mode setting list

Type	Pin	Pin setting and mode	
Command system	PORT00(ATAxATAPI)	High: ATA mode	Low: ATAPI mode
Device count	PORT01(2x1)	High: two-device mode	Low: one-device mode
Interface	PORT02(CPUxIDE)	High: CPU mode	Low: IDE mode

2.1.1 Command System Setting

This specifies the command system for the main CPU controlling this LSI. Set to the mode corresponding to the driver installed in the main CPU. See “2.7.2 Supported Command List” for detailed information on commands available in each mode.

Optical disk devices like CD, DVD, and MO drives cannot be controlled in ATA mode and will be ignored if connected. Specify ATAPI mode to use optical disk devices.

The master and slave will use the same command system if the device count setting specifies two-device mode.

2.1.2 Device Count Setting

This specifies the number of storage devices connected to the main CPU via this LSI. Set to two-device mode when controlling two devices (master snd slave) using the LSI. Set to one-device mode when controlling a single device; in this case, the CSEL signal shall be used as defined in the IDE standard.

The CSEL pin on this LSI should be set to “Master (=Low)” in two-device mode.

2.1.3 Interface Setting

This specifies the connection interface between the main CPU and this LSI. Set to IDE mode when connecting the LSI to the main CPU IDE bus; set to CPU mode when connecting to the CPU bus.

IDE mode enables use of PIO, Multi Word DMA, and Ultra DMA. PIO supports modes 0 to 4 (16.6 MB/s); Multi Word DMA supports modes 0 to 2 (16.6 MB/s); and Ultra DMA supports 0 to 5 (100 MB/s).

CPU mode enables use of PIO and DMA.

2.2 Internal Status Notification

The GPO pins indicates the LSI's internal status. The main CPU can receive the LSI's internal status by using these.

The PLL_Locked pin (port 13) indicates the LSI has started up without problems. It indicates “High” once the PLL begins oscillating when power is turned on and remains at “High” until power is turned off.

The connection pins (ports 10 to 12) indicate storage device connection/disconnection status and changes. For detailed information on connect and disconnect operations, see “2.7.6 Connection/Disconnection Specifications”.

For detailed information on the NSF notification pins (ports 14 to 17) used for USB logo certification, see “2.8.5 NSF”.

2.3 USB Device Connection Configuration

An overview of storage device connections is given below. For detailed information on supported USB devices, see “2.8 USB Function Specifications”.

Up to two storage devices can be connected. The third or subsequent storage devices connected will be ignored. The first of the two storage devices detected will be assigned as a master device; the second storage device detected will be assigned as a slave device.

Up to three USB hubs can be connected. Any additional USB hubs or storage devices connected to such additional USB hubs will be ignored.

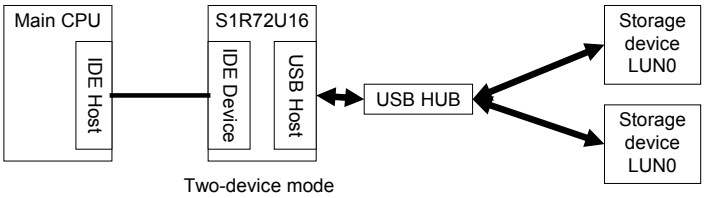


Fig. 2.1 Basic configuration

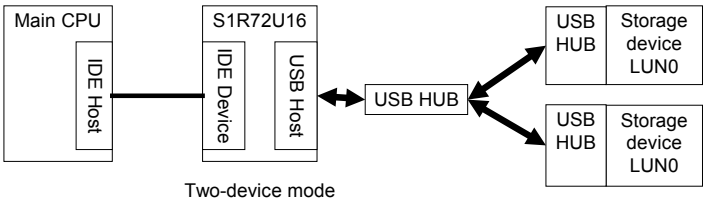


Fig. 2.2 Maximum configuration (for USB memory including hub function)

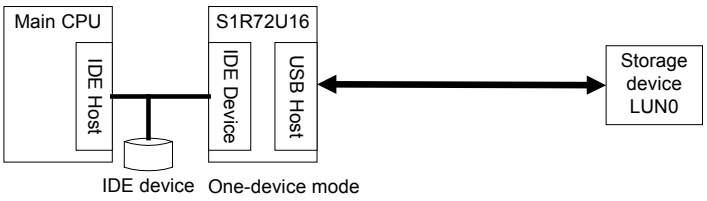


Fig. 2.3 Minimum configuration

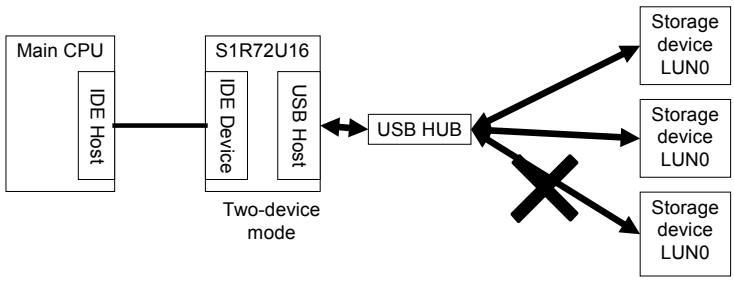


Fig. 2.4 Configuration exceeding device limits (storage devices)

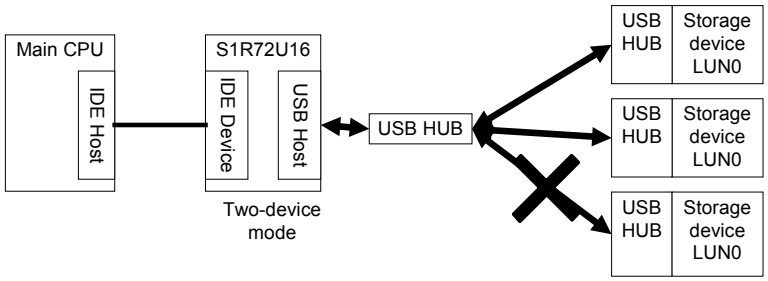


Fig. 2.5 Configuration exceeding device limits (USB hub)

2.3.1 LUN Treatment

One LUN is detected as a single storage device. If a single storage device partitioned into LUN0 and LUN1 will be detected as two storage devices, no additional storage devices will be detected due to the limit of two storage devices.

Figures 2.6 to 2.8 show the connection examples.

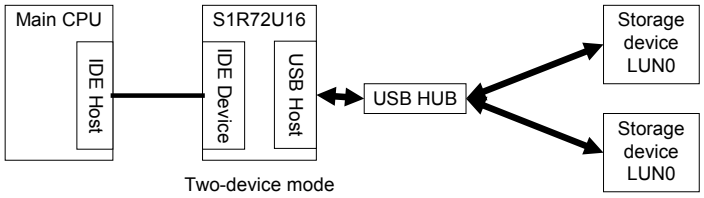


Fig. 2.6 LUN treatment in basic configuration

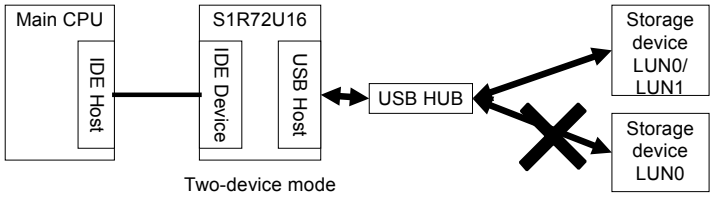


Fig. 2.7 One storage device divided into two LUNs

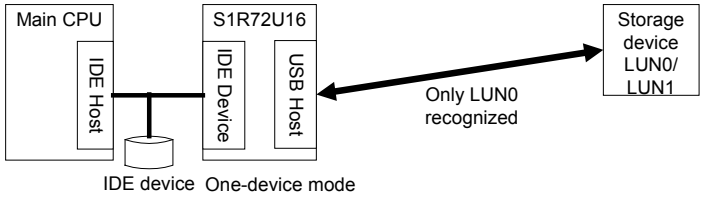


Fig. 2.8 LUN treatment in one-device mode

2.4 Operation Specifications for Resetting

This LSI supports ATA/ATAPI standard resetting (Hardware Reset, SRST, and DEVICE RESET command) and resets USB devices if the conditions described below are met. This means the main CPU has access to ATA/ATAPI resetting without considering USB standard resetting operations.

As reference, Table 2.2 shows the correspondence between ATA/ATAPI and USB standard resetting. And conditions for issuing USB standard resetting.

Table 2.2 Correspondence between ATA/ATAPI and USB standard resetting

ATA/ATAPI standard reset	USB standard reset	USB standard reset issuing conditions (issue if any are satisfied) (*2)
Hardware Reset	Port reset (bus initialization) (*1)	• Command is being executed (Status register BSY bit or DRQ bit is 1). • During the interval between return of error status to the main CPU after the occurrence of an error in USB protocol and reception of subsequent command. • During the interval between return of error status to the main CPU when no response is received from the USB device and reception of subsequent command. • Storage device is not connected.
SRST	Mass storage reset (individual device initialization)	• Command is being executed (Status register BSY bit or DRQ bit is 1). • During the interval between return of error status to the main CPU after the occurrence of an error in USB protocol and reception of subsequent command. • During the interval between return of error status to the main CPU when no response is received from the USB device and reception of subsequent command.
DEVICE RESET command (ATAPI mode only)		

*1 Since the port reset cause the USB devices disconnect temporarily, master and slave assignments for storage devices may change when a Hardware Reset is executed with multiple connected storage devices.

*2 When the storage device is normal state and the command is not executed, then the reset is not issued.

For detailed information on USB protocol errors, see “2.7.5.3 When Controlling a Storage Device”.

The LSI status is as shown below after resetting. The status after a Hardware Reset is the same as after power on. After a SRST or DEVICE RESET command, the data set by the main CPU is retained.

- All resets
  - Functions set by the DOWNLOAD MICROCODE command are retained.
  - The XCD0/XCD1 pins retain the status existing before resetting.
  - Sleep is reset (complies with ATA/ATAPI standard).
- Hardware Reset
  - Initializes XChgInt pin and sets to High.
  - Initializes data set by commands from main CPU (complies with ATA/ATAPI standard).

- SRST/DEVICE RESET command
  - ➢ XChgInt pin retains status existing before resetting.
  - ➢ Retains data set by commands from main CPU (complies with ATA/ATAPI standard).

2.5 Commands Issued Independently to Storage Devices

This LSI issues commands independently to storage devices under certain conditions, regardless of main CPU command issuing. The main CPU need not be aware of this command issuing.

2.5.1 Commands Issued to Obtain Storage Device Information

The LSI issues the commands shown in Table 2.3 to obtain storage device information when conditions detected indicate that the storage device may have been changed.

Table 2.3 Commands for obtaining storage device information

Command	Issuing conditions
INQUIRY	• When Hardware Reset, SRST, or DEVICE RESET command is detected (e.g., when power is turned on) • When storage device connection is detected • When an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command is detected

2.5.2 Commands Issued to Obtain Media Information

The LSI issues the commands shown in Table 2.4 in sequence to obtain media information in the following situations in which the storage device or media may have been changed and the issuing conditions are also satisfied.

- After detecting Hardware Reset, SRST, or DEVICE RESET command (e.g., when power is turned on)
- After detecting storage device connection
- After detecting a media change error from a storage device

Table 2.4 Commands obtaining media information

Command	Issuing conditions
TEST UNIT READY	When any of the following commands is received first under the conditions described above • When a command other than INQUIRY or REQUEST SENSE is received in ATAPI mode • When a command (command returning MC or NM error) is received to access the media in ATA mode
READ DISC STRUCTURE	When the TEST UNIT READY command above ends normally * Issued only in ATAPI mode when the storage device is a CD or DVD
READ CAPACITY	• When the READ DISC STUCTURE command above is issued and ends normally • When the READ DISC STUCTURE command above is not issued and the TEST UNIT READY command ends normally

* READ CAPACITY is issued before READ DISC STRUCTURE, when media change was notified from the storage device by TEST UNIT READY. (It was added in S1R72U16XXXE200.)

2.6 Power Management

The main CPU can manage USB device power via procedures that comply with the ATA/ATAPI standard. This section describes power-conservation functions (SUSPEND/RESUME) for the LSI and connected storage devices.

2.6.1 USB Device SUSPEND/RESUME

The main CPU can switch storage devices to power-conservation mode using the SLEEP command and resume by resetting. No special processing is needed at the main CPU other than the ATA/ATAPI standard.

This LSI switches USB devices to SUSPEND state on receiving a SLEEP command. In two-device mode, all USB devices switch to SUSPEND when a SLEEP command for both master and slave is received.

The LSI switches all USB devices to RESUME on receiving any of the reset commands described in "2.6.2 Sleep/Wakeup". In two-device mode, the DEVICE RESET command switches all USB devices to RESUME when a command for either a master or slave is received.

* The LSI switches all USB devices to RESUME on receiving a single DEVICE RESET command. Individual DEVICE RESET commands should be issued for storage devices (master/slave) controlled initially.

2.6.2 Sleep/Wakeup

The LSI automatically switches to Sleep state when all storage devices detected are in SUSPEND state. In two-device mode, the LSI does not switch to Sleep state unless SLEEP commands are issued for both the master and slave, even if only one storage device is actually present.

The LSI switches to Wakeup when any of the following resets are detected in Sleep state. No special processing is needed by the main CPU to switch the LSI to Sleep or Wakeup states.

- Hardware Reset
- SRST
- DEVICE RESET command (command results in an error in ATA mode)

2.6.3 Storage Devices that do not Support RESUME

Some storage devices do not support RESUME and may operate as shown below after the RESUME command.

- No response to issued command.
- Receives command but subsequently continues to return NAK.

If the storage device does not respond to the command issued, the LSI indicates that the storage device is not connected to the main CPU. If the storage device issues an NAK response, the reset described in "2.6.2 Sleep/Wakeup" will not terminate and persists in a Busy state (Status register BSY bit is 1).

Under these conditions, the main CPU should issue a Hardware Reset. The LSI initializes and reconnects the storage devices.

2.7 IDE Function Specifications

The main CPU is capable of controlling the LSI and storage devices connected to the LSI as devices complying with the ATA/ATAPI standard. This section describes detailed information on the ATA/ATAPI commands supported by the LSI, data returned to the main CPU, and connection/disconnection methods.

Observe the following precautions when using the LSI.

- Use ATAPI mode when controlling optical disk devices like CD, DVD, and MO drives.
- Set the CSEL pin to Master (= Low) when using the LSI in two-device mode.
- The maximum data size that can be transferred with a single command is 800000h bytes for -Ultra DMA transfer in the DATA-OUT (Write) direction.
- Disconnection/connection changes occur as storage devices are temporarily disconnected while processing the DOWNLOAD MICROCODE command.

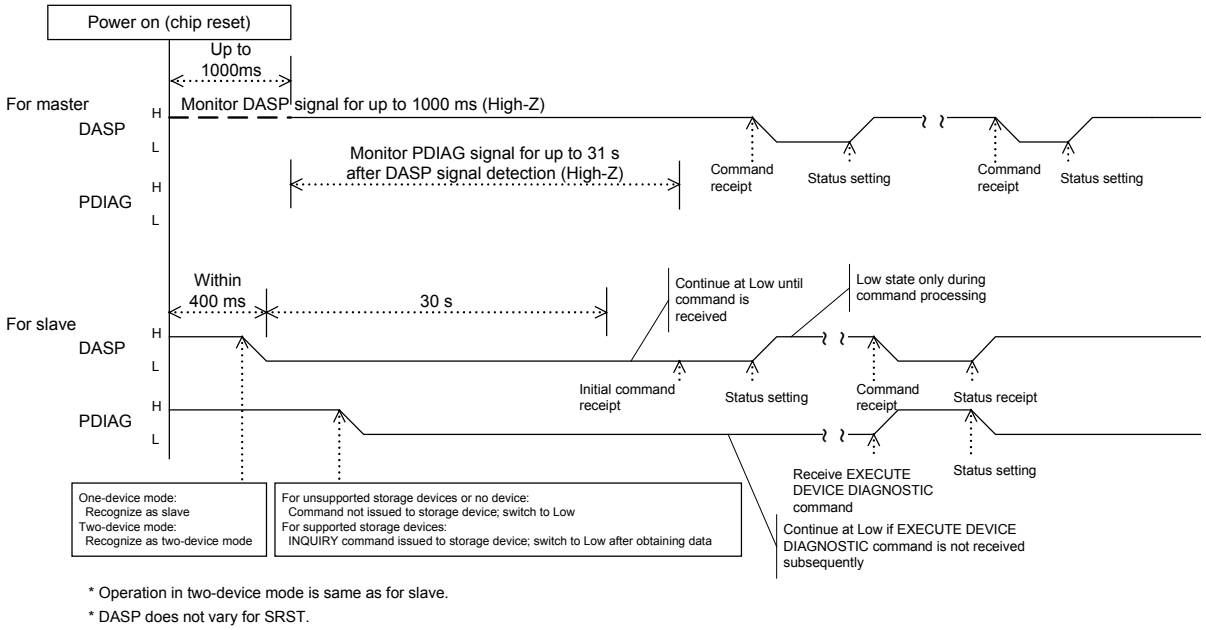
2.7.1 Operation Specifications for Initialization

The LSI performs the following processing during initialization (in Busy state). No special processing is needed by the main CPU except for initialization processing in accordance with the ATA/ATAPI standard.

- The DASP signal is asserted in two-device mode or for the slave in one-device mode.
- The storage device information is obtained if storage devices are connected.

For detailed information on initialization processing for the connect/disconnect pins, see "2.7.6.3.2 Operations on Detecting System Reset or Hardware Reset".

The LSI resets the Busy state once the storage device connection processing is complete, notifying the main CPU that the storage device is connected. Control of the storage device by the main CPU begins once this initialization is complete.



* Operation in two-device mode is same as for slave.

* DASP does not vary for SRST.

Fig. 2.9 DASP/PDIAG initialization specifications

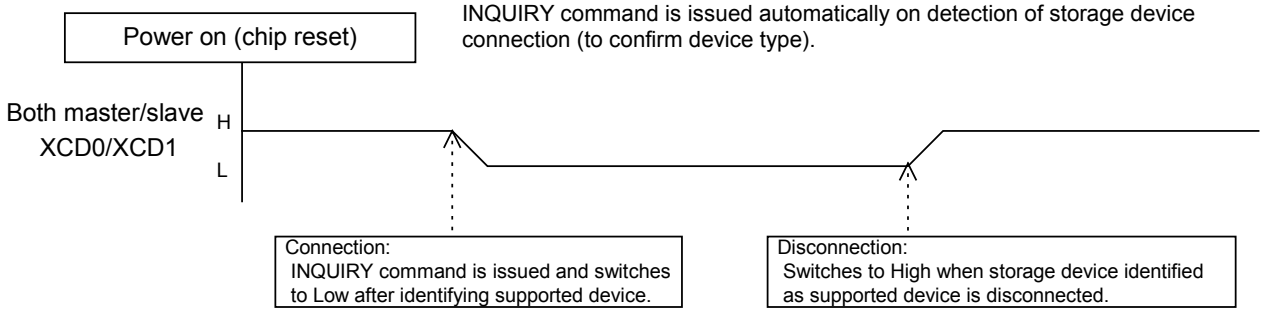


Fig. 2.10 XCD0/XCD1 initialization specifications

2.7.2 Supported Command List

The main CPU is capable of controlling the LSI using ATA/ATAPI commands. The commands supported by the LSI are shown below.

2.7.2.1 ATA Mode

Table 2.5 shows the supported ATA commands. The commands indicated in bold type are processed within the LSI and are not issued to storage devices. Shaded commands are issued to storage devices converted to ATAPI commands.

Table 2.5 Supported ATA command list

Transfer method	Transfer size	Code	Command	Remarks
No data	–	**E5h**	**CHECK POWER MODE**	Ends normally even if no storage device is connected.
		90h	**EXECUTE DEVICE DIAGNOSTIC**	Ends normally even if no storage device is connected.
		E7h	**FLUSH CACHE**	Returns normal completion status without taking any action.
		EAh	**FLUSH CACHE EXT**	
		DAh	GET MEDIA STATUS	Issues TEST UNIT READY command and checks device status.
		E3h	IDLE	Converts to START/STOP UNIT command (Immed bit = 0, Start bit = 1) Ends normally even if no storage device is connected.
		E1h	IDLE IMMEDIATE	Converts to START/STOP UNIT command (Immed bit = 1, Start bit = 1) Ends normally even if no storage device is connected.
		91h	**INITIALIZE DEVICE PARAMETER**	Ends normally even if no storage device is connected.
		00h	**NOP**	
		40h	READ VERIFY SECTOR(S)	Issues TEST UNIT READY command and checks device status.
		42h	READ VERIFY SECTOR(S) EXT	
		70h	SEEK	Converts to SEEK (10) command.
		EFh	**SET FEATURES**	Ends normally even if no storage device is connected.
		C6h	**SET MULTIPLE MODE**	Ends normally even if no storage device is connected.
		E6h	**SLEEP**	Ends normally even if no storage device is connected.
		E2h	STANDBY	Converts to START/STOP UNIT command (Immed bit = 0, Start bit = 0) Ends normally even if no storage device is connected.
		E0h	STANDBY IMMEDIATE	Converts to START/STOP UNIT command (Immed bit = 1, Start bit = 0) Ends normally even if no storage device is connected.

PIO IN	512	**ECh**	**IDENTIFY DEVICE**	Returns data generated from information obtained using INQUIRY and READ CAPACITY commands. Ends normally even if no storage device is connected.
	Sector count	C4h	READ MULTIPLE	Converts to READ (10) or READ (12) command.
		29h	READ MULTIPLE EXT	
		20h	READ SECTOR(S)	
		24h	READ SECTOR(S) EXT	
PIO OUT	Sector count	C5h	WRITE MULTIPLE	Converts to WRITE (10) or WRITE (12) command.
		39h	WRITE MULTIPLE EXT	
		30h	WRITE SECTOR(S)	
		34h	WRITE SECTOR(S) EXT	
		92h	**DOWNLOAD MICROCODE**	Data is transmitted to this LSI, and the function is updated. Ends normally even if no storage device is connected.
DMA IN	Sector count	C8h	READ DMA	Converts to READ (10) or READ (12) command.
		25h	READ DMA EXT	
DMA OUT	Sector count	CAh	WRITE DMA	Converts to WRITE (10) or WRITE (12) command.
		35h	WRITE DMA EXT	

Table 2.6 Specially supported commands for backward compatibility

Transfer method	Transfer size	Code	Command	Remarks
No data	–	**10h**	**RECALIBRATE**	Returns normal completion status without taking any action. Ends normally even if no storage device is connected.

Table 2.7 Unsupported commands returning errors

Transfer method	Transfer size	Code	Command	Remarks
No data	–	**08h**	**DEVICE RESET**	Returns error status.
PIO IN	512	**A1h**	**IDENTIFY PACKET DEVICE**	Does not transfer data; returns error status.

2.7.2.2 ATAPI Mode

Table 2.8 shows the supported ATA commands. Tables 2.9 and 2.10 show the supported ATAPI commands. The commands indicated in bold type are processed within the LSI and are not issued to storage devices. ATAPI commands are issued unchanged to the storage devices.

Table 2.8 Supported ATA command list

Transfer method	Transfer size	Code	Command	Remarks
No data	–	**E5h**	**CHECK POWER MODE**	Ends normally even if no storage device is connected.
		08h	**DEVICE RESET**	USB is reset if storage device is processing command. Ends normally even if no storage device is connected.
		90h	**EXECUTE DEVICE DIAGNOSTIC**	Ends normally even if no storage device is connected.
		E1h	**IDLE IMMEDIATE**	Ends normally even if no storage device is connected.
		00h	**NOP**	
		37h	**SET FEATURES**	Ends normally even if no storage device is connected.
		E6h	**SLEEP**	Ends normally even if no storage device is connected.
		E0h	**STANDBY IMMEDIATE**	Ends normally even if no storage device is connected.
PIO IN	512	**A1h**	**IDENTIFY PACKET DEVICE**	Returns data generated from information obtained using INQUIRY command. Ends normally even if no storage device is connected.
PIO OUT	Sector count	**92h**	**DOWNLOAD MICROCODE**	Data is transmitted to this LSI, and the function is updated. Ends normally even if no storage device is connected.
–	–	A0h	PACKET	

Table 2.9 Supported ATAPI command list (HDD, flash memory)

Transfer method	Transfer size	Code	Command	Remarks
No data	–	1Eh	PREVENT/ALLOW MEDIUM REMOVAL	
		2Bh	SEEK(10)	
		1Bh	START/STOP UNIT	
		00h	TEST UNIT READY	
		2Fh	VERIFY(10)	
		2Eh	WRITE AND VERIFY(10)	
PI/DI	Unspecified	04h	FORMAT UNIT	
		12h	INQUIRY	Ends normally even if no storage device is connected.
		5Ah	MODE SENSE(10)	
		25h	READ CAPACITY	
		23h	READ FORMAT CAPACITY	
		03h	**REQUEST SENSE**	Data which is in advance acquired by this command is returned. Ends normally even if no storage device is connected.
	Sector count	28h	READ(10)	
		A8h	READ(12)	
PO/DO	Unspecified	55h	MODE SELECT(10)	
	Sector count	2Ah	WRITE(10)	
		AAh	WRITE(12)	

Table 2.10 Supported ATAPI command list (CD, DVD, MO)

Transfer method	Transfer size	Code	Command	Remarks
No data	–	1Eh	PREVENT/ALLOW MEDIUM REMOVAL	
		2Bh	SEEK(10)	
		1Bh	START/STOP UNIT	
		00h	TEST UNIT READY	
		2Fh	VERIFY(10)	
		2Eh	WRITE AND VERIFY(10)	
		A1h	BLANK	
		5Bh	CLOSE TRACK/SESSION	
		2Ch	ERASE (10)	
		A6h	LOAD/UNLOAD MEDIUM	
		4Bh	PAUSE/RESUME	
		45h	PLAY AUDIO (10)	
		A5h	PLAY AUDIO (12)	
		A7h	PLAY AUDIO MSF	
		58h	REPAIR TRACK	
		53h	RESERVE TRACK	
		BAh	SCAN	
		BBh	SET CD SPEED	
		A7h	SET READ AHEAD	

		4Eh	STOP PLAY/SCAN	
		35h	SYNCHRONIZE CACHE	
PI/DI	Unspecified	04h	FORMAT UNIT	
		12h	INQUIRY	Ends normally even if no storage device is connected.
		5Ah	MODE SENSE(10)	
		25h	READ CAPACITY	
		23h	READ FORMAT CAPACITIES	
		03h	**REQUEST SENSE**	Data which is in advance acquired by this command is returned. Ends normally even if no storage device is connected.
		46h	GET CONFIGURATION	
		4Ah	GET EVENT/STATUS NOTIFICATION	
		ACh	GET PERFORMANCE	
		BDh	MECHANISM STATUS	
		3Ch	READ BUFFER	
		5Ch	READ BUFFER CAPACITY	
		51h	READ DISC INFORMATION	
		ADh	READ DISC STRUCTURE	
		44h	READ HEADER	
		42h	READ SUB-CHANNEL	
		43h	READ TOC/PMA/ATIP	
		52h	READ TRACK INFORMATION	
		A4h	REPORT KEY	
	Sector count	28h	READ(10)	
		A8h	READ(12)	
		BEh	READ CD	
		B9h	READ CD MSF	
PO/DO	Unspecified	55h	MODE SELECT(10)	
		5Dh	SEND CUE SHEET	
		BFh	SEND DISC STRUCTURE	
		A2h	SEND EVENT	
		A3h	SEND KEY	
		54h	SEND OPC INFORMATION	
		B6h	SET STREAMING	
		3Bh	WRITE BUFFER	
	Sector count	2Ah	WRITE(10)	
		AAh	WRITE(12)	

2.7.3 Information Specifications Returned for Each Command

The main CPU can obtain information on the storage device connected to the LSI using the commands described here. The methods used to generate the information are described below.

2.7.3.1 IDENTIFY DEVICE Data

Table 2.11 shows the data returned by the IDENTIFY DEVICE command. The LSI incorporates the information obtained from the connected storage device into data returned to the main CPU.

The values indicated in bold type are fixed. Values enclosed in bold frames are values generated based on information obtained from the storage device using the INQUIRY or READ CAPACITY commands. The position of the generated values is indicated by "x". The shaded areas indicate values replaced by the commands issued by the main CPU (colors indicate different commands). Thus, the values shown are default values.

Table 2.11 IDENTIFY DEVICE data

Words	Value	Details
0	**0080h**	ATA removable
1	xxxxh	Total cylinder count (determined by storage device capacity: Max value is 3FFFh) Calculated from data obtained using READ CAPACITY command (*1) Returns 0000h when no device is connected.
2	**0000h**	
3	**0010h**	Total header count
4 to 5	**0000h**	
6	**003Fh**	Sector count per track
7 to 9	**0000h**	
10 to 12	xxxxh	Serial number S1R72U16XXXE100 : word10～19 2020h fixed S1R72U16XXXE200 : word10～12 3030h fixed word13 3030h(Master), 3031h(Slave) word14～19 2020h fixed
13	xxxxh	
14 to 19	**2020h**	
20 to 22	**0000h**	
23 to 26	xxxxh	Firmware revision Setting data generated from data obtained using INQUIRY command (*2) Returns "rev1.0" when no device is connected.
27 to 46	xxxxh	Model number Setting data generated from data obtained using INQUIRY command (*3) Returns "____ S1R72U16" when no device is connected.
47	**8002h**	Maximum INTRQ assert sector size for READ/WRITE MULTIPLE command
48	**0000h**	
49	**0000111100000000b**	bit 11 = 1, bit 10 = 1: IORDY support and IORDY disable support bit 9 = 1: LBA support bit 8 = 1: DMA support
50	**0100000000000000b**	
51	**0200h**	PIO Mode2 support
52	**0000h**	
53	**0000000000000111b**	Word 88, words 64 to 70, words 54 to 58 enable

54	xxxxh	Current cylinder count (Default value is same as Word 1) Replaced by INITIALIZE DEVICE PARAMETERS command. Returns 0000h when no device is connected.
55	xxxxh	Current header count (Default value is same as Word 3) Set as INITIALIZE DEVICE PARAMETERS command Device/Head register lower bit value +1.
56	xxxxh	Current sector count per track (Default value is same as Word 6) Set as INITIALIZE DEVICE PARAMETERS command Sector Count register value.
57 to 58	xxxxh	Current total sector count (Determined by Word 54, 55, 56 values: Max value is 00FBFC10h:word57=FC10h, word58=00FBh) Returns 0000h when no device is connected.
59	**01xxh**	Lower 8 bits: Set current READ/WRITE MULTIPLE command INTRQ assert sector size to 01h. bit 8 = 1: Set Multiple support Lower 8 bits are replaced by SET MULTIPLE MODE command.
60 to 61	xxxxh	Total sector count Returns 0FFFFFFFh if device capacity is at least 128 Gbytes (1K calculated as 1024 bytes). Set data obtained by READ CAPACITY command. Returns 0000h when no device is connected.
62	**0000h**	
63	**00000xxx00000111b**	Multiword DMA mode 0, 1, 2 support (Default value is 0407h) Bits 8 to 10 are replaced by SET FEATURES command.
64	**0003h**	PIO mode 3, 4 support
65	**0078h**	Multiword DMA minimum transfer cycle per word.
66	**0078h**	Multiword DMA transfer cycle recommended by device.
67	**00F0h**	PIO transfer cycle
68	**0078h**	IORDY assert cycle
69 to 74	**0000h**	
75	**0000h**	Command queue size
76 to 79	**0000h**	
80	**0070h**	
81	**4000h**	
82	**0000000000001000b**	bit 3 = 1: Power Management Feature Set support
83	**01110x0000010001b**	bit 13 = 1: FLUSH CACHE EXT command support bit 12 = 1: FLUSH CACHE command support bit 10 = 1: 48-bit address support Set using data obtained by READ CAPACITY command. Device under 128G = 0, device 128G or over = 1 (1K calculated as 1024 bytes) bit 4 = 1: Removable Media Status Notification support bit 0 = 1: DOWNLOAD MICROCODE command support
84	**4000h**	
85	**0000000000001000b**	bit 3 = 1: Power Management Feature Set permission
86	**00110x0000010001b**	bit 13 = 1: FLUSH CACHE EXT command enable bit 12 = 1: FLUSH CACHE command enable bit 10 = 1: 48-bit address enable Set using data obtained by READ CAPACITY command. Device under 128G = 0, device 128G or over = 1 (1K calculated as 1024 bytes) bit 4 = 1: Removable Media Status Notification enable bit 0 = 1: DOWNLOAD MICROCODE command enable
87	**4000h**	

88	**00xxxxxx00111111b**	Ultra DMA mode 0, 1, 2, 3, 4, 5 support Bits 8 to 13 are replaced by SET FEATURES command
89 to 92	**0000h**	
93	**01x0000000000000b**	Bit13=xb : 0b (40-conductor cable use), 1b (80-conductor cable use)
94 to 99	**0000h**	
100 to 103	xxxxh	Maximum LBA (48-bit address) Returns 0000h if device capacity is less than 128 Gbytes (1K calculated as 1024 bytes). Set using data obtained by READ CAPACITY command. Returns 0000h when no device is connected.
104 to 126	**0000h**	
127	**0001h**	01h: Removable Media Status Notification support
128 to 254	**0000h**	
255	**0000h**	No checksum (because word 0 to 254 values are variable)

*1: The total cylinder count is calculated using the LBA value obtained by the READ CAPACITY command.

LBA ≥ 16514064

Fixed at 3FFFh

LBA < 16514064

LBA / 16 (Max Head) / 63 (Max Sector)

*2: Firmware revision is generated using Product Revision Level obtained by the INQUIRY command.
Product Revision Level (4 bytes) + space (4 bytes)

*3: Model number is generated using Vendor Identification and Product Identification obtained by the INQUIRY command.

1. Vendor Identification obtained as far as first space as manufacturer name
   * Manufacturer name is treated as missing if initial character is a space.
2. Product Identification obtained as product name
3. Generated as manufacturer name + space (1 byte) + product name

2.7.3.2 IDENTIFY PACKET DEVICE Data

Table 2.12 shows the data returned by the IDENTIFY PACKET DEVICE command. The LSI incorporates the information obtained from the connected storage device into the data returned to the main CPU.

The values indicated in bold type are fixed. Values enclosed in bold frames are values generated based on information obtained from the storage device using the INQUIRY or READ CAPACITY commands. The position of the generated values is indicated by "x". The shaded areas indicate values replaced by the commands issued by the main CPU (colors indicate different commands). Thus, the values shown are default values.

Table 2.12 IDENTIFY PACKET DEVICE data

Words	Value	Details
0	**100xxxxx10000000b**	bits 15 to 14 = 10b: ATAPI device bit 12 to 8 = xxxxxb: 00000b (HDD), 00101b (CD/DVD) or 00111b (MO) Set data device type obtained by INQUIRY command. * Returns 11111b (no connected device) when no device is connected. bit 7 = 1b: Removable device bits 6 to 5 = 00b: Maximum time from PACKET command receipt to DRQ assert is 3 msec bits 1 to 0 = 00b: 12-byte command support
1 to 9	**0000h**	
10 to 12	xxxxh	Serial number S1R72U16XXXE100 : word10～19 2020h fixed S1R72U16XXXE200 : word10～12 3030h fixed word13 3030h(Master), 3031h(Slave) word14～19 2020h fixed
13	xxxxh	
14 to 19	**2020h**	
20 to 22	**0000h**	
23 to 26	xxxxh	Setting data generated from data obtained using INQUIRY command (Generation method is same as for "2.7.3.1 IDENTIFY DEVICE Data") * Returns "rev1.0" when no device is connected.
27 to 46	xxxxh	Setting data generated from data obtained using INQUIRY command (Generation method is same as for "2.7.3.1 IDENTIFY DEVICE Data") * Returns "____ S1R72U16" when no device is connected.
47 to 48	**0000h**	
49	**0000111100000000b**	bit 11 = 1, bit 10 = 1: IORDY support and IORDY disable support bit 8 = 1: DMA support
50	**4000h**	
51	**0200h**	PIO Mode2 support
52	**0000h**	
53	**0000000000000110b**	Word 88, words 64 to 70 enable
54 to 62	**0000h**	
63	**00000xxx00000111b**	Multiword DMA mode 0, 1, 2 support (Default value is 0407h) Bits 8 to 10 are replaced by SET FEATURES command.
64	**0003h**	PIO mode 3, 4 support
65	**0078h**	Multiword DMA minimum transfer cycle per word.
66	**0078h**	Multiword DMA transfer cycle recommended by device.
67	**00F0h**	PIO transfer cycle

68	**0078h**	IORDY assert cycle
69 to 74	**0000h**	
75	**0000h**	Command queue size
76 to 79	**0000h**	
80	**0070h**	
81	**4000h**	
82	**0100001000011000b**	bit 14 = 1: NOP command support bit 9 = 1: DEVICE RESET command support bit 4 = 1: PACKET command support bit 3 = 1: Power management feature set support
83	**0100000000000001b**	bit 0 = 1: DOWNLOAD MICROCODE command support
84	**4000h**	
85	**0100001000011000b**	bit 14 = 1: NOP command enable bit 9 = 1: DEVICE RESET command enable bit 4 = 1: PACKET command enable bit 3 = 1: Power management feature set enable
86	**0000000000000001b**	bit 0 = 1: DOWNLOAD MICROCODE command enable
87	**4000h**	
88	**00xxxxxx00111111b**	Ultra DMA mode 0, 1, 2, 3, 4, 5 support Bits 8 to 13 are replaced by SET FEATURES command.
89 to 92	**0000h**	
93	**01x0000000000000b**	Bit13=xb : 0b (40-conductor cable use), 1b (80-conductor cable use)
94 to 254	**0000h**	
255	**0000h**	No checksum (because word 0 to 254 values are variable)

2.7.3.3 INQUIRY Data

Table 2.13 shows the data returned by the INQUIRY command.

The data returned will vary depending on whether storage devices are connected. The data length and values will depend on the storage device connected. The data length does not exceed 36 bytes when no storage device is connected.

Table 2.13 INQUIRY data with no storage device connected

Byte	Value	Details
0	00011111b	bit 3 to 0 = 11111b: Device type (11111b: No device type)
1	00000000b	bit 7 = 0b: RMB
2	02h	bit 7 to 6 = 00b: ISO Version bit 5 to 3 = 000b: ECMA Version bit 2 to 0 = 010b: ANSI Version
3	02h	bit 7 to 4 = 0000b: ATAPI Transport Version bit 3 to 0 = 0010b: Response Data Format
4	1Fh	Additional Length
5	00h	Reserved
6	00h	Reserved
7	10h	Reserved
8 to 15	“_____ ”	Vendor Information (“_” × 5 + “ ” × 3)
16 to 31	“S1R72U16 ”	Product Identification
32 to 35	“1.0”	Product Revision Level

2.7.4 Processing Unsupported Commands

The unsupported command processing for each command system is as shown below.

- ATA mode
  - ATA commands other than those in Tables 2.5 to 2.7: Converted to ATA PASS-THROUGH (12) commands and issued as vendor commands to storage device.
  - Unsupported ATA commands in Table 2.7: Command not issued to storage device; error returned to main CPU.
  - ATAPI commands: Command not issued to storage device; error returned to main CPU.
- ATAPI mode
  - ATA commands other than those in Table 2.8: Command not issued to storage device; error returned to main CPU.
  - ATAPI commands other than those in Tables 2.9 to 2.10: Issued as vendor command to storage device.

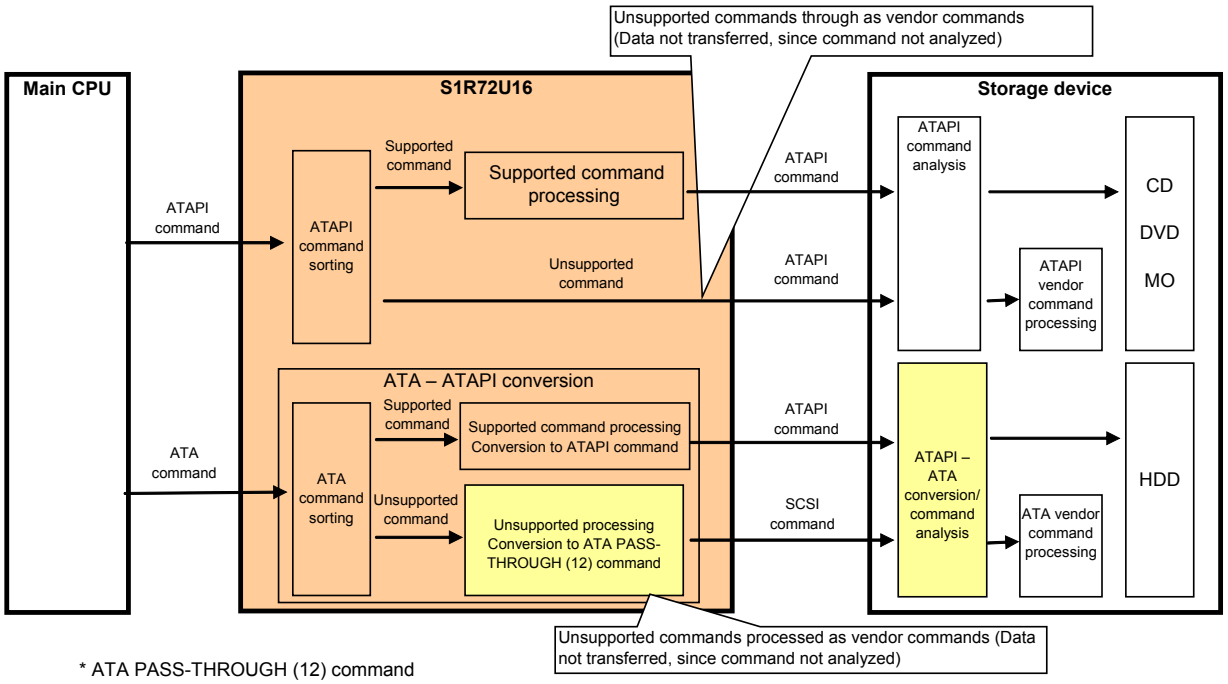
2.7.4.1 Vendor Commands

The main CPU can exert unique control by issuing vendor commands to the storage device using unsupported commands. Data cannot be transferred, however, since the LSI does not analyze vendor commands. Thus, ATA/ATAPI command protocols with no data should be used for the main CPU. Fig. 2.11 illustrates vendor command processing.

Vendor commands are processed as shown below, depending on command system settings.

- ATA mode
  - When issuing commands: Converted to ATA PASS-THROUGH (12) command and issued to storage device.
  - When obtaining status: Issued REQUEST SENSE command to storage device.
    - * An error is returned to the main CPU if the REQUEST SENSE command return packet data does not conform to the ATA PASS-THROUGH format.
- ATAPI mode
  - Issued through to the storage device.

For detailed information on the ATA PASS-THROUGH (12) command, see *Information Technology - SCSI/ATA Translation (SAT)*.



* ATA PASS-THROUGH (12) command
The status register value is obtained using the REQUEST_SENSE command with the command issuing the ATA command register value as its parameter.
The ATAPI – ATA conversion and command analysis component of the USB device must support this command.

Fig. 2.11 Vendor command outline

2.7.5 Operation Specifications for Error Occurrence

This section describes the processing performed by the LSI when an error occurs between the LSI and a storage device. Errors should be processed by the main CPU as necessary in accordance with the instructions given here.

2.7.5.1 When Storage Device Repeatedly Returns NAK

The LSI does not perform time-out processing when an NAK response is returned from a storage device. The LSI is in Busy state here (the Status register BSY bit or DRQ bit is 1). Thus, time-out processing should be performed at the main CPU, if required.

This phenomenon may occur whether initializing or controlling the storage device.

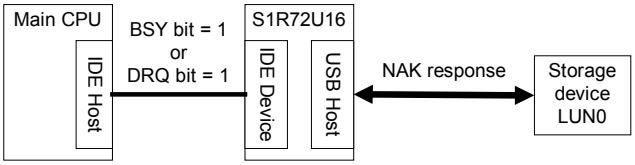


Fig. 2.12 When NAK response is returned

2.7.5.2 Storage Device Connection Processing

The LSI will treat a storage device as an unsupported device if an error occurs during connection processing. This means no special processing by the main CPU is needed.

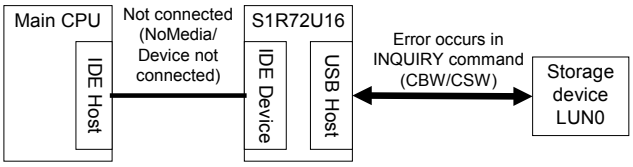


Fig. 2.13 Storage device detection

The error conditions are as shown below.

- ATA/ATAPI command protocol error
  - An error occurred in the INQUIRY command issued by the LSI.
- USB protocol error
  - Error ended or phase error ended in CBW/data transfer/CSW phases in compliance with Mass Storage Class Bulk Only Transport standards.
- No response from USB device
  - Three consecutive retries failed (retry processing completed within 1 ms on average).

2.7.5.3 When Controlling a Storage Device

Error status is returned in response to the command issued by the main CPU when an error occurs between the LSI and storage device while the storage device is under control by the main CPU. Processing should be performed by the main CPU based on error status, in accordance with the ATA/ATAPI standard.

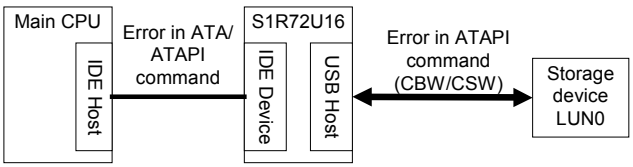


Fig. 2.14 When controlling storage device

When an error occurs, value of the ATA task file registers notified to the main CPU will be ATA/ATAPI standard values.

ATAPI commands include a REQUEST SENSE command for obtaining error details. The REQUEST SENSE command data is as shown below based on error conditions when the LSI is in ATAPI mode.

- When an error occurs in ATAPI command protocol
  - ➢ The value obtained from the storage device is returned to the main CPU.
- When an error occurs in the USB protocol or no response is received from the USB device
  - ➢ Sense Key: 04h, ASC: 08h, ASCQ: 00h (LOGICAL UNIT COMMUNICATION FAILURE) are returned to the main CPU.
- When a connection/disconnection error occurs
  - ➢ When the storage device is disconnected:
    Sense Key: 02h, ASC: 3Ah, ASCQ: 00h (MEDIUM NOT PRESENT) are returned to the main CPU.
  - ➢ When the storage device has been changed:
    Sense Key: 06h, ASC: 28h, ASCQ: 00h (MEDIUM MAY HAVE CHANGED) are returned to the main CPU.
- When an unsupported command is issued
  - ➢ Sense Key: 05h, ASC: 20h, ASCQ: 00h (INVALID COMMAND OPERATION CODE) are returned to the main CPU.
  - * An error is not returned by the LSI for the following commands, since they are specified as not returning errors under the ATA/ATAPI standards.
    In ATA mode: IDENTIFY DEVICE, EXECUTE DEVICE DIAGNOSTIC
    In ATAPI mode: IDENTIFY PACKET DEVICE, EXECUTE DEVICE DIAGNOSTIC, DEVICE RESET, INQUIRY, REQUEST SENSE

The error conditions of occurrence are as shown below.

- ATA/ATAPI command protocol error
  - An error occurred in the ATAPI command issued in CBW.
- USB protocol error
  - Error ended or phase error ended for CBW/data transfer/CSW phases in compliance with Mass Storage Class Bulk Only Transport standards.
- No response from USB device
  - Three consecutive retries failed (retry processing completed within 1 ms on average).

2.7.6 Connection/Disconnection Specifications

The LSI features the pins and register described below to support storage device connection and disconnection. This section may be skipped if the storage device is not treated as an ATA/ATAPI removable device.

2.7.6.1 Pins Used for Connection/Disconnection

The pins shown below are used to indicate whether a storage device is connected to the main CPU.

- XCD0 pin (PORT11)
- XCD1 pin (PORT12)
- XChgInt pin (PORT10)

The following bit can be used if the XChgInt pin cannot be used.

- ATA task file register Status register bit 1 (ChgInt bit)

Individual pin and bit specifications are described below.

2.7.6.1.1 XCD0 Pin

This is used by the main CPU to detect if master device is connected or disconnected.

Low when a storage device is connected; High when no storage device is connected. This does not change, even if a storage device is connected in Sleep state. The last status is indicated on Wakeup.

This pin does not change when USB hubs or unsupported USB devices are connected.

This pin operates identically to XCD1 when the device connection count is set to one-device mode.

2.7.6.1.2 XCD1 Pin

This is used by the main CPU to detect if slave device is connected or disconnected.

Low when a storage device is connected; High when no storage device is connected. This does not change even if a storage device is connected in Sleep state. The last status is indicated on Wakeup.

This pin does not change when USB hubs or unsupported USB devices are connected.

This pin operates identically to XCD0 when the device connection count is set to one-device mode.

2.7.6.1.3 XChgInt Pin

This is used by the main CPU to obtain connection/disconnection changes for storage devices. Set initially to High, it changes to Low if a device is connected or disconnected, then reverts to High on receipt of one of the commands shown in Table 2.14. Note that it does not switch to Low if a storage device is connected during the following intervals:

- Before the following commands are received after a system reset or hardware reset is detected
  - ATA mode: Receiving IDENTIFY DEVICE command
  - ATAPI mode: Receiving IDENTIFY PACKET DEVICE command
- Sleep state (changes to Low on Wakeup if device connected/disconnected during Sleep)

This pin cannot determine the connection/disconnection status of storage devices. The connection/disconnection status should be determined either using the commands shown in Table 2.14 or by checking pins XCD0 and XCD1.

Table 2.14 Connection states obtainable by issuing commands

ATA/ATAPI mode	Command	Data position	Value	Status
ATAPI mode	IDENTIFY PACKET DEVICE	Word0: bit8 to 12 (Device Type)	Except 1Fh	Connected
			1Fh	Disconnected
	INQUIRY	Byte0: bit0 to 4 (Device Type)	Except 1Fh	Connected
			1Fh	Disconnected
ATA mode	IDENTIFY DEVICE	Word60 to 61 (Total LBA)	Except 0000h	Connected
			0000h	Disconnected
	GET MEDIA STATUS	Error Register	Except 02h or 20h	Connected
			20h (MC: Media Change)	Connected: Single notification immediately after device connection
			02h (NM: No Media)	Disconnected
	READ/WRITE commands READ SECTOR(S) READ SECTOR(S) EXT READ DMA READ DMA EXT READ MULTIPLE READ MULTIPLE EXT READ VERIFY SECTOR(S) READ VERIFY SECTOR(S) EXT WRITE SECTOR(S) WRITE SECTOR(S) EXT WRITE DMA WRITE DMA EXT WRITE MULTIPLE WRITE MULTIPLE EXT	Error Register	Except 02h or 20h	Connected
			20h (MC: Media Change)	Connected: Single notification immediately after device connection
			02h (NM: No Media)	Disconnected

* Media Change and No Media are bits in the ATA task file register Error register. For detailed information, see the ATA/ATAPI-4, -5, -6 standards.

2.7.6.1.4 ATA Task File Register Status Register Bit1

This section describes departures from the ATA/ATAPI standards. For detailed information on the registers, see "3. Registers".

Bit1 in the Status register, discontinued in the ATA/ATAPI standards, is used as the ChgInt connection/disconnection notification bit. This bit has the same specifications as the XChgInt pin except when the logic is inverted. For detailed information on operations, see "2.7.6.1.3 XChgInt Pin". Table 2.15 shows the Status register.

Table 2.15 ATA task file registers (Status)

Register	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Status	BSY	DRDY	DF	#	DRQ	Obsolete	ChgInt	ERR

Obsolete: Discontinued bit (fixed at 0)
#: Bit dependent on command

↑
0 when XChgInt is High, and 1 when Low.

2.7.6.2 Procedure for Using Connect/Disconnect Pins

The main CPU can detect connection or disconnection using any of the following methods.

Set main CPU interrupt detection to both rising and falling edge detection when using the XCD0 and XCD1 pins as interrupt signals. Set main CPU interrupt detection to level detection when using the XChgInt pin as an interrupt signal in two-device mode.

- Using XCD0/XCD1 pins
  - Determine connection/disconnection state by monitoring XCD0/XCD1 pins and obtaining signal status.
    - * Both rising and falling edge shall be used for interrupt detection when using the XCD0/XCD1 pins as interrupt signals.
- Using XChgInt and XCD0/XCD1 pins
  - Monitor XChgInt and XCD0/XCD1 pins and obtain connection/disconnection changes from XChgInt pin.
  - Obtain connection/disconnection state from XCD0/XCD1 pins.
- Using XChgInt pin
  - Monitor XChgInt pin and obtain connection/disconnection changes from XChgInt pin.
  - Obtain connection/disconnection state using ATA/ATAPI command (refer to Table 2.14 for detailed information on connection/disconnection information obtainable with the command).
    - * In two-device mode, a command must be issued to the second storage device to obtain the state if no connection/disconnection occurs for the first storage device.

- Using ATA task file register Status register instead of XChgInt pin
  - Bit 1 of the Status register (ChgInt bit) is linked to the XChgInt pin, enabling this bit to be polled to check for connection/disconnection changes.

The main CPU should perform the following processing when a connection/disconnection notification from the LSI is detected.

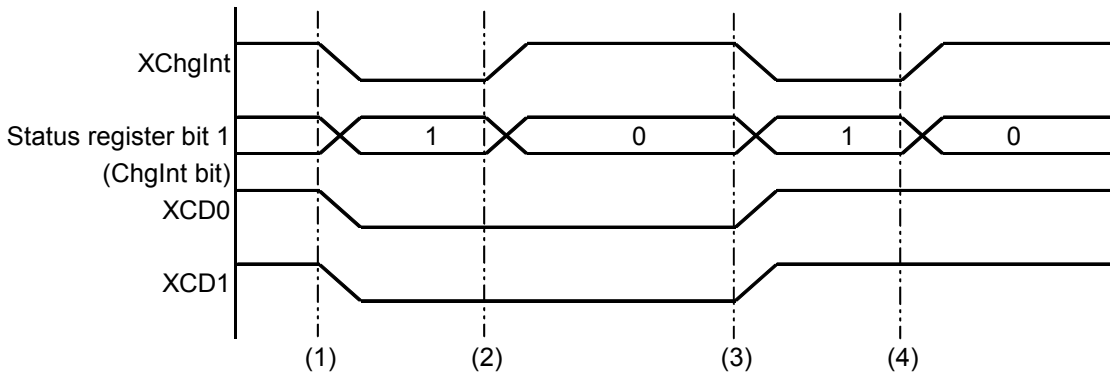
- ATA mode
  - Issue an IDENTIFY DEVICE command to obtain storage device information.
- ATAPI mode
  - Issue an INQUIRY command to obtain the storage device type.
  - Issue a READ CAPACITY command to obtain the storage device sector count and sector size.

2.7.6.3 Connection/Disconnection Pins Operation Specifications

This section describes how the connection/disconnection pins operate in different states.

2.7.6.3.1 Basic Operation when Storage Device is Connected or Disconnected

Fig. 2.15 illustrates the basic pin and bit operations when a storage device is connected and disconnected.



(1) Storage device is connected.

(2) Conditions are satisfied for the XChgInt pin to switch to High. (See “2.7.6.1.3 XChgInt Pin” for detailed information on High conditions.)

(3) Storage device is disconnected.

(4) Conditions are satisfied for the XChgInt pin to switch to High. (See “2.7.6.1.3 XChgInt Pin” for detailed information on High conditions.)

* When the connected device count is in two-device mode, pin XCD0 changes when the master storage device is connected/disconnected, while pin XCD1 changes when the slave storage device is connected/disconnected.

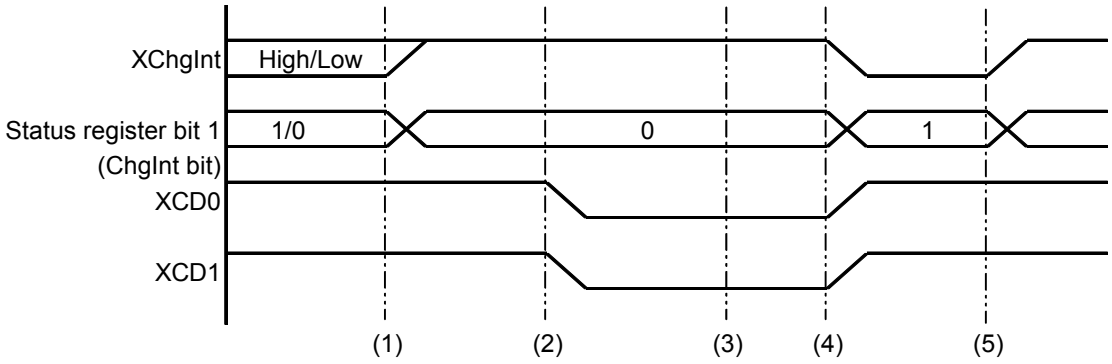
Fig. 2.15 Basic operation

2.7.6.3.2 Operations on Detecting System Reset or Hardware Reset

On detecting a System Reset or Hardware Reset, the XChgInt pin and ChgInt bit do not change until the IDENTIFY DEVICE command is received in ATA mode and the IDENTIFY PACKET DEVICE command is received in ATAPI mode.

Pins XCD0 and XCD1 change in accordance with the storage device connection/disconnection status, regardless of the commands received.

Fig. 2.16 illustrates pin and bit operations.



(1) System Reset or Hardware Reset is detected.
At the same time, the XChgInt pin switches to High and the ChgInt bit switches to 0.
The XCD0 and XCD1 pins are High when a System Reset is detected and remain at the previous state on detection of a Hardware Reset.

(2) Storage device is connected.
The XChgInt pin and ChgInt bit do not change, since no command has been received.

(3) ATA mode: IDENTIFY DEVICE command is received/ATAPI mode: IDENTIFY PACKET DEVICE command is received.
The XChgInt pin and ChgInt bit do not change here even if a device is connected or disconnected before this command is received.

(4) Storage device is disconnected.
The XChgInt pin changes to Low and the ChgInt bit changes to 1 when the storage device is disconnected after receiving the command.

(5) Conditions are satisfied for the XChgInt pin to switch to High. (See “2.7.6.1.3 XChgInt Pin” for detailed information on High conditions.)

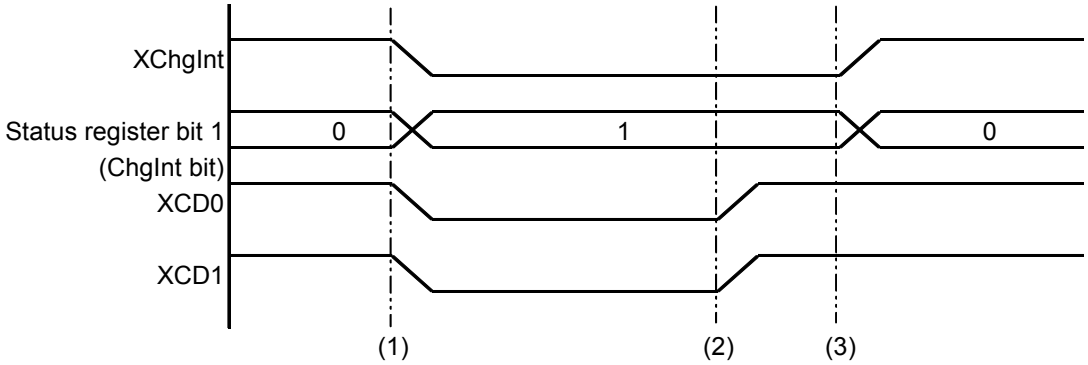
Fig. 2.16 Operations on detecting System Reset or Hardware Reset

2.7.6.3.3 Connection/Disconnection Operations when XChgInt Pin is Low

The XChgInt pin remains Low if a storage device is connected or disconnected while it is Low. The ChgInt bit also remains unchanged at 1.

The XCD0 and XCD1 pins change depending on the storage device connection and disconnection status, regardless of the XChgInt pin.

Fig. 2.17 illustrates operations for one-device mode. Fig. 2.18 illustrates operations for two-device mode.

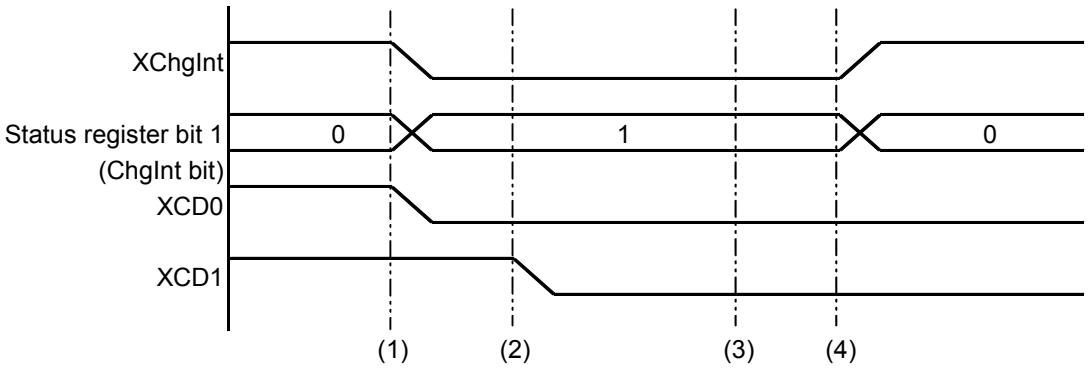


(1) Storage device is connected.

(2) Storage device is disconnected.
The XChgInt pin remains Low and ChgInt bit remains at 1.

(3) Conditions are satisfied for the XChgInt pin to switch to High. (See “2.7.6.1.3 XChgInt Pin” for detailed information on High conditions.)

Fig. 2.17 Pin operation for connection/disconnection when XChgInt pin is Low in one-device mode



(1) Master storage device is connected.

(2) Slave storage device is connected.
The XChgInt pin remains Low and ChgInt bit remains at 1.

(3) Conditions are satisfied for the master XChgInt pin to switch to High. (See “2.7.6.1.3 XChgInt Pin” for detailed information on High conditions.)
The XChgInt pin remains Low and ChgInt bit remains at 1, since slave conditions are not satisfied.

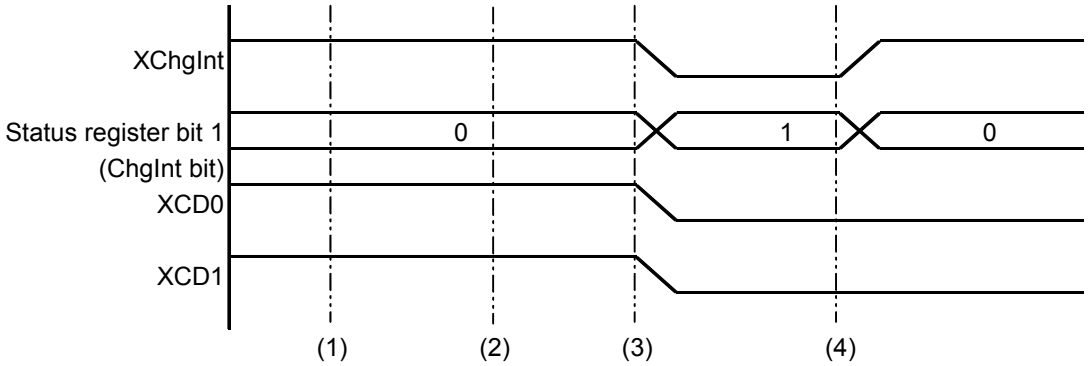
(4) Conditions are satisfied for the slave XChgInt pin to switch to High. (See “2.7.6.1.3 XChgInt Pin” for detailed information on High conditions.)
The XChgInt pin changes to High and ChgInt bit changes to 0, since both master and slave conditions are now satisfied.

Fig. 2.18 Pin operation for connection/disconnection when XChgInt pin is Low in two-device mode

2.7.6.3.4 Connection/Disconnection Operations in Sleep State

The connection/disconnection pins and ChgInt bit do not change if a storage device is connected or disconnected while the LSI is in Sleep state. Notification of connection or disconnection events occurring in Sleep state are issued to the main CPU on Wakeup.

Fig. 2.19 illustrates pin and bit operations.



(1) Switch to Sleep state.

(2) Storage device is connected.
The pins and bit do not change, since the LSI is in Sleep state.

(3) Wakeup
Notification is issued regarding the storage device connected in (2).

(4) Conditions are satisfied for the XChgInt pin to switch to High. (See “2.7.6.1.3 XChgInt Pin” for detailed information on High conditions.)

Fig. 2.19 Pin operation for connection/disconnection in Sleep state

2.7.7 Download Function

The download function is a function enabling the LSI internal RAM to be updated using the DOWNLOAD MICROCODE command.

The main CPU can issue a DOWNLOAD MICROCODE command at any time. Connected Storage devices will be temporarily disconnected for update processing.

If downloading fails, an error status is returned in response to the DOWNLOAD MICROCODE command. Note that the data in the internal RAM will have been overwritten by this stage, meaning subsequent operations cannot be guaranteed.

The downloaded data includes headers in addition to actual data for updating. The headers contain identifiers, destination initial address, data size, and CRC values. Table 2.16 shows the download data configuration. Table 2.17 shows the DOWNLOAD MICROCODE command format. Values indicated in bold type are fixed values.

Table 2.16 Download Data Configuration

Type	Offset	Details	Value	Remarks
Header	00h	Identifier	**D2h**	
	01h	Download data CRC value	xxh	Set results calculated using data only without headers or PAD. *1
	02h	Reserved	**00h**	
	03h	Reserved	**00h**	
	04h	Destination initial address (low order)	xxh	Set to 7E00h for TPL (See “2.8.4 TPL”). Offset 04h: 00h Offset 05h: 7Eh
	05h	Destination initial address	xxh	
	06h	Destination initial address	**00h**	
	07h	Destination initial address (high order)	**00h**	
	08h	Download data size (low order)	xxh	Set to x10 for TPL.
	09h	Download data size	xxh	
	0Ah	Download data size	**00h**	
	0Bh	Download data size (high order)	**00h**	
	0Ch	Reserved	**00h**	
	0Dh	Reserved	**00h**	
	0Eh	Reserved	**00h**	
	0Fh	Reserved	**00h**	
Data	10h	Update data	xxh	Set actual data to be updated.
	:	:	:	
	:	:	:	
	:	:	:	
PAD	xxh	Padding data	**00h**	Set padding data to ensure x512, since the DOWNLOAD MICROCODE command can only transfer data in one-sector blocks

*1: It is calculated automatically by "TPL Create tool" made in our company.

Table 2.17 DOWNLOAD MICROCODE command format

Register	7	6	5	4	3	2	1	0	Remarks
Features	Subcommand code = **01h**								
Sector Count	Sector count (low order)								Set sector count. (1 sector = 512 bytes)
LBA Low	Sector count (high order)								
LBA Mid	**00h**								
LBA High	**00h**								
Device	**0**	**0**	**0**	DEV	**0**	**0**	**0**	**0**	
Command	**92h**								

2.8 USB Function Specifications

2.8.1 Operation Overview

The LSI includes USB host functions and controls mass storage class storage devices in compliance with Universal Serial Bus Specification Revision 2.0 standards. ATAPI commands are used for control.

The LSI USB functions control USB devices under the conditions shown below.

- Supported USB devices are Bulk Only Transport Mass Storage Class, and Hub Class.
  - Subclass supports ATAPI and SCSI (SubClassCode values 01h, 02h, 03h, 05h, 06h).
  - Subclass UFI (SubClassCode value 04h) is not supported.
- The following USB devices are not supported:
  - Classes other than Mass Storage Class
  - Devices for which the subclass is UFI (SubClassCode value 04h) within Bulk Only Transport Mass Storage Class.
  - CBI Transport Mass Storage Class (e.g., USB FDD)
  - Devices not conforming to Mass Storage Class standards (e.g., devices predating Mass Storage Class standards)
- The capacity of the storage device that can be recognized is 2TByte (1K calculated as 1024 bytes) or less.
- Up to two storage devices can be controlled. Subsequent devices connected will be ignored.
  - * When storage devices support multiple LUNs, each LUN is treated as a separate device, even for individual devices.
- Up to three USB hubs can be connected. Subsequent hubs connected will be ignored.
  - * Some USB memory devices include hub functions. These will be counted as hubs.
  - * USB hubs may incorporate multiple hubs within a single device. These will be counted as multiple hubs.
- HS storage devices connected via FS USB hubs will be treated as FS storage devices.
- If the descriptor storage space is insufficient, even supported devices connected will be treated as unsupported devices.
  - * This will occur for USB devices for which Configuration Descriptor + Interface Descriptor + Endpoint Descriptor is 256 bytes or more, or if the number of descriptors of all connected supported devices exceeds 13 Interface Descriptors + 27 Endpoint Descriptors. (Sufficient space for Mass Storage Class)

- If the USB device continues to return NAK responses.

  * Time-out processing is not performed, since USB standards do not specify time-outs for this part. If time-outs are required during storage device control, time-out determination and resetting should be performed by the main CPU.

2.8.2 USB Device Detection

The LSI USB functions check whether a USB device is a supported storage device when detecting a connection. The device can be controlled if identified as a supported storage device.

The check criteria are as follows:

- Device is supported on TPL. (See "2.8.4 TPL")

  * TPL can be set by the download function. (See "2.7.7 Download Function")

- Device is Bulk Only Transport Mass Storage Class.

  * This is valid even when TPL is set.

- Sub Class is not UFI (USB Floppy disk Interface).

- Two controllable storage devices are not already connected.

  * Even a single storage device will be treated as two devices if configured as multiple LUNs.

If two or more storage devices are connected via a USB hub, the first storage device detected will be the master and the second device detected the slave. Subsequent devices will be ignored. The slave storage device does not become the master even if the master storage device is disconnected. Similarly, previously ignored third and subsequent devices cannot be controlled by the main CPU.

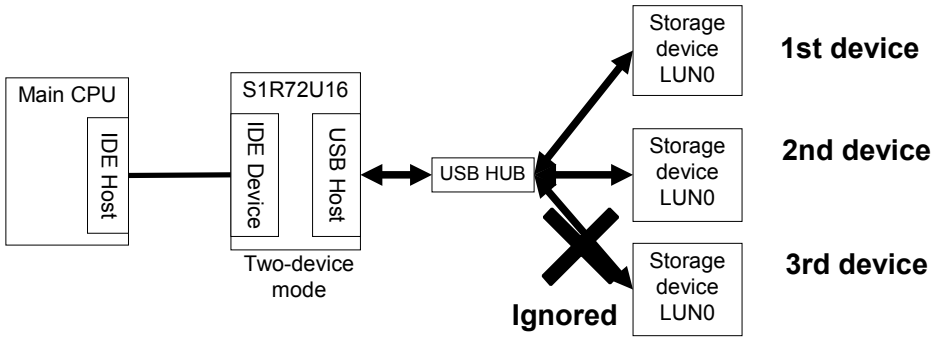


Fig. 2.20 With two devices connected

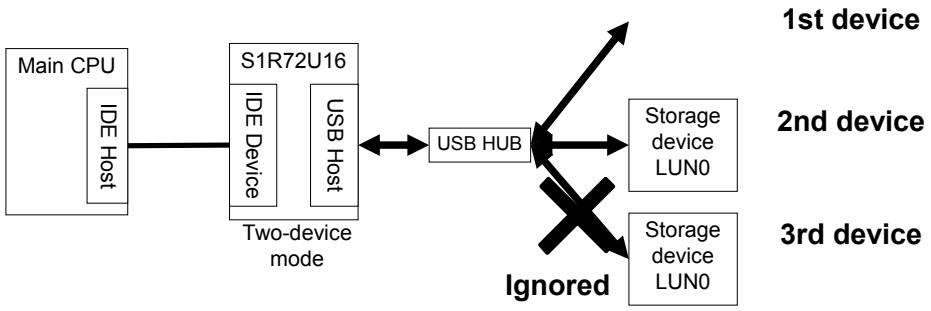


Fig. 2.21 With first device disconnected

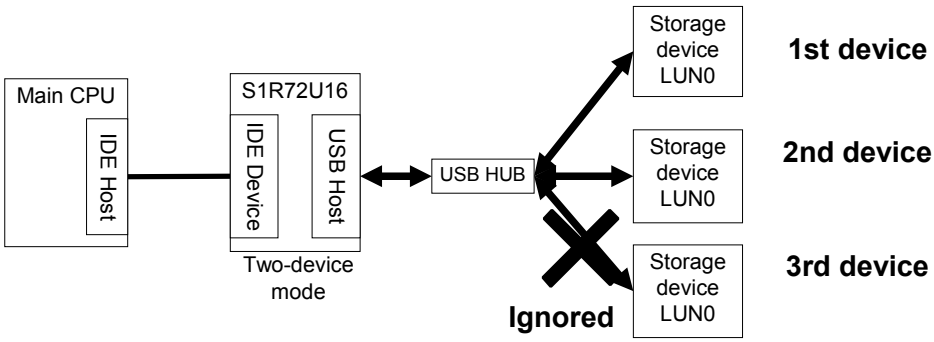


Fig. 2.22 With first device reconnected

2.8.3 Storage Device Control

The LSI conforms to the Mass Storage Class Bulk Only Transport standards and controls storage devices under the following conditions:

- Data transport will be performed when the CBW dCBWDataTransferLength is not 0.
- The data transfer direction is determined by the value of Direction in the CBW bmCBWFlags.
  - 0: Data out transfer (Host to Device)
  - 1: Data in transfer (Device to Host)
- Data transfers are determined as having ended if any of the following conditions apply:
  - Data corresponding to the CBW dCBWDataTransferLength has been transferred.
  - A short packet or zero-length packet is returned from the storage device.
  - STALL is returned from the storage device.
  - A packet error occurs three times in succession during data transfers.
- STALL is cancelled by a Clear Feature request if any of the following conditions apply:
  - STALL is returned during data transfer or CSW.
  - A packet error occurs three times in succession during data transfer or CSW.
- Invalid CSW is determined if any of the following conditions apply:
  - The CSW size is not 13 bytes.
  - dCSWSignature is not 53425355h.
  - dCSWTag does not match the CBW dCBWTag
  - bCSWStatus is not 00h, 01h, or 02h.
  - dCSWDataResidue exceeds the CBW dCBWDataTransferLength when bCSWStatus is 00h or 01h. (This condition was deleted in S1R72U16XXXE200.)
- A single attempt is made to re-obtain the CSW if an invalid CSW is obtained or if the CSW obtained failed.
- Reset Recovery is performed if any of the following conditions apply (Ends in phase error):
  - Storage device reset request from the IDE function.
  - STALL is returned as a response of CBW.
  - The CSW bCSWStatus is 02h.
  - The CBW cannot be received by the storage device.
  - An error is returned from the storage device for the Clear feature request.
  - CSW acquisition fails twice.
  - A packet error occurs three times in succession during data transfers.

2.8.4 TPL

The TPL (Target Peripheral List) is a list of supported USB devices. Depending on TPL settings, all USB devices (excluding USB hubs) not listed will be treated as unsupported devices. Embedded Host Compliance stipulates TPL implementation, and settings must be made when obtaining logos from a certification body. For detailed information, see the *S1R72U16 Embedded Host Compliance Guide.*

The TPL for this LSI can be set using download function (see "2.7.7 Download Functions"). The TPL data blocks downloaded are configured as shown below. Up to 44 blocks can be set in the list. Compatibility cannot be guaranteed if more than 44 blocks are set.

Table 2.18 TPL data configuration (10 bytes)

Item	Size (Byte)	Details	Value	Remarks
idVendor	2	Vendor ID		
idProduct	2	Product ID		
bcdDevice	2	Device revision		revision
bClass	1	Class ID	08h	Mass Storage Class
bSubClass	1	Subclass ID	01h, 02h, 03h, 05h, 06h	ATAPI, SCSI
bProtocol	1	Protocol ID	50h	Bulk Only Transport
Flag	1	Enabled flags	01h: Vendor ID enabled 02h: Product ID enabled 04h: USB revision enabled 10h: Class ID enabled 20h: Subclass ID enabled 40h: Protocol ID enabled	Validity is specified for multiple enabled flags using OR logic. Example 1: 03h if only vendor ID and product ID are enabled Example 2: 53h if vendor ID, product ID, class ID, and protocol ID are enabled

* 2-byte data is handled as LSB first. (Example: For 1234h, first byte is 34h and second byte is 12h)

* Values need not be specified for items for which TPL data enabled flags have not been set. (00h is recommended)

Table 2.19 TPL data list configuration

Offset	List
Byte0 to 9	TPL data 1
Byte10 to 19	TPL data 2
…	…
Byte430 to 439	TPL data 44

2.8.5 NSF

NSF (No Silent Failures) is a function for notifying the main CPU of errors detected by the USB function. Embedded Host Compliance stipulates NFL implementation and is required when obtaining logos from a certification body. For detailed information, see the *S1R72U16 Embedded Host Compliance Guide*.

There are four types of NSF, as shown below. They can be checked using ports 14 to 17 on the LSI.

- Unsupported Device
  Occurs when an unsupported USB device is detected. Can be checked using port 14 on the LSI.
- Too Many Devices
  Occurs when a third or subsequent storage device is detected. Can be checked using port 15 on the LSI.
- Too Many Hubs
  Occurs when a fourth or subsequent USB hub is detected. Can be checked using port 16 on the LSI.
- VBUS Over Current
  Occurs when an overcurrent is detected in VBUS. Can be checked using port 17 on the LSI.

Ports 14 to 17 switch to High if an NSF occurs and return to Low when the NSF is cleared. The conditions of occurrence and cancel timing are described in the following sections.

2.8.5.1 Unsupported Device

Occurs when an unsupported USB device is detected. This cannot be cleared until all unsupported devices have been disconnected.

Table 2.20 With two unsupported devices

Step	USB device connection status	GPO pin status
1	No unsupported device present	Low
2	Unsupported device A connected	High
3	Unsupported device B connected	High
4	Unsupported device B disconnected	High
5	Unsupported device A disconnected	Low

2.8.5.2 Too Many Devices

Occurs when a third or subsequent storage device is detected. This cannot be cleared until the third and subsequent storage devices detected have all been disconnected. Disconnecting the first and second storage devices detected will not clear the NSF unless the third and subsequent storage devices detected are disconnected.

Table 2.21 With four storage devices

Step	USB device connection status	GPO pin status
1	Two storage devices A and B present	Low
2	Storage device C connected	High
3	Storage device D connected	High
4	Storage device C disconnected	High
5	Storage device A disconnected	High
6	Storage device D disconnected	Low

2.8.5.3 Too Many Hubs

Occurs when a fourth or subsequent USB hub is detected. This cannot be cleared until the fourth and subsequent USB hubs detected have all been disconnected. Disconnecting the second and third USB hubs detected will not clear the NSF; the fourth and subsequent USB hubs detected must be disconnected.

Table 2.22 With five USB hubs

Step	USB device connection status	GPO pin status
1	Three USB hubs A, B, and C present	Low
2	USB hub D connected to USB hub A	High
3	USB hub E connected to USB hub A	High
4	USB hub D disconnected	High
5	USB hub C disconnected	High
6	USB hub E disconnected	Low

2.8.5.4 VBUS Over Current

Occurs when an overcurrent is detected in VBUS. This is automatically cleared after approximately one second has elapsed.

All USB devices connected are immediately disconnected when a VBUS Over Current occurs. They are then reconnected when the NFS is cleared, but the disconnection may recur if the cause of the overcurrent is not removed.

2.9 Development Support Functions

The following functions can be used by connecting the serial interface of the LSI to the RS-232 interface of a PC.

2.9.1 History Display Function

This displays the LSI internal execution history on a PC, facilitating system debugging in product development. For detailed information, see the *S1R72U16 Development Support Manual*.

2.9.2 USB Logo Certification Support Function

This is used when switching to test mode for electrical tests in certification testing. For detailed information, see the *S1R72U16 Embedded Host Compliance Guide*.

3. Registers

This LSI includes ATA task file registers defined in the ATA/ATAPI standards. The main CPU is capable of controlling the LSI by accessing these registers.

For detailed information on the ATA task file registers, refer to the *AT Attachment with Packet Interface - 4, 5, 6 (ATA/ATAPI - 4, 5, 6)* standards document.

The register initial value of ATA/ATAPI mode is shown in Table 3.1.

Table 3.1 The register initial value

Register	ATA mode	ATAPI mode
Sector Count	01h	01h
LBA Low	01h	01h
LBA Mid	00h	14h
LBA High	00h	EBh
Device	00h	00h
Status	50h	00h

Appendix A: ATA to ATAPI Conversion Specifications

This appendix describes ATA to ATAPI conversion specifications.

Values are described as shown below.

- ( ) indicates fixed values, < > indicates example values. (Values of the register in the form xxh are hexadecimal, xx are binary.)
- Values shown as Reserved, Obsolete, PAD, na, or obs are 0.

IDLE

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Timer period value							
Sector Number(LBA Low)	na							
Cylinder Low(LBA Mid)	na							
Cylinder High(LBA High)	na							
Device/Head	obs	na	obs	DEV	na			
Command	(E3h)							

○ Processing method

Convert to START/STOP UNIT command.

bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code(1Bh)							
1	Reserved							Immed(0)
2	Reserved							
3	Reserved						Format-Layer Number(00)	
4	Power Conditions(0000)				Reserved	FL(0)	LoEJ(0)	Start(1)
5	Control(00h)							
6	PAD							
7								
8								
9								
10								
11								

* IDLE command Timer period value is not used.

IDLE IMMEDIATE

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number(LBA Low)	na							
Cylinder Low(LBA Mid)	na							
Cylinder High(LBA High)	na							
Device/Head	obs	na	obs	DEV	na			
Command	(E1h)							

○ Processing method

Convert to START/STOP UNIT command.

bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code(1Bh)							
1	Reserved							Immed(1)
2	Reserved							
3	Reserved						Format-Layer Number(00)	
4	Power Conditions(0000)				Reserved	FL(0)	LoEJ(0)	Start(1)
5	Control(00h)							
6	PAD							
7								
8								
9								
10								
11								

SEEK

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number(LBA Low)	LBA[7:0] <67h>							
Cylinder Low(LBA Mid)	LBA[15:8] <45h>							
Cylinder High(LBA High)	LBA[23:16] <23h>							
Device/Head	obs	LBA	obs	DEV	LBA[27:24] <1h>			
Command	(70h)							

○ Processing method

Convert to SEEK (10) command.

bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code(2Bh)							
1	Reserved							
2	Logical Block Address[31:24] <01h>							
3	Logical Block Address[23:16] <23h>							
4	Logical Block Address[15:8] <45h>							
5	Logical Block Address[7:0] <67h>							
6	Reserved							
7	Reserved							
8	Reserved							
9	Control Byte (00h)							
10	PAD							
11								

STANDBY

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Timer period value							
Sector Number(LBA Low)	na							
Cylinder Low(LBA Mid)	na							
Cylinder High(LBA High)	na							
Device/Head	obs	na	obs	DEV	na			
Command	(E2h)							

○ Processing method

Convert to START/STOP UNIT command.

bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code(1Bh)							
1	Reserved							Immed(0)
2	Reserved							
3	Reserved						Format-Layer Number(00)	
4	Power Conditions(0000)				Reserved	FL(0)	LoEJ(0)	Start(0)
5	Control(00h)							
6	PAD							
7								
8								
9								
10								
11								

* STANDBY command Timer period value is not used.

STANDBY IMMEDIATE

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number(LBA Low)	na							
Cylinder Low(LBA Mid)	na							
Cylinder High(LBA High)	na							
Device/Head	obs	na	obs	DEV	na			
Command	(E0h)							

○ Processing method

Convert to START/STOP UNIT command.

bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code(1Bh)							
1	Reserved							Immed(1)
2	Reserved							
3	Reserved						Format-Layer Number(00)	
4	Power Conditions(0000)				Reserved	FL(0)	LoEJ(0)	Start(0)
5	Control(00h)							
6	PAD							
7								
8								
9								
10								
11								

READ SECTOR(s)

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count <98h>							
Sector Number(LBA Low)	LBA[7:0] <67h>							
Cylinder Low(LBA Mid)	LBA[15:8] <45h>							
Cylinder High(LBA High)	LBA[23:16] <23h>							
Device/Head	obs	LBA	obs	DEV	LBA[27:24] <1h>			
Command	(20h)							

○ Processing method

Convert to READ (10) command.

bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code(28h)							
1	Reserved			DPO(0)	FUA(0)	Reserved		Obsolete
2	Logical Block Address[31:24] <01h>							
3	Logical Block Address[23:16] <23h>							
4	Logical Block Address[15:8] <45h>							
5	Logical Block Address[7:0] <67h>							
6	Reserved							
7	Transfer Length[15:8] <00h>							
8	Transfer Length[7:0] <98h>							
9	Control(00h)							
10	PAD							
11								

* The READ (10) command Transfer Length [15:8] will be 01h, and Transfer Length [7:0] will be 00h when the READ SECTOR (S) command Sector Count is 00h, since this indicates 256 sector specification.

READ DMA

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count <98h>							
Sector Number(LBA Low)	LBA[7:0] <67h>							
Cylinder Low(LBA Mid)	LBA[15:8] <45h>							
Cylinder High(LBA High)	LBA[23:16] <23h>							
Device/Head	obs	LBA	obs	DEV	LBA[27:24] <1h>			
Command	(C8h)							

○ Processing method

Convert to READ (10) command. See READ SECTOR (S) command for conversion details.

READ MULTIPLE

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count <98h>							
Sector Number(LBA Low)	LBA[7:0] <67h>							
Cylinder Low(LBA Mid)	LBA[15:8] <45h>							
Cylinder High(LBA High)	LBA[23:16] <23h>							
Device/Head	obs	LBA	obs	DEV	LBA[27:24] <1h>			
Command	(C4h)							

○ Processing method

Convert to READ (10) command. See READ SECTOR (S) command for conversion details.

WRITE SECTOR(S)

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count <12h>							
Sector Number(LBA Low)	LBA[7:0] <43h>							
Cylinder Low(LBA Mid)	LBA[15:8] <65h>							
Cylinder High(LBA High)	LBA[23:16] <87h>							
Device/Head	obs	LBA	obs	DEV	LBA[27:24] <9h>			
Command	(30h)							

○ Processing method

Convert to WRITE (10) command.

bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code(2Ah)							
1	Reserved				FUA(0)	TSR(0)	Reserved	
2	Logical Block Address[31:24] <09h>							
3	Logical Block Address[23:16] <87h>							
4	Logical Block Address[15:8] <65h>							
5	Logical Block Address[7:0] <43h>							
6	Reserved							
7	Transfer Length[15:8] <00h>							
8	Transfer Length[7:0] <12h>							
9	Control(00h)							
10	PAD							
11								

* The WRITE (10) command Transfer Length [15:8] will be 01h and Transfer Length [7:0] will be 00h when the WRITE SECTOR (S) command Sector Count is 00h, since this indicates 256 sector specification.

WRITE DMA

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count <12h>							
Sector Number(LBA Low)	LBA[7:0] <43h>							
Cylinder Low(LBA Mid)	LBA[15:8] <65h>							
Cylinder High(LBA High)	LBA[23:16] <87h>							
Device/Head	obs	LBA	obs	DEV	LBA[27:24] <9h>			
Command	(CAh)							

○ Processing method

Convert to WRITE (10) command. See WRITE SECTOR (S) command for conversion details.

WRITE MULTIPLE

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count <12h>							
Sector Number(LBA Low)	LBA[7:0] <43h>							
Cylinder Low(LBA Mid)	LBA[15:8] <65h>							
Cylinder High(LBA High)	LBA[23:16] <87h>							
Device/Head	obs	LBA	obs	DEV	LBA[27:24] <9h>			
Command	(C5h)							

○ Processing method

Convert to WRITE (10) command. See WRITE SECTOR (S) command for conversion details.

READ SECTOR(S) EXT

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	Reserved							
Previous	Reserved							
Sector Count	Sector Count[7:0] <76h>							
Previous	Sector Count[15:8] <98h>							
Sector Number(LBA Low)	LBA[7:0] <BCh>							
Previous	LBA[31:24] <56h>							
Cylinder Low(LBA Mid)	LBA[15:8] <9Ah>							
Previous	LBA[39:32] <34h>							
Cylinder High(LBA High)	LBA[23:16] <78h>							
Previous	LBA[47:40] <12h>							
Device/Head	obs	LBA	obs	DEV	Reserved			
Command	(24h)							

○ Processing method

Convert to READ (10) command if Sector Count is a value other than 0000h, and READ (12) command if Sector Count is 0000h.

* The READ SECTOR (S) EXT command LBA [47:40] and LBA [39:32] are not used, since they cannot be set to READ commands.

[READ (10)]

bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code(28h)							
1	Reserved			DPO(0)	FUA(0)	Reserved		Obsolete
2	Logical Block Address[31:24] <56h>							
3	Logical Block Address[23:16] <78h>							
4	Logical Block Address[15:8] <9Ah>							
5	Logical Block Address[7:0] <BCh>							
6	Reserved							
7	Transfer Length[15:8] <98h>							
8	Transfer Length[7:0] <76h>							
9	Control(00h)							
10	PAD							
11								

[READ (12)]

bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code(A8h)							
1	Reserved			DPO(0)	FUA(0)	Reserved		Obsolete
2	Logical Block Address[31:24] <56h>							
3	Logical Block Address[23:16] <78h>							
4	Logical Block Address[15:8] <9Ah>							
5	Logical Block Address[7:0] <BCh>							
6	Transfer Length[31:24] <00h>							
7	Transfer Length[23:16] <01h>							
8	Transfer Length[15:8] <00h>							
9	Transfer Length[7:0] <00h>							
10	Reserved							
11	Control(00h)							

* Conversion is to READ (12) command when the READ SECTOR (S) EXT command Sector Count [15:8] and Sector Count [7:0] are 00h, since this indicates 65536 sector specification. Transfer Length [23:16] will be 01h, Transfer Length [15:8] will be 00h, and Transfer Length [7:0] will be 00h.

READ DMA EXT

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	Reserved							
Previous	Reserved							
Sector Count	Sector Count[7:0] <76h>							
Previous	Sector Count[15:8] <98h>							
Sector Number(LBA Low)	LBA[7:0] <BCh>							
Previous	LBA[31:24] <56h>							
Cylinder Low(LBA Mid)	LBA[15:8] <9Ah>							
Previous	LBA[39:32] <34h>							
Cylinder High(LBA High)	LBA[23:16] <78h>							
Previous	LBA[47:40] <12h>							
Device/Head	obs	LBA	obs	DEV	Reserved			
Command	(25h)							

○ Processing method

RConvert to READ (10) or READ (12) command. See READ SECTOR (S) EXT command for conversion details.

READ MULTIPLE EXT

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	Reserved							
Previous	Reserved							
Sector Count	Sector Count[7:0] <76h>							
Previous	Sector Count[15:8] <98h>							
Sector Number(LBA Low)	LBA[7:0] <BCh>							
Previous	LBA[31:24] <56h>							
Cylinder Low(LBA Mid)	LBA[15:8] <9Ah>							
Previous	LBA[39:32] <34h>							
Cylinder High(LBA High)	LBA[23:16] <78h>							
Previous	LBA[47:40] <12h>							
Device/Head	obs	LBA	obs	DEV	Reserved			
Command	(29h)							

○ Processing method

Convert to READ (10) or READ (12) command. See READ SECTOR (S) EXT command for conversion details.

WRITE SECTOR(S) EXT

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	Reserved							
Previous	Reserved							
Sector Count	Sector Count[7:0] <34h>							
Previous	Sector Count[15:8] <12h>							
Sector Number(LBA Low)	LBA[7:0] <54h>							
Previous	LBA[31:24] <BAh>							
Cylinder Low(LBA Mid)	LBA[15:8] <76h>							
Previous	LBA[39:32] <DCh>							
Cylinder High(LBA High)	LBA[23:16] <98h>							
Previous	LBA[47:40] <FEh>							
Device/Head	obs	LBA	obs	DEV	Reserved			
Command	(34h)							

○ Processing method

Convert to WRITE (10) command if Sector Count is a value other than 0000h, and WRITE (12) command if Sector Count is 0000h.

* The WRITE SECTOR (S) EXT command LBA [47:40] and LBA [39:32] are not used, since they cannot be set to WRITE commands.

[WRITE (10)]

bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code(2Ah)							
1	Reserved				FUA(0)	TSR(0)	Reserved	
2	Logical Block Address[31:24] <BAh>							
3	Logical Block Address[23:16] <98h>							
4	Logical Block Address[15:8] <76h>							
5	Logical Block Address[7:0] <54h>							
6	Reserved							
7	Transfer Length[15:8] <12h>							
8	Transfer Length[7:0] <34h>							
9	Control(00h)							
10	PAD							
11								

[WRITE (12)]

bit / Byte	7	6	5	4	3	2	1	0
0	Operation Code(AAh)							
1	Reserved				FUA(0)	TSR(0)	Reserved	
2	Logical Block Address[31:24] <BAh>							
3	Logical Block Address[23:16] <98h>							
4	Logical Block Address[15:8] <76h>							
5	Logical Block Address[7:0] <54h>							
6	Transfer Length[31:24] <00h>							
7	Transfer Length[23:16] <01h>							
8	Transfer Length[15:8] <00h>							
9	Transfer Length[7:0] <00h>							
10	Streaming (0)	VNR(0)	Reserved					
11	Control(00h)							

* Conversion is to WRITE (12) command when the WRITE SECTOR (S) EXT command Sector Count [15:8] and Sector Count [7:0] are 00h, since this indicates 65536 sector specification. Transfer Length [23:16] will be 01h, Transfer Length [15:8] will be 00h, and Transfer Length [7:0] will be 00h.

WRITE DMA EXT

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	Reserved							
Previous	Reserved							
Sector Count	Sector Count[7:0] <34h>							
Previous	Sector Count[15:8] <12h>							
Sector Number(LBA Low)	LBA[7:0] <54h>							
Previous	LBA[31:24] <BAh>							
Cylinder Low(LBA Mid)	LBA[15:8] <76h>							
Previous	LBA[39:32] <DCh>							
Cylinder High(LBA High)	LBA[23:16] <98h>							
Previous	LBA[47:40] <FEh>							
Device/Head	obs	LBA	obs	DEV	Reserved			
Command	(35h)							

○ Processing method

Convert to WRITE (10) or WRITE (12) command. See WRITE SECTOR (S) EXT command for conversion details.

WRITE MULTIPLE EXT

○ Command format

bit / Register	7	6	5	4	3	2	1	0
Features	Reserved							
Previous	Reserved							
Sector Count	Sector Count[7:0] <34h>							
Previous	Sector Count[15:8] <12h>							
Sector Number(LBA Low)	LBA[7:0] <54h>							
Previous	LBA[31:24] <BAh>							
Cylinder Low(LBA Mid)	LBA[15:8] <76h>							
Previous	LBA[39:32] <DCh>							
Cylinder High(LBA High)	LBA[23:16] <98h>							
Previous	LBA[47:40] <FEh>							
Device/Head	obs	LBA	obs	DEV	Reserved			
Command	(39h)							

○ Processing method

Convert to WRITE (10) or WRITE (12) command. See WRITE SECTOR (S) EXT command for conversion details.

Revision History

Date	Revision details			
	Rev.	Page	Type	Details
05/15/2007	0.10	All	New	Newly established
05/31/2007	0.20	All	Revise	Changed Contents to separate page and change subsequent page numbering.
		2	Add	Added internal status notification, and change subsequent 2.x section numbering.
		5	Add	Added status after resetting.
		6	Add	Added the following sentence to section 2.5.2. “In two-device mode, the LSI does not switch to Sleep state unless SLEEP commands are issued for both the master and slave, even if only one storage device is actually present.”
		7	Correct	Corrected Fig. 2.9 and add DASP signal for Master.
		8 to 10	Correct	Corrected remarks in Tables 2.3 to 2.8.
		20	Add/ correct	Added interrupt detection method when pins XChgInt and XCD0/XCD1 are used as interrupt signals in section 2.6.6.2, and correct itemized list.
		21 to 24	Correct	Corrected location of state changes in Figures 2.15 to 2.19.
		26 to 31	Revise	Renumbered pages for sections within section 2.6.
		29	Correct	Changed following items in Table 2.16 and add values. bDeviceClass → bClass, bDeviceSubClass → bSubClass, bDeviceProtocol → bProtocol
07/01/2007	1.00	6	Add	Added details of Status bit to Table 2.2 indicating that command is being processed.
		8	Add	Added details to Section 2.5 of commands issued independently by LSI, and renumbered subsequent Section 2.X.
		13, 14	Correct	Standardized details in Tables 2.5 and 2.8.
		15, 16	Correct	Standardized REQUEST SENSE details in Tables 2.9 and 2.10.
		24	Add	Added details of Status bit to Section 2.7.5.1 indicating Busy state.
		25	Add	Added details and notes for unsupported commands to Section 2.7.5.3.
		27 to 34	Correct	Changed Status register bit 1 to ChgInt bit, and changed pins to connect/disconnect pins.
		31	Add	Added explanation for (3) in Fig. 2.16.
		37	Add/ correct	Added subclass details to Section 2.8.1 and corrected description of unsupported USB devices.
		40	Add	Added details of ending state for Reset Recovery in Section 2.8.3.
10/15/2007	1.10	Scope	Add	Added “notice.”
		2	Add	Added description of attribute memory to indicate inconsistency with CF standards.
		23	Correct	Added “DRQ bit =1” in Fig. 2.12.
04/01/2008	2.00	2,3,6,7,11, 16 to 20, 28, 29, 35, 37, 40, 41, 45 to 48	Correct	Corrected details for Section 2, 2.3, 2.8.1, 2.8.3, 3 and Appendix A. Corrected details for Table 2.2, 2.4, 2.5, 2.11, 2.12, 2.14, 2.15, 2.16, 2.18.

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Document Code: 411135603
First Issue July 2007
Printed April 2008 in JAPAN