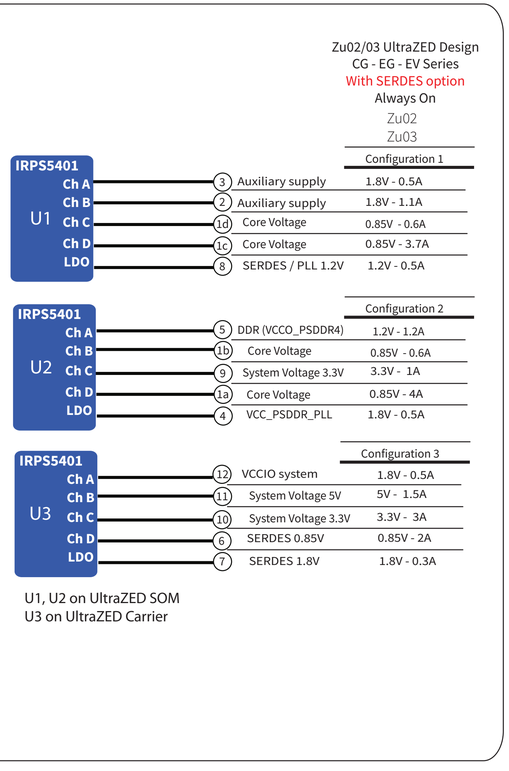
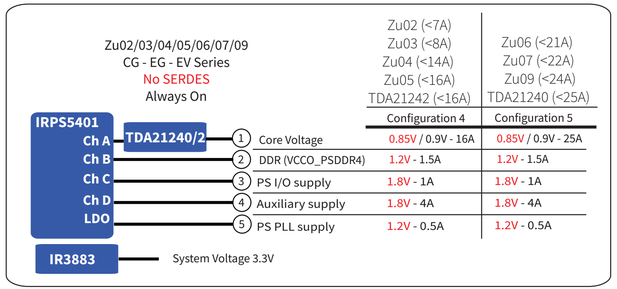
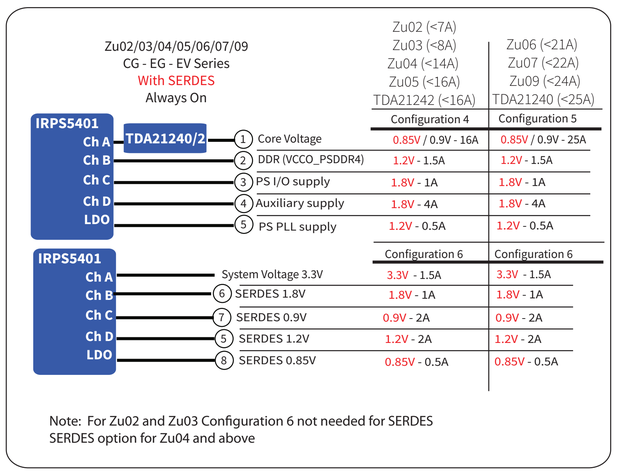
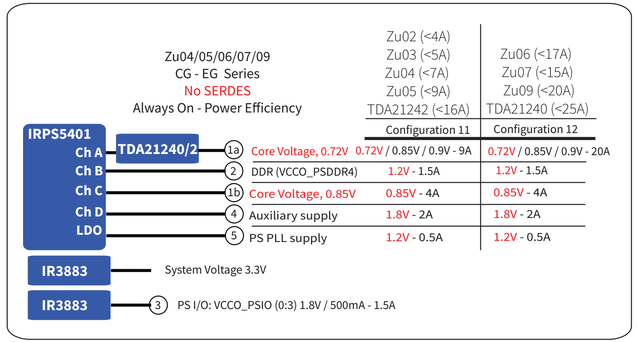
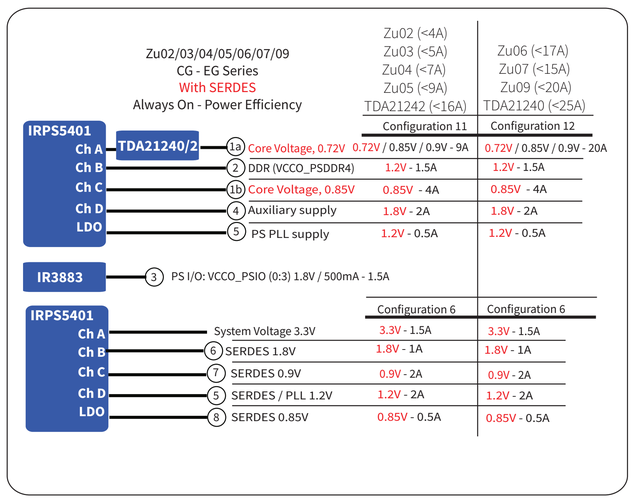


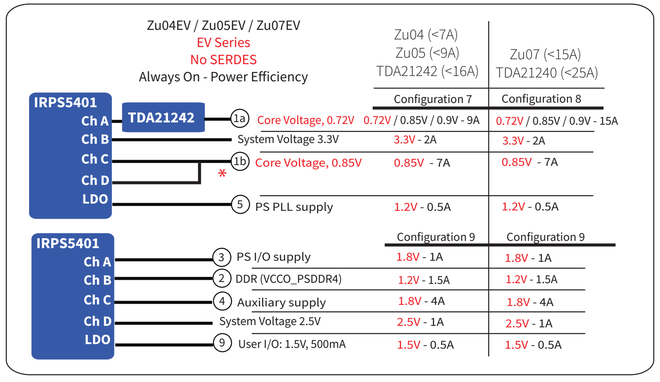


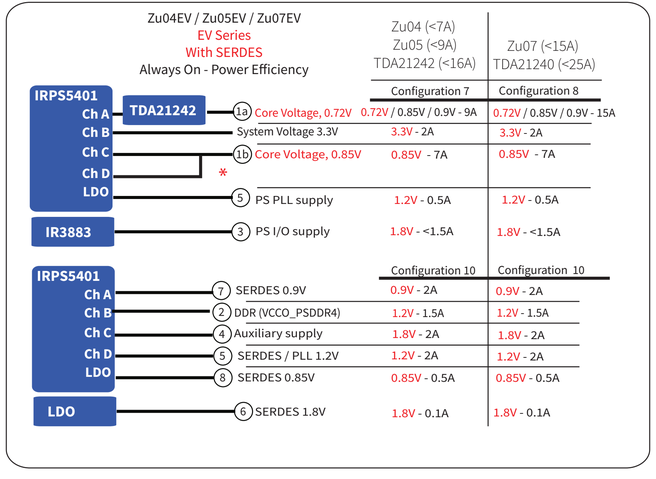


Note: For Zu02 and Zu03 Configuration 6 not needed for SERDES
SERDES option for Zu04 and above









Xilinx
Zynq UltraScale+ MPSoC
Power Macros for
Zu02 to Zu19
CG / EG / EV SERIES

Part Number: 12 Configurations
IRPS5401MXI03TRP

For Zu11 to Zu19 see page 2

See also Summary Table for Configuration files for all 12 designs, page 2

*For Zu04/05/07EV:

Xilinx may update UG583 where the VCCINT_VCU rail will be separated from the VCCBRAM rail to 0.9V; in this case Configurations 7 and 8, the ch C can be dedicated to the VCCBRAM rails at 0.85V and the ch D can be re-purposed for VCCINT_VCU at 0.9V. Contact Infineon for design details. tony.ochoa@infineon.com

Infineon - Avnet Zynq UltraScale+ MPSoC Power Cookbook Macro Boards

Configuration 1

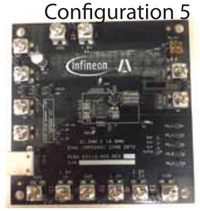
Configuration 4

Configuration 7

Configuration 10

Configuration 2

Configuration 5



Configuration 8

Configuration 11

Configuration 3

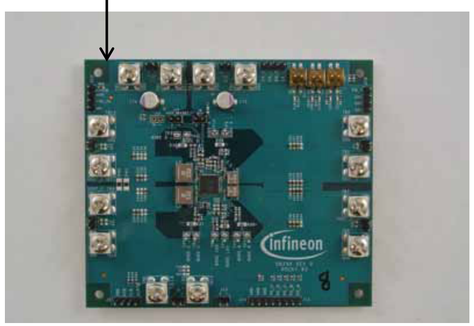
Configuration 6

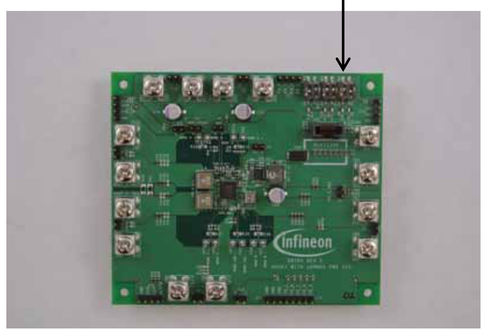
Configuration 9

Configuration 12

Infineon - Standard Evaluation Boards

Board	Family	Description
EVAL_PS5401-INT	DC/DC Converter	5 output PMIC • 4A+4A+2A+2A+0.5A
EVAL_PS5401-25A	DC/DC Converter	5 output PMIC with 25A PowerStage • 4A+4A+2A+0.5A + 25A
EVAL_PS5401-40A	DC/DC Converter	5 output PMIC with 40A PowerStage • 4A+4A+2A+0.5A + 40A





Infineon DC/DC PMIC	MTP Resistor Address	Application – Voltage Outputs	PowerStage	EXT_A INDUCTOR	Zynq US+ config #
IRPS5401MXI03TRP Part Number: 12 Configurations	8870	1.8/1.8/.85/.85/1.2	N/A		1
	10000	1.2/.85/3.3/.85/1.8	N/A		2
	11000	1.8/5/3.3/.85/1.8	N/A		3
	2320	.85/1.2/1.8/1.8/1.2	TDA21242	VLB10050HT-R20M	4
	2870	.85/1.2/1.8/1.8/1.2	TDA21240	VLB10050HT-R12M	5
	3480	3.3/1.8/.9/1.2/.85	N/A		6
	4120	.72/3.3/.85/1.2	TDA21242	VLB10050HT-R30M	7
	4750	.72/3.3/.85/1.2	TDA21240	VLB10050HT-R20M	8
	5490	1.8/1.2/1.8/2.5/1.5	N/A		9
	6190	.9/1.2/1.8/1.2/.85	N/A		10
	6980	.72/1.2/.85/1.8/1.2	TDA21242	VLB10050HT-R30M	11
	7870	.72/1.2/.85/1.8/1.2	TDA21240	VLB10050HT-R20M	12

For Zu11 to Zu19:

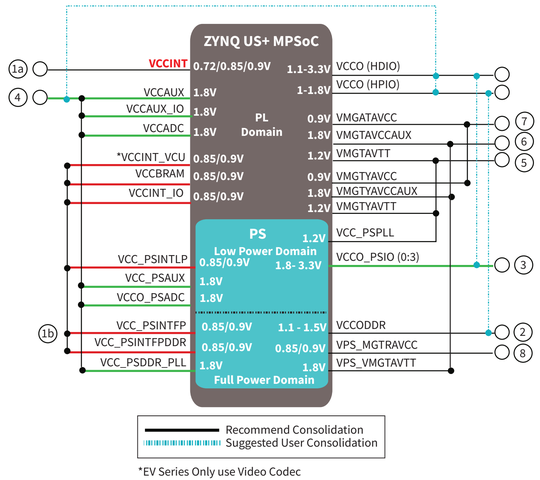
For Zu15 use Zu09 Configuration 5* or 12* & 6

For Zu11 use Zu09 Configuration 5* or 12* & 6 (for SERDES <2A)
if SERDES < 6A, use IR38060 for MGTAVCC/VTT
see “EVAL_38060-PMAC1” for higher current SERDES

For Zu17/Zu19 use Zu09 Configuration 5* or 12* & 6 (for SERDES <2A)
if SERDES < 6A, use IR38060 for MGTAVCC/VTT
if SERDES <10A, use IR38062 for MGTAVTT
* Adjustment needed for L, C, Ki, Kp for chA to increase current to 25-40A

Xilinx Zynq UltraScale+ MPSoC
Power Macros for
Zu02 to Zu19
CG / EG / EV SERIES

ZYNQ UltraScale+
Always On - Power Efficiency
Separate Core Voltage @ 0.72V
Rail Consolidation



*EV Series Only use Video Codec

Zu04/05/06/07/09
CG - EG Series
No SERDES
Always On - Power Efficiency

			Zu06 (<17A) Zu07 (<15A) Zu09 (<20A) TDA21240 (<25A)
			Configuration 12
IRPS5401 Ch A	TDA21240/2	1a Core Voltage, 0.72V	0.72V / 0.85V / 0.9V - 20A
Ch B		2 DDR (VCCO_PSDDR4)	1.2V - 1.5A
Ch C		1b Core Voltage, 0.85V	0.85V - 4A
Ch D		4 Auxiliary supply	1.8V - 2A
LDO		5 PS PLL supply	1.2V - 0.5A
IR3883		System Voltage 3.3V	
IR3883		3 PS I/O: VCCO_PSIO (0:3) 1.8V / 500mA - 1.5A	

Zu02/03/04/05/06/07/09
CG - EG Series
With SERDES
Always On - Power Efficiency

			Zu06 (<17A) Zu07 (<15A) Zu09 (<20A) TDA21240 (<25A)
			Configuration 12
IRPS5401 Ch A	TDA21240/2	1a Core Voltage, 0.72V	0.72V / 0.85V / 0.9V - 20A
Ch B		2 DDR (VCCO_PSDDR4)	1.2V - 1.5A
Ch C		1b Core Voltage, 0.85V	0.85V - 4A
Ch D		4 Auxiliary supply	1.8V - 2A
LDO		5 PS PLL supply	1.2V - 0.5A
IR3883		3 PS I/O: VCCO_PSIO (0:3) 1.8V / 500mA - 1.5A	
			Configuration 6
IRPS5401 Ch A		System Voltage 3.3V	3.3V - 1.5A
Ch B		6 SERDES 1.8V	1.8V - 1A
Ch C		7 SERDES 0.9V	0.9V - 2A
Ch D		5 SERDES / PLL 1.2V	1.2V - 2A
LDO		8 SERDES 0.85V	0.85V - 0.5A

For Zu17/Zu19 use Zu09 Configuration 5 & 6 (for SERDES <2A)
OR
use Zu09 Configurations 12 & 6 (for SERDES <2A)

1) How to Adjust the Vcore voltage for the Zu09 design to create the Zu19 design.

For a 40A output (modify chA of Configuration 5 or 12):

- LOUT = PA2607-151NL
- COUT = 1x 470uF POS, 2x 100uF MLCC, 20x 22uF MLCC
- Kp = 37dec
- Ki = 45dec

2) If many SERDES lanes used you then do NOT use Configuration 6 but instead:

if SERDES < 6A, use IR38060 for MGTAVCC/VTT (see designs on EVAL_38060-PMAC1)
if SERDES <10A, use IR38062 for MGTAVTT

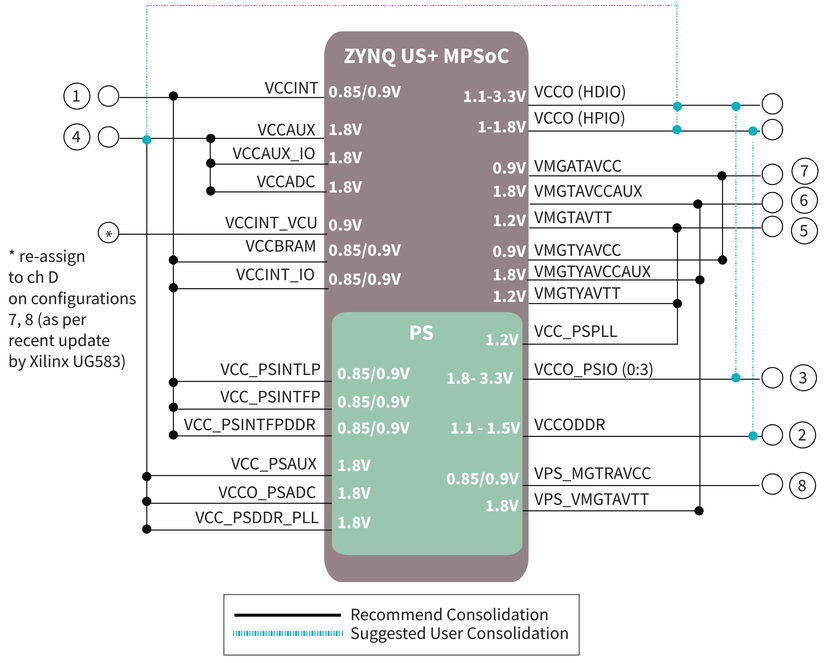
then for smaller SERDES rails, use LDOs
(i.e. VPS_MGTRAVCC. 0.85V / 300mA
VPS_MGTRAVTT / VMGTAVCCAUX / VMGTYVCCAUX. 1.8V / 400mA)

Xilinx
Zynq UltraScale+ MPSoC
Power Macros for
Zu02 to Zu19
CG / EG / EV SERIES

Part Number: 12 Configurations
IRPS5401MXI03TRP

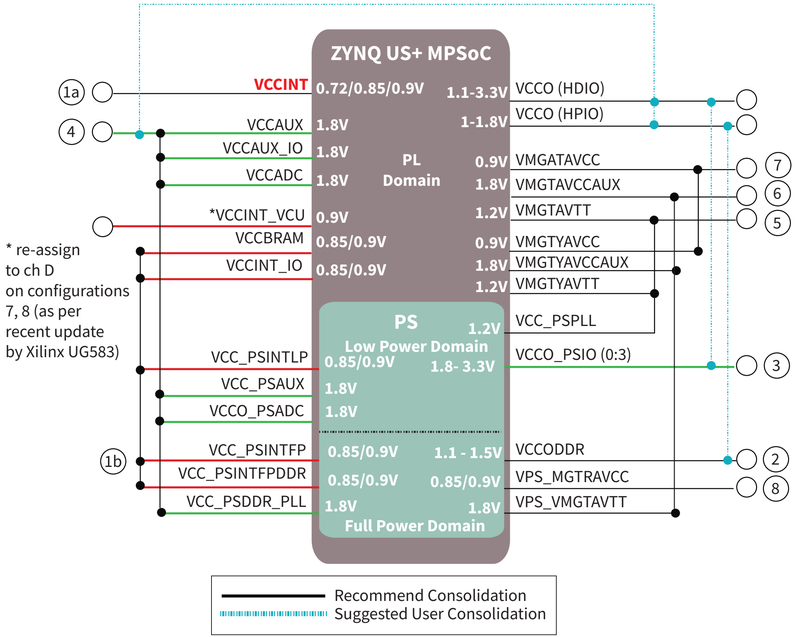
ALWAYS ON: COST-OPTIMIZED POWER RAIL CONSOLIDATION

ZYNQ UltraScale+
Always On
Rail Consolidation



ALWAYS ON: POWER/EFFICIENCY RAIL CONSOLIDATION FOR LOW POWER DEVICES

ZYNQ UltraScale+
Always On - Power Efficiency
Separate Core Voltage @ 0.72V
Rail Consolidation



*EV Series Only use Video Codec

Xilinx
Zynq UltraScale+ MPSoC
Power Macros for
Zu02 to Zu19
CG / EG / EV SERIES

Part Number: 12 Configurations
IRPS5401MXI03TRP

For Zu11 to Zu19 see page 2

See also Summary Table for Configuration files for all 12 designs, page 2