ECE1200

eSPI to LPC Bridge

Features

- Detects and Supports Modern Standby State (S0ix) with Low Standby Current
- ACPI 6.1 Compliant
- Configuration Register Set
  - Compatible with ISA Plug-and-Play Standard
  - Host-Programmable Base Address
- Supports LPC-based SIO and EC devices such as:
  - SCH555x, SCH5347B
  - SCH311x, SCH322x
- eSPI Peripheral Channel Cycles in 64K I/O Space will pass through as LPC I/O cycles, except for the local Plug-and-Play INDEX/DATA portal registers
- eSPI Peripheral Channel Cycles in Memory Space will all pass through as LPC Memory Cycles
- Enhanced Serial Peripheral Interface (eSPI)
  - 1.8V Operation
  - Intel eSPI Base Specification 1.0 compliant
  - Supports the Peripheral Channel and Virtual Wire Channel interfaces
  - Supports up to 50 MHz maximum operating frequency
- LPC Master Interface
  - 3.3V operation
  - Generates LPC Clock on two output pins
  - Provides 24 MHz nominal bus clock frequency
  - Provides CLKRUN# clock control interface
  - LPC Specification 1.1 Compatible
  - LPC I/O and Memory Cycles Supported
  - Supports Serial IRQ Interface, both Continuous and Quiet modes
- XNOR Board Test Mode
- Package Options
  - 40-pin VQFN RoHS Compliant Package (LDX)
- Industrial Temperature Range
  - -40°C to +85°C

Products

Catalog Part Number	Package	Temperature Range	Initial Register Portal Address	Delivery Packaging
ECE1200-I/LD	40-VQFN, sawn (LDX)	Industrial	8Ch	Tray

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1.0 GENERAL DESCRIPTION

The ECE1200 is a device designed to implement a Bridge function from an eSPI-configured Intel Chipset to a legacy downstream system, providing Master interfaces for an LPC bus, Serial IRQ and CLKRUN# features.

The ECE1200 is directly powered by two Suspend (S5) supply planes, at 3.3V and 1.8V nominal. The 1.8V supply is provided on two sets of pins: VTR_18 for I/O pins, and VTR_18_CORE for internal logic. The 3.3V supply VTR_33 is for 3.3V I/O pins only.

The ECE1200 senses a Runtime power plane (VCC) using the pin LPC_EN, which is intended to come from the PCH_PWROK signal supplied from the system. It uses this to emulate VCC-powered functionality on the appropriate pins in order to avoid backdrive in the system.

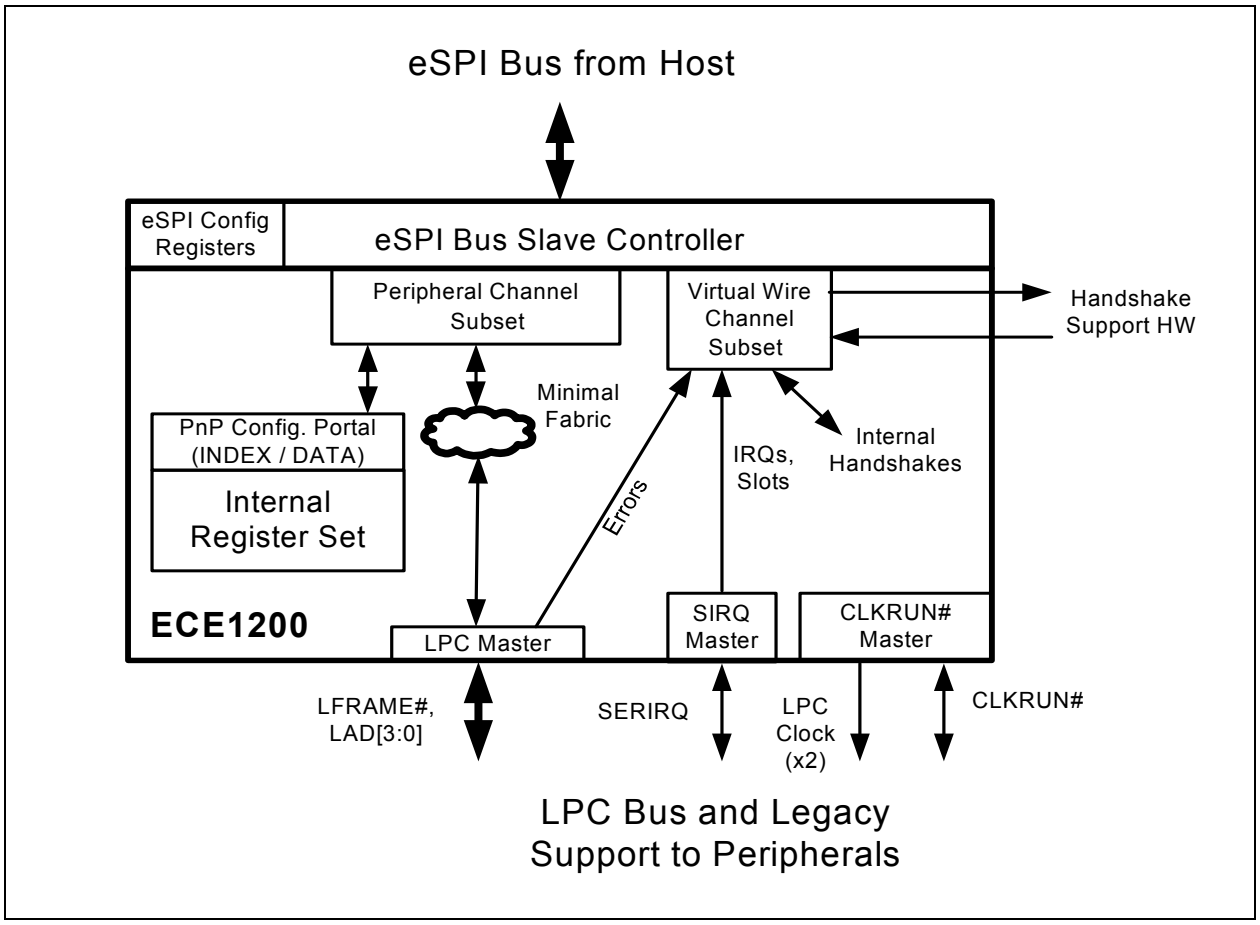


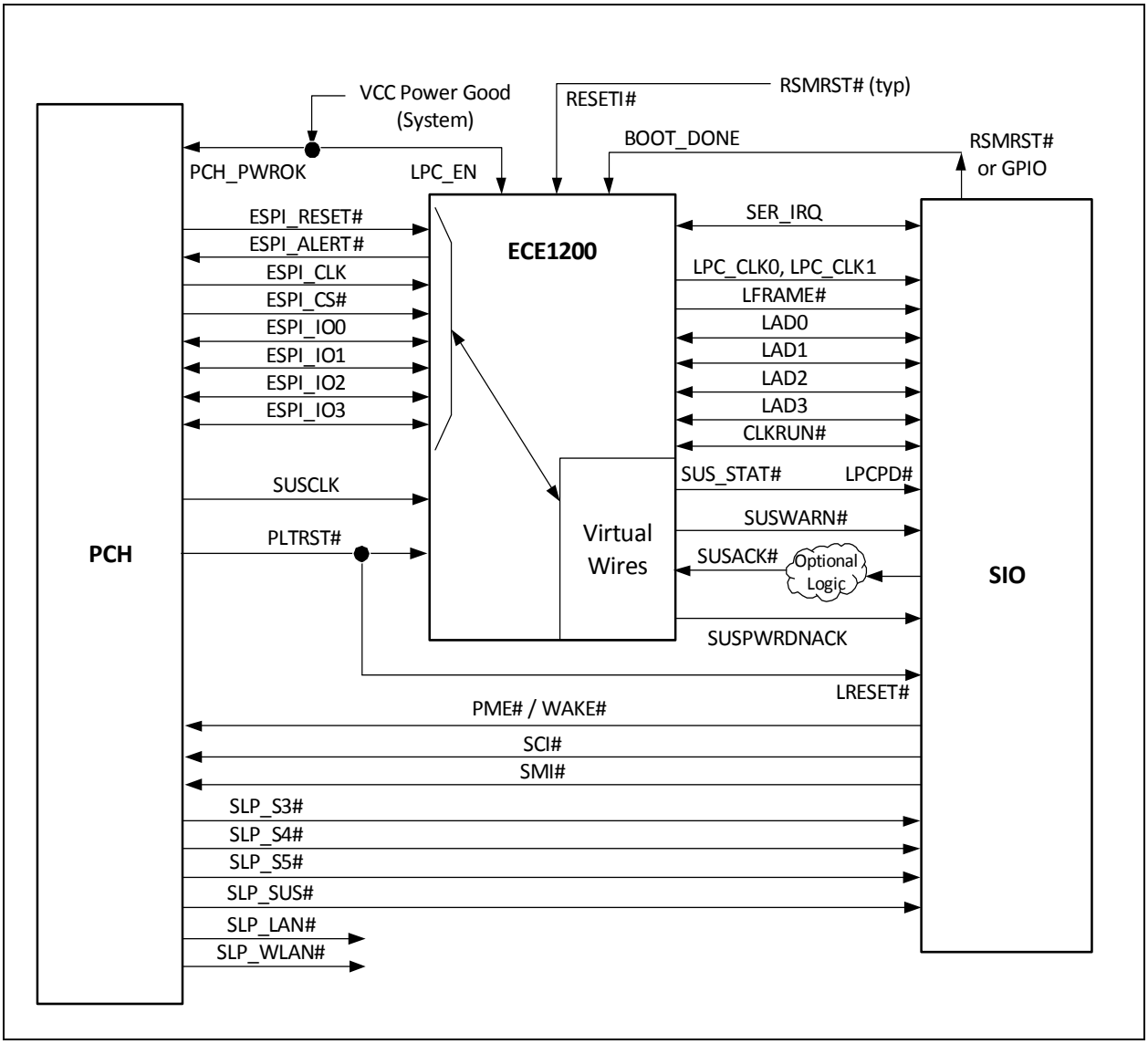
TABLE 1-1: GENERAL TERMINOLOGY

Term	Definition
System Host, or Host Chipset	Refers to the complex of the System CPU and surrounding elements, from which originates the I/O and Memory traffic to the ECE1200 over the eSPI Interface.
PCH	The specific element of the Host Chipset that connects to the ECE1200 from the Host side, serving as the Master in the eSPI protocol, and controlling the pins that serve as Host-side sideband signals to the ECE1200.

1.1 System Block Diagrams

1.1.1 GENERAL SYSTEM BLOCK DIAGRAM

The ECE1200 is shown here as a single eSPI Slave, or the Primary Slave of two or more (on eSPI_CS0#).

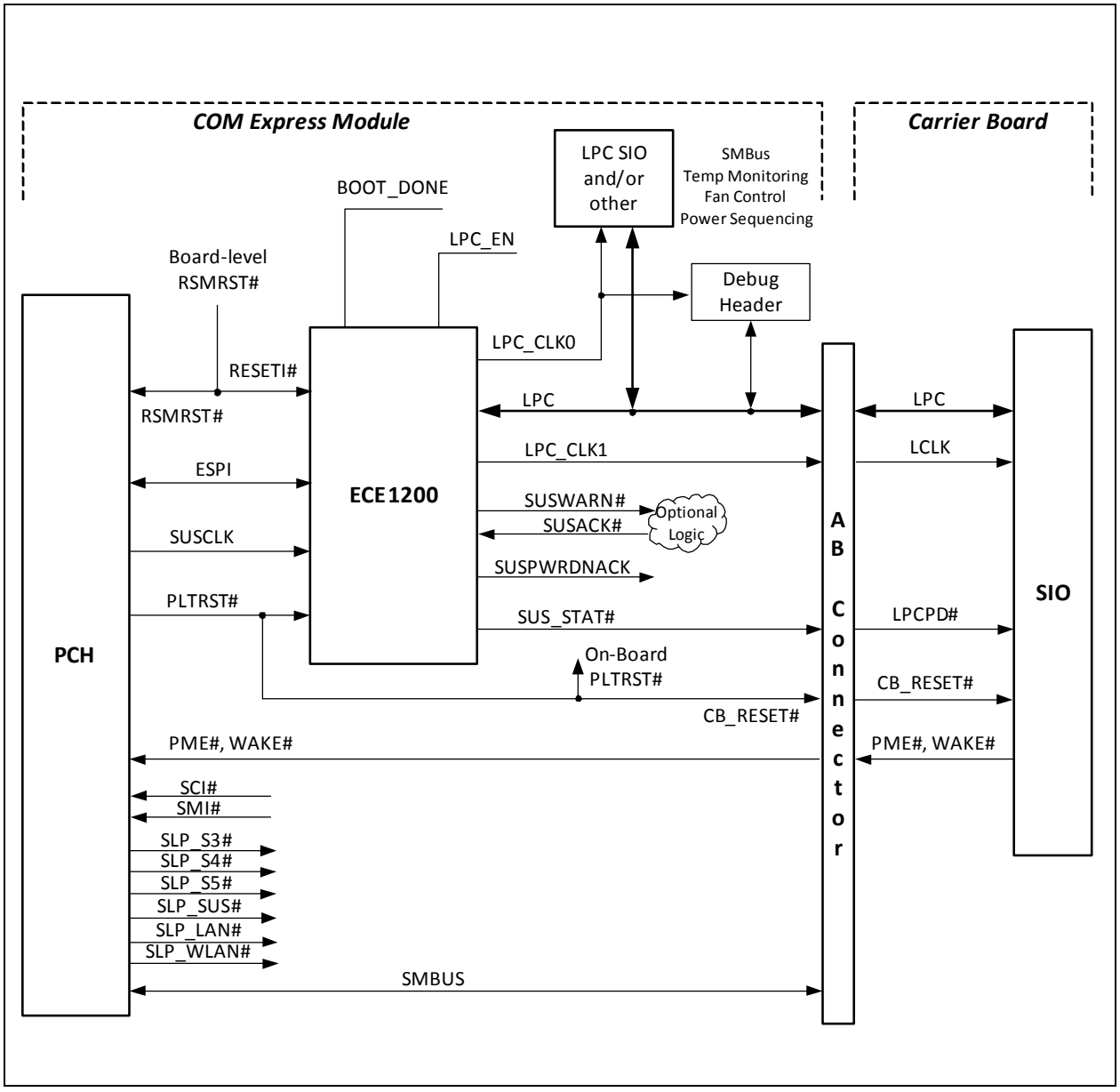


Note 1: SMI# can instead be presented on SER_IRQ pin (time slot 2) and propagated to the PCH as a Virtual Wire.

2: RCIN# is not supported as a PCH pin in eSPI configuration, and should be exercised internal to the PCH.

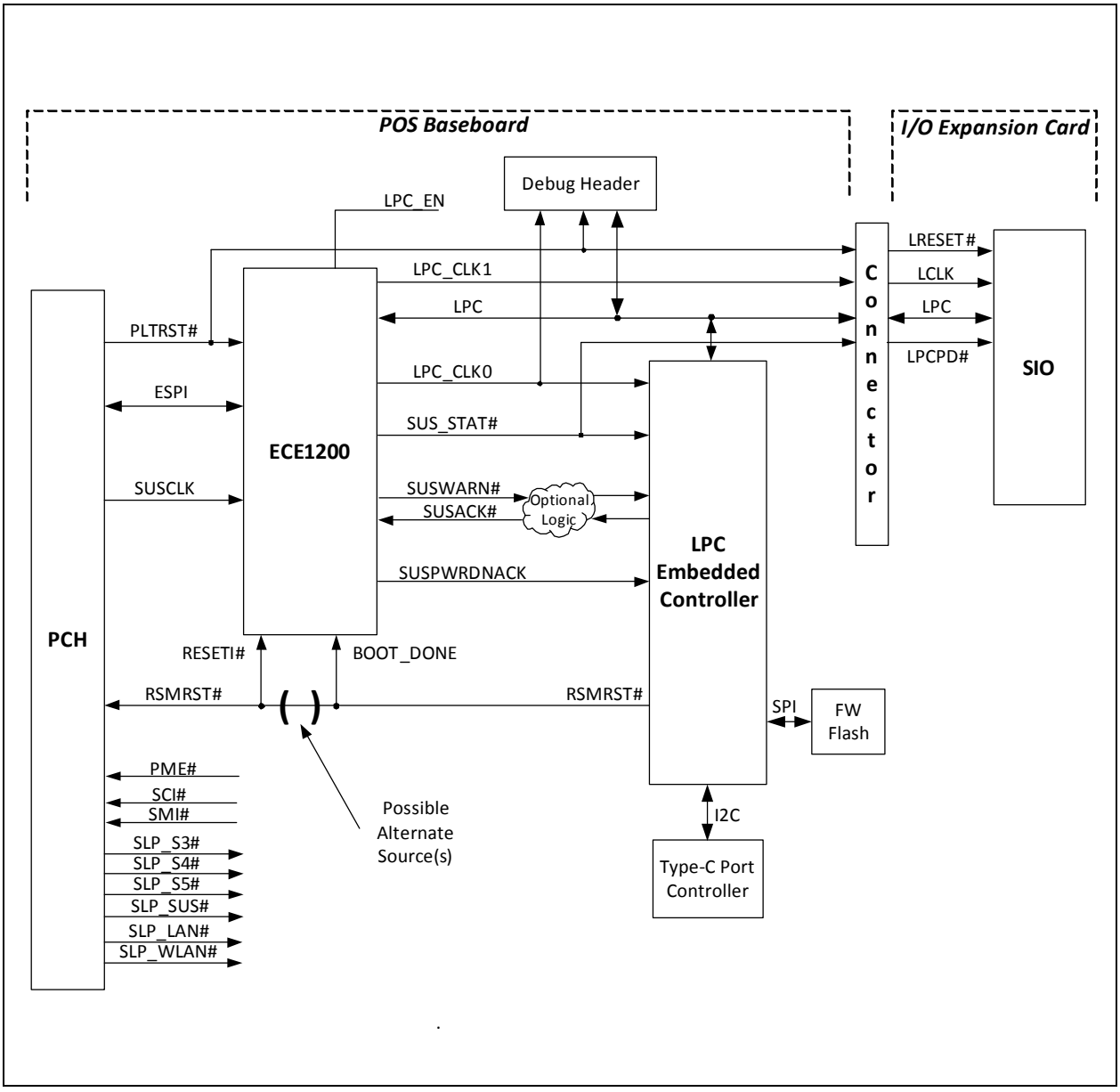
1.1.2 SYSTEM BLOCK DIAGRAM, COM EXPRESS

The ECE1200 is shown here as a single eSPI Slave, or the Primary Slave of two or more (on eSPI_CS0#).

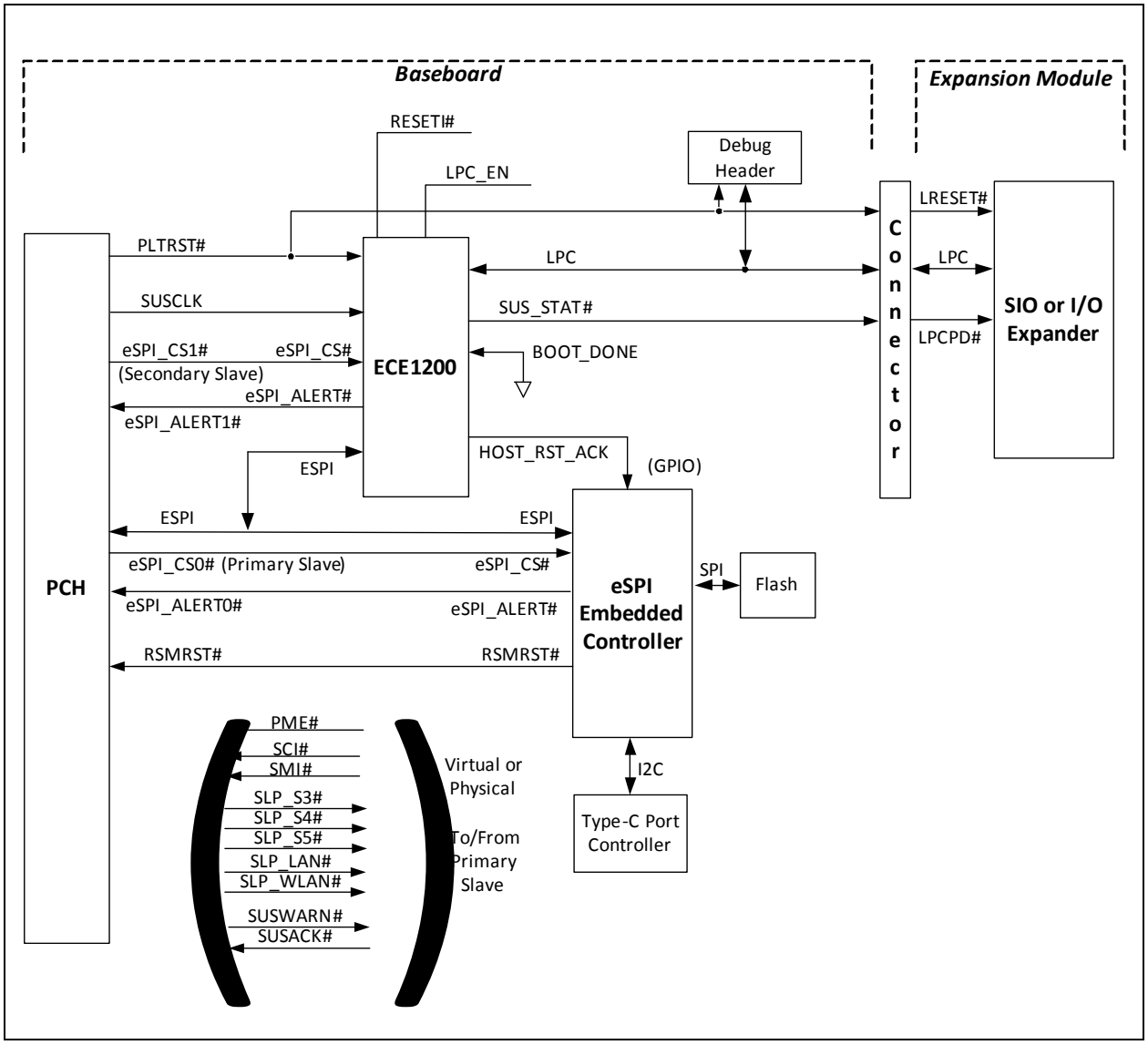


1.1.3 SYSTEM BLOCK DIAGRAM, POS

The ECE1200 is shown here as a single eSPI Slave, or the Primary Slave of two or more (on eSPI_CS0#).



1.1.4 SYSTEM BLOCK DIAGRAM, ECE1200 AS SECONDARY ESPI SLAVE



Note 1: This configuration has two eSPI Slaves. The ECE1200 is the Secondary slave device, with some limitations imposed by the Host PCH. It can receive any of the fixed Legacy decodes, but has only one Generic I/O decode range and one Generic Memory decode range available to it.

2: Each eSPI Slave has an individual eSPI_CS# input, and will be configured by the PCH hardware (as directed by its Soft-Straps) to present its ALERT# events on its individual eSPI_ALERT# output pin.

3: The Primary eSPI Slave device will be an EC functionality, and will provide the mandatory eSPI handshaking. The pin BOOT_DONE, strapped permanently low, inhibits these actions by the ECE1200.

4: Although the ECE1200 receives the HOST_RST_WARN Virtual Wire, it does not have direct authority to send the HOST_RST_ACK handshake response as a Virtual Wire. The ECE1200 instead presents its handshake HOST_RST_ACK as a physical pin when BOOT_DONE is strapped low, and it is expected that the Primary eSPI Master will use this signal to inhibit its sending of the HOST_RST_ACK Virtual Wire to the PCH until this pin is also high.

2.0 PIN CONFIGURATION

2.1 Description

The Pin Configuration chapter defines the Pin List and the Package.

2.2 Pin List

Pins are listed in Section 2.2.1 below.

Note:	The column **Emulated Power Well** indicates when signals are enabled: **VCC** means that the LPC_EN pin must be high, meaning that Main (S0) power rails in the system are valid, before these pins are allowed to drive high. **VTR** means that they may drive (high or low) as soon as all VTR power is present and RESETI# is high. This behavior is ensured only if the TEST pin remains low.

2.2.1 PIN ASSIGNMENTS, 40-PIN VQFN

40-pin VQFN	Pin Name	Direction (Other than Test Modes)	Pin Type	Signal Power Well	Emulated Power Well	Back-drive Protect
--	VSS (Pad on Underside)	--	GND	0V	--	
1	ESPI_ALERT#	O	eSPI	VTR_18	VTR	
2	VTR_18	--	PWR	1.8V	--	
3	ESPI_IO2	IO	eSPI	VTR_18	VTR	
4	ESPI_IO0	IO	eSPI	VTR_18	VTR	
5	ESPI_CLK	I	eSPI	VTR_18	VTR	
6	ESPI_IO1	IO	eSPI	VTR_18	VTR	
7	ESPI_IO3	IO	eSPI	VTR_18	VTR	
8	VTR_18	--	PWR	1.8V	--	
9	TEST	I	DIO	VTR_33	VTR	
10	LPC_EN	I	DIO	VTR_33	VTR	
11	VTR_33	--	PWR	3.3V	--	
12	BOOT_DONE	I	DIO	VTR_33	VTR	
13	PLTRST#	I	DIO	VTR_33	VTR	
14	VTR_CORE_18	--	PWR	1.8V	--	
15	SUSCLK	I	DIO	VTR_33	VTR	Y
16	SUS_STAT#	O	PCI	VTR_33	VTR	
17	SUSACK#	I	DIO	VTR_33	VTR	
18	RESETI#	I	DIO	VTR_33	VTR	
19	SUSWARN#	O	DIO	VTR_33	VTR	
20	ESPI_STRAP_0	I	DIO	VTR_33	VTR	
21	ESPI_STRAP_1	I	DIO	VTR_33	VTR	
22	VTR_33	--	PWR	3.3V	--	
23	LPC_CLK0	O	LCLK	VTR_33	VCC	
24	LPC_CLK1	O	LCLK	VTR_33	VCC	
25	LAD0	IO	PCI	VTR_33	VCC	
26	LAD1	IO	PCI	VTR_33	VCC	
27	LAD2	IO	PCI	VTR_33	VCC	
28	LAD3	IO	PCI	VTR_33	VCC	
29	LFRAME#	O	PCI	VTR_33	VCC	
30	VTR_33	--	PWR	3.3V	--	
31	SER_IRQ	IO	PCI	VTR_33	VCC	
32	CLKRUN#	IO	PCI_24	VTR_33	VCC	
33	No Connect	--	--	--	--	--
34	No Connect	--	--	--	--	--
35	SUSPWRDNACK / HOST_RST_ACK	O	DIO	VTR_33	VTR	
36	ESPI_RESET#	I	eSPI	VTR_18	VTR	
37	No Connect	--	--	--	--	--
38	No Connect	--	--	--	--	--
39	No Connect	--	--	--	--	--
40	ESPI_CS#	I	eSPI	VTR_18	VTR	

2.3 Strapping Options

2.3.1 TEST PIN

The pin named TEST must be kept permanently low in normal operation. It may be pulled high only for test purposes, and when high it redefines all pin functions. See Section 7.0, "Test Mechanisms," on page 57.

2.3.2 ESPI_STRAP_0, ESPI_STRAP_1 PINS

These pins should remain open (N/C) except for test purposes. They are included as inputs to the XNOR Chain test mode.

2.3.3 BOOT_DONE PIN

This pin defines whether the eSPI role of the ECE1200 is as a Primary Slave or a Secondary Slave. It may be strapped in the system, or it may be dynamically changed (once) in the power-on sequence.

The state of BOOT_DONE selects the multiplexed output function of pin SUSPWRDNACK / HOST_RST_ACK:

- BOOT_DONE=1: SUSPWRDNACK
- BOOT_DONE=0: HOST_RST_ACK

See Section 5.5.2, "BOOT_DONE," on page 26 for details of its usage. See also the figures in Section 1.1, "System Block Diagrams," on page 5 for connection examples.

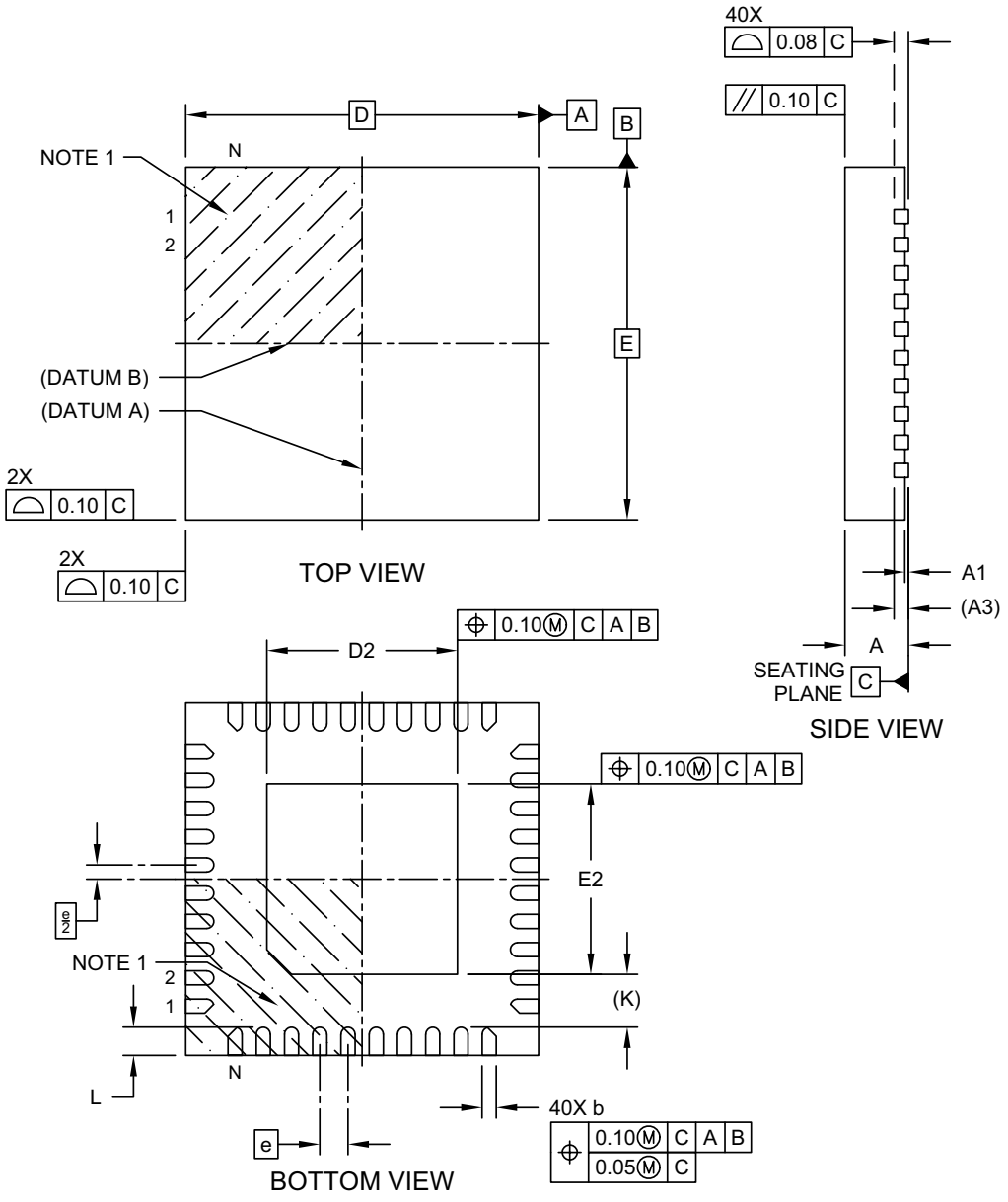
2.4 Package

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.

2.4.1 40-PIN VQFN PACKAGE OUTLINE

40-Lead Very Thin Plastic Quad Flat, No Lead Package (LDX) - 5x5 mm Body [VQFN] With 2.7x2.7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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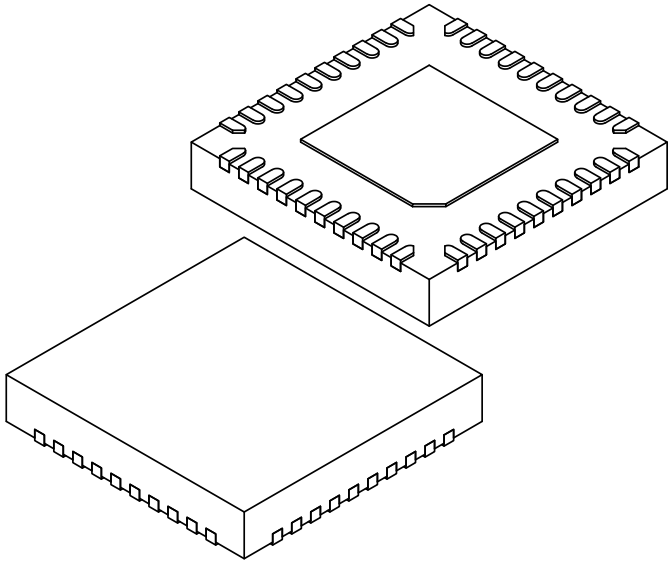
40-Lead Very Thin Plastic Quad Flat, No Lead Package (LDX) - 5x5 mm Body [VQFN] With 2.7x2.7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		40	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Overall Width	E		5.00BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Terminal Width	b	0.15	0.20	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.75 REF	

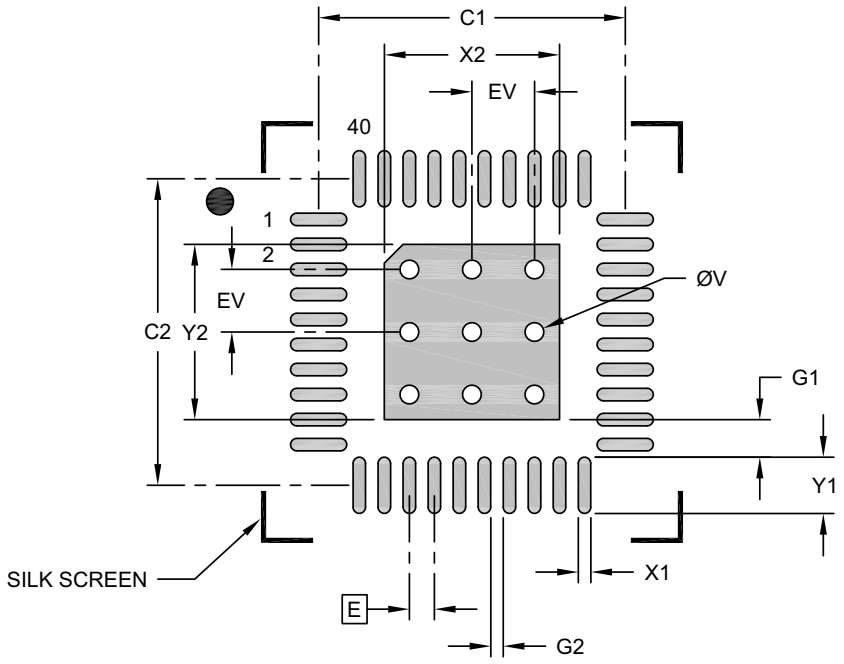
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-496 Rev A Sheet 2 of 2

40-Lead Very Thin Plastic Quad Flat, No Lead Package (LDX) - 5x5 mm Body [VQFN] With 2.7x2.7 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.90
Contact Pad to Center Pad (X40)	G1	0.60		
Contact Pad to Contact Pad (X36)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2496 Rev A

3.0 POWER, CLOCKS, AND RESETS

3.1 Introduction

This Power, Clocks, and Resets (PCR) chapter identifies all the power supplies, clock sources, and reset inputs to the chip and defines all the derived power, clock, and reset signals. In addition, this section identifies Power, Clock, and Reset events that may be used to generate an interrupt event, as well as, the Chip Power Management Features.

3.2 References

No references have been cited for this chapter.

3.3 Interrupts

The Power, Clocks, and Resets logic generates no interrupt events to the Host system.

3.4 Power

3.4.1 POWER SOURCES

Table 3-1 lists the pins from which the ECE1200 draws current. These current values are defined in Section 8.3, "Power Consumption," on page 62.

Timing sequences between these power rails are given in Section 9.5.1, "VTR Sequencing and RESETI# Timing," on page 69.

TABLE 3-1: POWER SOURCE DEFINITIONS

Power Well	Nominal Voltage	Description	Source
VTR_33	3.3V	3.3V I/O Power Supply This supply is used to power the 3.3V I/O pins. It is to be connected to the “Always-on” / “Suspend” / ”S5” supply rails in system. There is no need to connect it to a deeper power well, such as the Deep Sleep Well, even if that is what powers the downstream LPC device(s). This supply must be on prior to the RESETI# signal being deasserted (system RSMRST#).	Pin Interface
VTR_18	1.8V	1.8V I/O Power Supply This supply is used to power the 1.8V I/O pins. It is to be connected to the 1.8V “Always-on” / “Suspend” / ”S5” supply rails in system. There is no need to connect it to a deeper power well, such as the Deep Sleep Well, even if that is what powers the downstream LPC device(s). This supply must be on prior to the RESETI# signal being deasserted (system RSMRST#).	Pin Interface

TABLE 3-1: POWER SOURCE DEFINITIONS (CONTINUED)

Power Well	Nominal Voltage	Description	Source
VTR_CORE_18	1.8V	1.8V Core Logic Power Supply This supply is used to power the internal logic. It is to be connected to the 1.8V “Always-on” / “Suspend” / ”S5” supply rails in system. It is on its own pin in order to allow isolation and decoupling from the VTR_18 pin, otherwise it is identical. There is no need to connect it to a deeper power well, such as the Deep Sleep Well, even if that is what powers the downstream LPC device(s). This supply must be on prior to the RESETI# signal being deasserted (system RSMRST#).	Pin Interface

Note: The VTR_33 supply must always be at or above the voltage on the 1.8V supply pins, including during power-on and power-off sequences, otherwise excessive current may occur. VTR_18 and VTR_CORE_18 must turn on at the same time as, or after, the VTR_33 supply is powered. VTR_18 and VTR_CORE_18 must come from the same system well, rising and falling together.

3.4.2 POWER GOOD SIGNALS

The Power Good timing is defined in the Section 9.5, "Voltage Sequencing and Power Good Timing," on page 69.

TABLE 3-2: POWER GOOD SIGNAL DEFINITIONS

Power Good Signal	Description	Source
RESETI#	This is the Power-On Reset (POR) input for all the VTR input wells.	RESETI# is to be held low initially, and set high following a delay after all of the VTR power pins have reached their valid levels. RESETI# is to be pulled low as soon as either of these voltages drop below this threshold. At no time may this signal glitch during power transitions. It is strongly recommended that this pin be connected to the system RSMRST# signal, which will assure these needs.
LPC_EN	This input is used to indicate when the Main (S0) power rail voltages are on and stable.	LPC_EN indicates to the ECE1200 when the downstream resources (LPC, Serial IRQ and CLKRUN#) are powered. The low state prevents these pins from driving high, avoiding backdrive of the other components. At no time may this signal glitch during power transitions. It is strongly recommended that this pin be connected to the system PCH_PWROK signal, which will assure these needs.

3.4.3 SYSTEM POWER SEQUENCING

See Section 9.7, "System Power State Transition Diagrams," on page 69 for behavior under system power state changes.

3.5 Clocks

The following section defines the clocks that are generated and derived.

3.5.1 CLOCK SOURCES

The table defines raw clocks that are either generated externally or via an internal oscillator.

TABLE 3-3: SOURCE CLOCK DEFINITIONS

Clock Name	Frequency	Description	Source
SUSCLK	32.768 kHz	32.768 kHz Suspend Well Clock input. Used to generate 48MHz internal clocking, and the 24MHz LPC Clock.	From Host Chipset. Note that this clock may be running before VTR voltages are present.
eSPI_CLK	20--50 MHz	eSPI Transfer Clock, asynchronous to all others. Only runs during active transfers.	From Host Chipset.

Note 3-1 The SUSCLK input from the Chipset may not be at a valid 32 kHz frequency until some period of time after the deassertion of RSMRST#. See chipset specification for the actual timing.

Note 3-2 The internal 48 MHz Ring Oscillator acquires a frequency lock referenced to the external 32kHz clock source. It is not externally presented, but it is the basis of the LPC_CLK outputs when they are enabled.

3.5.2 GENERATED CLOCK OUTPUTS

This section describes clocks generated by the ECE1200 that may be used by the external system.

TABLE 3-4: GENERATED CLOCK DEFINITIONS

Clock Name	Frequency	Description	Source
48 MHz Ring Oscillator	48 MHz	Multiplied up from 32KHz input	SUSCLK
LPC_CLK[1:0]	24 MHz	System clock outputs for LPC, Serial IRQ and CLKRUN#	48 MHz Ring Oscillator

3.6 Resets

TABLE 3-5: DEFINITION OF RESET SIGNALS

Reset	Description	Source
RESETI#	External Pin that serves as the VTR POR event when pulsed low. Resets the entire device.	Pin Input Intended to come from system RSMRST#.
eSPI_RESET#	Reset signal associated with the eSPI interface. Restarts the eSPI interface if pulsed low. Will be held low by the system while RESETI# (RSMRST#) is low, and rises after the rising edge of RESETI#.	Pin Input Intended to come from system eSPI_RESET#.
PLTRST#	Platform Reset.	Pin Input Intended to come from system PLTRST#, serving also as system LRESET# / PCI_RESET#.

3.7 Chip Power Management Features

Various mode bits in the register set may be set in order to save power. Some of these are the standard LPC features (Serial IRQ Quiet Mode, CLKRUN#), and some are added in order to place the part into deeper sleep states internally. See Section 6.6, "Low Power Modes," on page 34.

Sleep states generally involve only gating clocking internally, and exiting them is nearly immediate. Waking from a Sleep state only takes any significant amount of time if the ECE1200's own Deep Sleep mode is selected (VW_C10_STOPOSC in the Power Save Register) and the Host CPU is waking from the C10 power state. In this case a delay in response happens until the 48 MHz Ring Oscillator restarts and locks again to its frequency. Note that this delay may in turn be bypassed using the FORCE_OSC_LOCK bit, but this will provide an inaccurate (and slower) clock until a true lock has been achieved.

A Wake from Deep Sleep may also be triggered by the CLKRUN# pin, generally because of the Quiet Mode mechanism. It is necessary for the requesting device to tolerate the lack of LPC clocks during the Frequency Lock delay. The ECE1200 also responds by pulling CLKRUN# low itself at this time, enabling clocks, since the interface is no longer idle.

When there is a delay involved in exiting Deep Sleep, any I/O instruction from the Host CPU will be held using the Deferred Completion mechanism of eSPI until frequency lock has been acquired. Note that eSPI I/O traffic is not a Wake mechanism, since the CPU has to have awakened already for it to do this. The eSPI interface will already have transmitted the new HOST_C10 Virtual Wire state, which performs the Wake.

4.0 LPC INTERFACE

4.1 Introduction

The Low Pin Count (LPC) Interface provides the Master end of the LPC Bus Interface, by bridging from the eSPI Interface (Section 5.0, "Enhanced Serial Peripheral Interface (eSPI)," on page 24). Generated LPC transfer cycles are defined in Table 4-2, "LPC Cycle Types Generated".

Also provided are the Master end of the legacy Serial IRQ interface for interrupts, and the legacy Clock Control interface via the CLKRUN# signal.

4.2 References

- Intel® Low Pin Count (LPC) Interface Specification, v1.1
- PCI Local Bus Specification, Rev. 2.2
- Serial IRQ Specification for PCI Systems Version 6.0
- PCI Mobile Design Guide Rev 1.0

4.3 Interface

4.3.1 SIGNAL DESCRIPTION

TABLE 4-1: LPC LEGACY SIGNAL DESCRIPTION TABLE

Name	Direction	Description
LAD[3:0]	Input/Output	The 4-bit LPC multiplexed command, address, and data bus.
LFRAME#	Output	Active low signal indicates start of new cycle and termination of broken cycle.
PLTRST#, used as LRESET#	Input	LRESET# is the LPC legacy name of the active low signal PLTRST# used as LPC Interface Reset. It is received from the Chipset's PLTRST# output, in parallel with all LPC slaves. Also called PCI Reset in system.
LPC_CLK_[1:0], each used as an LCLK	Outputs (2)	Provided as a 24-MHz frequency. Two pins are provided for distribution of loading, and may be individually enabled, disabled or controlled by CLKRUN#.
SER_IRQ	Input/Output	Serial IRQ pin used with the LCLK signal to transfer interrupts.
CLKRUN#	Input/Output	Clock Control for LCLK outputs
SUS_STAT#, used as LPCPD#	Output	LPC Power Down: Indicates that the device should prepare for power to be removed from the LPC I/F. This is propagated from the Virtual Wire named SUS_STAT#.

4.3.2 REGISTER INTERFACES

The register set providing control for the LPC block is defined in Section 6.0, "Device Register Set and Initialization," on page 32. Initialization of registers is not required in order to propagate bridged I/O or Memory traffic to LPC, but is required for initializing and enabling SER_IRQ and CLKRUN# features.

4.4 Power, Clocks and Reset

This section defines the Power, Clock, and Reset parameters of the block.

4.4.1 POWER DOMAINS

Name	Description
LPC_EN from PCH_PWROK (VCC / Main / S0 On)	The LPC Interface block is powered by VTR_33 and VTR_CORE_18. However, these features are active only while LPC_EN is high, indicating that system Main (VCC / S0) power is also good. This is “Emulated VCC” behavior.

4.4.2 CLOCKING

The LPC Interface runs from a 48MHz internal reference, 48 MHz Ring Oscillator, which is derived from the SUSCLK input. In turn, it generates the 24MHz timebase for the LPC clocks.

4.4.3 RESETS

Name	Description
RESETI#	Power on Reset to the entire chip, externally provided.
PLTRST# (as LRESET#)	This is the Platform Reset, used to reset internal LPC resources.

For the sequences of Power and Reset state transitions, see Section 9.7, "System Power State Transition Diagrams," on page 69.

4.5 LPC Controller Description

The LPC Controller is compliant with the Intel® Low Pin Count (LPC) Interface Specification, v1.1. Section 4.5.1, "Cycle Types Generated" further clarifies which LPC Interface features have been implemented and qualifies any system specific requirements.

The LPC Controller accepts all eSPI I/O and Memory traffic that is directed to it from the Chipset, and passes it to the LPC bus except for the two I/O addresses used for accessing its internal register set (see Section 6.0, "Device Register Set and Initialization," on page 32). Traffic that is unclaimed or rejected on the LPC bus may optionally be detected and reported to the Chipset by selectable eSPI mechanisms.

Slave devices on LPC may use the SER_IRQ mechanism to notify the host of an event.See Section 4.7, "Serial IRQ," on page 22.

The CLKRUN# feature is provided, allowing negotiation with LPC slave devices to turn off the LPC clock(s) as desired.

4.5.1 CYCLE TYPES GENERATED

The following cycle types are generated by the LPC Interface Controller. Note that they are all 1 byte in length. eSPI I/O or Memory cycles that are larger than 1 byte are allowed, and are broken down into individual bytes, transferred least-significant byte first.

TABLE 4-2: LPC CYCLE TYPES GENERATED

Cycle Type	Transfer Size
I/O Read	1 byte
I/O Write	1 byte
Memory Read	1 byte
Memory Write	1 byte

4.5.2 SYNC FIELD HANDLING

The SYNC field in an LPC transfer provides status for each byte transferred. The LPC Interface recognizes only the following SYNC encodings:

TABLE 4-3: SYNC FIELD ENCODINGS RECOGNIZED

SYNC Code	Interpretation
0000	Ready
0101	Short Wait
0110	Long Wait
1010	Error
other	Unrecognized, considered Reserved

4.5.2.1 Wait SYNCs on LPC

Both Long Wait and Short Wait SYNC responses are handled identically, expecting either the Ready or Error SYNC code to appear. The ECE1200 device does not impose a time-out, leaving that to the Host Chipset.

4.5.2.2 Unclaimed LPC Cycle

An unclaimed LPC cycle is detected if no recognized SYNC code is seen after 3 clocks, or if an unrecognized SYNC code is detected after Wait SYNCs. This will terminate the current byte by the ABORT mechanism, and all subsequent byte transfers from the same eSPI transfer will be abandoned. The result reported over eSPI will be determined based on the type of eSPI transfer:

Non-Posted (I/O Read, I/O Write or Memory Read):
UNSUCCESSFUL COMPLETION, and other reporting as programmed in the Unclaimed Non-Posted Error Handling Register, Section 6.9.4, on page 39.

Posted (Memory Write only):
as programmed in the Unclaimed Posted Error Handling Register, Section 6.9.8, on page 41.
UNSUCCESSFUL COMPLETION is not a possible response to a Posted transfer.

See Section 4.8, "Error Reporting and Logging Registers," on page 23 for details of error posting and logging within the ECE1200.

4.5.2.3 Error (Abort) SYNC

An LPC cycle that is claimed, but is then terminated by the Error SYNC code, will terminate the current byte, and all subsequent byte transfers from the same eSPI transfer. The result reported over eSPI will be determined based on the type of eSPI transfer:

Non-Posted (I/O Read, I/O Write or Memory Read):
UNSUCCESSFUL COMPLETION, and other reporting as programmed in the Sync Abort Non-Posted Error Handling Register, Section 6.9.5, on page 40

Posted (Memory Write only):
as programmed in the Sync Abort Posted Error Handling Register, Section 6.9.9, on page 41.
UNSUCCESSFUL COMPLETION is not a possible response to a Posted transfer.

See Section 4.8, "Error Reporting and Logging Registers," on page 23 for details of error posting and logging within the ECE1200.

4.6 LPC Clock Run Control CLKRUN#

The CLKRUN# pin is used to indicate the status of the LPC Clock(s) as well as to request that stopped clocks be restarted. The standard for CLKRUN# operation is in the document PCI Mobile Design Guide Rev 1.0.

There is only one CLKRUN# control, but it can be associated with either or both of the LPC Clock pins. A disabled Clock is not affected by CLKRUN#, and remains disabled.

CLKRUN# Support is off by default, meaning that CLKRUN# is driven permanently low and LPC clocks are not gated. This remains the initial state of CLKRUN# by default when the feature is enabled as well. If the Serial IRQ feature is in Quiet Mode and idle, and the LPC bus has been idle for a defined period of time, CLKRUN# will be driven high by the ECE1200, and then parked high using an external pull-up resistor. Any LPC Slave device that requires clocks still to be running will pull CLKRUN# back low itself, and clocks will then continue uninterrupted. If however no Slave device pulls CLKRUN# low, then the ECE1200 will stop the LPC clocks, holding them low.

Once clocks are off, activating CLKRUN# low will re-start them. This may happen by Slave device action, or by the ECE1200 internally upon detecting a request for LPC traffic from the Host Chipset.

When clocks are stopped by CLKRUN# activity, other power saving modes may be engaged. See Section 6.6, "Low Power Modes," on page 34 and Section 3.7, "Chip Power Management Features," on page 18.

4.6.1 ENABLING THE CLKRUN# FUNCTION

See Section 6.8.6, "Set Up Optional CLKRUN# Clock Gating," on page 37.

4.7 Serial IRQ

The ECE1200 device supports Serial IRQ as the Master controller, adhering to the Serial IRQ Specification for PCI Systems Version 6.0. Both Continuous Mode and Quiet Mode operation are supported. The full 21-slot frame format is presented, as has been common practice in LPC-based Southbridge devices.

Serial IRQ inputs are bridged to the equivalent eSPI Virtual Wire traffic. See Section 6.8.4, "Set Up Serial IRQ," on page 36 for the detail and programmable options of the Serial IRQ feature. The Serial IRQ Master supports the following serial inputs:

Legacy Interrupts:

- IRQ1
- IRQ[3:7]
- IRQ[9:12]
- IRQ[14:15]

PCI-Derived Interrupts, mappable to selected IRQ levels, including those above IRQ15:

- INTA#
- INTB#
- INTC#
- INTD#

Discrete signals:

- SMI#
- IOCHCK# (IOCHK#)

Other inputs are considered deprecated vestiges according to common practice, and are ignored.

The SMI# input on Serial IRQ is considered a signal from downstream sources, and is not captured in the ECE1200 internal register set. Polling for it in the internal register set will fail, and it will appear only in the LPC source device.

The IOCHCK# (IOCHK#) input is treated as an error condition, and three situations may be detected

The IOCHK Non-Posted Error Handling Register, Section 6.9.5, on page 40 defines the action to be taken if the IOCHK# input is activated during the Wait phase of a Non-Posted LPC transfer (I/O Read or Write, or Memory Read).

The IOCHK Posted Error Handling Register, Section 6.9.10, on page 41 defines the action to be taken if the IOCHK# input is activated during the Wait phase of a Posted LPC transfer (Memory Write).

These situations above do not by themselves terminate the LPC transfer, and the peripheral device must terminate the transfer itself (by a SYNC code other than Wait).

The IOCHK Idle Error Handling Register, Section 6.9.7, on page 40 defines the action to be taken if the IOCHK# input is activated outside of an LPC transfer.

4.7.1 ENABLING THE SERIAL IRQ FUNCTION

The Serial IRQ feature is disabled by default, and must be enabled. To enable Serial IRQ channel the host must initialize it as described in Section 6.8.4, "Set Up Serial IRQ," on page 36. This may be done either before or after LPC sources have been initialized.

4.8 Error Reporting and Logging Registers

4.8.1 VIRTUAL WIRE STATES AND CLEARING

Four eSPI Virtual Wires are available for reporting LPC errors or the IOCHK# event, as programmed in the various Error Handling registers mentioned above. Each Virtual Wire, once posted and signaled to the Chipset, can be polled and cleared by register accesses. The Virtual Wires are:

- ERROR_FATAL
- ERROR_NONFATAL
- SMI#
- SCI#

The Virtual Wires ERROR_FATAL and ERROR_NONFATAL are polled and cleared in the eSPI Virtual Wire Errors Register, Section 6.9.11, on page 42. They are also cleared by an eSPI_RESET# event.

The Virtual Wires SMI# and SCI# are polled and cleared in the eSPI Virtual Wire Error Events Register, Section 6.9.12, on page 42. These Virtual Wires are cleared by PLTRST# events as well as eSPI_RESET# events (eSPI_RESET# low asserts PLTRST# low as well).

The SMI# Virtual Wire is not recorded in the ECE1200 if it is the result of a Serial IRQ report. In that case, it will be recorded in the originating device, and can be polled and cleared there, propagating through the ECE1200 as it changes state on the Serial IRQ port. A PLTRST# event will clear it in the ECE1200, as well as at the originating device.

4.8.2 LPC CYCLE ERROR LOGGING

The various error conditions occurring during an LPC transfer are logged as individual bits in two registers:

- The LPC Error Log Non-Posted Register, Section 6.11.8, on page 55 holds errors detected in Non-Posted transfers.
- The LPC Error Log Posted Register, Section 6.11.9, on page 55 holds errors detected in Posted transfers.

In addition, the address and type of LPC access are captured on each error:

- The Error Cycle Attributes Register, Section 6.11.14, on page 56 holds the type of access: Read vs.Write and I/O vs. Memory.
- The four Error Cycle Address registers, starting at Section 6.11.10, on page 56, hold the address captured from the LPC bus on an error. I/O addresses load only the low-order two bytes of the address; Memory addresses load all four bytes.

5.0 ENHANCED SERIAL PERIPHERAL INTERFACE (ESPI)

5.1 Introduction

The Intel® Enhanced Serial Peripheral Interface (eSPI) in the ECE1200 is a hard-wired subset of the eSPI functionality, dedicated to bridging I/O and Memory traffic with LPC, and Serial IRQ traffic. It also implements Virtual Wires, by which it restores legacy signals and supports new eSPI requirements internally.

5.2 References

1. Intel Doc #327432, *Enhanced Serial Peripheral Interface (eSPI): Interface Base Specification*
2. Intel Doc #562633, *Enhanced Serial Peripheral Interface (eSPI) Compatibility Specification*

5.3 Terminology

This table defines specialized terms localized to this feature.

TABLE 5-1: TERMINOLOGY

Term	Definition
System Host	Refers to the external Chipset that originates the I/O and Memory traffic over the eSPI Interface.
Master / Slave	Following the SPI convention, the System Host is the eSPI Master and the ECE1200 is the eSPI Slave. The Slave can request the Master's attention using the ALERT# functionality, but all traffic is driven by the Master.
Virtual Wire / Virtual Wire Channel	A Virtual Wire is a 1-bit digital state that is transferred between the System Host and the ECE1200. Some Virtual Wires are translated to/from physical pins by the ECE1200. Other Virtual Wires present IRQs to the Host System from the Serial IRQ feature, participate in handshakes for system power state transitions, or signal exceptions to the Host System. The eSPI Virtual Wire Channel is a category of eSPI traffic that is multiplexed onto the eSPI pins for transferring Virtual Wires.
Peripheral Channel	This is a category of eSPI traffic that is multiplexed onto the eSPI pins for performing I/O and Memory traffic originating from the System Host.
eSPI Configuration Registers	A set of registers that are dedicated to initial low-level setup of the eSPI bus by the System Host. They are accessible only using the eSPI GET_CONFIGURATION and SET_CONFIGURATION commands, and are separate from the internal register set that is accessed by I/O traffic.

5.4 Bus Interface

5.4.1 BUS PINS

Table 5-2, "eSPI Bus Signal Description Table" lists the eSPI bus signals on the pin interface. These are documented by Intel specifications.

TABLE 5-2: ESPI BUS SIGNAL DESCRIPTION TABLE

Signal Name	Direction	Description
eSPI_CS#	Input	eSPI Chip Select, Low-Active
eSPI_CLOCK	Input	eSPI Clock
eSPI_ALERT#	Output	eSPI Alert signal, Low-Active. Exercised only if the Host System specifically enables it, which it will do if there are other eSPI Slaves in the system. Otherwise the default configuration is to present ALERT# events on the eSPI_IO1 pin.
eSPI_RESET#	Input	POR for eSPI domain, and the Global Reset exercised by the Host System for serious errors. Low-Active.
eSPI_IO0	Input/Output	eSPI Data Bus, bit 0. Input (MOSI) in x1 Bus Mode. In wider bus modes it holds the LS data bit.
eSPI_IO1	Input/Output	eSPI Data Bus, bit 1. Output (MISO) in x1 Bus Mode. Also, by default and if there is only a single Slave in a point-to-point configuration, it presents the ALERT# state while the eSPI bus is idle.
eSPI_IO2	Input/Output	eSPI Data Bus, bit 2. Used only in x4 mode.
eSPI_IO3	Input/Output	eSPI Data Bus, bit 3. Used only in x4 mode, as MS bit.

5.5 Sideband Support Interface

5.5.1 ESPI SIDEBAND SUPPORT PIN LIST

Table 5-3, "eSPI Sideband Signal Description Table" lists a set of signals that are typically needed for supporting (or bypassing) certain features of eSPI that are propagated as Virtual Wires.

TABLE 5-3: ESPI SIDEBAND SIGNAL DESCRIPTION TABLE

Signal Name	Direction	Description
BOOT_DONE	Input	Selects eSPI Slave role as Primary (high) vs. Secondary (low). Also allows a delayed assumption of the Primary Slave role.
SUSWARN#	Output	Presents the state of the Virtual Wire SUS_WARN#, restoring the legacy PCH pin function.
SUSACK#	Input	Restores the legacy PCH pin function. Edges on this pin are transmitted to the PCH as the Virtual Wire SUS_ACK#.
SUSPWRDNACK / HOST_RST_ACK	Output	In the Primary Slave role, presents the state of the Virtual Wire SUSPWRDNACK, restoring the legacy PCH pin function. In the Secondary role, presents the HOST_RST_ACK state as a physical signal.

5.5.2 BOOT_DONE

The BOOT_DONE option selects the eSPI Slave role (Primary or Secondary) that the ECE1200 should assume. The Secondary Slave role is more passive than the Primary Slave role, in that it does not participate in Virtual Wire handshake responses over eSPI. It does receive the initial Virtual Wire, but for information only. For examples of system configurations and BOOT_DONE connections for them, see the figures in Section 1.1, "System Block Diagrams," on page 5.

BOOT_DONE is not sampled at any one time, but has its effect continuously, and may either be strapped to a static value or be changed once, as explained below.

- BOOT_DONE = permanently High means that the ECE1200 serves as the Primary eSPI slave. This means that the Chipset has only one ESPI_CS# pin, or that there are two eSPI slaves and the ESPI_CS# on the ECE1200 is connected to the Chipset's ESPI_CS0# pin.
  The output pin SUSPWRDNACK/HOST_RST_ACK is driven as the SUSPWRDNACK function, and the internal HOST_RST_ACK state is transmitted as a Virtual Wire.
  At the first opportunity, the Virtual Wires SLAVE_BOOT_LOAD_DONE and SLAVE_BOOT_LOAD_STATUS are both transmitted as '1' to the Chipset, freeing the system to boot above the S5 state.
- BOOT_DONE = permanently Low means that the ECE1200 serves as a Secondary eSPI slave of two or more in the system (that is, it is connected to ESPI_CS1# or higher from the Chipset).
  The SLAVE_BOOT_LOAD_DONE and SLAVE_BOOT_LOAD_STATUS Virtual Wires are not transmitted, and instead come from the Primary Slave, which is required to be present also.
  The output pin SUSWARN# is driven from its Virtual Wire, but is not expected to be used by the system. The input pin SUSACK# has no function in this configuration, and its state will be ignored.
  The output pin SUSPWRDNACK/HOST_RST_ACK is driven as the HOST_RST_ACK function.
- BOOT_DONE = Low then High is a way of delaying booting of the system, by an ECE1200 wired as the Primary Slave, if some system consideration requires a further delay after RSMRST# has gone high. While BOOT_DONE remains low, the Virtual Wires SLAVE_BOOT_LOAD_DONE and SLAVE_BOOT_LOAD_STATUS are not yet transmitted to the Chipset. On the rising edge of BOOT_DONE, these Virtual Wires are transmitted as '1' values, and the ECE1200 assumes its Primary eSPI Slave role from this time onward. No Virtual Wire traffic is lost in this sequence, because it does not commence until the SLAVE_BOOT_LOAD_xxx Virtual Wires have been sent from a Primary slave.
  The output pin SUSPWRDNACK/HOST_RST_ACK is initially driven low (as HOST_RST_ACK, temporarily), then driven as the SUSPWRDNACK function (also initially low) when BOOT_DONE rises.

TABLE 5-1: BOOT_DONE

BOOT_DONE	Description
0	ECE1200 assumes the Secondary eSPI Slave role. Certain Virtual Wire interactions will not occur, deferring to another Primary device for this traffic. SUSPWRDNACK/HOST_RST_ACK pin = HOST_RST_ACK
1	ECE1200 assumes the Primary eSPI Slave role. At the first opportunity, it will transmit VWires SLAVE_BOOT_LOAD_DONE and SLAVE_BOOT_LOAD_STATUS as '1' to the Chipset. SUSPWRDNACK/HOST_RST_ACK pin = SUSPWRDNACK
0 then 1	ECE1200 assumes the Primary eSPI Slave role at the rising edge. It will transmit VWires SLAVE_BOOT_LOAD_DONE and SLAVE_BOOT_LOAD_STATUS as '1' to the Chipset, either immediately or at the first opportunity provided by the eSPI Master in the Chipset. SUSPWRDNACK/HOST_RST_ACK pin = SUSPWRDNACK
1 then 0	Undefined action, and not allowed. It may lead to undefined operation in the system.

5.5.3 SUSWARN#

This output restores a pin that may no longer be available on an eSPI-configured Chipset. It presents the state of the Virtual Wire replacement.

It is intended to be used for any required legacy purposes, in conjunction with the SUSACK# pin.

5.5.4 SUSACK#

This input restores a pin that may no longer be available on an eSPI-configured Chipset. Edges on this pin are transmitted as Virtual Wire events to the Chipset.

It is intended to be used for any required legacy purposes, in conjunction with the SUSWARN# pin.

5.5.5 SUSPWRDNACK / HOST_RST_ACK

This pin is multiplexed by the state of the BOOT_DONE pin.

5.5.5.1 Primary Role: SUSPWRDNACK

In the Primary Slave role (BOOT_DONE = 1), this pin presents the state of the Virtual Wire SUSPWRDNACK, replacing a physical signal no longer presented by some eSPI-mode PCH devices.

In this role, the HOST_RST_ACK state is transmitted as a Virtual Wire.

5.5.5.2 Secondary Role: HOST_RST_ACK

In the Secondary Slave role (BOOT_DONE = 0), there is a Virtual Wire handshake (HOST_RST_WARN / HOST_RST_ACK) that cannot be completed locally. The Secondary Slave receives the Virtual Wire HOST_RST_WARN indication, but is not allowed to transmit the response HOST_RST_ACK. Only the Primary Slave may do this.

Instead, it must communicate by a physical signal with the Primary Slave (an EC), which can then use this to delay its own transmission of HOST_RST_ACK as a Virtual Wire. HOST_RST_ACK is therefore presented as a physical signal in this configuration.

The HOST_RST_ACK signal goes high in response to the rising edge of Virtual Wire HOST_RST_WARN, delayed until the LPC and Serial IRQ interfaces have been gracefully halted.

SUSPWRDNACK is seen by the Primary Slave as a Virtual Wire, and is expected to be processed there instead.

5.6 Register Interface

The registers associated with eSPI itself are only the eSPI Configuration Registers. They are accessed only for initialization of eSPI communication parameters, by Chipset hardware after removal of the eSPI_RESET# signal. See Section 5.8, "eSPI Configuration Registers," on page 29 for details of these special registers.

Other registers, used for controlling the Bridging functionality between eSPI and LPC, are described in Section 6.0, "Device Register Set and Initialization," on page 32.

5.7 Description

5.7.1 OPERATING FREQUENCY

The part supports standard eSPI specifications up to the 50MHz operating frequency. It does not, however, enforce a limit to the Host Chipset, which remains in full control of the frequency selection. See the Intel Compatibility Specification document listed in Section 5.2, "References" for the “Soft-Straps” that declare this for the system.

Any additional eSPI Slave may have its own independent frequency setting, including the maximum 66MHz, and its traffic will have no effect on this device.

5.7.2 PERIPHERAL CHANNEL SUBSET

The eSPI Peripheral Channel supports I/O and Memory traffic initiated by the Host System. It does not support eSPI Memory Mastering emulation to Host DRAM, nor the associated LTR command.

It therefore does not attempt to re-create legacy LPC DMA or Mastering.

5.7.3 VIRTUAL WIRE CHANNEL SUBSET

As referenced to the Intel Compatibility Specification document listed in Section 5.2, "References", a subset of Virtual Wires is implemented as shown in Table 5-4. “RFU” represents a Virtual Wire that is implemented for future use only.

In Table 5-4, the following notations are used:

- IDX is the Virtual Wire Index number for the group of 4 Virtual Wires.
- Dir is the Virtual Wire direction for that Index: “Dn” (Down) is Master to Slave, “Up” is Slave to Master.

TABLE 5-4: VIRTUAL WIRES IMPLEMENTED

IDX	Dir	Bit 3	Bit 2	Bit 1	Bit 0	Defaults	Reset Domain
2h	Dn	X	SLP_S5#	SLP_S4#	SLP_S3#	x000	eSPI_RESET#
3h	Dn	X	OOB_RST_ WARN	PLTRST#	SUS_STAT#	x000	eSPI_RESET#
4h	Up	PME#	WAKE#	X	OOB_RST_ ACK	11x0	eSPI_RESET#
5h	Up	SLAVE_BOOT_ LOAD_STATUS	ERROR_ NONFATAL	ERROR_ FATAL	SLAVE_BOOT_ LOAD_DONE	0000	eSPI_RESET#
6h	Up	HOST_RST_ ACK	RCIN#	SMI#	SCI#	0111	PLTRST#
7h	Dn	X	X	X	HOST_RST_ WARN	xxx0	PLTRST#
40h	Up	X	X	RFU	SUS_ACK#	xx00	eSPI_RESET#
41h	Dn	SLP_A#	X	SUS_PWRDN_ ACK	SUS_WARN#	0x00	eSPI_RESET#
42h	Dn	X	X	SLP_WLAN#	SLP_LAN#	xx00	eSPI_RESET#
43h	Dn	(“Generic” Down)				0000	eSPI_RESET#
44h	Dn	(“Generic” Down)				0000	eSPI_RESET#
45h	Up	(“Generic” Up from Primary Slave CS0#)				0000	eSPI_RESET#
46h	Up	(“Generic” Up from Primary Slave CS0#)				0000	eSPI_RESET#
47h	Dn	X	X	X	HOST_C10	xxx0	PLTRST#
48h	Up	(“Generic” Up from Secondary Slave CS1#)				0000	eSPI_RESET#
49h	Up	(“Generic” Up from Secondary Slave CS1#)				0000	eSPI_RESET#
4Ah	Dn	X	X	RFU	X	xx0x	eSPI_RESET#

Color Key:	No Shading: Implemented and used regardless of BOOT_DONE pin state	Yellow: Sent Up only if BOOT_DONE pin is high	Orange: Sent up as ‘1’ if BOOT_DONE pin is high.	Gray: Not implemented. X = Undefined by eSPI spec	Blue: Generated internally. Sent Up as the Virtual Wire if BOOT_DONE == 1 or presented on the physical pin if BOOT_DONE == 0

5.8 eSPI Configuration Registers

The eSPI Configuration Register Set is only accessible using the low-level eSPI protocol commands GET_CONFIGURATION and SET_CONFIGURATION. These are typically issued only by Chipset hardware state machines, as directed by its own Soft-Straps, for initialization of eSPI communication parameters. These commands include a Location field in order to designate which register is being accessed, but this Location does not reside within the Memory or I/O space visible to CPU software.

These registers are accessible to Host software using a specialized portal in the PCH. However, accessing them is neither required nor recommended, even during BIOS POST. They are shown here only to support interpretation of eSPI traffic for debug. See Intel’s specifications (Section 5.2) for full detail of their content and usage.

Note that the ECE1200 does not enforce a clock speed limit using these registers. It is designed to operate at a maximum frequency of 50MHz, and this is what must be declared in the Chipset’s Soft-Strap settings for eSPI communication with this device. Any additional eSPI Slave may have its own frequency setting, including 66MHz, and its traffic will have no effect on this device.

TABLE 5-5: ESPI CONFIGURATION REGISTER SUMMARY

Location	Register Name
04h	eSPI Device Identification Register
08h	eSPI General Capabilities and Configurations Register
10h	eSPI Channel 0 (Peripheral) Capabilities and Configurations Register
20h	eSPI Channel 1 (Virtual Wire) Capabilities and Configurations Register

5.8.1 ESPI DEVICE IDENTIFICATION REGISTER

Location	04h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:8	Reserved	R	0h	-
7:0	Version ID	R	01h	-

5.8.2 ESPI GENERAL CAPABILITIES AND CONFIGURATIONS REGISTER

Location	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31	CRC Checking Enable	R/W	0	eSPI
30	Response Modifier Enable	R/W	0	eSPI
29	Reserved	R	0	-
28	Alert Mode	R/W	0	eSPI
27:26	IO Mode Select	R/W	00b	eSPI
25:24	IO Mode Support	R	11b	-
23	Open Drain ALERT# Select	R/W	0	eSPI
22:20	Operating Frequency Select	R/W	000b	eSPI
19	Open Drain ALERT# Supported	R	1	-
18:16	Max Operating Frequency Supported (No limit declared)	R	100b	-
15:12	Max WAIT States Allowed	R/W	0000b	eSPI
11:8	Reserved	R	0000b	-
7:0	Channels Supported (Only Peripheral and Virtual Wire channels)	R	03h	-

5.8.3 ESPI CHANNEL 0 (PERIPHERAL) CAPABILITIES AND CONFIGURATIONS REGISTER

Location	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:15	Reserved	R	0h	-
14:12	Max Read Request	R/W	001b	PLTRST
11	Reserved	R	0	-
10:8	Max Payload Size Selected	R/W	001b	PLTRST
7	Reserved	R	0	-
6:4	Max Payload Size Supported	R	001b	-
3	Reserved	R	0	-
2	Bus Master Enable	R/W	0	PLTRST
1	Ready (follows Enable bit)	R	1	PLTRST
0	Enable	R/W	1	PLTRST

5.8.4 ESPI CHANNEL 1 (VIRTUAL WIRE) CAPABILITIES AND CONFIGURATIONS REGISTER

Location	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
31:22	Reserved	R	0h	-
21:16	Operating Maximum VWire Count	R/W	0h	eSPI
15:14	Reserved	R	0	-
13:8	Max VWire Count Supported	R	3Fh	eSPI
7:2	Reserved	R	0h	-
1	Ready (follows Enable bit)	R	0	eSPI
0	Enable	R/W	0	eSPI

6.0 DEVICE REGISTER SET AND INITIALIZATION

6.1 Introduction

This chapter defines the register set of the ECE1200 device, and the mechanism used to access them.

All accesses to ECE1200 internal registers use the Plug-and-Play Configuration Port mechanism, which occupies only two contiguous bytes in an otherwise unused section of the Host I/O addressing space. All other I/O and Memory traffic directed to the ECE1200 is transparently presented on the LPC bus, and this happens immediately without any requirement for setup. This includes passing other Plug-and-Play traffic directly and immediately to other devices' Configuration Ports, such as 2Eh/2Fh and 4Eh/4Fh, allowing them to be initialized first.

It is, however, necessary eventually to access the internal register set, because this is where the Master resources associated with the Serial IRQ and CLKRUN# features are configured and enabled, and where optimizations for additional power saving may be selected. The ECE1200 device uses the same Plug-and-Play Configuration Port to provide access to registers that have Runtime as well as Configuration purposes.

Initially the Configuration Port resides at I/O addresses 008Ch (INDEX) and 008Dh (DATA), chosen so that it is reliably out of the way of legacy I/O traffic. But it can be moved to any other desired address at a 2-byte boundary, where the first ("even") address is the INDEX byte, followed by the DATA byte at the next ("odd") byte address.

6.2 Terminology

According to Plug-and-Play standards, registers fall into regions defined as "Global" or "Logical Device".

TABLE 6-1: TERMINOLOGY

Term	Definition
Global Registers	Registers that are always accessible via the Configuration Port.
Logical Device Registers	Registers belonging to a "Logical Device" in the device. These registers are bank-selected into a shared region, using one of the Global Registers to make the selection.

6.3 Register Interface

The Host-accessible Plug-and-Play Configuration port is the means of accessing internal registers, which are organized as shown in FIGURE 6-1: on page 33.

The INDEX I/O location is written with an "Index" value to select the register to be accessed. The DATA I/O location is then used with 8-bit I/O Read or Write instructions to access the selected register.

There is a single Global region which resides at Index values of 00h through 2Fh. As defined above, these registers are not subject to bank selection, and are therefore accessible at all times.

Within the Global region, there is a register called "Logical Device Number", residing at Index 07h. Writing an 8-bit value here selects a Logical Device bank of registers, which may then be accessed using Indexes 30h through FFh.

In this device, there are two Logical Devices:

- Logical Device number 00h is the "eSPI Logical Device", holding registers that manage the Host CPU interface.
- Logical Device number 01h is the "LPC Logical Device", holding registers that manage the LPC, SERIRQ and CLKRUN# functionality.

Sequence to Access a Logical Device Register:

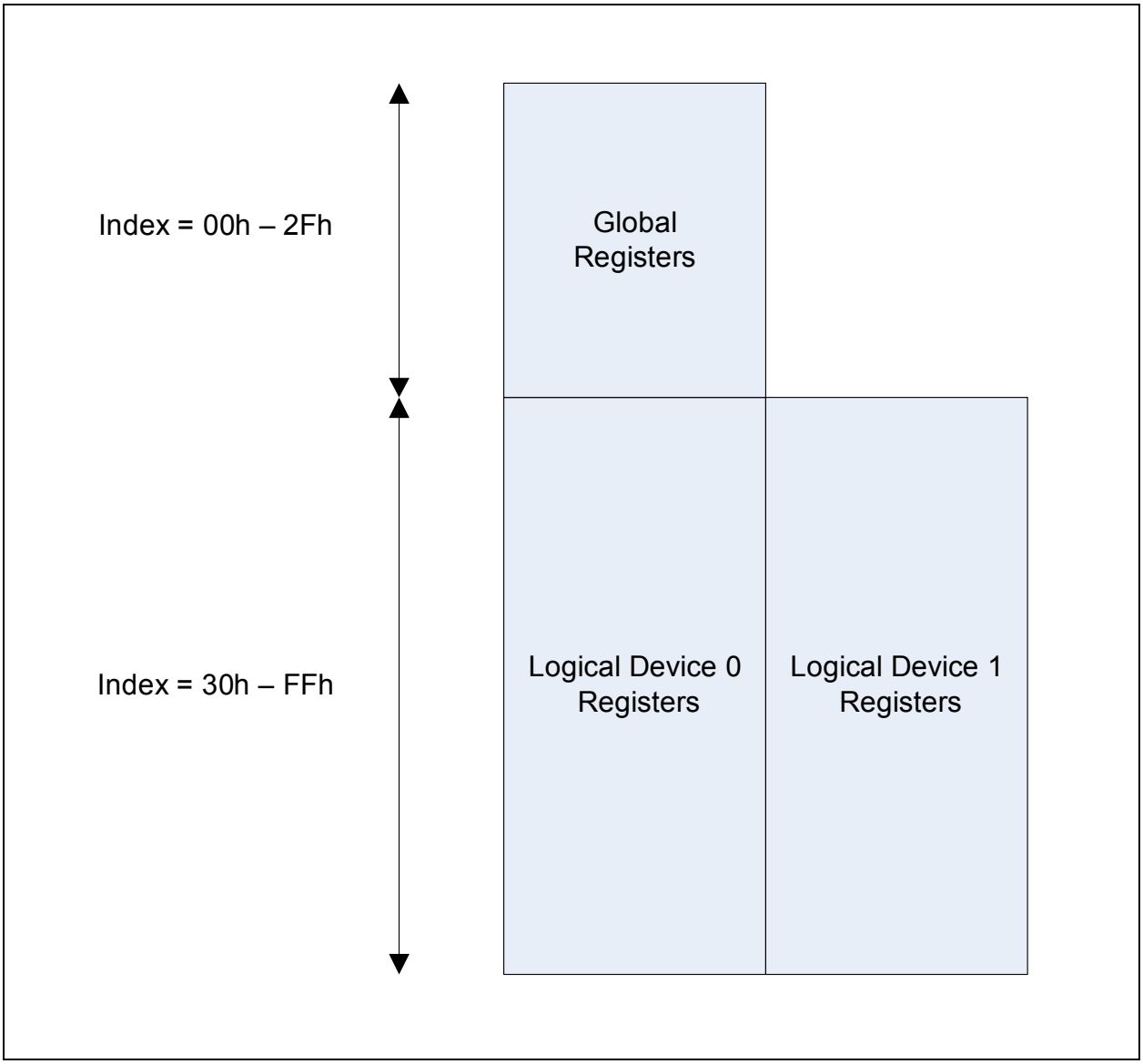
a) Select the Logical Device using the Logical Device Number Register, by writing 07h into the INDEX Port and then the Logical Device number value (00h or 01h) to the DATA Port.

b) Write the address of the desired Logical Device register to the INDEX Port and then write or read the value of the register itself through the DATA Port.

Note 1: If accessing a Global Register, step (a) is not required.

2: Any write to an undefined or Reserved register is terminated normally on the eSPI bus without any modification of state in the ECE1200. Any read to a Reserved register returns 00h.

FIGURE 6-1: BLOCK DIAGRAM OF REGISTER SET



6.3.1 REGISTER INTERFACE ENABLE / DISABLE

The Configuration Port is disabled by default and must be enabled by placing the device into CONFIG MODE. This is done by writing the value 55h into the INDEX location. Any Reset event to the device, including PLTRST#, will again disable the interface, requiring it to be re-enabled by this method.

The Configuration Port can also be disabled explicitly by writing the value AAh to the INDEX location. Register accesses will be disabled until the value 55h is again written to the INDEX location. The Configuration Port still claims I/O transfers even while disabled, so the Disabled state does not cause these transfers to be propagated to LPC.

6.4 Register Reset Domains

This section defines the Reset events that affect the register set.

Name	Description
PLTRST	Activation of the PLTRST# input pin by the Chipset. This is a CPU Reset, also called “PCI Reset”. This same signal goes from the Chipset, in parallel, to LPC devices as “LRESET#.
eSPI_RESET	Activation of the eSPI_RESET# input pin by the Chipset. This happens on every Power On Reset of this chip, and also on certain error conditions detected by the Chipset that do not remove power to the device. This reset state also activates the PLTRST reset.
RESETI	Reset In: Power On Reset to the device, signaled by activation of the RESETI# input pin low. This signal comes to both the ECE1200 device and the Chipset from the system as the RSMRST# signal. This signal resets all the registers and logic in this block to its default state, and also activates the eSPI_RESET and PLTRST resets.

6.5 Interrupts

IRQ interrupts are asserted through the Serial IRQ feature only.

The SMI# Virtual Wire may be configured to come from its dedicated Serial IRQ slot.

IRQs, and SMI# from Serial IRQ, are acknowledged only at the source, requiring no separate interaction with the ECE1200 device.

Error exceptions may be configured to be transmitted on detection of certain LPC errors, These consist of the eSPI Virtual Wires ERROR_FATAL, ERROR_NONFATAL, SMI# or SCI#. Where provided for in the eSPI protocol, the UNSUCCESSFUL COMPLETION response is also sent for these errors, unconditionally.

The IOCHK# (or IOCHCK#) slot in the Serial IRQ frame may also be configured to generate one of the error exceptions above. This may be made conditional on whether an LPC transfer was in progress at the time.

Error exceptions on LPC, or IOCHK# activation, are reported in local registers, and are to be acknowledged there.

6.6 Low Power Modes

By default, the ECE1200 device operates at full power. There are the following options, which may be selected by initialization after each PLTRST reset event:

- One of the two LPC Clock pins may be disabled. This is done in the Clock Enable Register. By default, both LPC Clock pins are enabled.
- The Serial IRQ feature may be placed in Quiet Mode. This is done in the SERIRQ Enable and Mode Register.
- A Serial IRQ clock gating mode may be selected to stop internal clocking of the Serial IRQ Master whenever it is idle and in Quiet Mode. This is done in the SERIRQ Enable and Mode Register.
- The CLKRUN# feature may be enabled to gate either or both LPC clocks while both the LPC and Serial IRQ interfaces are idle. This requires the Serial IRQ Quiet Mode to be selected also. The CLKRUN# functionality is configured using the Clock Enable Register, the CLKRUN Control Register and the CLKRUN Idle Clocks Register.
- Internal clocking as well as external clocking may be gated while LPC clocks are idle (typically due to the CLKRUN# feature). This is called Light Sleep, and is enabled using the IDLE_GATEOSC bit in the Power Save Register.
- Deep Sleep mode may be selected. In this mode, whenever the LPC and Serial IRQ features are idle and the CLKRUN# feature has turned the LPC clocks off, the HOST_C10 Virtual Wire will be monitored from the Chipset. If HOST_C10 is high under these conditions, the ECE1200 device will turn off its internal oscillator, entering its Deep Sleep state. Recovery from this state takes a period of time to establish a new frequency lock against the SUSCLK input. Deep Sleep is enabled using the VW_C10_STOPOSC bit in the Power Save Register.
  To avoid the recovery delay, the FORCE_OSC_LOCK bit may also be set to ‘1’, and the tradeoff is that the clocking in the device (including the LPC Clocks) will be slower than specified until the full lock is achieved.

6.7 System Settings

The following items constitute a list of Chipset options to be addressed in the design process.

6.7.1 SET UP SOFT-STRAPS FOR ESPI

The ECE1200 device is capable of operating at the 50MHz eSPI DC and AC specifications. However, it does not itself enforce this limit. The Chipset's PCH Soft-Strap settings (in Flash) must select this, or a lower frequency, as the maximum for correct operation.

Other Soft-Strap selections will choose such eSPI options as the bus width and the number of Slave devices. These selections are communicated to the Slave(s) by Chipset hardware actions, and do not involve any software setup.

6.7.2 DEFER PCH SUSWARN# AND SUSACK# PINS TO ECE1200

The earliest eSPI-capable PCH devices have lost the SUSWARN# and SUSACK# pins in the trade-off to support eSPI, requiring that these pins be implemented as Virtual Wires instead. For this reason, these pins are re-created on the ECE1200 pinout. SUSWARN# and SUSACK# represent a mandatory handshake in any system that uses the Intel Deep Sleep Well (DSW) state. SUSWARN# is an output pin, and the SUSACK# input pin must follow it, both rising and falling edges, with an optional system-imposed external delay if necessary. It is acceptable to tie these pins together in the simplest case.

In later PCH devices, these pins may again be provided on the PCH itself. In at least one case (IceLake), these pins are provided, but multiplexed with the SMBus "SMLink1" pins, with SUSWARN# / SUSACK# being the default. If the SMLink1 capability is needed (for Chipset Temperature and RTC Register access) then it must be selected, and the SUSWARN# / SUSACK# functionality can still come from the ECE1200 device as Virtual Wires instead. For pre-boot configuration of the PCH pins, see the Intel documentation.

If, however, it is desired to keep the SUSWARN# / SUSACK# pin functionality on the PCH pins, then it is recommended that the SUSACK# pin on the ECE1200 device be tied permanently low (its expected default state) so that Virtual Wire traffic from it does not get transmitted to the Chipset.

If the ECE1200 device is connected to eSPI Chip Select #1 (with the BOOT_DONE pin held low), then it does not participate in the SUSWARN# / SUSACK# handshakes, though it will still present the SUSWARN# state on its own output pin. This handshake, and considerations for providing it, become instead a system design decision between the "Primary" eSPI device on Chip Select #0 and the PCH.

6.8 Initialization Steps

Listed below are the recommendations for establishing communication with the ECE1200 and performing setup.

6.8.1 LPC SETUP (NONE)

There is no setup of the ECE1200 required to begin LPC traffic. The LPC bus receives all I/O and Memory traffic that is routed to the ECE1200 by the Chipset, except for two bytes at its I/O Base Address for internal register access.

6.8.2 BASE ADDRESS RE-ASSIGNMENT (OPTIONAL)

From its reset state, the ECE1200 device's access portal for internal registers is configured to occupy I/O addresses 008Ch and 008Dh in order to avoid addressing conflict with other legacy devices. In nearly all system configurations, it is accessible immediately at these addresses, requiring no special routing considerations within the Host Chipset. But the ECE1200 may also be re-configured, if desired, in order to move it into another I/O region.

The default addresses reside in an unused section of the Host Chipset's Port 80h region (also called the "Debug Port region" or "RPR region") of the Host I/O space, where 8Ch is the INDEX location and 8Dh is the DATA location. The I/O address of the INDEX location is called the ECE1200 device's "Base Address".

Re-assignment of this default Base Address is only required if the system's Port 80h display function is not located on the LPC bus, downstream of the ECE1200. See Section 6.8.2.1, "Routing Within the Host Chipset," on page 36, for a brief application note on possible system routing variations.

If it is desired to perform a Base Address re-assignment, use the following steps:

1. According to Section 6.8.2.1, "Routing Within the Host Chipset," on page 36, set up the Host Chipset to ensure that Port 80h / RPR traffic is routed to the ECE1200, if only temporarily.
2. According to Section 6.3.1, write the value 55h to the INDEX I/O location at 8Ch to enable register access.
3. If it is possible that this sequence is happening without a previous PLTRST# reset assertion, ensure that Logical Device 0 is selected, by doing the following:
   a) Write 07h to the INDEX location 8Ch, designating the global Logical Device Number Register.
   b) Write 00h to the DATA location 8Dh.
4. Designate a new Base Address:
   a) Write 36h to the INDEX location 8Ch, designating the I/O BAR Address LS Register.
   b) Write the LS byte of the new Base Address to the DATA location 8Dh.
   c) Write 37h to the INDEX location 8Ch, designating the I/O BAR Address MS Register.
   d) Write the MS byte of the new Base Address to the DATA location 8Dh.

   Note that all four Writes must be performed, and in this order, even if they do not change a value that is already in one of the registers. Until this sequence is done completely, none of the 16-bit value changes internally.
5. If routing in the Chipset for Step 1 above was intended to be temporary, it may now be restored.

From this point onward, the ECE1200 will recognize only the new Base Address, and no longer 8Ch/8Dh, for accesses to its internal registers.

6.8.2.1 Routing Within the Host Chipset

The initial default routing within the Host Chipset directs the Port 80h I/O region (including Ports 8Ch/8Dh) to the eSPI bus, on eSPI Chip Select #0 (CS0#).

In eSPI Chipsets supporting more than one device on separate Chip Selects, the ECE1200 may reside on a different Chip Select (for example CS1#). A bit is provided in these Chipsets to re-route the Port 80h / RPR region to one of these other Chip Selects. As an example, for eSPI CS1# in the C620 series Chipset's PCH, this is the DPCS1RE bit, at bit position [14] of register PCCS1IORE.

Another available routing selection in most Chipsets is to map the Port 80h / RPR region onto the PCIe bus instead of eSPI. Since that routes the region away from eSPI entirely, the ECE1200 will need to have its Base Address re-assigned elsewhere unconditionally. Within the PCH, this routing is controlled by the RPR bit in register GCR, but note that this bit's default state still routes to eSPI initially.

6.8.3 ENABLE REGISTER ACCESS

If not already done as part of Section 6.8.2, "Base Address Re-Assignment (Optional)," on page 35, then write the value 55h to the INDEX I/O location to enable register access according to Section 6.3.1.

6.8.4 SET UP SERIAL IRQ

The SERIRQ Enable and Mode Register must be initialized in order to set up and start Serial IRQ traffic. It is in the Logical Device 01h register region.

When starting the Serial IRQ function, it is necessary to set the SIRQ_EN bit and the SIRQ_MD bit both to '1' in the same Write transfer. This starts the Serial IRQ traffic in Continuous Mode initially. Quiet Mode may be selected optionally at a later time.

IRQ slots are propagated over eSPI using their legacy IRQ numbers by default, but may be re-designated if desired using registers in Logical Device 00h, at indexes ACh through B7h.

The slots INTA# through INTD# are disabled by default, but may be assigned an IRQ number over eSPI using registers in Logical Device 00h, at indexes B8h through BBh. Levels on these slots are simply propagated to the PCH on the designated eSPI IRQ Virtual Wires, and the processing of them is left to the APIC block of the PCH and the ISRs attached to them.

The SMI# and IOCHK# slots are optional and disabled by default, but may be enabled as desired.

- SMI# will be transmitted over eSPI always as the SMI# Virtual Wire. Use SERIRQ Exception Enables Register in Logical Device 01h to enable the Serial IRQ slot.
- The IOCHK# slot can be attached to any one of four Virtual Wires for error handling. Use SERIRQ Exception Enables Register in Logical Device 01h to enable the slot, and Global registers IOCHK Non-Posted Error Handling Register, IOCHK Posted Error Handling Register and IOCHK Idle Error Handling Register to configure the handling for IOCHK# occurring within a Non-Posted transfer, a Posted transfer, or neither (LPC idle), respectively.

6.8.5 SELECT LPC CLOCK OUTPUTS

By default, both LPC Clock outputs are running. To save power, it is possible to turn off an Enable bit provided for each output. A disabled clock is unaffected by the CLKRUN# feature, and remains held low. See the Clock Enable Register in the Logical Device 01h register space.

6.8.6 SET UP OPTIONAL CLKRUN# CLOCK GATING

By default, any LPC Clock pin that remains enabled (above) is free-running. To optionally allow the CLKRUN# function to gate them during idle LPC and SERIRQ times, it is necessary to:

1. Designate whether each pin will be controlled by CLKRUN#, using bits in the Clock Enable Register in the Logical Device 01h register space.
2. Enable the CLKRUN# feature itself in the CLKRUN Control Register in the Logical Device 01h register space. Until this is done, the CLKRUN# pin is held low, and the designated LPC clock output(s) will not be gated.

For CLKRUN# gating to operate, it is also necessary for the Serial IRQ feature to be set to Quiet Mode. Until this is done, the CLKRUN# pin will remain low and clocks will not be gated.

6.8.7 SET UP OPTIONAL LPC ERROR HANDLING

The various errors that may be signaled in LPC traffic may be routed over eSPI. These are “Unclaimed” (which includes invalid SYNC codes) and “SYNC Abort”, which is an error occurring in a Claimed cycle.

In eSPI terms, “Non-Posted” traffic (I/O Read or Write, and Memory Read) will unconditionally provide the eSPI UNSUCCESSFUL COMPLETION response on these errors, and this may be enough.

However, “Posted” traffic (Memory Write) does not have the opportunity to respond this way. If error indications are required, this must be done asynchronously using a Virtual Wire.

Therefore, an LPC error condition may be attached to a Virtual Wire for reporting of Posted errors. Non-Posted errors may also be attached to Virtual Wires in addition to the UNSUCCESSFUL COMPLETION response. The Virtual Wire may be selected as either ERROR_FATAL, ERROR_NONFATAL, SMI# or SCI#.

See the Global register set, indexes 08h through 10h for these settings. By default, no Virtual Wire handlings are selected.

Errors are reported in the Global registers at indexes 12h and 13h. These registers are where polling for errors occurs and where they can be acknowledged / cleared.

In addition, there is a group of logging registers in Logical Device 01h, indexes F2h through F8h, where the LPC error type, the LPC address and the access type (Read vs.Write, and I/O vs. Memory) are captured. These registers are not cleared on PLTRST events, so they may be read after a system restart.

6.9 Global Register Set

Registers for the Global Register region are shown in the following summary table, according to the INDEX value used to select them. This region, from INDEX values 00h through 2Fh, is accessible regardless of the setting of the Logical Device Number Register.

TABLE 6-2: GLOBAL REGISTER SUMMARY

Index	Register Name
00h	Test
01h	Test
02h	Test
03h	Reserved
04h	Reserved
05h	Reserved
06h	Reserved
07h	Logical Device Number Register
08h	Unclaimed Non-Posted Error Handling Register
09h	Sync Abort Non-Posted Error Handling Register
0Ah	Reserved
0Bh	IOCHK Non-Posted Error Handling Register
0Ch	IOCHK Idle Error Handling Register
0Dh	Unclaimed Posted Error Handling Register
0Eh	Sync Abort Posted Error Handling Register
0Fh	Reserved
10h	IOCHK Posted Error Handling Register
11h	Reserved
12h	eSPI Virtual Wire Errors Register
13h	eSPI Virtual Wire Error Events Register
14h	Test
15h	Test
16h	Test
17h	Test
18h	Test
19h	Test
1Ah	Test
1Bh	Test
1Ch	Device Revision Register
1Dh	Device Sub ID Register
1Eh	Device ID LS Register
1Fh	Device ID MS Register
20h	Legacy Device ID Register
21h	Legacy Device Rev Register
22h	Test
23h	Test
24h	Test
25h	Test
26h	Test
27h	Test

TABLE 6-2: GLOBAL REGISTER SUMMARY (CONTINUED)

Index	Register Name
28h	Test
29h	Test
2Ah	Power Save Register
2Bh	Test
2Ch	Test
2Dh	Reserved
2Eh	Test
2Fh	Test

6.9.1 RESERVED

Reserved Register locations are unused for any purpose. Writes are ignored, and Reads return “0”.

6.9.2 TEST

Test Registers are reserved for Microchip use in testing. Contents of these registers are unspecified and may change dynamically. Writing these locations, even to rewrite their contents, may cause behavior that is unspecified: do not write them at all, except as directed by Microchip customer support.

6.9.3 LOGICAL DEVICE NUMBER REGISTER

Index	07h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Logical Device Number	R/W	00h	PLTRST

6.9.4 UNCLAIMED NON-POSTED ERROR HANDLING REGISTER

Index	08h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	Reserved	R	0h	-
3:0	Handling selected for Unclaimed Non-Posted LPC transfers, in addition to UNSUCCESSFUL COMPLETION eSPI response: 0h = No additional action 1h = Post VWire ERROR_NONFATAL 2h = Post VWire ERROR_FATAL 3h = Post VWire SMI# 4h = Post VWire SCI#	R/W	0h	PLTRST

6.9.5 SYNC ABORT NON-POSTED ERROR HANDLING REGISTER

Index	09h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	Reserved	R	0h	-
3:0	Handling selected for explicit ABORT Sync code on Non-Posted LPC transfers, in addition to UNSUCCESSFUL COMPLETION eSPI response: 0h = No additional action 1h = Post VWire ERROR_NONFATAL 2h = Post VWire ERROR_FATAL 3h = Post VWire SMI# 4h = Post VWire SCI#	R/W	0h	PLTRST

6.9.6 IOCHK NON-POSTED ERROR HANDLING REGISTER

Index	0Bh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	Reserved	R	0h	-
3:0	Handling selected for IOCHK# received during Non-Posted LPC transfers. The LPC transfer will continue, and may succeed or fail on its own. 0h = No additional action 1h = Post VWire ERROR_NONFATAL 2h = Post VWire ERROR_FATAL 3h = Post VWire SMI# 4h = Post VWire SCI#	R/W	0h	PLTRST

6.9.7 IOCHK IDLE ERROR HANDLING REGISTER

Index	0Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	Reserved	R	0h	-
3:0	Handling selected for IOCHK# received while no LPC transfer is in progress: 0h = No action (ignore) 1h = Post VWire ERROR_NONFATAL 2h = Post VWire ERROR_FATAL 3h = Post VWire SMI# 4h = Post VWire SCI#	R/W	0h	PLTRST

6.9.8 UNCLAIMED POSTED ERROR HANDLING REGISTER

Index	0Dh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	Reserved	R	0h	-
3:0	Handling selected for an unclaimed Posted LPC transfer (Memory Write). 0h = No action (ignore) 1h = Post VWire ERROR_NONFATAL 2h = Post VWire ERROR_FATAL 3h = Post VWire SMI# 4h = Post VWire SCI#	R/W	0h	PLTRST

6.9.9 SYNC ABORT POSTED ERROR HANDLING REGISTER

Index	0Eh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	Reserved	R	0h	-
3:0	Handling selected for an explicit ABORT Sync code received during a Posted LPC transfer (Memory Write). 0h = No action (ignore) 1h = Post VWire ERROR_NONFATAL 2h = Post VWire ERROR_FATAL 3h = Post VWire SMI# 4h = Post VWire SCI#	R/W	0h	PLTRST

6.9.10 IOCHK POSTED ERROR HANDLING REGISTER

Index	10h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	Reserved	R	0h	-
3:0	Handling selected for IOCHK# received during a Posted LPC transfer (Memory Write). 0h = No action (ignore) 1h = Post VWire ERROR_NONFATAL 2h = Post VWire ERROR_FATAL 3h = Post VWire SMI# 4h = Post VWire SCI#	R/W	0h	PLTRST

6.9.11 ESPI VIRTUAL WIRE ERRORS REGISTER

Index	12h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	Reserved	R	0	-
6	Reserved	R	0	-
5	CLEAR_NFE Write ‘1’ to clear the NFE_STATUS bit. Reads as ‘0’ always.	WO	0	eSPI_RESET
4	NFE_STATUS Current state of the ERROR_NONFATAL Virtual Wire. Cleared by the CLEAR_NFE bit.	RO	0	eSPI_RESET
3	Reserved	R	0	-
2	Reserved	R	0	-
1	CLEAR_FE Write ‘1’ to clear the FE_STATUS bit. Reads as ‘0’ always.	W	0	eSPI_RESET
0	FE_STATUS Current state of the ERROR_FATAL Virtual Wire. Cleared by the CLEAR_FE bit.	RO	0	eSPI_RESET

6.9.12 ESPI VIRTUAL WIRE ERROR EVENTS REGISTER

Index	13h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	Reserved	R	0	-
6	Reserved	R	0	-
5	CLEAR_SCIE Write ‘1’ to clear the SCIE_STATUS bit. Reads as ‘0’ always.	W	0	PLTRST
4	SCIE_STATUS Current state of the SCI Error (‘1’ = forcing SCI# low). Cleared by the CLEAR_SCIE bit.	RO	0	PLTRST
3	Reserved	R	0	-
2	Reserved	R	0	-
1	CLEAR_SMIE Write ‘1’ to clear the SMIE_STATUS bit. Reads as ‘0’ always.	W	0	PLTRST
0	SMIE_STATUS Current state of the SMI Error (‘1’ = forcing SMI# low). Cleared by the CLEAR_SMIE bit.	RO	0	PLTRST

6.9.13 DEVICE REVISION REGISTER

Index	1Ch			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Device Revision	R	-	-

6.9.14 DEVICE SUB ID REGISTER

Index	1Dh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Device Sub ID	R	65h	-

6.9.15 DEVICE ID LS REGISTER

Index	1Eh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Device ID (Least-Significant 8 bits)	R	21h	-

6.9.16 DEVICE ID MS REGISTER

Index	1Fh			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Device ID (Most-Significant 8 bits)	R	00h	-

6.9.17 LEGACY DEVICE ID REGISTER

Index	20h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Legacy Device ID 8 bits only: This encoding defers to the 16-bit Device ID.	R	FEh	-

6.9.18 LEGACY DEVICE REV REGISTER

Index	21h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Legacy Device Revision	R	-	-

6.9.19 POWER SAVE REGISTER

Index	2Ah			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	OSC_LOCKED '1' in this bit indicates that the on-chip oscillator is locked to the 32KHz SUSCLK input.	R	-	PLTRST
6	FORCE_OSC_LOCK Writing '1' into this bit forces the oscillator output to be used for all activity regardless of whether it is locked. The LPC clocks will be slower than specified if not locked.	R/W	0	PLTRST
5	Reserved	R	0	-
4	Reserved	R	0	-
3	Reserved	R	0	-
2	Reserved	R	0	-
1	IDLE_GATEOSC A '1' written into this bit will save power by gating off internal clocking to some chip functions whenever they are idle.	R/W	0	PLTRST
0	VW_C10_STOPOSC Connected Standby support to save internal power. A '1' written into this bit will enable Deep Sleep Mode to be entered whenever the HOST_C10 Virtual Wire is high while all the device interfaces (eSPI, LPC, SERIRQ and LPC Clocks) are already idle. In Deep Sleep Mode the internal oscillator is turned off.	R/W	0	PLTRST

6.10 eSPI Register Set, Logical Device 00h

Registers in the eSPI Register region are used in managing the Host interface functions over eSPI. They are shown in the following summary table, according to the INDEX value used to select them. This region is accessible from INDEX values 30h through FFh while the value 00h is held in the Logical Device Number Register.

TABLE 6-3: ESPI REGISTER SUMMARY

Index	Register Name
30h	Test
31h - 33h	Reserved
34h	Test
35h	Test
36h	I/O BAR Address LS Register
37h	I/O BAR Address MS Register
38h -- 54h	Reserved
55h	Inaccessible (INDEX=55h is Enable Configuration Mode code)
56h -- A9h	Reserved
AAh	Inaccessible (INDEX=AAh is Disable Configuration Mode code)
ABh	Reserved
ACh	Map SERIRQ IRQ1 Slot Register
ADh	Map SERIRQ IRQ3 Slot Register
AEh	Map SERIRQ IRQ4 Slot Register
AFh	Map SERIRQ IRQ5 Slot Register
B0h	Map SERIRQ IRQ6 Slot Register
B1h	Map SERIRQ IRQ7 Slot Register
B2h	Map SERIRQ IRQ9 Slot Register
B3h	Map SERIRQ IRQ10 Slot Register
B4h	Map SERIRQ IRQ11 Slot Register
B5h	Map SERIRQ IRQ12 Slot Register
B6h	Map SERIRQ IRQ14 Slot Register
B7h	Map SERIRQ IRQ15 Slot Register
B8h	Map SERIRQ INTA# Slot Register
B9h	Map SERIRQ INTB# Slot Register
BAh	Map SERIRQ INTC# Slot Register
BBh	Map SERIRQ INTD# Slot Register
BCh -- BFh	Test
C0h -- EFh	Reserved
F0h	Test
F1h -- FFh	Reserved

6.10.1 I/O BAR ADDRESS LS REGISTER

This register holds the least-significant half of the I/O address of the Configuration Port used to access the internal register set. The I/O address provided here is the address of the INDEX byte, and the DATA byte occupies this address plus one. Initially these registers select the default locations: INDEX at 008Ch and DATA at 008Dh.

Both of these registers must be written, LS first and then MS, before the new I/O address is used, otherwise unspecified behavior may result.

Bit[0] of this register must always be written as '0' (expressing an Even address).

Index	36h of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	I/O Address of the Configuration Port, Least-Significant 8 bits. The written value is not used internally until the associated MS register is subsequently written.	R/W	8Ch	PLTRST

6.10.2 I/O BAR ADDRESS MS REGISTER

This register holds the most-significant half of the I/O address of the Configuration Port used to access the internal register set. Upon writing this byte, all further accesses must use the newly-written I/O address for the INDEX and DATA locations.

Index	37h of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	I/O Address of the Configuration Port, Most-Significant 8 bits. The new I/O address is used immediately after this register is written. The LS register must have been written first.	R/W	00h	PLTRST

6.10.3 MAP SERIRQ IRQ1 SLOT REGISTER

Index	ACh of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 2. By default it selects the legacy IRQ1 function. FFh written in this register disconnects this slot from any IRQ; otherwise, any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	01h	PLTRST

6.10.4 MAP SERIRQ IRQ3 SLOT REGISTER

Index	ADh of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 4. By default it selects the legacy IRQ3 function. FFh written in this register disconnects this slot from any IRQ; otherwise, any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	03h	PLTRST

6.10.5 MAP SERIRQ IRQ4 SLOT REGISTER

Index	AEh of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 5. By default it selects the legacy IRQ4 function. FFh written in this register disconnects this slot from any IRQ; otherwise, any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	04h	PLTRST

6.10.6 MAP SERIRQ IRQ5 SLOT REGISTER

Index	AFh of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 6. By default it selects the legacy IRQ5 function. FFh written in this register disconnects this slot from any IRQ; otherwise, any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	05h	PLTRST

6.10.7 MAP SERIRQ IRQ6 SLOT REGISTER

Index	B0h of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 7. By default it selects the legacy IRQ6 function. FFh written in this register disconnects this slot from any IRQ; otherwise, any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	06h	PLTRST

6.10.8 MAP SERIRQ IRQ7 SLOT REGISTER

Index	B1h of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 8. By default it selects the legacy IRQ7 function. FFh written in this register disconnects this slot from any IRQ; otherwise, any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	07h	PLTRST

6.10.9 MAP SERIRQ IRQ9 SLOT REGISTER

Index	B2h of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 10. By default it selects the legacy IRQ9 function. FFh written in this register disconnects this slot from any IRQ; otherwise, any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	09h	PLTRST

6.10.10 MAP SERIRQ IRQ10 SLOT REGISTER

Index	B3h of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 11. By default it selects the legacy IRQ10 function. FFh written in this register disconnects this slot from any IRQ; otherwise, any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	0Ah	PLTRST

6.10.11 MAP SERIRQ IRQ11 SLOT REGISTER

Index	B4h of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 12. By default it selects the legacy IRQ11 function. FFh written in this register disconnects this slot from any IRQ; otherwise, any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	0Bh	PLTRST

6.10.12 MAP SERIRQ IRQ12 SLOT REGISTER

Index	B5h of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 13. By default it selects the legacy IRQ12 function. FFh written in this register disconnects this slot from any IRQ; otherwise, any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	0Ch	PLTRST

6.10.13 MAP SERIRQ IRQ14 SLOT REGISTER

Index	B6h of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 15. By default it selects the legacy IRQ14 function. FFh written in this register disconnects this slot from any IRQ; otherwise, any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	0Eh	PLTRST

6.10.14 MAP SERIRQ IRQ15 SLOT REGISTER

Index	B7h of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 16. By default it selects the legacy IRQ15 function. FFh written in this register disconnects this slot from any IRQ; otherwise, any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	0Fh	PLTRST

6.10.15 MAP SERIRQ INTA# SLOT REGISTER

Index	B8h of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 18. By default it is disconnected by its initial FFh value, but any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	FFh	PLTRST

6.10.16 MAP SERIRQ INTB# SLOT REGISTER

Index	B9h of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 19. By default it is disconnected by its initial FFh value, but any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	FFh	PLTRST

6.10.17 MAP SERIRQ INTC# SLOT REGISTER

Index	BAh of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 20. By default it is disconnected by its initial FFh value, but any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	FFh	PLTRST

6.10.18 MAP SERIRQ INTD# SLOT REGISTER

Index	BBh of Logical Device 00h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Programs the eSPI IRQ to be connected to SERIRQ Slot 21. By default it is disconnected by its initial FFh value, but any IRQ number recognized by the Chipset may be selected by placing its number here.	R/W	FFh	PLTRST

6.11 LPC Register Set, Logical Device 01h

Registers in the LPC Register region are used for managing the downstream interfaces: LPC, Serial IRQ and CLKRUN#. They are shown in the following summary table, according to the INDEX value used to select them. This region is accessible from INDEX values 30h through FFh while the value 01h is held in the Logical Device Number Register.

TABLE 6-4: LPC REGISTER SUMMARY

Index	Register Name
30h	Test
31h -- 37h	Reserved
38h	Clock Enable Register
39h	Reserved
3Ah	Reserved
3Bh	Clock Control Lock Register
3Ch	CLKRUN Control Register
3Dh	CLKRUN Idle Clocks Register
3Eh	Test
3Fh	Reserved
40h	SERIRQ Enable and Mode Register
41h -- 54h	Reserved
55h	Inaccessible (INDEX=55h is Enable Configuration Mode code)
56h -- 5Fh	Reserved
60h	Test
61h -- 63h	Reserved
64h	Test
65h	Test
66h	Test
67h	Test
68h	Test
69h	Test
6Ah -- A9h	Reserved
AAh	Inaccessible (INDEX=AAh is Disable Configuration Mode code)
ABh -- EFh	Reserved
F0h	SERIRQ Exception Enables Register
F1h	SERIRQ Clocking Register
F2h	LPC Error Log Non-Posted Register
F3h	LPC Error Log Posted Register
F4h	Error Cycle Address 0 Register

TABLE 6-4: LPC REGISTER SUMMARY (CONTINUED)

Index	Register Name
F5h	Error Cycle Address 1 Register
F6h	Error Cycle Address 2 Register
F7h	Error Cycle Address 3 Register
F8h	Error Cycle Attributes Register
F9h -- FFh	Reserved

6.11.1 CLOCK ENABLE REGISTER

Index	38h of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	Reserved	R	0	-
3	CLKRUN_CTL_EN_1 '1' = LPC_CLK1 pin may be turned off by CLKRUN#. '0' = LPC_CLK1 pin is free-running. (default) This bit is lockable in the Clock Control Lock Register.	R/W	0	PLTRST
2	CLKRUN_CTL_EN_0 '1' = LPC_CLK0 pin may be turned off by CLKRUN#. '0' = LPC_CLK1 pin is free-running. (default) This bit is lockable in the Clock Control Lock Register.	R/W	0	PLTRST
1	CLK1_EN '1' = LPC_CLK1 pin may present LPC clocks. (default) '0' = LPC_CLK1 pin is held low. This bit is lockable in the Clock Control Lock Register.	R/W	1	PLTRST
0	CLK0_EN '1' = LPC_CLK0 pin may present LPC clocks. (default) '0' = LPC_CLK0 pin is held low. This bit is lockable in the Clock Control Lock Register.	R/W	1	PLTRST

6.11.2 CLOCK CONTROL LOCK REGISTER

Index	3Bh of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:5	Reserved	R	0	-
4	CLKRUN_EN_LK '1' = The CLKRUN_EN bit in the CLKRUN Control Register is locked Read-Only in its current state. The '1' value written here remains, read-only, until the next reset event. '0' = The CLKRUN_EN bit is Read/Write. (default)	R/W/L	0	PLTRST
3	CLKRUN_CLK1_LK '1' = The CLKRUN_CTL_EN_1 bit in the Clock Enable Register is locked Read-Only in its current state. The '1' value written here remains, read-only, until the next reset event. '0' = The CLKRUN_CTL_EN_1 bit is Read/Write. (default)	R/W/L	0	PLTRST
2	CLKRUN_CLK0_LK '1' = The CLKRUN_CTL_EN_0 bit in the Clock Enable Register is locked Read-Only in its current state. The '1' value written here remains, read-only, until the next reset event. '0' = The CLKRUN_CTL_EN_0 bit is Read/Write. (default)	R/W/L	0	PLTRST
1	CLK1_EN_LK '1' = The CLK1_EN bit in the Clock Enable Register is locked Read-Only in its current state. The '1' value written here remains, read-only, until the next reset event. '0' = The CLK1_EN bit is Read/Write. (default)	R/W/L	0	PLTRST
0	CLK0_EN_LK '1' = The CLK0_EN bit in the Clock Enable Register is locked Read-Only in its current state. The '1' value written here remains, read-only, until the next reset event. '0' = The CLK0_EN bit is Read/Write. (default)	R/W/L	0	PLTRST

6.11.3 CLKRUN CONTROL REGISTER

Index	3Ch of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	0	-
0	CLKRUN_EN '1' = The CLKRUN# feature is enabled. '0' = The CLKRUN# feature is disabled and cannot stop the LPC_CLK0 or LPC_EN1 clock. (default) This bit is lockable in the Clock Control Lock Register.	R/W/L	0	PLTRST

6.11.4 CLKRUN IDLE CLOCKS REGISTER

Index	3Dh of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:2	Number of Idle Clocks This is the minimum number of clocks after CLKRUN# goes high before LPC clocks get turned off. Zero represents the CLKRUN# compliant minimum. (default) A Non-Zero value increases this time by 4 clocks per unit.	R/W	00h	PLTRST
1	Reserved	R	0	-
0	Reserved.	R	0	-

6.11.5 SERIRQ ENABLE AND MODE REGISTER

Index	40h of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7	SIRQ_EN ‘1’ = The Serial IRQ feature is enabled. When writing ‘1’ to this bit initially, it is required to write ‘1’ to the SIRQ_MD bit also. ‘0’ = The Serial IRQ feature is disabled. (default)	R/W	0	PLTRST
6	SIRQ_MD ‘1’ = Serial IRQ is in Continuous Mode. ‘0’ = Serial IRQ is in Quiet Mode. (This is the hardware default, but it must be overwritten temporarily to ‘1’ when enabling Serial IRQ.)	R/W	0	PLTRST
5:2	FORMAT This field permanently selects the 21-slot format, and is presented Read-Only for legacy purposes.	R	0100b	PLTRST
1:0	START_PW ‘00’ = Start Pulse is 4 clocks wide. (default) ‘01’ = Start Pulse is 6 clocks wide. ‘10’ = Start Pulse is 8 clocks wide. ‘11’ = Reserved	R/W	00b	PLTRST

6.11.6 SERIRQ EXCEPTION ENABLES REGISTER

Index	F0h of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:6	Reserved	R	00b	-
5	IOCHK_N_SERIRQ_EN_LOCK ‘1’ = The IOCHK_N_SERIRQ_EN bit in this register is locked Read-Only in its written state. The ‘1’ value written here also remains, read-only, until the next reset event. ‘0’ = The IOCHK_N_SERIRQ_EN bit is Read/Write. (default)	R/W/L	0	PLTRST
4	SMI_N_SERIRQ_EN_LOCK ‘1’ = The SMI_N_SERIRQ_EN bit in this register is locked Read-Only in its written state. The ‘1’ value written here also remains, read-only, until the next reset event. ‘0’ = The SMI_N_SERIRQ_EN bit is Read/Write. (default)	R/W/L	0	PLTRST
3:2	Reserved	R	00b	-
1	IOCHK_N_SERIRQ_EN ‘1’ = The IOCHK# slot (Slot 17) in the SERIRQ frame is sampled and allowed to propagate to the eSPI interface. ‘0’ = The IOCHK# slot does not propagate. (default)	R/W/L	0	PLTRST
0	SMI_N_SERIRQ_EN ‘1’ = The SMI# slot (Slot 3) in the SERIRQ frame is sampled and allowed to propagate to the eSPI interface as the SMI# Virtual Wire. ‘0’ = The SMI# slot does not propagate. (default)	R/W/L	0	PLTRST

6.11.7 SERIRQ CLOCKING REGISTER

Index	F1h of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	Reserved	R	00h	-
0	SERIRQ CLK_GATE_CTL ‘1’ = Enables internal clocking at all times to the Serial IRQ circuits. (default) ‘0’ = Allows internal clocking to be shut off to Serial IRQ circuits when idle.	R/W	1	PLTRST

6.11.8 LPC ERROR LOG NON-POSTED REGISTER

Index	F2h of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:4	Reserved	R	0h	-
3	IORM_CHKIDL '1' = An IOCHK# event has occurred while the LPC bus is idle. '0' = No IOCHK# event has occurred during LPC idle, since this bit was last cleared.	R/W1C	0	eSPI_RESET
2	IORM_CHK_ACTIVE '1' = An IOCHK# event has occurred during a Non-Posted transfer on LPC (I/O Read or Write, or Memory Read). '0' = No IOCHK# event has occurred during a Non-Posted LPC transfer, since this bit was last cleared.	R/W1C	0	eSPI_RESET
1	IORM_ABTSYN '1' = An Abort SYNC event has occurred during a Non-Posted transfer on LPC (I/O Read or Write, or Memory Read). '0' = No Abort SYNC event has occurred during a Non-Posted LPC transfer, since this bit was last cleared.	R/W1C	0	eSPI_RESET
0	IORM_UNCL '1' = An Unclaimed or Invalid SYNC event has occurred during a Non-Posted transfer on LPC (I/O Read or Write, or Memory Read). '0' = No Unclaimed or Invalid SYNC event has occurred during a Non-Posted LPC transfer, since this bit was last cleared.	R/W1C	0	eSPI_RESET

6.11.9 LPC ERROR LOG POSTED REGISTER

Index	F3h of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:3	Reserved	R	00h	-
2	MW_CHK_ACTIVE '1' = An IOCHK# event has occurred during a Posted transfer on LPC (Memory Write). '0' = No IOCHK# event has occurred during a Posted LPC transfer, since this bit was last cleared.	R/W1C	0	eSPI_RESET
1	MW_ABTSYN '1' = An Abort SYNC event has occurred during a Posted transfer on LPC (Memory Write). '0' = No Abort SYNC event has occurred during a Posted LPC transfer, since this bit was last cleared.	R/W1C	0	eSPI_RESET
0	MW_UNCL '1' = An Unclaimed or Invalid SYNC event has occurred during a Posted transfer on LPC (Memory Write). '0' = No Unclaimed or Invalid SYNC event has occurred during a Posted LPC transfer, since this bit was last cleared.	R/W1C	0	eSPI_RESET

6.11.10 ERROR CYCLE ADDRESS 0 REGISTER

Index	F4h of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Byte 0 of the LPC address that was being presented on the occurrence of the last error. This is the least-significant byte of any address.	R/W	00h	eSPI_RESET

6.11.11 ERROR CYCLE ADDRESS 1 REGISTER

Index	F5h of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Byte 1 of the LPC address that was being presented on the occurrence of the last error. In I/O accesses, this is the most-significant address byte.	R/W	00h	eSPI_RESET

6.11.12 ERROR CYCLE ADDRESS 2 REGISTER

Index	F6h of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Byte 2 of the LPC address that was being presented on the occurrence of the last error. Valid in Memory accesses only.	R/W	00h	eSPI_RESET

6.11.13 ERROR CYCLE ADDRESS 3 REGISTER

Index	F7h of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:0	Byte 3 of the LPC address that was being presented on the occurrence of the last error. Valid in Memory accesses only, as the most-significant address byte.	R/W	00h	eSPI_RESET

6.11.14 ERROR CYCLE ATTRIBUTES REGISTER

Index	F8h of Logical Device 01h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:2	Reserved	R	00h	-
1	RD_NWR ‘1’ = The last LPC error occurred on a Read access. ‘0’ = The last LPC error occurred on a Write access.	R/W	0	eSPI_RESET
0	IO_NMEM ‘1’ = The last LPC error occurred on an I/O access, and the low-order two bytes of the Error Cycle Address registers hold the I/O space address. ‘0’ = The last LPC error occurred on a Memory access, and all four bytes of the Error Cycle Address registers are used to hold the Memory address.	R/W	0	eSPI_RESET

7.0 TEST MECHANISMS

7.1 Introduction

This device has the following test mechanism:

- XNOR Chain for board connectivity test

7.2 References

No references have been cited for this chapter.

7.3 Terminology

Terms are defined in the text below.

7.4 XNOR Chain

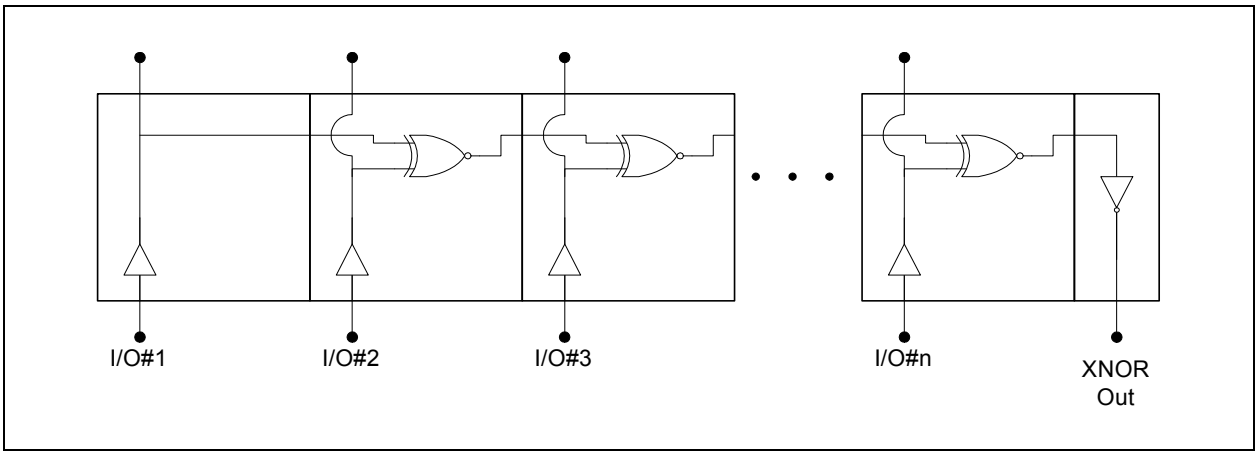
7.4.1 OVERVIEW

The XNOR Chain test mode provides a means to confirm that all ECE1200 pins are in contact with the motherboard during assembly and test operations.

An example of an XNOR Chain test structure is illustrated below in Figure 7-1, "XNOR Chain Test Structure". When the XNOR Chain test mode is enabled all pins, except for those listed in Section 7.4.2, "Excluded Pins", are disconnected from their internal functions and routed as inputs to the XNOR Chain. This allows a single input pin to toggle the XNOR Chain output if all other input pins are held high or low. The XNOR Chain output is the pin SUSWARN#.

The tests that are performed when the XNOR Chain test mode is enabled require the board-level test hardware to control the device pins and observe the results at the XNOR Chain output pin; e.g., as described in Section 7.4.3, "Test Procedure," on page 58.

FIGURE 7-1: XNOR CHAIN TEST STRUCTURE



7.4.2 EXCLUDED PINS

All pins are included in the XNOR chain, except the following:

- Power Pins (VTR_33, VTR_18, VTR_CORE_18)
- Ground Pad (VSS), on underside
- Pin RESETI#, which is the Chip Reset.
- Pin TEST, which is the Test Enable.
- Pins LAD[2:0], which are the Test Mode Selection code.
  NOTE that pin LAD3 is still part of the XNOR chain.
- Pin SUSWARN#, which is the XNOR Test Output
- All pins listed as “n/c” in Section 2.2.1, "Pin Assignments, 40-Pin VQFN".
  These need not be connected to anything, even for test purposes.

7.4.3 TEST PROCEDURE

7.4.3.1 Setup

Warning: Ensure power supply is off during Setup.

1. Connect the VSS pad to ground.
2. Connect the VTR_33, VTR_18 and VTR_CORE_18 pins to their unpowered power source.
3. Connect the VREF_CPU pin to an unpowered 1.8V power source.
4. Connect an oscilloscope or voltmeter to the Test Output pin.
5. All other pins should be pulled to ground.

7.4.3.2 Testing

1. Turn on the 3.3V power source to VTR_33 pins first.
2. Turn on the 1.8V power source to the VTR_18 and VTR_CORE_18 pins.
3. Enable the XNOR Chain as defined in Section 7.4.3.3, "Procedure to Enable the XNOR Chain".
4. Bring one input pin in the XNOR Chain high. The output on the SUSWARN# pin should toggle within 30ns. Then individually toggle each of the remaining pins in the chain. Each time a single input pin is toggled either high or low the SUSWARN# output pin should toggle.
5. Once the XNOR test is completed, exit the XNOR Chain Test Mode by the following:
   a) set pin RESETI# low,
   b) remove power to VTR_18 and VTR_CORE_18, then
   c) remove power to VTR_33.

7.4.3.3 Procedure to Enable the XNOR Chain

Perform the following with at least 1 microsecond between steps.

1. Set the RESETI# pin high.
2. Set the pins LAD[2:0] to the binary value 001.
3. Set the TEST pin high.
4. Bring the pins LAD[2:0] to the binary value 111.
5. Bring all XNOR input pins (Section 7.4.2) low.
6. The XNOR output on SUSWARN# should be seen as low.

8.0 ELECTRICAL SPECIFICATIONS

8.1 Maximum Ratings*

*Stresses exceeding those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note:	When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

8.1.1 ABSOLUTE MAXIMUM THERMAL RATINGS

TABLE 8-1: ABSOLUTE MAXIMUM THERMAL RATINGS

Parameter	Maximum Limits
Operating Temperature Range	-40°C to +85°C (Industrial)
Storage Temperature Range	-55° to +150°C
Lead Temperature Range	Refer to JEDEC Spec J-STD-020B

8.1.2 ABSOLUTE MAXIMUM SUPPLY VOLTAGE RATINGS

TABLE 8-2: ABSOLUTE POWER SUPPLY RATINGS

Symbol	Parameter	Maximum Limits
VTR_CORE_18	1.8V Logic Power Supply with respect to ground	-0.3V to +1.98V
VTR_18	1.8V I/O Power Supply with respect to ground	-0.3V to +1.98V
VTR_33	3.3V I/O Power Supply with respect to ground	-0.3V to +3.63V

8.1.3 ABSOLUTE MAXIMUM I/O VOLTAGE RATINGS

Parameter	Maximum Limits
Voltage with respect to ground on SUSCLK input pin while device is powered off. (Backdrive Tolerance)	-0.5V to +3.63V
Voltage with respect to ground on any signal pin other than SUSCLK.	-0.5V to ([Power Well of pin] + 0.5V) (Note 8-1)

Note 8-1 The Power Supply used to power the buffer is shown in the Signal Power Well column of **Section 2.0 "Pin Configuration"**.

8.2 Operational Specifications

8.2.1 POWER SUPPLY OPERATIONAL CHARACTERISTICS

TABLE 8-3: POWER SUPPLY OPERATING CONDITIONS

Symbol	Parameter	MIN	TYP	MAX	Units
VTR_CORE_18	1.8V Core Logic Power Supply with respect to ground	1.71	1.80	1.89	V
VTR_18	1.8V I/O Power Supply with respect to ground	1.71	1.80	1.89	V
VTR_33	3.3V I/O Power Supply with respect to ground	3.135	3.3	3.465	V

Note: The specification for the VTR_CORE_18, VTR_18 and VTR_33 supplies represents +/- 5% from nominal.

8.2.2 PCI AND PCI-24 PIN TYPE DC ELECTRICAL CHARACTERISTICS

The specifications for the PCI-compliant pins are listed here from the PCI Standard directly, to include only those specifications that are relevant to LPC, SER_IRQ and CLKRUN# pin functions.The PCI-24 pin type is the same as the rest of the PCI pins for these specifications.

TABLE 8-4: PCI AND PCI-24 DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	MIN	MAX	Units	Notes
Input High Voltage	V_{ih}		0.7 x VTR_33	VTR_33 + 0.5	V	
Input Low Voltage	V_{il}		-0.5	0.3 x VTR_33	V	
Input Pull-up Voltage	V_{ipu}		0.7 x VTR_33		V	Voltage guaranteed to avoid internal Receiver leakage.
Input Leakage Current	I_{il}	Vin > 0V and Vin < VTR_33		+/- 10	uA	Applies both to inputs and to hi-Z output states of I/O pins.
Output High Voltage	V_{oh}	I_{out} = -500 uA	0.9 x VTR_33		V	
Output Low Voltage	V_{ol}	I_{out} = 1500 uA		0.1 x VTR_33	V	
Input Pin Capacitance	C_{in}			10	pF	

8.2.3 LCLK PIN TYPE DC ELECTRICAL CHARACTERISTICS

The specifications for the LPC Clocks are listed here. These pin characteristics are not part of the PCI specification, since they are outputs instead of inputs.

TABLE 8-5: LCLK DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Output High Voltage	V_{OH}	I_{OH} = -16mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 16mA			0.4	V	

8.2.4 ESPI PIN TYPE DC ELECTRICAL CHARACTERISTICS

The DC specifications for eSPI pins are found in the Intel eSPI Interface Base Specification. See Section 5.2, "References," on page 24 for the eSPI document references.

8.2.5 DIO PIN TYPE DC ELECTRICAL CHARACTERISTICS

The specifications for the DIO Digital 3.3V I/O pins are listed here.

TABLE 8-6: DIO DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units	Notes
Input High Voltage	V_{IHI}		2.0			V	
Input Low Voltage	V_{ILI}				0.8	V	
Input Leakage Current	I_{IH}				+/- 10	uA	Note 8-2
Schmitt Hysteresis	V_{HYS}			400		mV	
Output High Voltage	V_{OH}	I_{OH} = -8mA	2.4			V	
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4	V	
Input Pin Capacitance	C_{IN}				20	pF	

Note 8-2 The Input Leakage specification applies both to inputs and to hi-Z outputs.

8.2.5.1 Backdrive Tolerance

Only the SUSCLK input is specified as Backdrive Tolerant, and its characteristic is given below.

TABLE 8-7: SUSCLK BACKDRIVE CHARACTERISTIC

(T_A = 0°C to +85°C)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
Input Leakage	I_{IL}	-2		+12.3	µA	VIN=3.47V, and all VTR=0V

8.2.6 THERMAL CHARACTERISTICS

Note: These values are PRELIMINARY, pending characterization.

TABLE 8-8: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Device					
Operating Junction Temperature Range	T_J	—	—	+125	°C
Operating Ambient Temperature Range - Industrial	T_A	-40	—	+85	°C
Internal Chip Power Dissipation (using V_{TR} = VTR_CORE_18 pin): $P_{INT} = V_{TR} \times I_{VTR}$ from Table 8-10 and Table 8-3 (e.g., 1.89V x 0.9mA = 1.7mW)	P_D	$P_{INT} + P_{I/O}$			W
I/O Pin Power Dissipation (each pin using its V_{TR} level VTR_33 or VTR_18): I/O = Sum (({V_{TR}– V_{OH}} x I_{OH}) + Sum (V_{OL} x I_{OL}))					
Maximum Allowed Power Dissipation (considering ambient air only)	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 8-9: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 40-pin VQFN (LDX)	θ_{JA}	50.0	—	°C/W	1, 2
	θ_{JC}	9.4	—	°C/W	1
	θ_{JB}	31.0	—	°C/W	1

Note 1: Thermal resistance values are determined by packaging simulations.
2: θ_{JA} as listed here assumes airflow of 0 m/s.

8.3 Power Consumption

Note: These values are PRELIMINARY, pending characterization.

TABLE 8-10: SUPPLY CURRENT

Case	Device State	Supply Rail	Typical (nom V, 25° C)	Max (max V, 70° C)	Max (max V, 85° C)	Units
1	Full On, Active LPC Traffic, with both LPC Clocks Running	VTR_33	11.45			mA
		VTR_18	25			uA
		VTR_CORE_18	1.25			mA
2	Full On, Active LPC Traffic, with one LPC Clock Running	VTR_33	TBD			mA
		VTR_18	25			uA
		VTR_CORE_18	1.25			mA
3	LPC Idle, Clocks Off: due to CLKRUN# High or Clocks explicitly turned off	VTR_33	2.0			uA
		VTR_18	2.3			uA
		VTR_CORE_18	0.9			mA
4	LPC On and Reset: LPC_EN High, PLTRST# Low, Both LPC Clocks Running (forced). (Transient State during Host Boot)	VTR_33	11.1			mA
		VTR_18	2.2			uA
		VTR_CORE_18	1.06			mA
5	Light Sleep LPC Clocks off and Gated Clock mode selected (IDLE_GATEOSC bit on).	VTR_33	2.0			uA
		VTR_18	2.3			uA
		VTR_CORE_18	0.44			mA
6	Deep Sleep Host C10 / S0ix State with Disabled Internal Oscillator mode selected (VW_C10_STOPOSC bit on).	VTR_33	2.0			uA
		VTR_18	2.3			uA
		VTR_CORE_18	3.6			uA

TABLE 8-10: SUPPLY CURRENT (CONTINUED)

Case	Device State	Supply Rail	Typical (nom V, 25° C)	Max (max V, 70° C)	Max (max V, 85° C)	Units
7	LPC Unpowered; Sub-S0 state: LPC_EN low, eSPI Active.	VTR_33	0.0			uA
		VTR_18	2.3			uA
		VTR_CORE_18	1.0			mA
8	LPC Unpowered, eSPI Reset: eSPI_RESET# low and RESETI# high (Transient State)	VTR_33	0.0			uA
		VTR_18	2.3			uA
		VTR_CORE_18	3.2			mA
9	Full Chip Reset (RESETI# low)	VTR_33	0.0			uA
		VTR_18	0.0			uA
		VTR_CORE_18	2.7			uA

9.0 TIMING DIAGRAMS

Note: Timing values are preliminary and may change after characterization.

9.1 SUSCLK Input Timing

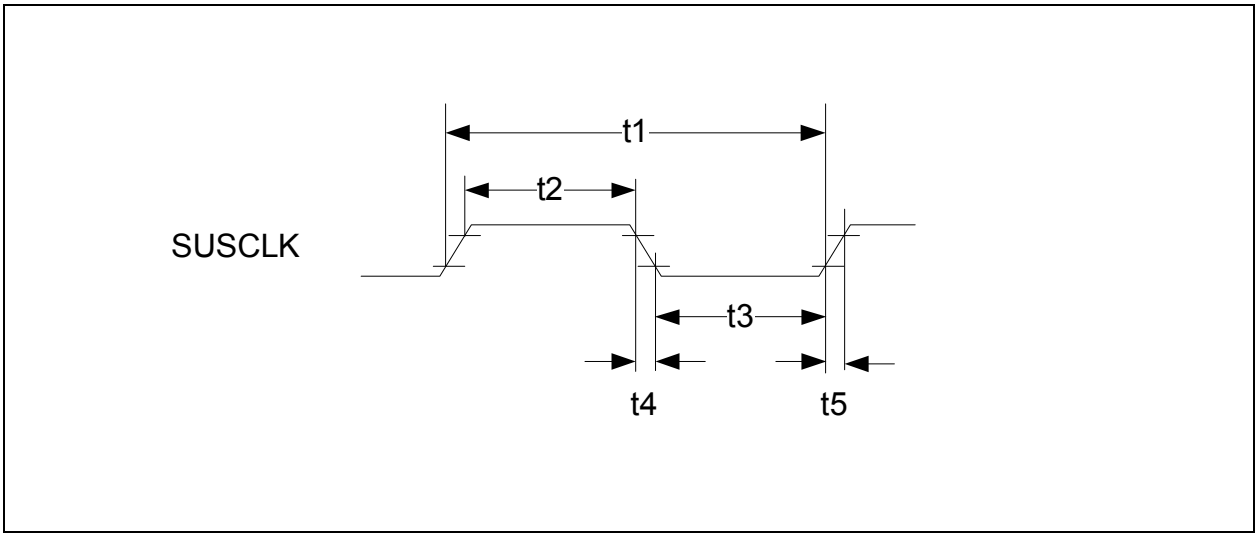


TABLE 9-1: SUSCLK TIMING PARAMETERS

Parameter	Symbol	MIN	TYP	MAX	Unit	Notes
Period	t1		30.52		us	1
High Time	t2	10				2
Low Time	t3					2
Rise Time	t4			1		2
Fall Time	t5					2
Frequency	1 / t1		32.768		kHz	1

Note 1: Period is required to be accurate within +/- 100ppm.

2: High, Low, Rise and Fall times use reference points of 20% and 80% of the full voltage swing, as shown.

9.2 LPC Interface Timing

9.2.1 LPC_CLK[1:0] OUTPUT TIMING

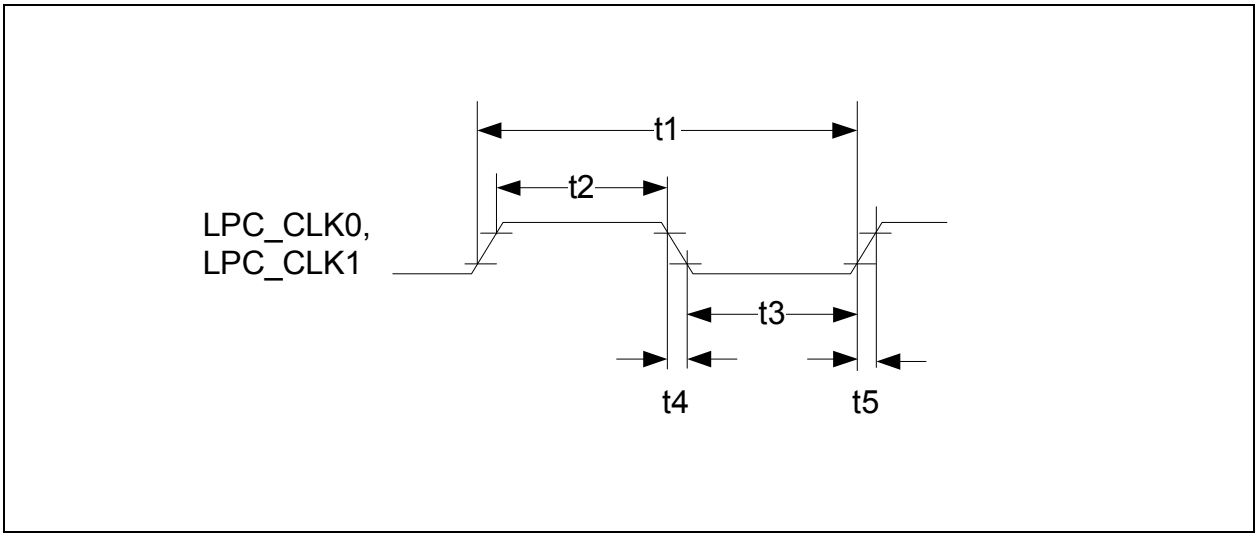


TABLE 9-2: LPC CLOCK TIMING PARAMETERS

Parameter	Symbol	MIN	TYP	MAX	Unit	Notes
Period	t1	40	41.7	44	ns	1, 2
High Time	t2	15				3
Low Time	t3					3
Rise Time	t4			3		3
Fall Time	t5					3

Note 1: Nominal period (TYP) reflects 24MHz frequency.

2: When allowed to operate without frequency lock, the maximum period does not apply.

3: High, Low, Rise and Fall times use reference points of 20% and 80% of the full voltage swing, as shown.

9.2.2 PCI, PCI_24 PIN TYPE OUTPUT TIMING

See the table in Section 2.2.1, "Pin Assignments, 40-Pin VQFN," on page 10 for the pin types.

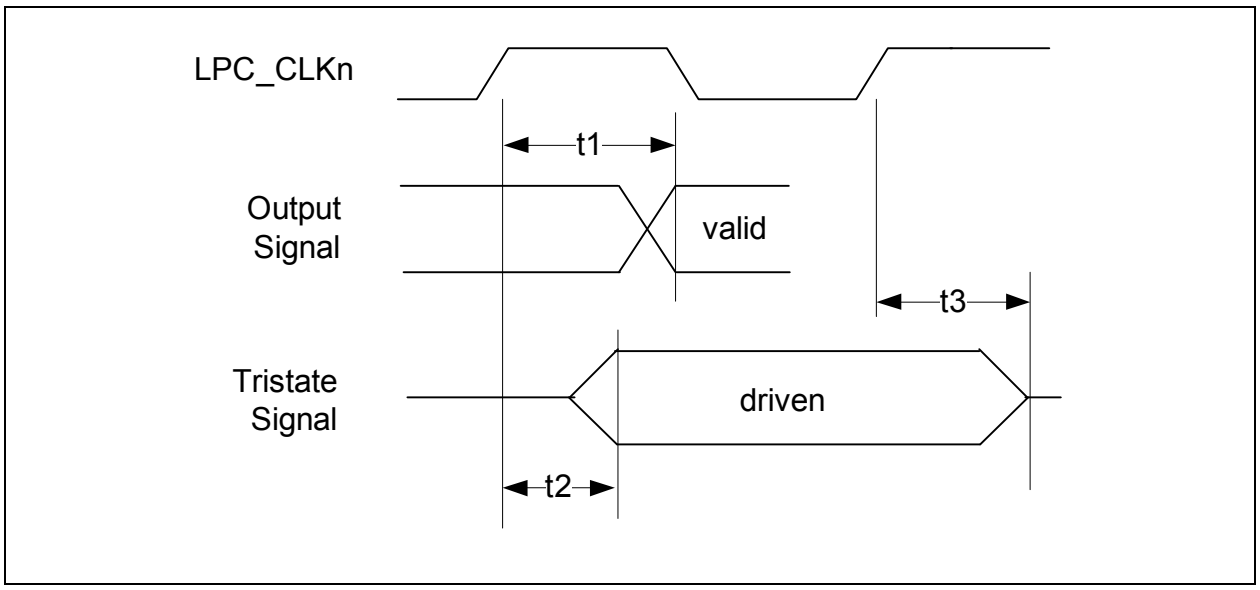


TABLE 9-3: PCI, PCI_24 PIN TYPE OUTPUT TIMING PARAMETERS

Parameter	Symbol	Pin Type	MIN	TYP	MAX	Unit	Notes
Clock to Valid	t1	PCI	2		11	ns	
		PCI_24	3		15		1
Clock to Actively Driven	t2	PCI	2		11		
		PCI_24	3		15		1
Clock to Floating	t3	PCI, PCI_24			28		

Note 1: PCI_24 pin specs are slightly de-rated for 24MHz operation instead of original 33MHz PCI standard.

9.2.3 PCI, PCI_24 PIN TYPE INPUT TIMING

See the table in Section 2.2.1, "Pin Assignments, 40-Pin VQFN," on page 10 for the pin types. PCI and PCI_24 pin types have identical input characteristics.

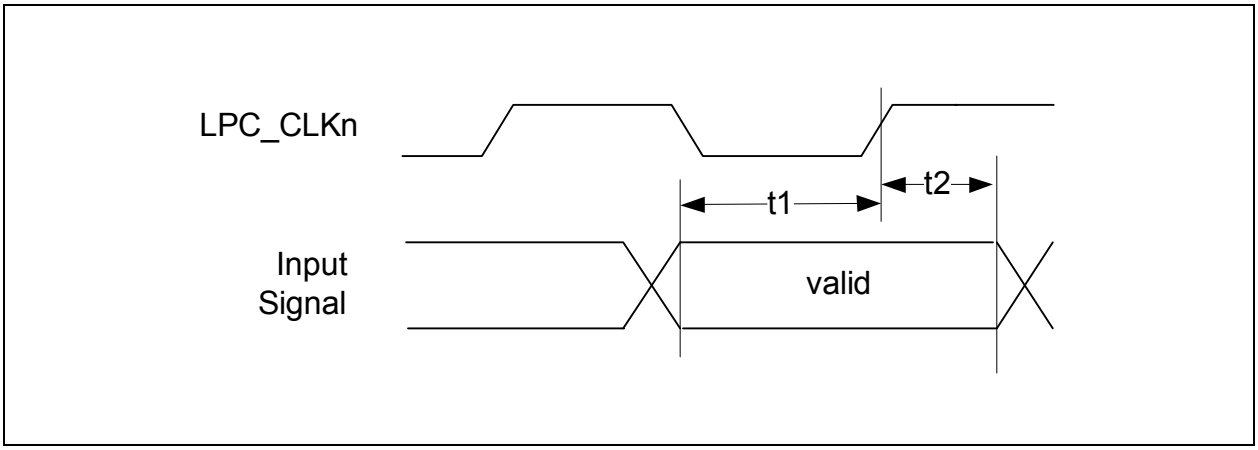


TABLE 9-4: PCI, PCI_24 PIN TYPE INPUT TIMING PARAMETERS

Parameter	Symbol	MIN	TYP	MAX	Unit	Notes
Valid Input Setup to Clock	t1	7			ns	1
Valid Input Hold From Clock	t2	0				1

Note 1: PCI and PCI_24 pin input specs are identical.

9.3 eSPI Interface Timing

The eSPI Interface conforms to the timings specified by Intel for 50MHz eSPI operation. See the eSPI reference documents listed in Section 5.2, "References," on page 24.

The frequency is selected strictly using Soft-Strap settings for the Intel Chipset, and the ECE1200 does not itself negotiate to limit it. During initialization of the eSPI bus, the frequency used is 20MHz max, until the Soft-Strap options take effect.

The clock frequency actually provided by the Intel Chipset may be documented as 48MHz instead. See the relevant Intel specifications.

9.4 Wake Timing

9.4.1 WAKE FROM DEEP SLEEP STATE BY ESPI ACCESS

Note: Timing values are preliminary and may change after characterization.

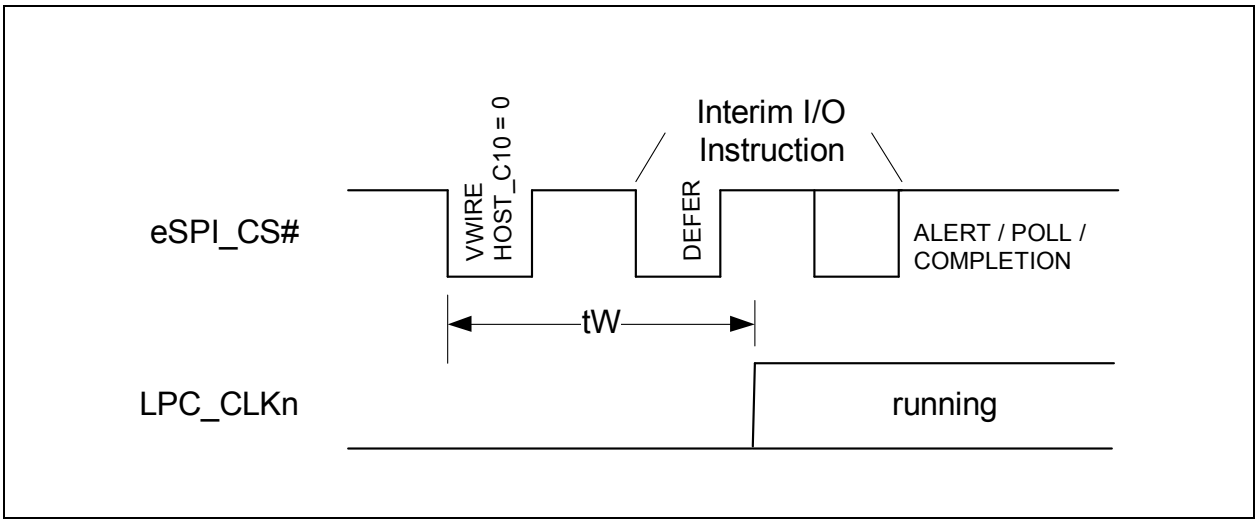


TABLE 9-5: WAKE DELAY FROM DEEP SLEEP BY ESPI ACCESS

Parameter	Symbol	MIN	TYP	MAX	Unit	Notes
Wake from Deep Sleep	tW			3.0	ms	

Note: Other Wake scenario timings are TBD.

9.5 Voltage Sequencing and Power Good Timing

9.5.1 VTR SEQUENCING AND RESETI# TIMING

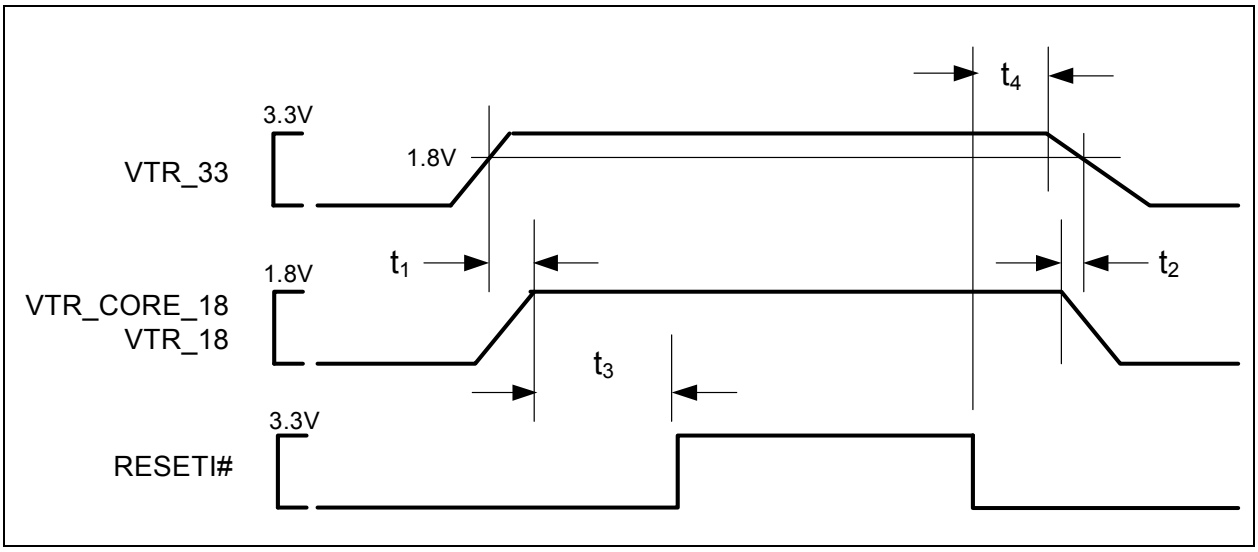


TABLE 9-6: VTR TIMING

Parameters	Symbol	MIN	TYP	MAX	Unit	Notes
VTR_33 > 1.8V to VTR_18 or VTR_CORE_18 On	t1	0			ns	
VTR_18 and VTR_CORE_18 Off to VTR_33 < 1.8V	t2	0			ns	
All VTR voltages valid to RESETI# high	t3	10			ms	Note:
RESETI# low to any VTR voltage invalid	t4	0			ns	Note:

Note: RESETI# must remain low and must not glitch during VTR power presentation / removal.

9.6 Strap Option Sampling Timing

The ESPI_STRAP_0 and ESPI_STRAP_1 pins are sampled and latched internally for test purposes. It is recommended that they be left floating or N/C except in XNOR Chain test mode, so that internal weak pull-ups can pull them high to the VTR_33 level.

TABLE 9-7: GENERIC STRAP OPTION SAMPLING TIMING

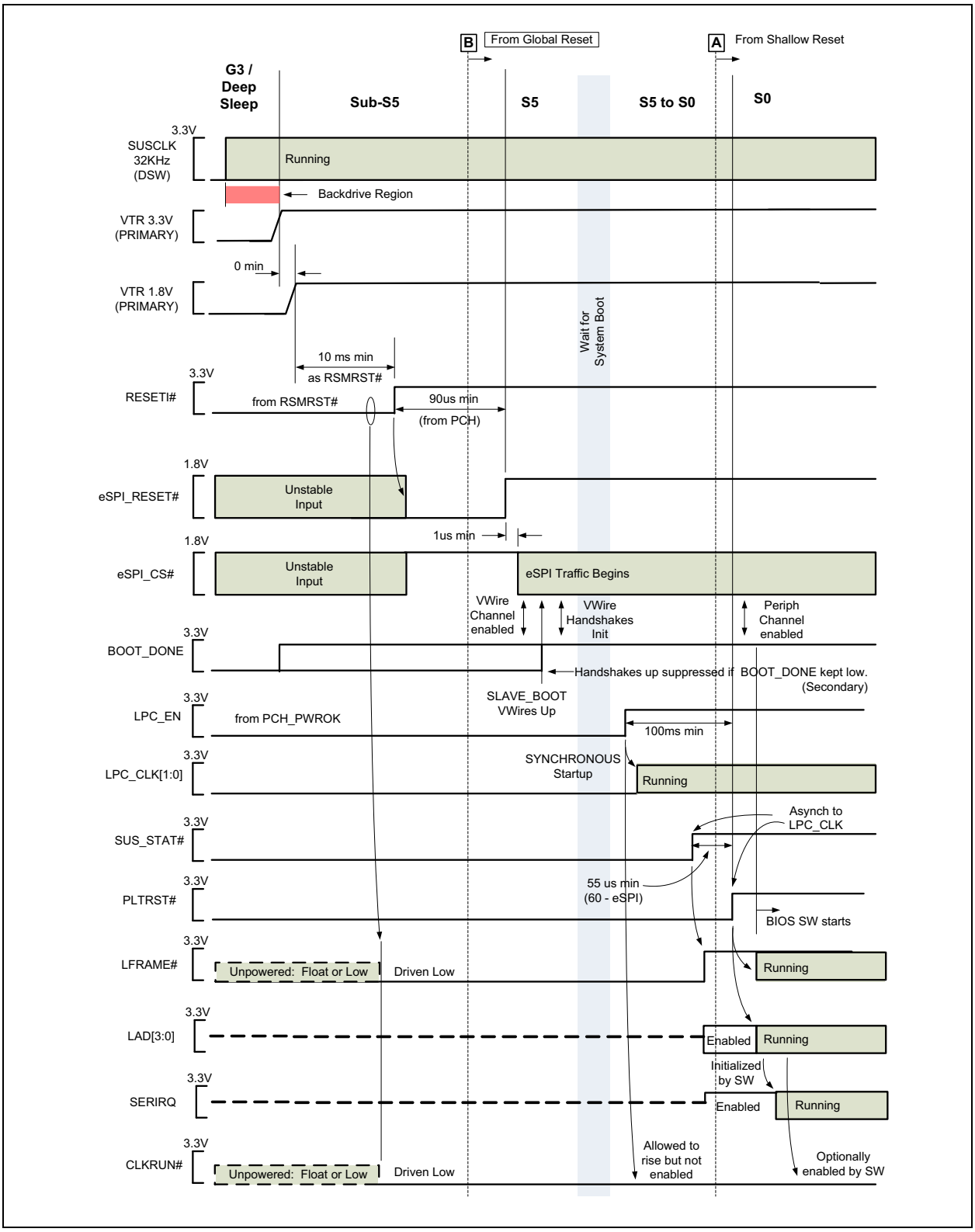
Parameters	Symbol	MIN	TYP	MAX	Units	Notes
ESPI_STRAP_[1:0] pins setup to RESETI# Rising Edge	$t_{STRAPSET}$	500			us	
ESPI_STRAP_[1:0] pins hold from RESETI# Rising Edge	$t_{STRAPHOLD}$	0			us	

9.7 System Power State Transition Diagrams

The following set of diagrams illustrates the behavior of the ECE1200 during transitions in the system-level power state.

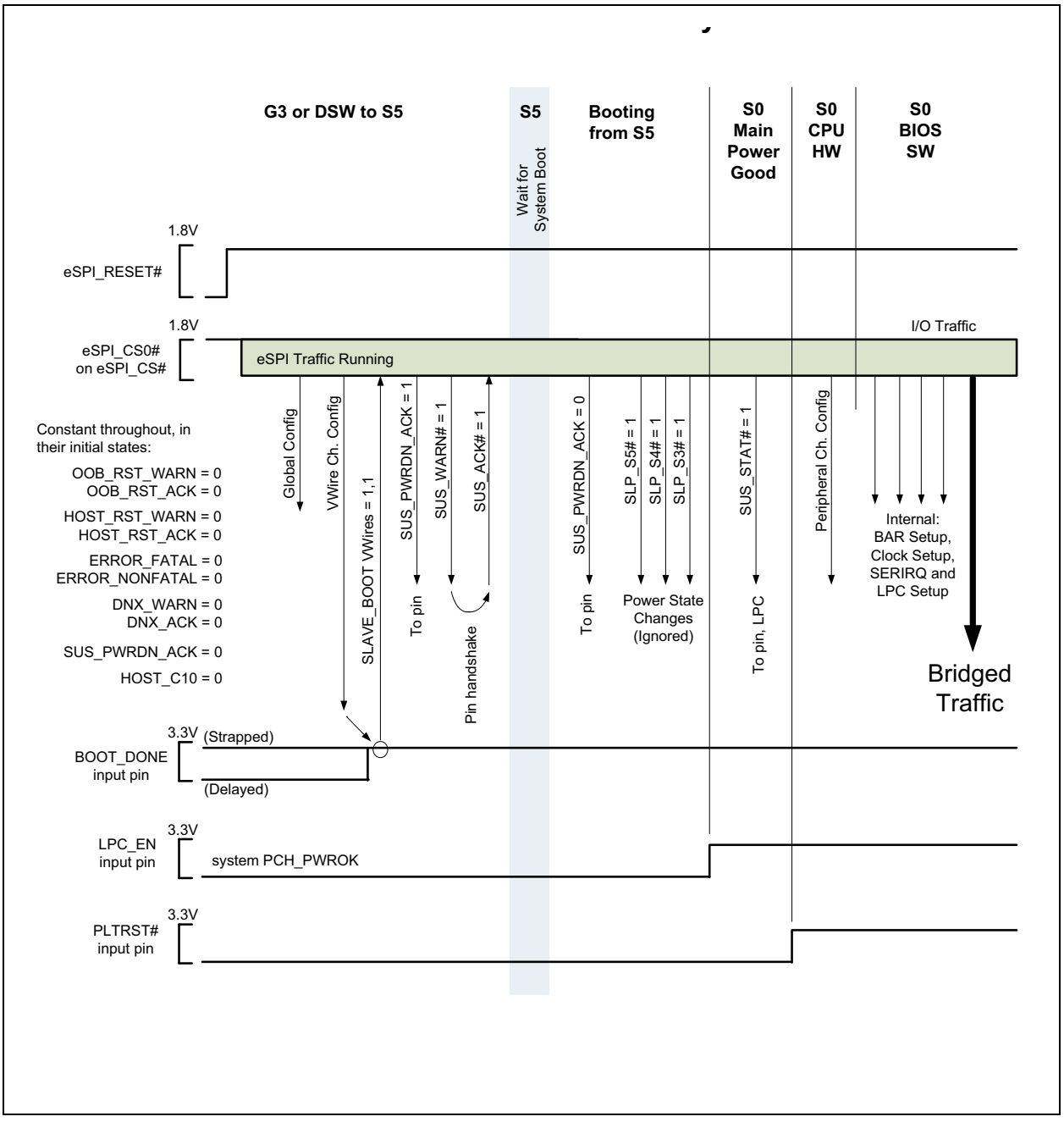
9.7.1 INITIAL BRING-UP FROM SYSTEM G3 TO S0

FIGURE 9-1: INITIAL BRING-UP FROM SYSTEM G3 TO S0



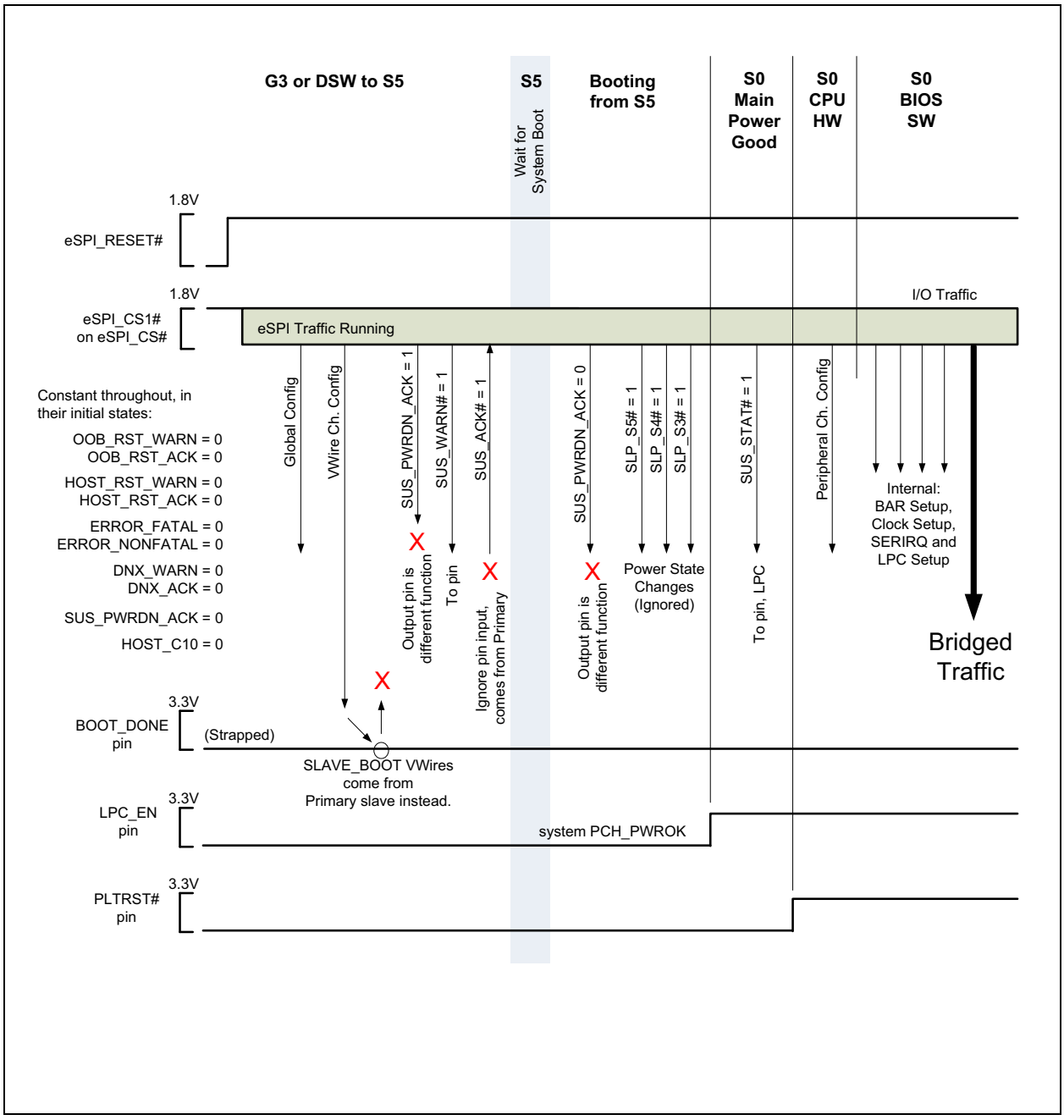
9.7.2 G3 TO S0 VIRTUAL WIRE DETAIL AS PRIMARY ESPI SLAVE

FIGURE 9-2: G3 TO S0 VWIRES, PRIMARY SLAVE



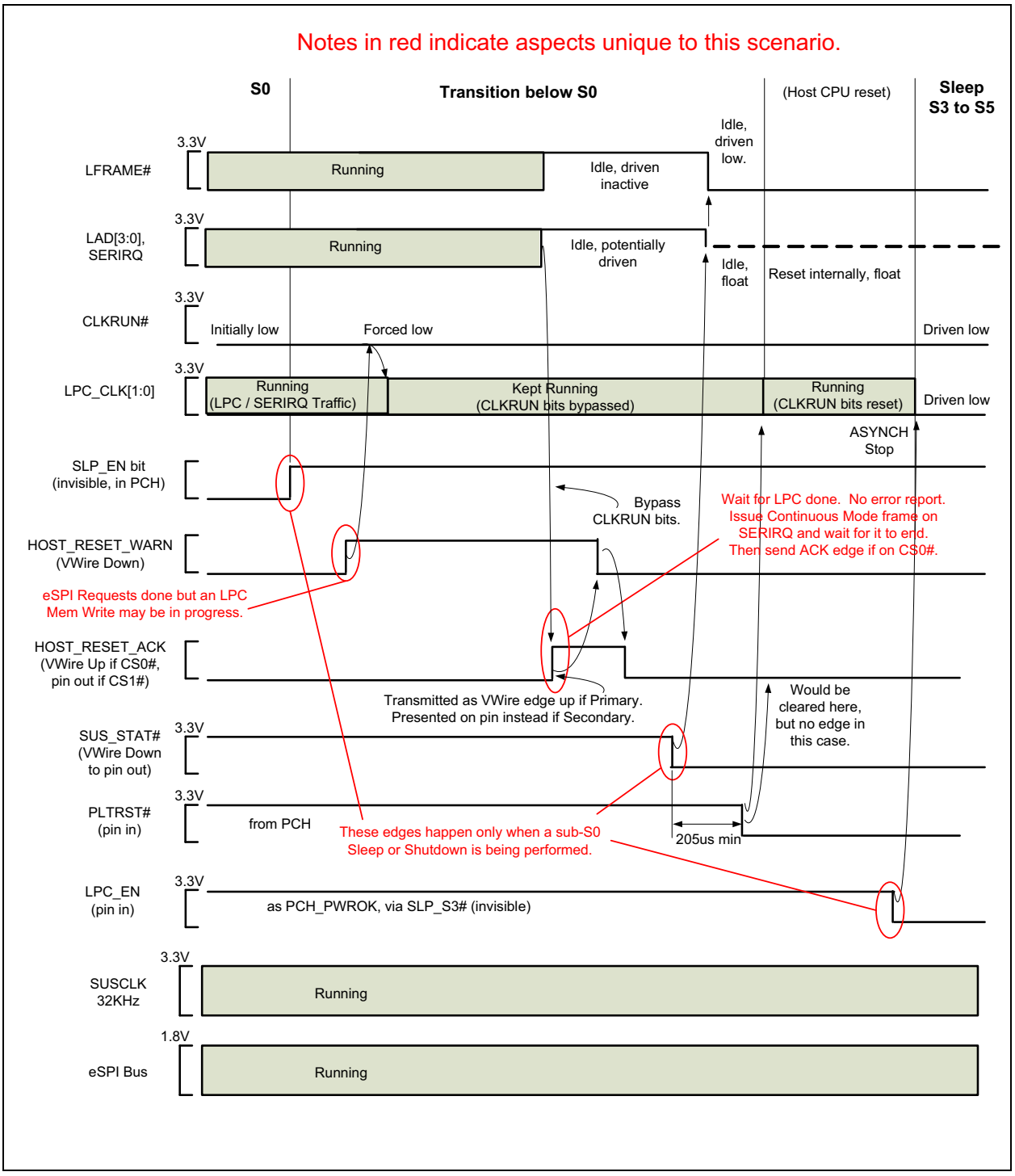
9.7.3 G3 TO S0 VIRTUAL WIRE DETAIL AS SECONDARY ESPI SLAVE

FIGURE 9-3: G3 TO S0 VWIRES, SECONDARY SLAVE



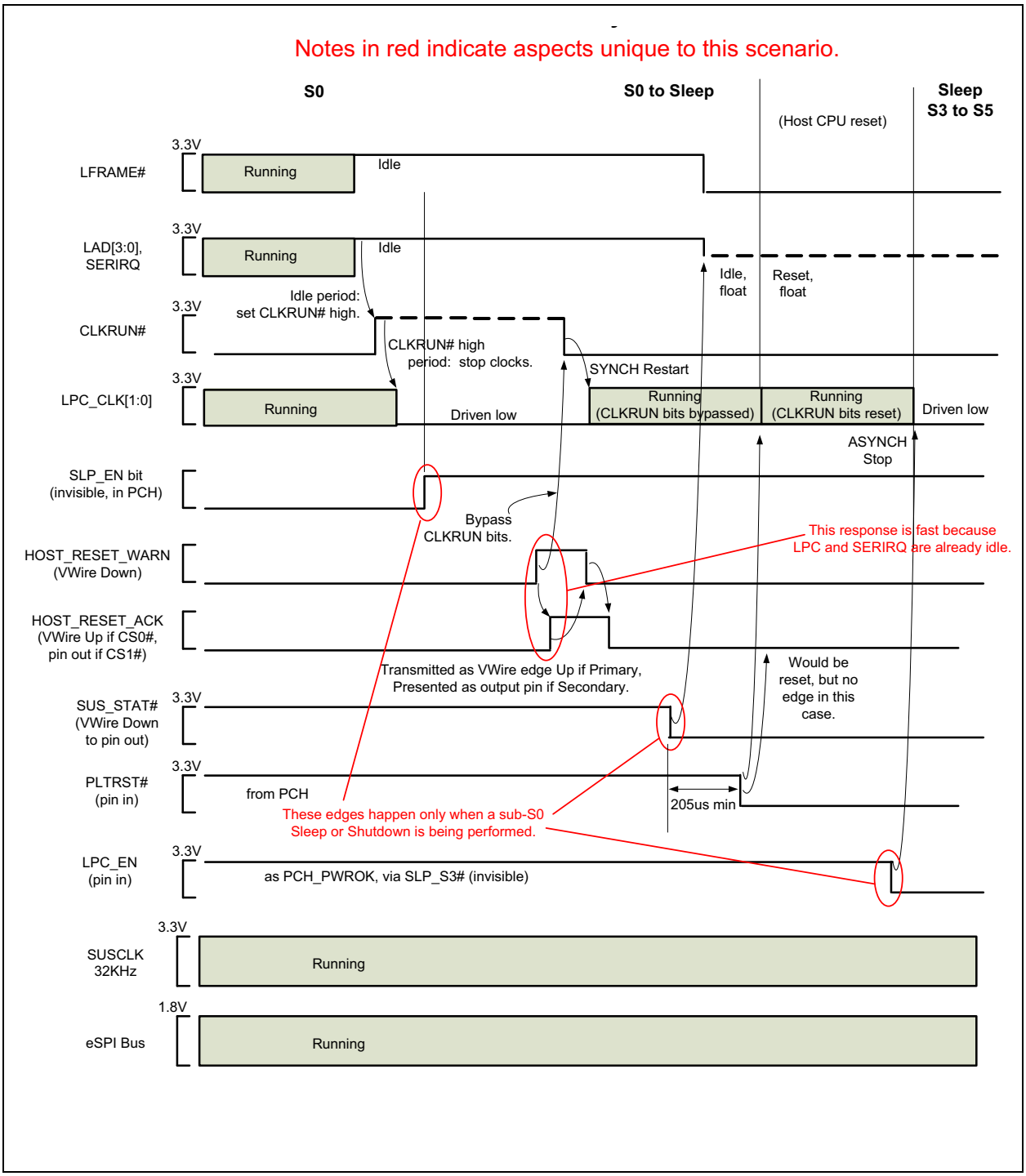
9.7.4 TEARDOWN FROM S0 TO S5, LPC CLOCKS RUNNING

FIGURE 9-4: TEARDOWN FROM S0 TO S5, LPC CLOCKS RUNNING



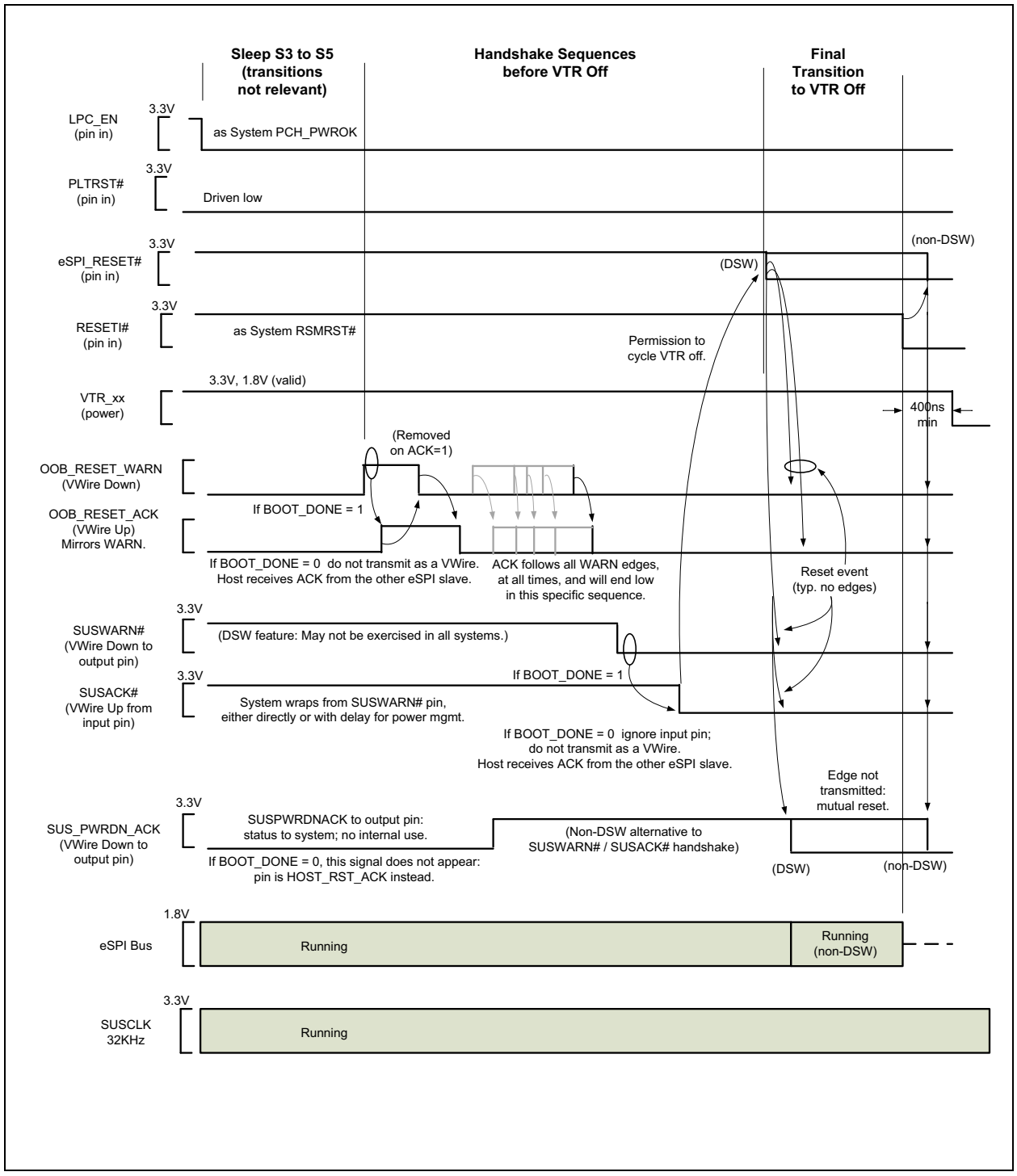
9.7.5 TEARDOWN FROM S0 TO S5, LPC CLOCKS OFF

FIGURE 9-5: TEARDOWN FROM S0 TO S5, LPC CLOCKS OFF



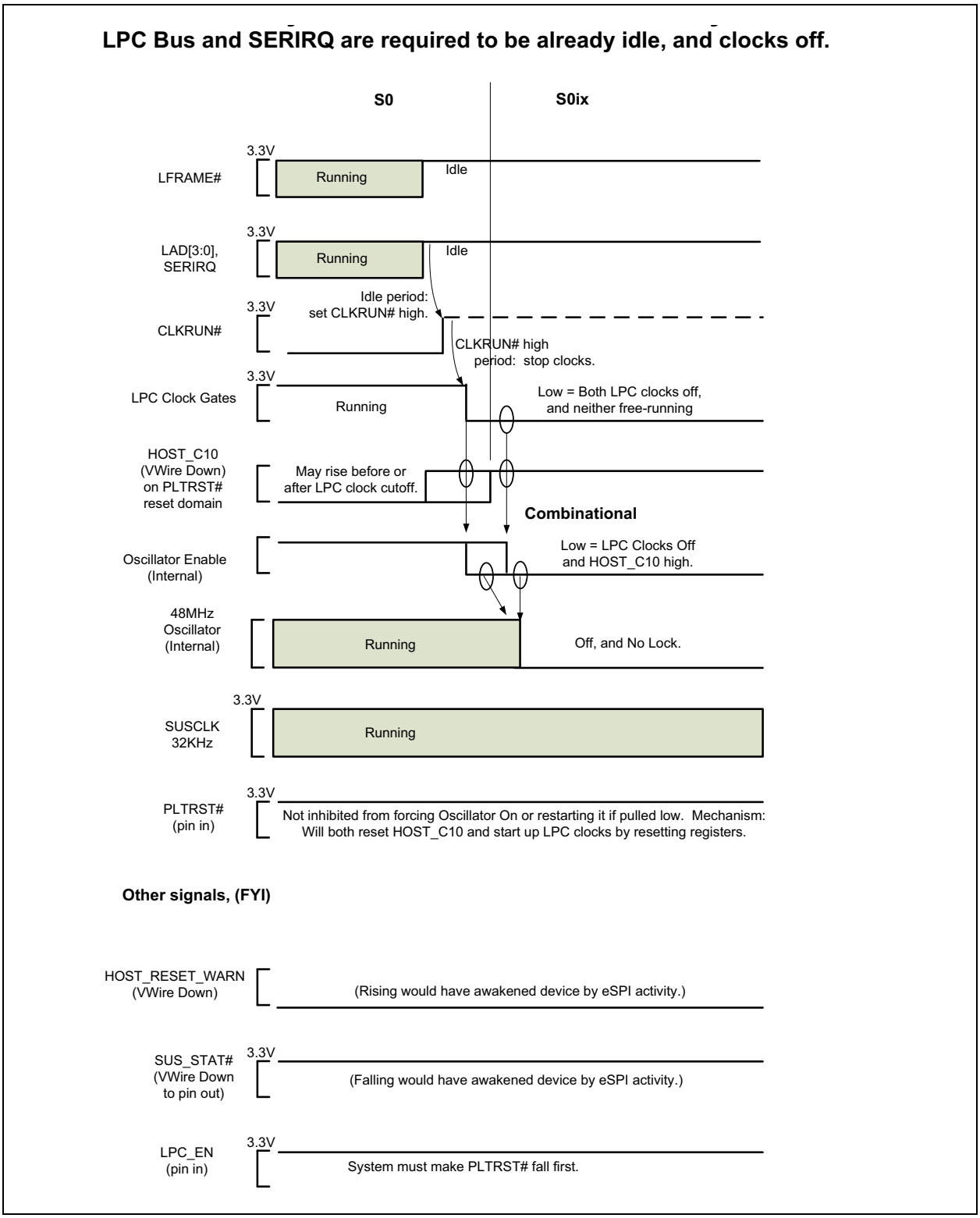
9.7.6 TEARDOWN FROM S5 TO VTR OFF

FIGURE 9-6: TEARDOWN FROM S5 TO VTR OFF



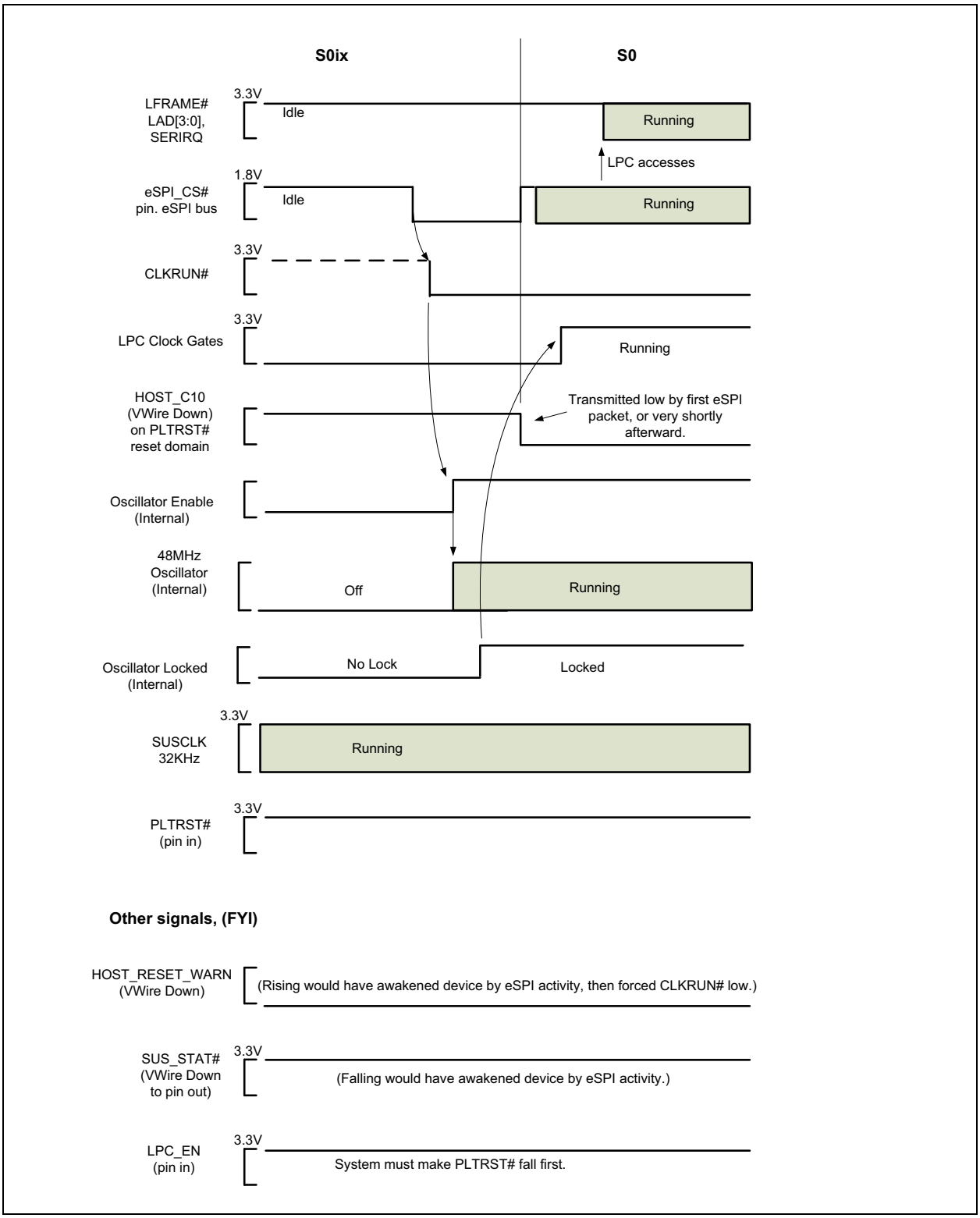
9.7.7 ENTRY INTO S0IX STATE (CONNECTED STANDBY, C10)

FIGURE 9-7: ENTRY INTO S0IX STATE (CONNECTED STANDBY, C10)



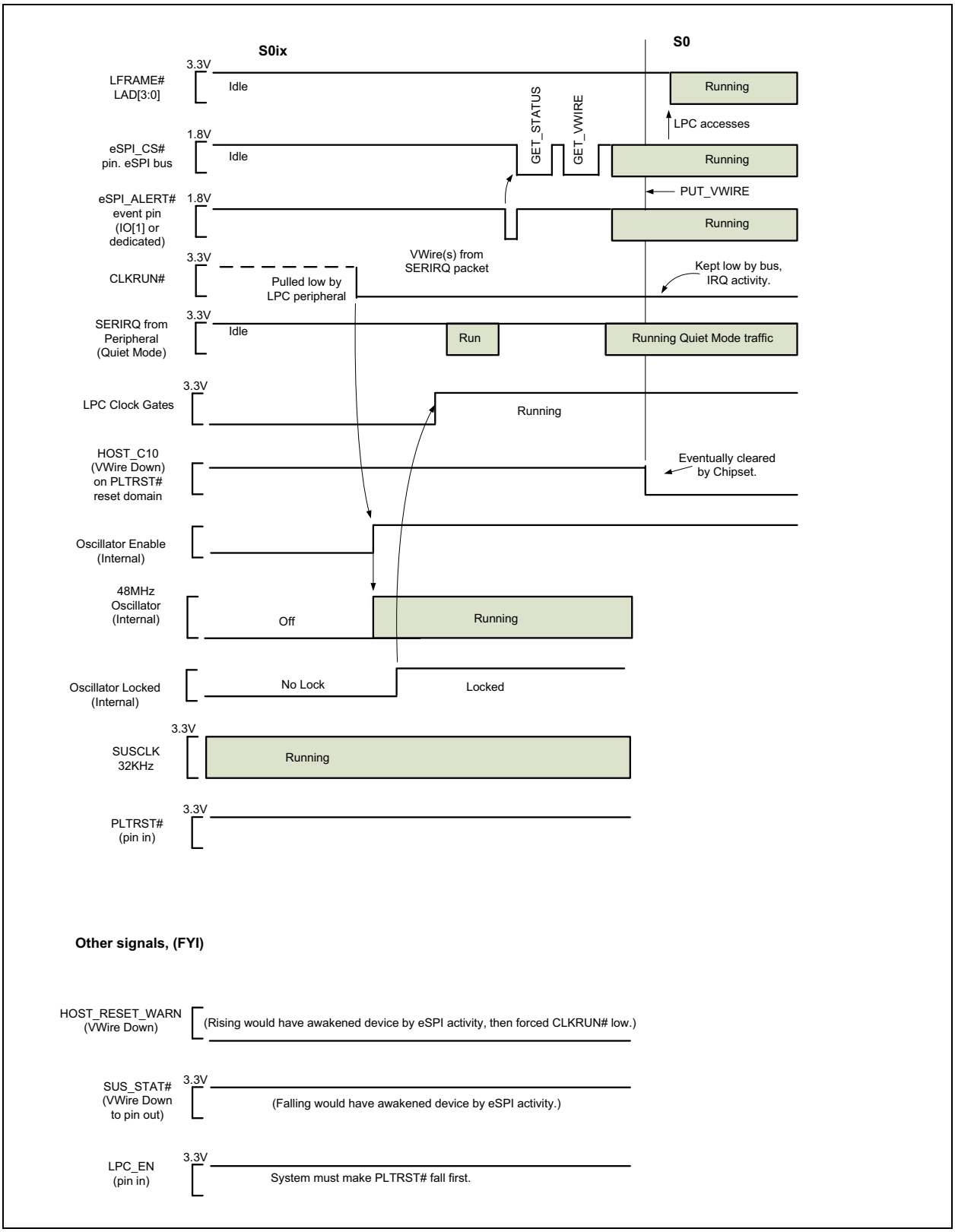
9.7.8 WAKE FROM S0IX STATE VIA ESPI TRAFFIC

FIGURE 9-8: WAKE FROM S0IX STATE VIA ESPI TRAFFIC



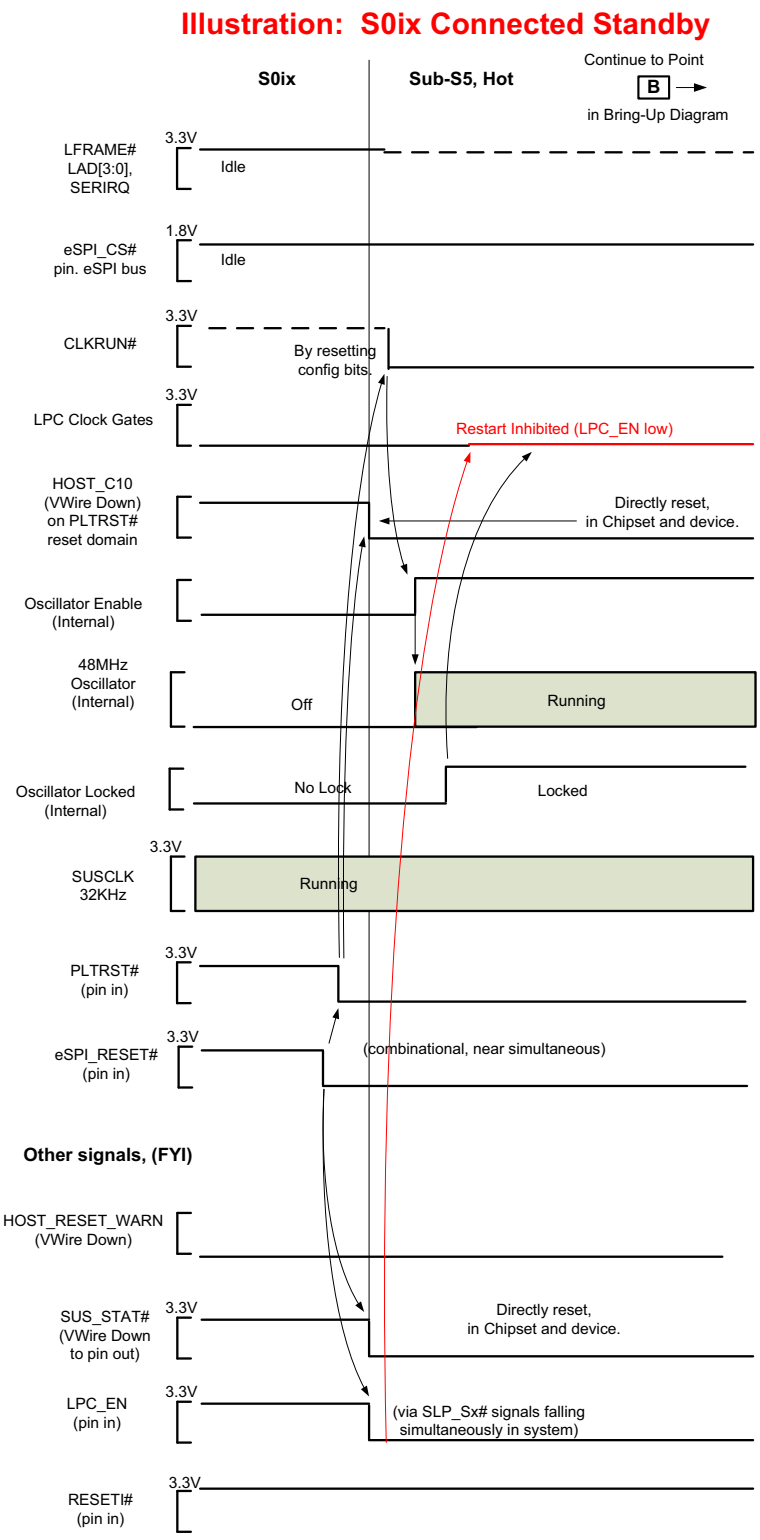
9.7.9 WAKE FROM S0IX STATE VIA CLKRUN# AND SERIRQ

FIGURE 9-9: WAKE FROM S0IX STATE VIA CLKRUN# AND SERIRQ



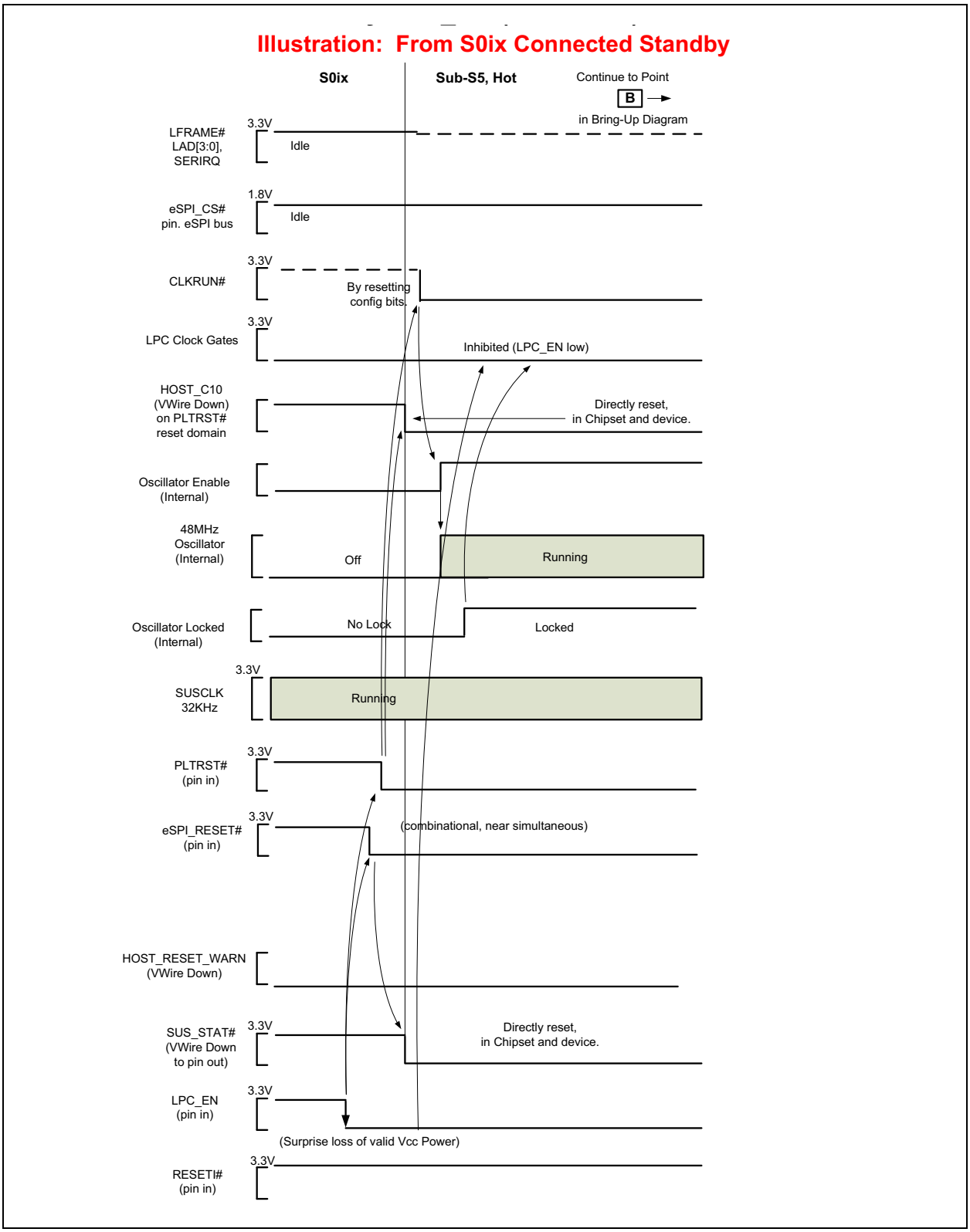
9.7.10 TEARDOWN DUE TO GLOBAL RESET (OTHER THAN BROWNOUT)

FIGURE 9-10: TEARDOWN DUE TO GLOBAL RESET (OTHER THAN BROWNOUT)



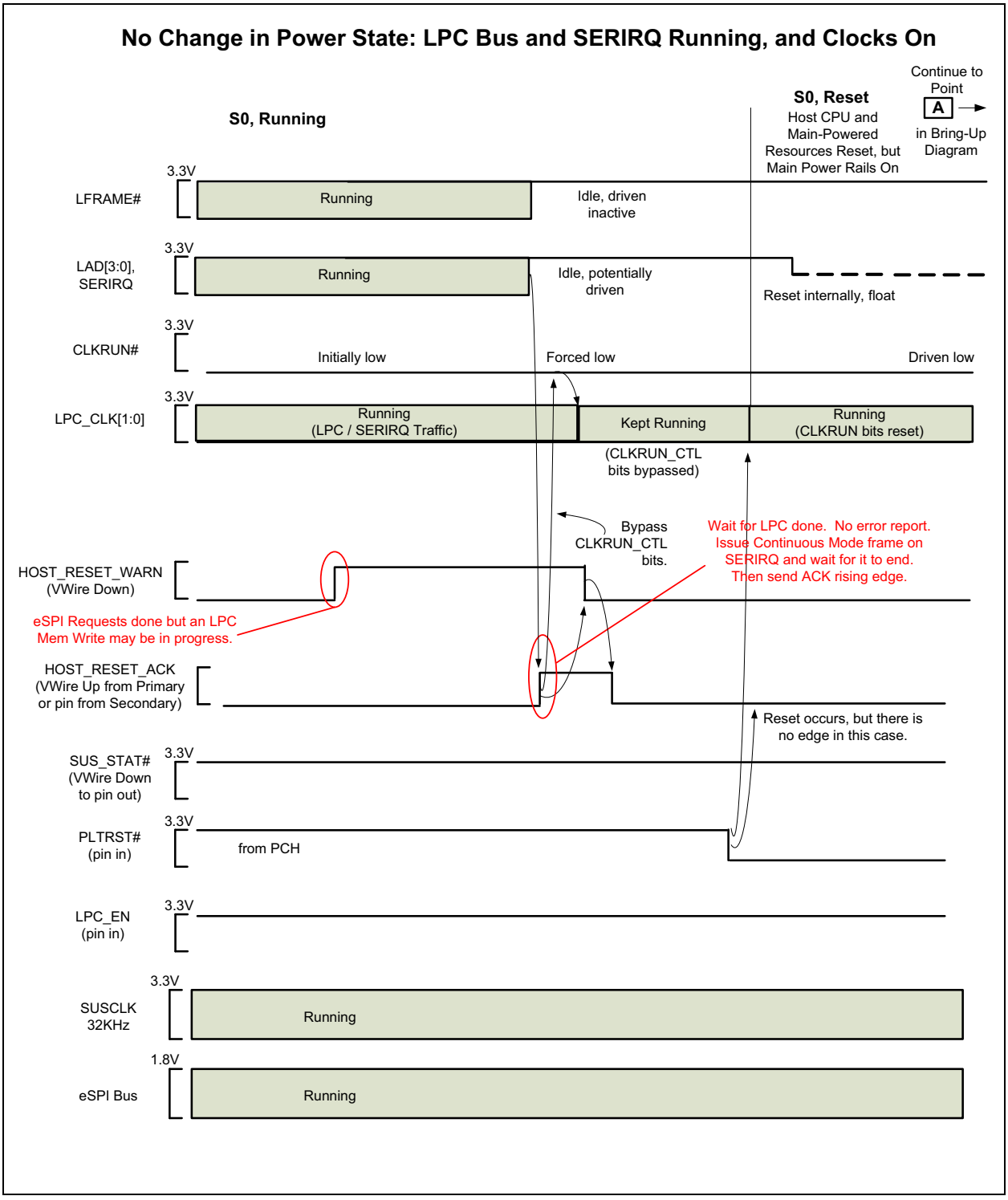
9.7.11 TEARDOWN DUE TO GLOBAL RESET (BROWNOUT / LPC_EN LOSS)

FIGURE 9-11: TEARDOWN DUE TO GLOBAL RESET (BROWNOUT / LPC_EN LOSS)



9.7.12 SHALLOW PLTRST# RESET (WITHOUT POWER CYCLE)

FIGURE 9-12: SHALLOW PLTRST# RESET (WITHOUT POWER CYCLE)



APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level/Date	Section/Figure/Entry	Correction
DS00003093B (07-10-19)	All	Defines Functional Rev. B silicon. Changes Default Base Address, eSPI_STRAP pins' function.
DS00003093A (05-21-19)	Data Sheet Release	

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PART NO.[1] - [X/]	XXX[2] - [XX] - [X][3]
Device	Temperature Range / Package / Version/ Revision / Tape and Reel Option

Note: [ ] indicate designators that have blank options

Devices:	ECE1200[1]	
Temperature Range Option:	I/	= -40°C to +85°C (Industrial)
Package:	LD	= 40 pin VQFN[2]
Version/Revision:	Blank	= Standard Version: no other versions at this time.
Packaging Option:	Blank	= Tray packaging[3]

Example:

a) ECE1200-I/LD = Industrial temperature, 40 VQFN, Standard version, Tray packaging

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html.

3: Packaging Option identifier, if present, only appears in the cat-

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