M21315

HD/SD-SDI Auto-rate Reclocker w/4:1 Selector

Rev V2

Applications

- Serial Routing Switchers
- Distribution Amplifiers
- SMPTE Coaxial Cable Interface
- Studio video applications
- Broadcast video applications
- Distribution video applications

Standards Compliance

- SMPTE 259M, 292M, 344M and DVB-ASI

Features

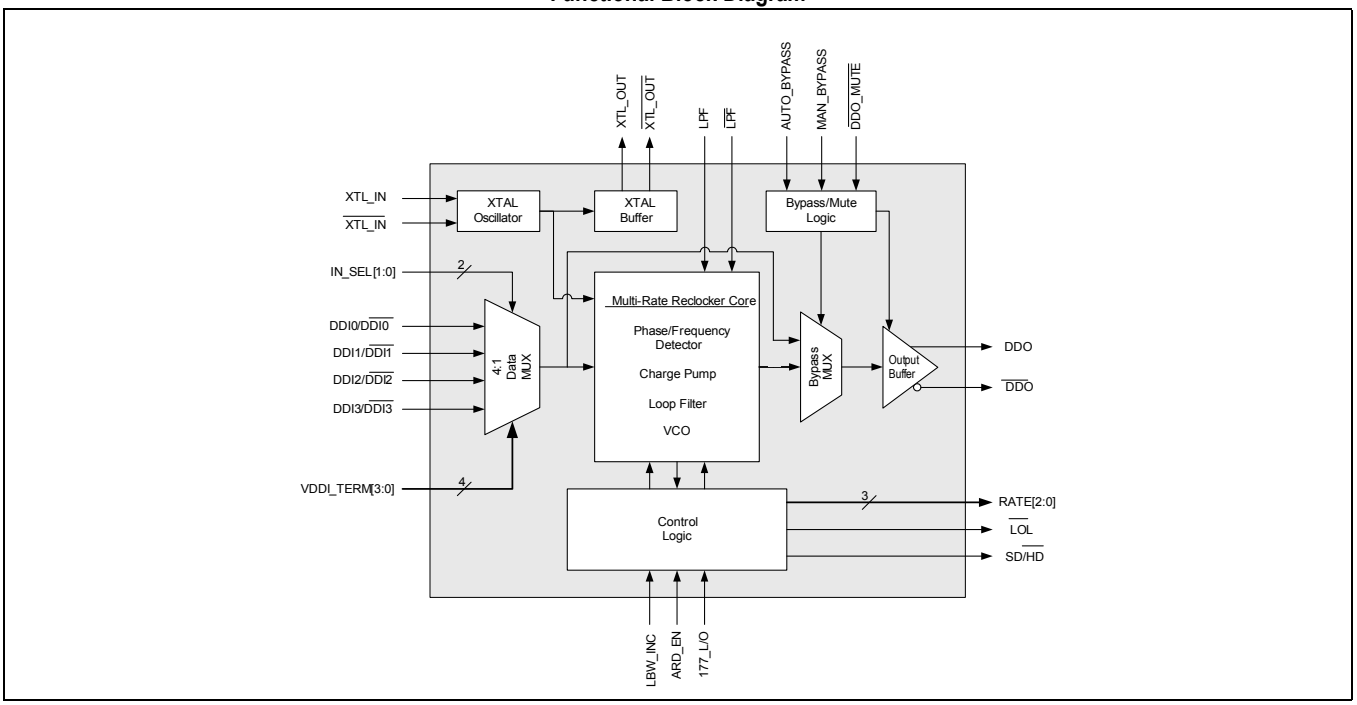
- SD/HD operation: 143, 177, 270, 360, 540, 1483.5, 1485 Mbps and DVB-ASI at 270 Mbps
- Auto and manual rate selection modes with rate indication in Auto
- 4:1 Input MUX and Loss of Lock (LOL) indicator
- Input buffers are compatible with PCML voltage levels
- Differential I/O with on chip termination resistors
- Selectable auto MUTE or BYPASS with manual BYPASS option
- Pin to pin compatible with GS1575 (without serial clock out and loss of signal indicator)
- Low typical power dissipation (430 mW @ 3.3V)
- 3.3V power supply operation
- Extended temperature operation: -10°C to +85°C

The M21315 is a high-speed, low-power reclocker designed to remove both random and inter-symbol interference (ISI) jitter from the input data for SMPTE and DVB-ASI serial digital video applications. MACOM's high-performance reclocker offers significant power reduction compared to legacy reclocking solutions.

The M21315 is based on a custom and proprietary reclocker core. The high-performance reclocker design results in high-jitter tolerance, especially in the presence of duty-cycle-distortion (DCD) that typically arises with AC coupling and video pathological test patterns. The M21315 also offers improved auto rate detect acquisition times over legacy reclocker solutions.

The M21315 supports SMPTE HD/SD-SDI data rates from 143 Mbps to 1485 Mbps. The M21315 is functionally and pin compatible with the GS1575B (without serial clock out and loss of signal indicators). The M21315 occupies the same footprint as the GS9075B (without serial clock out and loss of signal indicator). The M21315 also consumes less power than the GS1575B or GS9075B.

Functional Block Diagram



Ordering Information

Part Number	Package	Operating Data Rate	Operating Temperature
M21315G-XX*	64-pin, MLF, RoHS compliant	143 - 1485 Mbps	–10 °C to 85 °C
* The letter “G” designator after the part number indicates that the device is RoHS-compliant. Consult the MACOM price list for exact part numbers when ordering.			

Revision History

Revision	Level	Date	Description
V2	Release	May 2015	Updated logos and page layout. No content changes.
B (V1)	Release	March 2008	Revised packaging dimensions graphic Figure 1-2.
A	Preliminary	August 2007	Preliminary Release.

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1.0 Product Specification

1.1 General Specifications

Table 1-1. Absolute Maximum Ratings (1)

Symbol	Parameter	Minimum	Maximum	Units
V_{DD}	Device Power	V_{SS} - 0.5	V_{SS} + 3.6	V
V_{HS}	High-Speed Signal Pins	V_{SS} - 0.5	V_{SS} + 0.5	V
V_{ID}	Control/Interface Pins	V_{SS} - 0.5	V_{SS} + 0.5	V
T_{STORE}	Storage Temperature	–65	+150	°C
ESD_{HBML}	Human Body Model (low-speed pins)	2000	—	V
ESD_{HBMH}	Human Body Model (high-speed pins)	2000	—	V
ESD_{CDM}	Charged Device Model	500	—	V
I_{DC}	Maximum DC input current	—	25	mA

NOTE:

1. No Damage

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{DD}	Device Power	—	3.14	3.3	3.47	V
V_{SS}	V_{SS}: Chip Ground	—	—	0	—	V
T_{AMB}	Ambient Temperature	—	-10	—	+85	°C
θ_{JA}	Junction to ambient Thermal Resistance	—	—	28.6	—	°C/W

Table 1-3. DC Power Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
Total I_{DD}	Total I_{DD}(constant for all supply voltages)	1, 3	—	130	150	mA
Total $P_{DISS3.3V}$	Total P_{DISS} (@3.3V)	2	—	430	520	mW

NOTES:

1. Entire table specified at recommended operating conditions - see Table 1-2.
2. Typical computed with nominal power supply voltage, maximum computed with nominal +5% power supply voltage.
3. Current specified with 800 mV differential output swing.

1.2 Input/Output Level Specifications:

Table 1-4. CMOS I/O Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{OH}	Output Logic High	1	0.8 x V_{DD}	V_{DD}	—	V
V_{OL}	Output Logic Low	1	—	0.0	0.2 x V_{DD}	V
I_{OH}	Output Current (logic high)	—	-10	—	0	mA
I_{OL}	Output Current (logic low)	—	0	—	10	mA
V_{IH}	Input Logic High	—	0.75 x V_{DD}	—	V_{DD} + 0.3	V
V_{IL}	Input Logic Low	—	0	—	0.25 x V_{DD}	V
I_{IH}	Input Current (logic high)	—	-100	—	100	µA
I_{IL}	Input Current (logic low)	—	-100	—	100	µA

NOTE:

1. Entire table specified at recommended operating conditions - see Table 1-2. Specification is for a maximum load of 20 pF.

Table 1-5. High-Speed Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{IN}	Input Bit Rate (reclocker bypassed)	—	0	—	1500	Mbps
DR_{IN}	Input Bit Rate (reclocker enabled)	—	143	—	1485	Mbps
V_{ID}	Input Differential Voltage (peak - peak)	2,3	100	—	2000	mV
V_{ICM}	Input Common-Mode Voltage	—	V_{SS} + 1.15	—	AV_{DD}	V
V_{IMAX}	Maximum Input High Voltage	—	—	—	AV_{DD} + 400	mV
V_{IMIN}	Minimum Input Low Voltage	—	V_{SS}+1.0	—	—	V
$\Delta V_T T$	Maximum voltage difference between input common-mode voltage and **VDDI_TERM[3:0]**	—	—	—	600	mV
R_{IN}	**VDDI_TERM[3:0]** input termination impedance to AV_{DD}	—	40	50	60	Ω

NOTES:

1. Specified at recommended operation conditions-see Table 1-2
2. Example 1200 mV_{pp} differential = 600 mV_{pp} for each single-ended terminal
3. Minimum input level defined as error free operation at 10^{-12} BER with PRBS input pattern

Table 1-6. High-speed Output Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
t_r/t_f	Rise/Fall Time (20-80%) for all levels	—	—	120	150	ps
V_{OCM}	Output Common Mode Voltage	—	V_{DD} –525	—	V_{DD} –350	mV
V_{OD}	Differential Output Voltage Swing	3	1300	1600	2000	mV
R_O	**VDDO_TERM** Termination impedance to $\mathbf{V_{DD}}$	—	40	50	60	Ω

NOTES:

1. Specified at recommended operating conditions – see Table 1-2
2. Example 1200 mV_{P-P} differential = 600 mV_{P-P} for each single-ended terminal.
3. Measured with a 50Ω high speed oscilloscope.

1.3 Reclocker Performance Specifications

Table 1-7. Reclocker Output Jitter Performance

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
J_{ERMS}	Reclocker Enabled Output Data Jitter @ 1.485 Gbps (RMS)	1,2	—	5.5	9	ps
J_{EPP}	Reclocker Enabled Output Data Jitter @ 1.485 Gbps (pp)	1,2	—	38	55	ps
J_{EPP}	Reclocker Enabled Output Data Jitter @ 1.485 Gbps (pp)	1,2	—	56	80	mUI
J_{BRMS}	Reclocker Bypassed Output Data Jitter @ 1.485 Gbps (RMS)	1,2	—	—	6	ps
J_{BPP}	Reclocker Bypassed Output Data Jitter @ 1.485 Gbps (pp)	1,2	—	—	35	ps
J_{BPP}	Reclocker Bypassed Output Data Jitter @ 1.485 Gbps (pp)	1,2	—	—	52	mUI
J_{EPP}	Reclocker Enabled Output Data Jitter @ < 600 Mbps (pp)	1,2	—	—	40	mUI
J_{ERMS}	Reclocker Enabled Output Data Jitter @ < 600 Mbps (RMS)	1,2	—	—	6.7	mUI
J_{BPP}	Reclocker Bypassed Output Data Jitter @ < 600 Mbps (pp)	1,2	—	—	30	mUI
J_{BRMS}	Reclocker Bypassed Output Data Jitter @ < 600 Mbps (RMS)	1,2	—	—	5	mUI

NOTES:

1. All jitter is measured using a 2^{23}-1 PRBS pattern, and/or HD/SD-SDI color bar test pattern.
2. All jitter is measured using a wideband scope (minimum 10 GHz bandwidth).

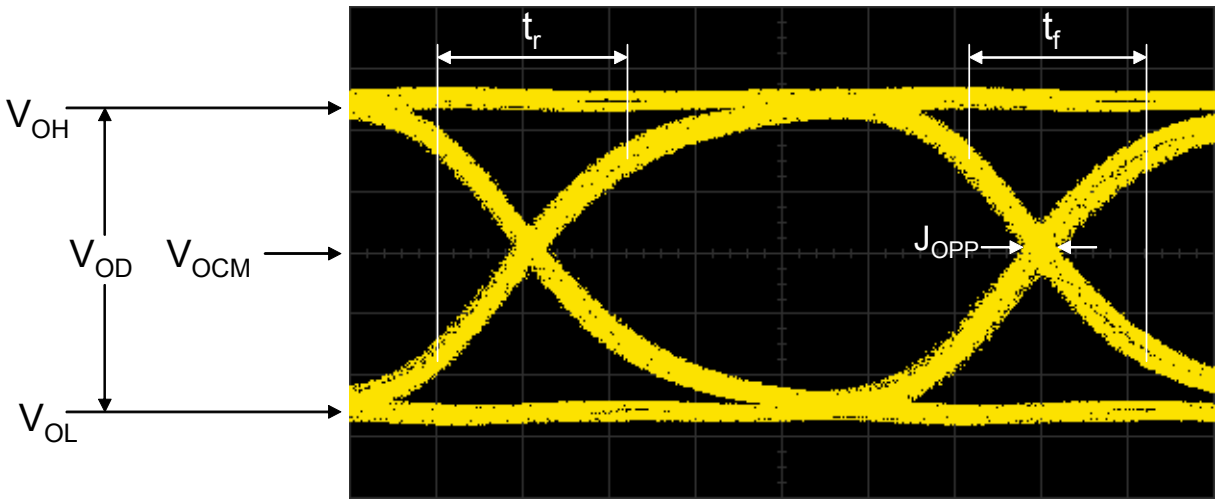
Table 1-8. Reclocker High-speed Performance

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
J_{TOL}	PLL pathological pattern jitter tolerance	2	0.4	—	—	UI
L_{BWPK}	Loop bandwidth peaking		—	0.1	—	dB
t_{LKA}	Asynchronous Lock (Auto Rate Detect lock time)	3	—	2	5	ms
t_{LKS}	Synchronous Switch Lock TIme @ 1.485 Gbps	4	—	110	150	ns
t_{LKS}	Synchronous Switch Lock TIme @ 270 Mbps	4	—	330	400	ns

NOTES:

1. Entire table specified at recommended operating conditions – see Table 1-2.
2. Jitter tolerance is measured with pathological test pattern.
3. Switching from one data rate to a different data rate.
4. Switching from one data rate to the same data rate.

Figure 1-1. Output Symbols Definition



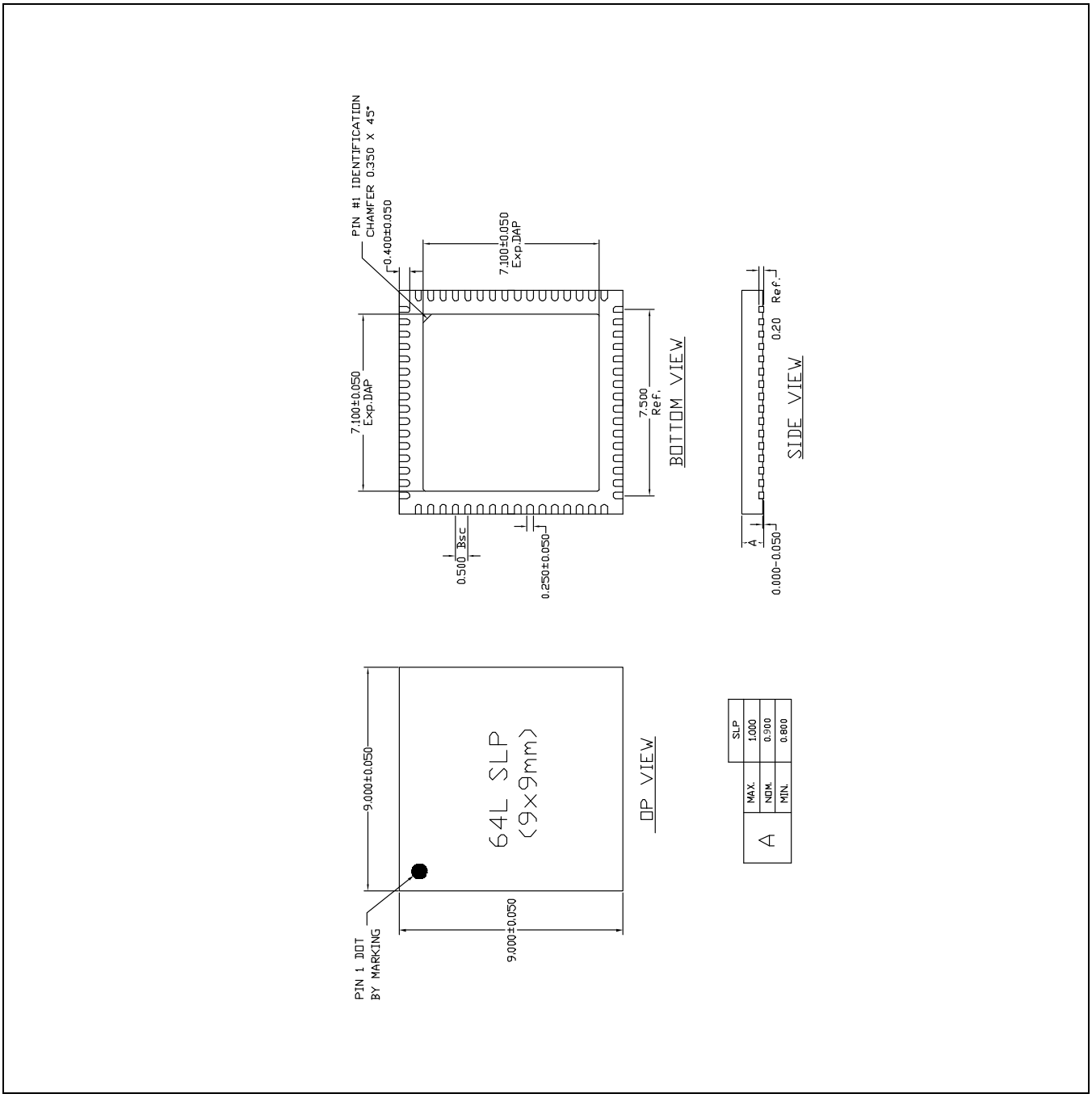
V_{OH}: Average voltage high level
V_{OL}: Average voltage low level
V_{OD}: (VOH) – (VOL)
V_{OCM}: Common Mode Voltage
J_{OPP}: Output Jitter Peak-Peak
t_r: 20-80% Rise Time
t_f: 80-20% Fall Time

NOTE: Waveform above is differential.

1.4 Package Specification

The M21315 is available in a 64-pin 9 mm x 9 mm MLF package. The package drawing is shown in Figure 1-2. The M21315 is available in a package that is fully RoHS compliant.

Figure 1-2. Package Drawing



1.5 Manufactureability

The values shown in this section may change; however, these are standard requirements.

1.5.1 Electrostatic Discharge

Tested per JESD22-A114. This device passes 2000V of ESD Human Body Model (HBM) testing.
Tested per JESD22-C101. This device passes 500V of ESD Charged Device Model (CDM) testing.
Tested per EIA/JESD78. This device passes 150mA of trigger current at 85°C during Latchup testing.

1.5.2 Peak Reflow Temperature

M21315G (RoHS compliant package): Peak reflow temperature is 260°C per JEDEC standards.

1.5.3 Moisture Sensitivity Level (MSL)

All versions of this device (Std Pb-type and RoHS compliant packages) are Moisture Sensitivity Level (MSL) 3 per J-STD-020B and J-STD-033.

1.6 Design Considerations

See Digital Video Interfacing Application Note (212xx-APP-001-A) for guidance on the following:

- Component Placement and Layout
- Routing Considerations

1.6.1 Thermal Considerations

The M21315 consumes less power than legacy devices, therefore they will contribute less thermal energy and should result in a lower operating temperature.

2.0 Functional Description

2.1 General Description

2.1.1 Reclocker General Overview

The M21315 reclocker is a dual-loop based design. The primary phase-locked loop (PLL) functions to 1) lock the VCO to the incoming data rate and 2) to retime the incoming data to remove jitter. In general, the VCO tuning range for a multi-rate design is much larger than the frequency pull-in range of the reclocker phase detector. As a result, a secondary frequency-locked loop (FLL) is added to tune the VCO to the approximate data frequency so the clock and data recovery unit (CDR) can lock onto valid data. The FLL uses an external crystal as an absolute frequency reference. As a result, the external reference is only used to assist the CDR frequency locking and the jitter performance of the reference has no effect on the recovered data output jitter.

2.1.2 Frequency Acquisition

When the reclocker is out of lock ($\overline{LOL}$ = Low), the FLL is enabled. The FLL compares the input data to the external reference and drives the VCO towards a target frequency that is very close to the incoming data rate frequency. The FLL is shut off when the VCO frequency and the frequency of the input data are within +/- 2000 ppm of each other. When FLL is shut off, $\overline{LOL}$ = High, to indicate a lock condition. If data is present, then the phase lock loop of the reclocker will lock to the incoming data. When in lock, the FLL control circuit continues to monitor the frequency difference between the VCO and the reference. If the difference exceeds +/- 3000 ppm, a loss of lock condition is indicated and frequency acquisition is initiated. If there is no input data present, an internal loss of signal detector will keep $\overline{LOL}$=Low until an input signal has been detected. The output signal from the reclocker is undefined when there is no valid signal at the input of the reclocker. When a valid input signal is detected, frequency acquisition is initiated and the reclocker will lock to the appropriate data rate.

2.2 Pin Descriptions

2.2.1 General Nomenclature

Throughout this data sheet, physical pins will be denoted in **bold** print. An array of pins can be called by each individual pin name (e.g. **MF0**, **MF1**, **MF2**, **MF3**, and **MF6**) or as an array (e.g. **MF[0..3,6]** or **MF[0:3,6]**).

2.2.2 Pin Descriptions

Table 2-1. Control/Interface/Low-Speed Pins (1 of 2)

Pin Name	Pin #	Function	Default	Type
XTL_IN/$\overline{\text{XTL\_IN}}$	52,53	Reference clock or crystal input. For GS1575B compatible operation, a 14.140 MHz series resonance crystal is required.	Internal pull up	I-Analog
XTL_OUT/$\overline{\text{XTL\_OUT}}$	50,51	Reference frequency output for chained reclocker applications	—	O-Analog
IN_SEL[1:0]	18,17	Input control signal that selects the active high-speed serial input 00b: Select **DDI0/$\overline{\text{DDI0}}$** 01b: Select **DDI1/$\overline{\text{DDI1}}$** 10b: Select **DDI2/$\overline{\text{DDI2}}$** 11b: Select **DDI3/$\overline{\text{DDI3}}$**	Internal pull down	I-CMOS
ARD_EN	21	Input control signal that enables Auto Rate Detect (ARD) functionality or manual rate setting mode. ARD_EN = High: Auto Rate Detector (ARD) enabled, ARD_EN = Low: Manual rate selection mode	Internal pull up	I-CMOS
RATE[2:0]	26,25,24	Bidirectional control signals used to indicate the data rate in ARD enabled mode or to force a data rate setting in Manual mode ARD_EN = High: RATE[2:0] pins indicate the date rate the M21315 is locked to according to pin decoding shown below ARD_EN = Low: RATE[2:0] pins are used to force a particular data rate according to the pin decoding shown below. RATE[2:0] = 000: 143 Mbps data rate RATE[2:0] = 001: 177 Mbps data rate RATE[2:0] = 010: 270 Mbps data rate RATE[2:0] = 011: 360 Mbps data rate RATE[2:0] = 100: 540 Mbps data rate RATE[2:0] = 101: 1483.5/1485 Mbps data rate	Internal pull down	I/O- CMOS
177_L/O	27	Input control signal used to lock out the 177Mbps data rate from the ARD search order sequences. This signal is mainly for drop-in compatibility with the GS1535 as the M21315 locks correctly with DVB-ASI data. 177_L/O = High: 177 Mbps data rate locked out from ARD search order 177_L/O = Low: 177 Mbps data rate included in ARD search order	Internal pull up	I-CMOS

Table 2-1. Control/Interface/Low-Speed Pins (2 of 2)

Pin Name	Pin #	Function	Default	Type
$\overline{\text{LOL}}$	28	Output Status indication signal for reclocker Loss of Lock. See the Frequency Acquisition section for more detailed information. $\overline{\text{LOL}}$ = High: Reclocker PLL is locked $\overline{\text{LOL}}$ = Low: Reclocker PLL is not locked	—	O-CMOS
SD/$\overline{\text{HD}}$	33	Output status indication signal to control slew rate of downstream cable driver. SD/$\overline{\text{HD}}$ = High: Reclocker locked to a SD data rate (143-540 Mbps) SD/$\overline{\text{HD}}$ = Low: Reclocker locked to a HD rate (1.4835/1.485 Gbps)	—	O-CMOS
AUTO_BYPASS	20	Input control signal that automatically bypasses the data directly from the input to the output if the Reclocker PLL can NOT lock to the incoming data stream. AUTO_BYPASS = High: Auto bypass reclocker if lock is not achieved AUTO_BYPASS = Low: Reclocker continues to attempt data lock but output data BER may be high.	Internal pull up	I-CMOS
MAN_BYPASS	19	Input control signal used to force a reclocker PLL bypass regardless of the setting of the AUTO_BYPASS signal. MAN_BYPASS = High: Force bypass (regardless of Autobypass state) MAN_BYPASS = Low: Enables normal AUTO_BYPASS operation	Internal pull down	I- CMOS
$\overline{\text{DDO\_MUTE}}$	36	Input control signal that forces the DDO/$\overline{\text{DDO}}$ outputs to logic low states. $\overline{\text{DDO-MUTE}}$ = High: Normal output operation $\overline{\text{DDO-MUTE}}$ = Low: Forces output to a logic low state	Internal pull up	I-CMOS
LPF/$\overline{\text{LPF}}$	62,63	Loop Filter inputs on GS1535 that are left FLOATING on M21315. Loop filter is internal. Leave pins floating.	—	Analog
LBW_INC	34	Input control signal used to increase the loop bandwidth (LBB) of the M21315. LBW_INC pin 34 can be used alone to increase the LBW of the M21315 as a GS1575B compatible function. LBW_INC = 0: 3.5 MHz HD LBW, 1.0 MHz SD LBW LBW_INC = 1: (default) 1.5 MHz HD LBW, 0.52 MHz SD LBW	Internal pull up	I-CMOS
NC	29,35,38,39, 40,45,54,55, 56,57,58,59	No internal connection.	—	—

NOTES:

1. Internal pull-up/pull-down is 100 KΩ.
2. NAME/RSVD Indicates additional features of the M21315 that are mapped to the reserved pins of the GS1535. When left floating as recommended by the GS1535 data sheet, the M21315 defaults to a pin for pin and functionally compatible mode.

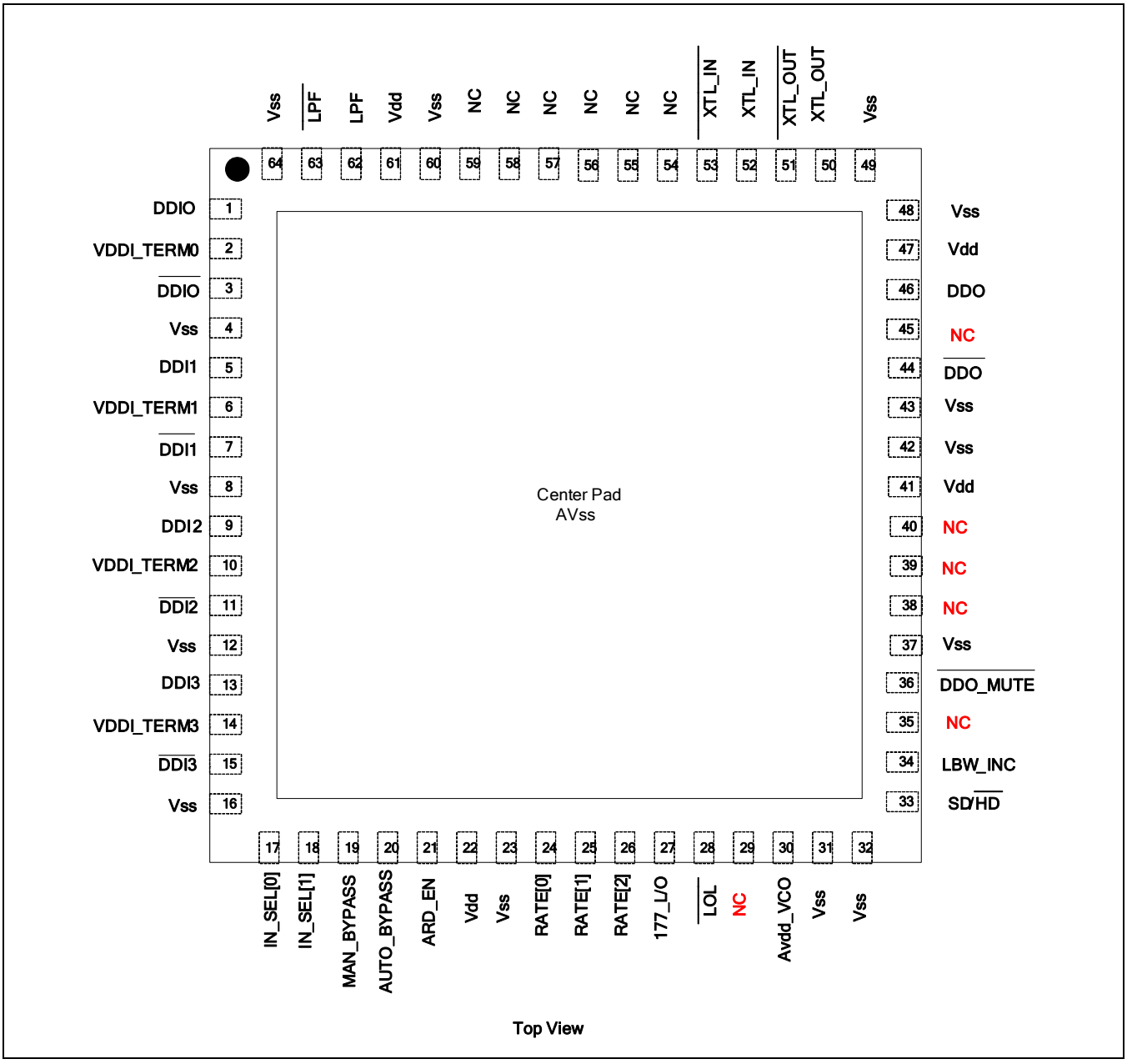
Table 2-2. Power Pins

Pin Name	Pin #	Function	Type
V_{SS}	4,8,12,16,23,31, 32,37,42,43,48, 49,60,64	Power Supply Ground	Power
V_{DD}	22,41,47,61	Positive Power Supply	Power
AV_{DD_VCO}	30	VCO Power Supply This pin should be connected to a “quiet” power supply.	Power
Center Pad	—	Ground	Power

Table 2-3. High-speed Signal Pins

Pin Name	Pin #	Function	Default	Type
DDI/$\overline{\text{DDI}}$[3:0]	1,3,5,7,9, 11,13,15	Non-inverting and inverting high speed serial data inputs. Inputs are compatible with PCML, LVDS, or LVPECL voltage levels.	100Ω differential	I-High-speed
VDDI_TERM[3:0]	2,6,10,14	Input termination pin (center tap for 100Ω) Case 1: Tie to a positive supply for 50Ω to supply terminal Case 2: Leave floating and decouple to ground for 100Ω differential		I-Low-speed
DDO/$\overline{\text{DDO}}$	44,46	Non-inverting and inverting high speed serial data outputs.	100Ω differential	O-High-speed

Figure 2-1. M21315 Pin Out



2.2.1.1 Reset

The M21315 reclocker automatically resets after power up thus an external reset is not required. The M21315 is fully operational 10 ms after the power supply has stabilized to within 10% of the final value.

2.2.2.2 Input Selection Multiplexer

The M21315 contains a 4:1 input selection multiplexer. The **IN_SEL[1:0]** pins select one of the four possible inputs that will be retimed by the reclocker block and passed to the output. The mapping of the multiplexer pins is shown in Table 2-1. If the **IN_SEL[1:0]** pins are left floating, the 4:1 input multiplexer defaults to input **DDI0**/**DDI0.**

2.2.2.3 High-Speed I/O Pins

The high-speed inputs are designed to be used in both AC coupled and DC coupled (PCML) modes. The high-speed differential inputs contain on-chip 50Ω termination from **DDI[n]** to **VDDI_TERM[n]** as well as from **DDI[n]** to **VDDI_TERM[n]**. With **VDDI_TERM[n]** tied to $\mathbf{V_{DD}}$, the single-ended input impedance is 50Ω. This mode is recommended for AC coupled inputs or with DC coupled PCML when the PCML is driven from the same supply voltage. For use in other DC coupled situations, it is recommended that the termination voltage for the M21315 be floated. For backwards compatibility with the GS1575B, **VDDI_TERM[n]** contains a weak internal bias near $\mathbf{V_{DD}}$ and the pin can be left floating for direct connection to the M21324 or the GS1524. In all cases, **VDDI_TERM[n]** should be decoupled to $\mathbf{V_{SS}}$ to reduce input noise with a 10nF capacitor. The GS1575B compatible input and an alternative is shown in Figure 2-2 and Figure 2-3.

Figure 2-2. Input Circuit for GS1575B Drop-in

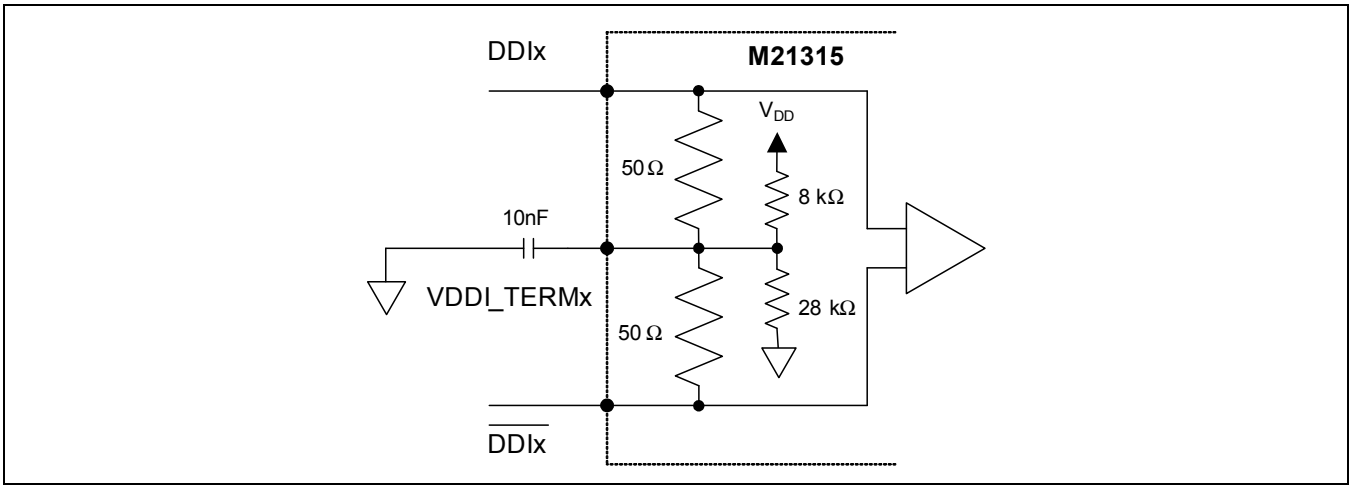
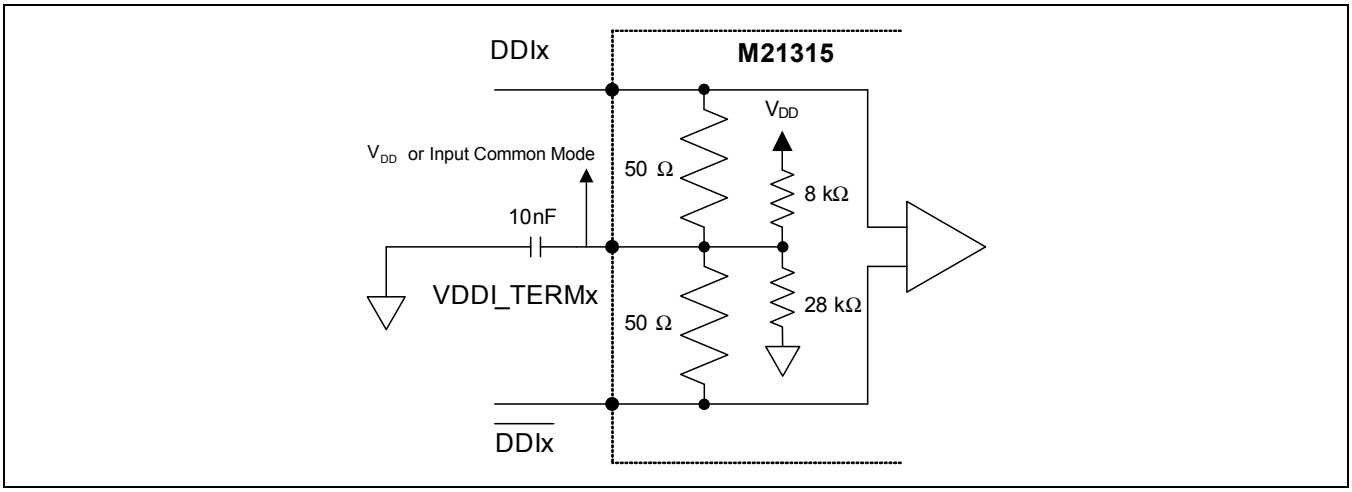


Figure 2-3. Input circuit for DC/AC coupled General Case



The high-speed output contains integrated 50Ω resistors from both **DDO** and **$\overline{\text{DDO}}$** to **VDDO_TERM**. **VDDO_TERM** should be bypassed to **V_{SS}** with a 10nF capacitor. **VDDO_TERM** is internally biased to **V_{DD}**.

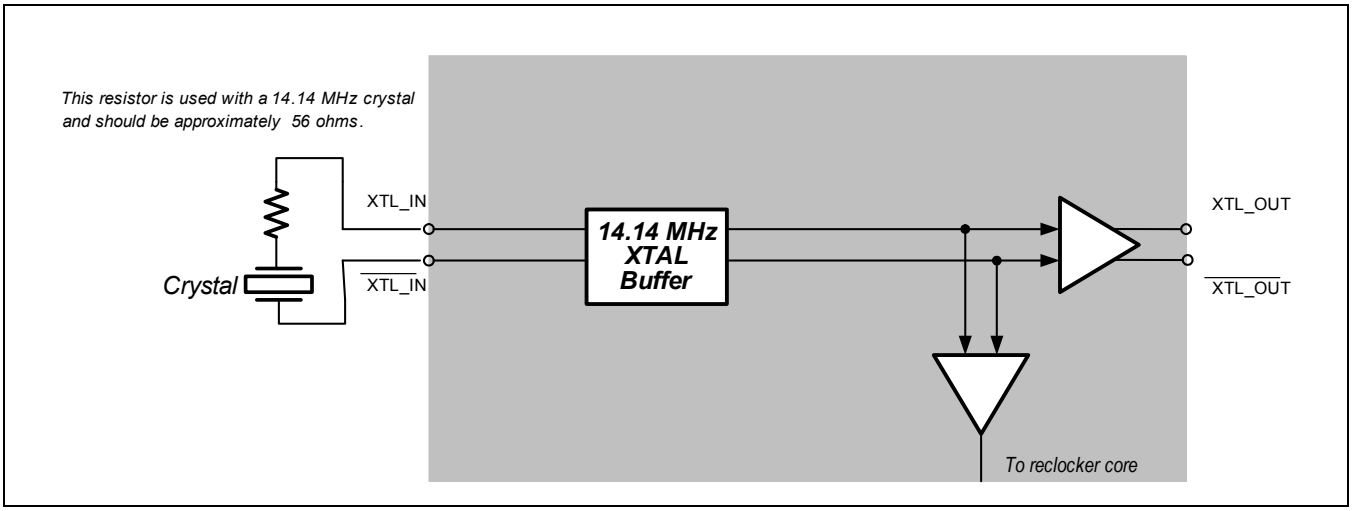
The output swing and common mode of the M21315 is the same as those of the GS1575B.

2.2.2.4 Reclocker Reference Frequency

The reclocker frequency acquisition requires an external crystal connected to **XTL_IN/$\overline{\text{XTL\_IN}}$**. For daisy-chained reclocker applications, a buffered reference output is made available on **XTL_OUT/$\overline{\text{XTL\_OUT}}$**.

The input reference frequency is 14.140 MHz. A 14.140 MHz series resonant crystal with the same form factor as the GO1535 crystal should be used. The crystal should be connected as shown in Figure 2-4 below. A 56Ω resistor is recommended.

Figure 2-4. Crystal Interface



The series resonant crystal should operate at 14.14MHz with a frequency stability of +/- 50 ppm or better, equivalent series resistance of 80Ω or less, drive level of < 0.2 mW, and static capacitance of less than 5.0 pF.

The M21315 can also operate with a reference from an external clock buffer or oscillator instead of a crystal. The M21315 can accept a single ended or differential 14.14 MHz reference clock. When driving the M21315 with a single ended reference clock, the clock signal should be connected to the **XTL_IN** pin and the **$\overline{\text{XTL\_IN}}$** pin should be left floating. If the **XTL_IN** pins on the M21315 are connected to a clock driver or oscillator, the requirements for the signal connected to the M21315 are detailed in Table 2-4.

Table 2-4. Reference Clock/Oscillator Input Specifications

Mode	14.14 MHz Reference Frequency	
	Min	Max
Input Common Mode	V_{DD}-2.0	V_{DD}-1.2
Differential input swing (p-p)	500mV	
Single ended input swing (p-p)	250mV	
Drive Impedance		60Ω

NOTES:

1. When driving a reference clock single ended, connected the clock signl to the **XTL_IN** pin and leave the **$\overline{\text{XTL\_IN}}$** pin floating.
2. TTL Input levels are supported for 14.14 MHz reference frequency.
3. With a 14.14 MHz reference, the reference signal can be cascaded from one M21315 to another.

2.2.2.5 Reclocker Loop Bandwidth

Unlike the GS1575B, the loop filter for the M21315 reclocker is fully integrated into the part. As a result, **LPF/$\overline{\text{LPF}}$** pins are used for MACOM testing and should be left floating. This can be accomplished by not populating the loop filter capacitor used with the GS1575B. As in the GS1575B, when **LBW_INC** =Floating, a lower bandwidth of 1.5 MHz for 1485 Mbps data rates and 0.52 MHz for 270 Mbps data rates is selected.

For other SD-SDI rates, the bandwidth scales proportionately to the bit rate, using the 270 Mbps as a reference point. For example, at 540 Mbps, the bandwidth is 2x the 270 Mbps bandwidth. When **LBW_INC** = Low, the bandwidth increases to 3.5 MHz for 1485 Mbps data rates and 1 MHz for 270 Mbps data rates.

Table 2-5. Loop Bandwidth Control Settings

	HD LOOP BANDWIDTH SETTING (1485 Mbps)	SD LOOP BANDWIDTH SETTING (270 Mbps)
0	3.5 MHz	1.0 MHz
1	1.5 MHz (default)	0.52 MHz (default)

NOTE:

Typical values. Loop bandwidth scales to lower frequency with reduced data rates.

2.2.2.6 Loss of Lock Alarm

A loss of lock alarm pin, **LOL**, is provided to indicate if the reclocker is in lock. When the reclocker has achieved lock, **LOL** = High. If the reclocker is out of lock, **LOL** = Low. For synchronous switching at the same data rate, the lock time is lower if a higher loop bandwidth is selected.

2.2.2.7 Auto Rate Detect (ARD)

The reclocker is designed to operate in two modes. In the first mode, with **ARD_EN** = High, the Auto Rate Detect is enabled which automatically locks the CDR to the rates typically used in SD-SDI, HD-SDI, and DVB-ASI applications. The locked data rate is then reported with the **RATE[2:0]** pins as shown in Table 2-6.

The M21315 does not have any of the false lock issues exhibited by the GS1535 or the GS1575B with DVB/ASI 8b/10b encoded data or idle patterns; however, for backwards compatibility, it is possible to lock out the 177 Mbps data rate by setting **177_L/O** = High which removes 177Mbps from the ARD search sequence.

Note that this pin is only active if **ARD_EN** = High. With the ARD disabled (**ARD_EN** = Low), the reclocker locking frequency is forced by using the **RATE[2:0]** pins as inputs and selecting the data rate as shown in Table 2-7.

Table 2-6. Rate Report Mapping when ARD is Enabled

RATE[2:0]	Bit Rate
000b	143 Mbps
001b	177 Mbps
010b	270 Mbps
011b	360 Mbps
100b	540 Mbps
101b	1485/1483.5 Mbps

Table 2-7. Rate Select with ARD Disabled

RATE[2:0]	Bit Rate
000b	143 Mbps
001b	177 Mbps
010b	270 Mbps
011b	360 Mbps
100b	540 Mbps
101b	1485/1483.5 Mbps

For system reporting purposes as well as to set the output slew rate on the cable drivers, the **SD/HD** output is used to indicate if the reclocker has locked to a HD rate. For SD-SDI rates, **SD/HD** = High and for the HD-SDI rate **SD/HD** =Low. This pin is used to set the output slew rate of the downstream cable driver.

177_L/O = High would remove the 177 Mbps rate from the search sequence resulting in a slightly faster asynchronous lock time but as there are not any false locking issues with DVB-ASI with the M21315 this is not required.

Also, if the M21315 is out-of-lock, the search pattern will not start unless the M21315 detects that there are transitions in the data through an internal loss of signal detector.

2.2.2.7.1 Bypass and $\overline{\text{DDO\_MUTE}}$

The reclocker can be forced into the bypass mode (input data to output without retiming) with **MAN_BYPASS** = High. With **MAN_BYPASS** = Low (normal operation), **AUTO_BYPASS** = High enables the auto bypass mode that puts the reclocker into the bypass mode whenever **LOL** = Low (ie. the reclocker is out of lock).

This implies that if both **MAN_BYPASS** and **AUTO_BYPASS** = Low, when the reclocker is not in lock, undefined data may pass to the output. This mode may be used for troubleshooting or debug purposes.

The reclocker output can be forced to a logic low with **$\overline{\text{DDO\_MUTE}}$** = Low. This function can be used to squelch the retimed noise output, or random transitions that are generated by AC coupled inputs when the upstream signals are disconnected.

Table 2-8. Manual and Auto Bypass Settings

	AUTO_BYPASS	Functional Description
0	0	Retimed Reclocker Output
0	1	Bypass if Reclocker out of lock
1	0	Forced Bypass
1	1	Forced Bypass

Appendix

A.1 Glossary of Terms/Acronyms

Table A-1. Glossary and Acronyms

ASIC	Application Specific Integrated Circuit
DTV	Digital Television
DVB	Digital Video Broadcast
EQ	Equalizer or Equalization
HD	High Definition
SD	Standard Definition
SDI	Serial Digital Interface
SMPTE	Society of Motion Picture and Television Engineers

A.2 Reference Documents

A.2.1 External

Society of Motion Picture and Television Engineers

SMPTE 292M Bit-Serial Digital Interface for High-Definition Television Systems

SMPTE 259M 10-Bit 4:2:2 Component and 4f_{SC} Composite Digital Signals - Serial Digital Interface

SMPTE 344M 540Mb/s Serial Digital Interface

DVB-ASI Digital Video Broadcast