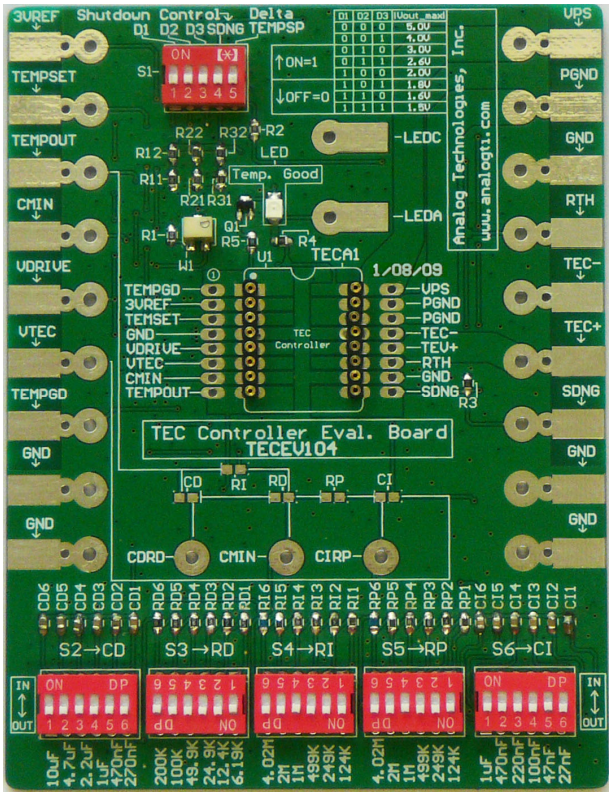

Figure 1. The Physical Photo of TECEV104

INTRODUCTION

The TECA1-xV-xV-D (there is no internal compensation network inside) is an electronic module designed for driving TEC with up to 2A ultra low noise current. The output voltage range is from 0V to 5V when powered by a 5V power supply. This TEC controller module can be evaluated conveniently by using this evaluation board TECEV104. Moreover, TECEV104 can evaluate other TEC controllers including TECA1-xV-xV-DAH, TEC5V4A-D and TEC5V6A-D. It is recommended to read this application note with the TEC controller's datasheet which provides more detail information about the specifications and applications guidance for the TEC controller module.

The main purpose of using the evaluation board is to tune the compensation network on the board for matching the characteristics of users' thermal load. The objectives of the tuning are to minimize the response time of the thermal control loop and the dynamic temperature tracking errors, while keeping the control loop stable.

The user will be able to set the maximum output voltage, set the set-point temperature, monitor the output voltage and the actual thermal load temperature, tune the compensation network for matching the thermal load, etc..

BOARD DESCRIPTION

The TEC controller evaluation board TECEV104 is consisted of a complete tuning and application circuit for driving a TEC. It can set the output voltage limit, tune the compensation network, set internal operating temperature point, and has an LED for indicating the temperature status of the controller, and has numerous connection pads for making connections with external components and instruments.

Its photo is shown in Figure 1. The TEC controller module is located in the center of the TECEV104 Evaluation Board. The voltages of all its pins can be measured directly by probing the vias on the left and right side of the module sockets which are connected directly with pins of the electronic module. Some of the pins are also connected to the soldering pads with two vias on the edges of the board. The names of all these nodes are marked on the board.

The silkscreen layer of the evaluation board is shown in Figure 2 with other top layers, including top silkscreen, top copper, top solder mask, and multilayer (vias). Figure 3 only shows the image of top silkscreen layer. There is no component in the bottom side of the board, so that there is no bottom silkscreen layer image.

Note: This evaluation board is only compatible with TEC controllers of **DIP** package.

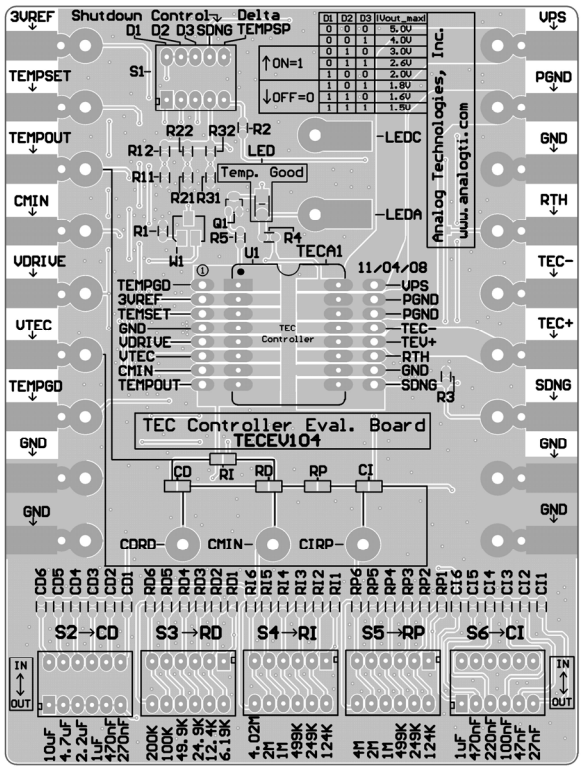

Figure 2. Top Silkscreen Layer with Other Top Layers

There are solder pads on the left and right edges of the board. These pads can be used for connecting the external instruments or components with and the connections can be made by soldering wires, clipping by alligator clips or probing by probes. See Figure 1, 2 and 3. There are solder pads also on the top and the lower side center of the board. These pads can be used for connecting the external instruments or components and the connections can be made by probing with probes or soldering wires.

On the top of the board, there is a switch bank. A potentiometer is located on the lower side the switch bank. On the bottom of the board, there are 5 switch banks. When the set-point temperature and the actual target temperature are less than 0.1°C in difference, the LED on the top lower location will be lit up.

On the board, the compensation network has been initialized before the ship. The initial values of these parameters are shown in table 1.

Table 1 The initial values

Parameter	Value	Note
R_P	2MΩ	
R_I	2MΩ	
R_D	24.9kΩ	
C_I	100nF	
C_D	1μF	

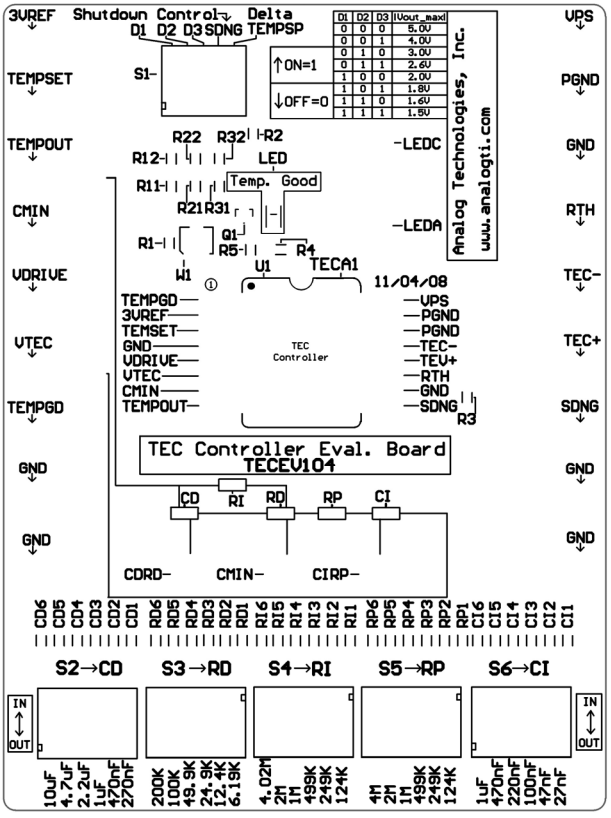

Figure 3. Top Silkscreen

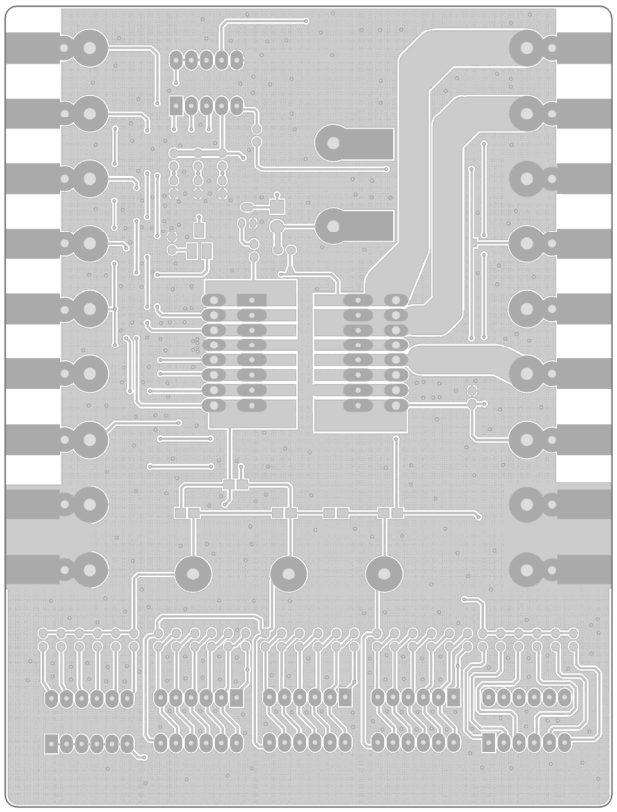

Figure 4. Top Layers without Top Screen Layer

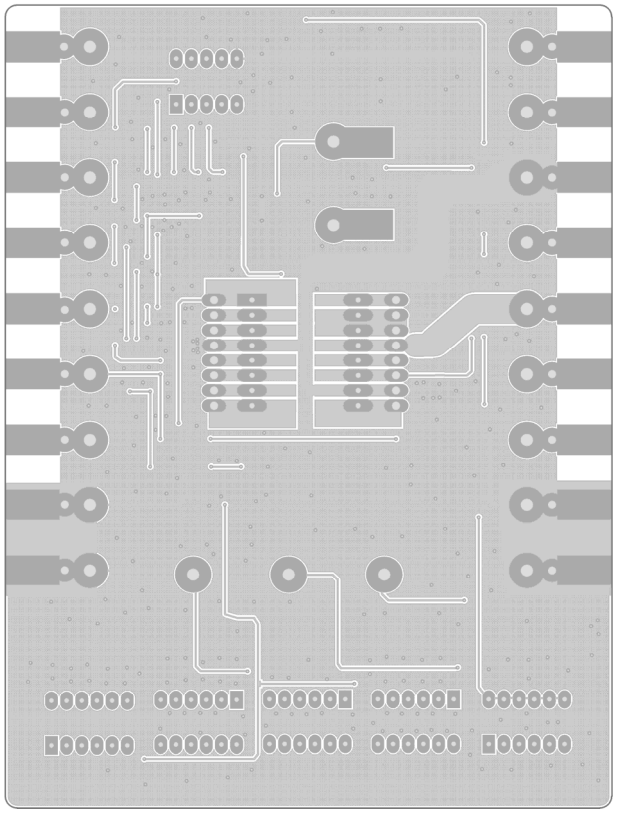

Figure 5. Bottom Layers

Figure 4 shows the top layers without the silkscreen layer.

Figure 5 below shows the bottom layers, including bottom copper, bottom solder mask, and multilayer (vias). Please notice that this is a "see through" image from the top side.

Figures 4 and 5 can be used as a layout reference for designing a system using the TEC controller in the system. These are the main points:

1. Connect the power supply return node directly to the PGND pin of the controller before connecting it to any other points. For thermal management purpose, the returned node was not done in this way on the evaluation board.

2. Use as large copper area as possible for the PCB traces of the solder pads of all the pins so that these copper areas become heat-sinks and help dissipating the heat generated by the controller.

Figure 6 shows the mirrored bottom layers which is a directly-seen image from the bottom side.

The schematic is shown in Figure 7.

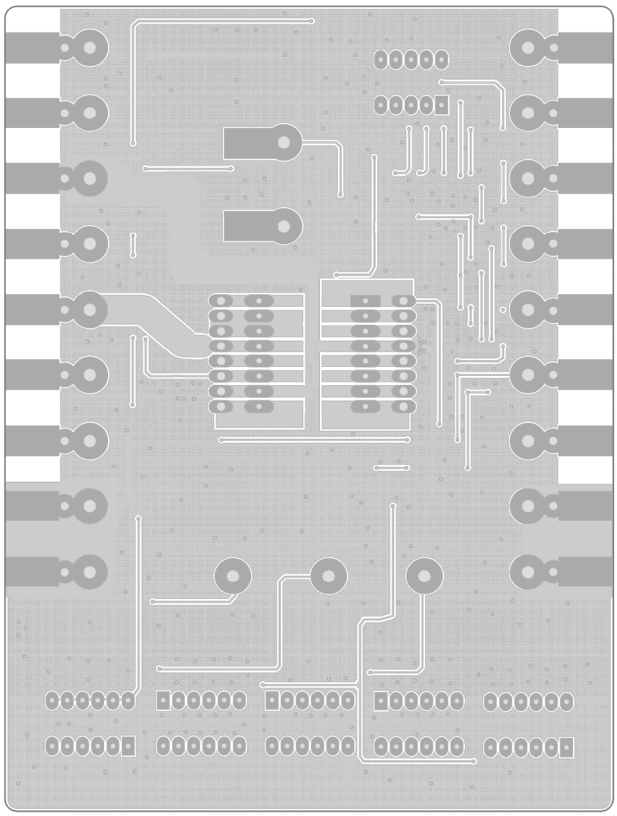

Figure 6. Mirrored Bottom Layers

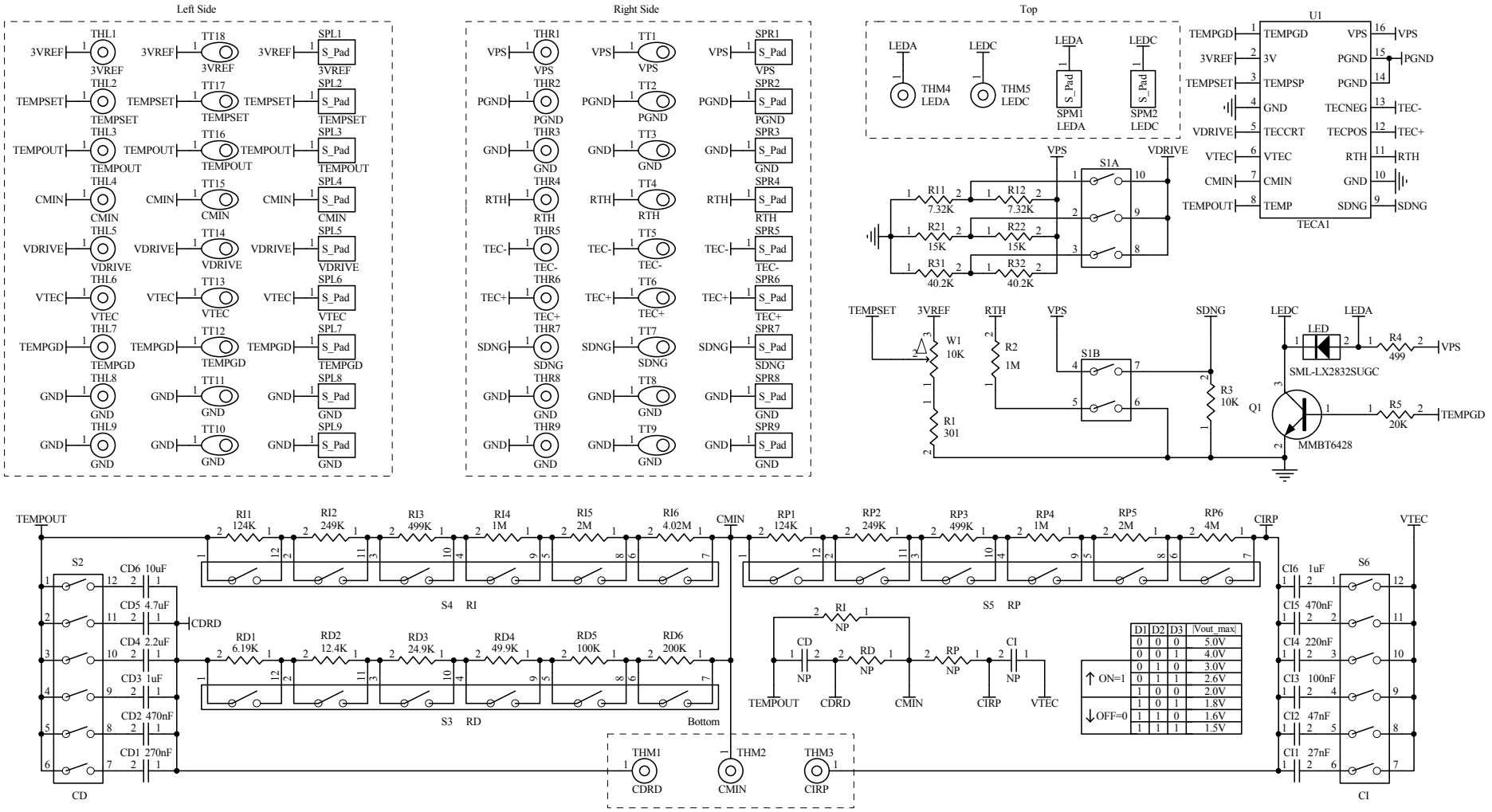

Figure 7. Schematic of TEC Controller Evaluation Board TECEV104

This evaluation board TECEV104 is compatible with the TECA1-xV-xV-D, TECA1-xV-xV-DAH, TEC5V4A-D and TEC5V6A-D TEC controllers.

Table 2 is printed on the actual TECEV104, which shows the values of V_{OUTMAX} when X=5 (i.e. TECA1-5V-5V-D).

Table 3 shows the value of V_{OUTMAX}, which is changing with X value.

Table 2. For TECA1-5V-5V-D

	D1	D2	D3	V_{OUTMAX}
	0	0	0	5.0V
	0	0	1	4.0V
↑ ON=1	0	1	0	3.0V
	0	1	1	2.6V
	1	0	0	2.0V
↓ OFF=0	1	0	1	1.8V
	1	1	0	1.6V
	1	1	1	1.5V

Table 3. For TECA1-5V-XV-D

	D1	D2	D3	V_{OUTMAX} (V)
	0	0	0	$X\times\frac{5}{5}$
	0	0	1	$X\times\frac{4}{5}$
↑ ON=1	0	1	0	$X\times\frac{3}{5}$
	0	1	1	$X\times\frac{2.6}{5}$
	1	0	0	$X\times\frac{2}{5}$
↓ OFF=0	1	0	1	$X\times\frac{1.8}{5}$
	1	1	0	$X\times\frac{1.6}{5}$
	1	1	1	$X\times\frac{1.5}{5}$

GETTING STARTED

1. Hook up the power supply, TEC and thermistor. There are 2 solder pads in the upper right area on the edge for connecting the DC power supply voltages in the right polarity as indicated onto the board. Usually the power supply is set to 5V. There are also 2 solder pads in the center right area on the edge for connecting the TEC terminals in the right polarity as indicated onto the board. Connect the thermistor terminals to the board, there is no polarity requirement. On the top of the board, there is the switch bank S1, the fifth switch Delta TEMPSP is used to adjust the compensation network of temperature control loop by inputting a square wave disturbing signal in temperature input point, which enables the system to generate corresponding response waveform. At this time, observe the waveform change by oscilloscope, and adjust and optimize the compensation network of the temperature control loop so as to achieve the best waveform at the same time. Response waveform is achieved by measuring VTEC with oscilloscope, as shown in Figure 8 and Figure 9. The compensation network components consist of RI, RD, RP, CD and CI, which will be adjusted by S2, S3, S4, S5 and S6 (When turning one of these switches to higher position, the corresponding value will be applied). These connections can be done by clipping or soldering on the pads, see Figure 1. Check the evaluation board connections, making sure that they are all correctly connected.

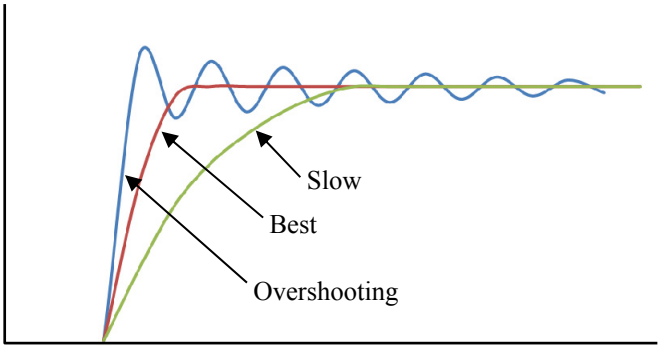

Figure 8. Rise Waveforms of VTEC

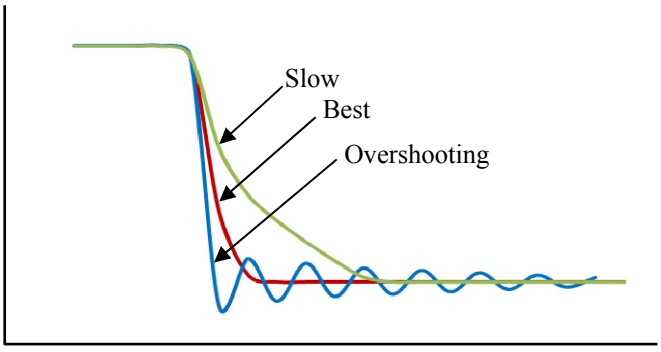

Figure 9. Fall Waveforms of VTEC

2. Turn on and off the controller. This can be done by either turning off the power supply or turning off the shut-down pin of the controller. To do the latter, turn the switch SDNG to its lower position to turn off the controller, which shorts circuit the shutdown pin SDNG to the ground, or turn the switch SDNG to its upper position to turn on the controller.

3. Check the voltage reference. Use a voltmeter to check the voltage reference pin 3VREF having an accurate 3V.

Tune the compensation network. The purpose for this step is to match the controller compensation network with the thermal load characteristics thus that the response time and temperature tracking error are minimized. Adjust the potentiometer W1 to change the set-point temperature TEMPSET just a small amount, simulating a step function. At the same time, connect an oscilloscope at the VTEC test pin (on the left side of the evaluation board), set it to a scrolling mode (0.2 Second/Division or slower) and monitor the waveform of VTEC as TEMPSET is fed by a step function signal. The circuit in the compensation network is shown in Figure 10 below.

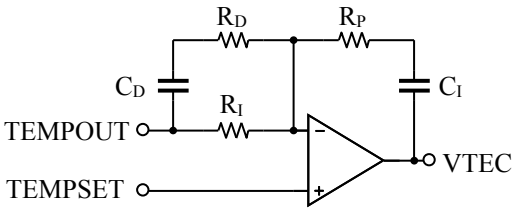

Figure 10. Compensation network

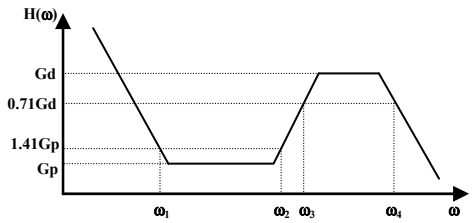

Figure 11. Transfer Function of the Compensation Network

The transfer function of the compensation network, defined as H(ω)=VTEC(ω)/TEMPOUT(ω), is shown in Figure 11.

In principle, these are the impacts of the components to the tuning results:

a. R_P/R_I determines the gain for the proportional component of the feedback signal which is from the thermistor, Gp = R_P/R_I, in the control loop, the higher the gain, the smaller the short term error in the target temperature (which is of the cold side of the TEC) compared with the set-point temperature, but the higher the tendency of the loop's instability.

b. R_P/R_D determines the gain for the differential component, Gd = $R_P/(R_D//R_I) \approx R_P/R_D$, where symbol "//" stands for

two resistors in parallel, since $R_I >> R_D$, $R_D//R_I \approx R_D$. The higher the gain, the shorter the rise time of the response, the more the overshoot and/or the undershoot will be.

c. C_I*R_P determines the corner frequency, $\omega_1= 1/(C_I*R_P)$, where the integral component starts picking up, as the frequency goes down. It determines the cut-off frequency below which the TEC controller will start having a large open loop gain. The higher the open loop gain, the smaller the tracking error will be.

d. C_D*R_I determines the corner frequency, $\omega_2=1/(C_D*R_I)$, where the differential component starts picking up (see Figure 11), as the frequency goes up.

e. C_D*R_D determines the corner frequency, $\omega_3=1/(C_D*R_D)$, where the differential component starts getting flat. It determines the cut-off frequency above which the TEC controller will give extra weight or gain in response.

f. $1nF*R_P$ determines the corner frequency, $\omega_4=1/(1nF*R_P)$, where the differential component starts rolling down. Since this frequency is way higher than being needed for controlling the TEC, ω_4 does not need to be tuned. The capacitor is built into the TEC controller module, not the evaluation board.

To start the tuning, turn off the differential circuit by setting C_D Open. Turn W1 quickly by a small angle, back and forth, approximately 5 seconds per change. Set C_I to 1uF, set R_I to 1M, and increase the ratio of R_P/R_I as much as possible, provided the loop is stable, i.e. there are no oscillations seen in VTEC. Then, minimize C_I as much as possible, provided the loop is stable. The next step is to minimize Rd and maximize C_D while maintaining about 10% overshoot found in VTEC. Optimum result can be obtained after diligent and patient tuning. The tuning is fun and important.

When the TEC controller is used for driving a TEC to stabilize the temperature of a diode laser, there is no need to turn on the laser diode while tuning the TEC controller. To simulate the active thermal load given by the laser diode, setting the set-point temperature lower than the room temperature is enough.

For a typical laser head used in EDFA's or laser transmitters (found in DWDM applications, for instance), R_I = 1MΩ, R_P = 1MΩ, C_I = 470nF, C_D = 2.2μF, and R_D = 200kΩ. These values may vary, depending on the characteristics of a particular thermal load.

To be conservative in stability, use larger C_I and larger R_I; to have quicker response, use smaller Rd and larger C_D.

The closer to the TEC the thermistor is mounted, the easier to have the loop stabilized, the shorter the rise time and the settling time of the response will be.

4. After tuning, the values of the capacitors for C_D and C_I can be read off the capacitor selection switches. The values of the resistors, R_I, Rd and R_P, can be measured by an Ohm-meter by connecting to the resistor pins. As seen in the photo of Figure 3, R_I can be read off between TEMPOUT and CMIN test points; R_D can be read off between CMIN and CDRD test points; R_P can be read off between CMIN and CIRP test points.

5. After the compensation network is tuned properly, we can now adjust set-point temperature to see if the TEC controller can drive the target temperature to a certain range and with high stability. Turn the temperature set-point TEMPSET potentiometer W1 while monitoring its output voltage at TEMPSET test point (2nd row on left side of the board), watch the LED: when it turns to green, the target temperature is locked to the set-point temperature within 0.1°C or less. The relationship between the set-point voltage vs. the set-point temperature is given in the datasheet. After seeing the LED lock into the set-point temperature, VTEC should be a constant voltage as shown in the oscilloscope and the voltage between TEMPSET and TEMPOUT should be very small, less than 10mV. When a standard TEC controller is used, the 10mV represent a 0.07° temperature error.

6. Set output voltage limit. Turning switches D1, D2, and D3, up and down will set the TECA1-5V-XV-D to different output voltage limit: 1.5V, 1.6V, 1.8V, 2.0V, 2.6V, 3.0V, 4.0V and 5.0V. See Figure 1, 2, 3 and 7.

7. To know more parameters of the TEC controller.

a. To know the actual target temperature, use a voltage meter to measure the voltage between the TEMPOUT and the GND pins, the reading result is: target temperature = 15°C + (TEMPOUT voltage (V))*6.67°C for approximation (see the curve in the TEC controller data sheet).

b. To know how hard the TEC is working, measure the voltage VTEC by a voltage meter or an ADC, TEC voltage = 2.5V – V_{VTEC}. When the TEC voltage (from the calculation) is positive, it is in cooling mode; when the TEC voltage is negative, it is in heating mode.

c. To try other values of capacitors not provided by the evaluation board for the capacitors in the compensation network, turn down the capacitor switches, to the "OUT" position, connect the component to the corresponding soldering pads as marked on the evaluation board, see Figure 1.

d. To shut down the TEC controller, turn the Shutdown Control switch SDNG to the "Off" position, see Figure 1.

e. To control the set-point temperature directly by using a DAC, set the set-point temperature POT W1 to the middle point (25°C), on which the TEMPSET is about 1.5V, the half value of the reference voltage, connect TEMPSET test point to the output of the DAC and use this formula for approximation when the input voltage is between 0V and 3V:
set-point temperature (°C) = 15°C + (TEMPOUT voltage (V))*6.67°C. The maximum voltage allowed is V_{VPS} (power supply). See the curve in the TEC controller data sheet.

f. To control the TEC voltage directly by using a DAC, connect VTEC to the output of the DAC and use this formula: TEC voltage = 2.5V – V_{VTEC} (V).

g. To shut down the TEC controller by using a microprocessor, turn off the Shutdown Control switch, connect SDNG test point (3rd row from the bottom side, on right side of the board) to one of its digital outputs. When pulling low, the TEC controller is shut off. When pulling high SDNG, the TEC controller is turned on.

h. The evaluation schematic is given in Figure 7.

Using the TEC controller for more applications not described here, and/or having any questions, please feel free to contact us.

Note: This evaluation board, TECEV104, is only compatible with TEC controllers of DIP package.

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