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U_DDR3-RAM
DDR3-RAM.SchDoc

U_Ethernet
Ethernet.SchDoc

U_USB-PHY
USB-PHY.SchDoc

U_SOC
SOC.SchDoc

U_CPLD
CPLD.SchDoc

U_POWER2
POWER2.SchDoc

U_HyperFlash_RAM
HyperFlash_RAM.SchDoc

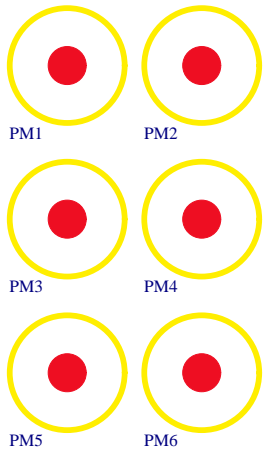
U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc


U_Connectors
Connectors.SchDoc

U_POWER
POWER.SchDoc

LOGO1
TE Logo PRINT Layer
LOGO PRINT



Serial
Serialnumber 6,3 x 6.3mm

			Title: TE0782 - Overview	
			A4	Number: TE0782 TE0782-02-045-2I
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page1 of 31
Filename: TE0782.SchDoc				

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A

A

B

B

C

C

D

D

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U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc



U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc



U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



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		Title: TE0782 - Connectors	
		A4	Number: TE0782 TE0782-02-045-2I
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Filename: Connectors.SchDoc		Page2 of 31	

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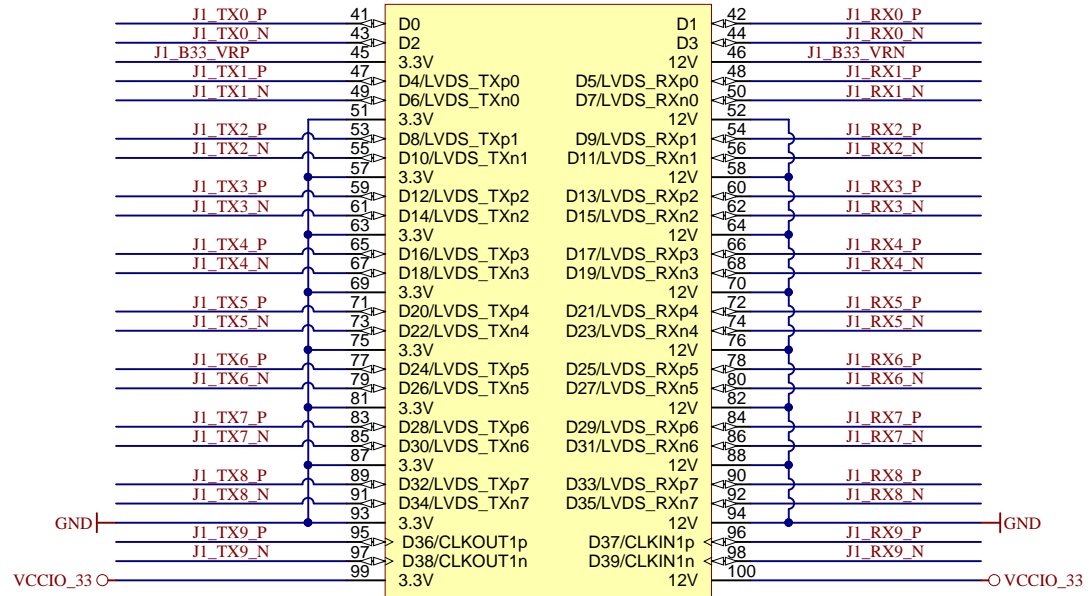
C

C

D

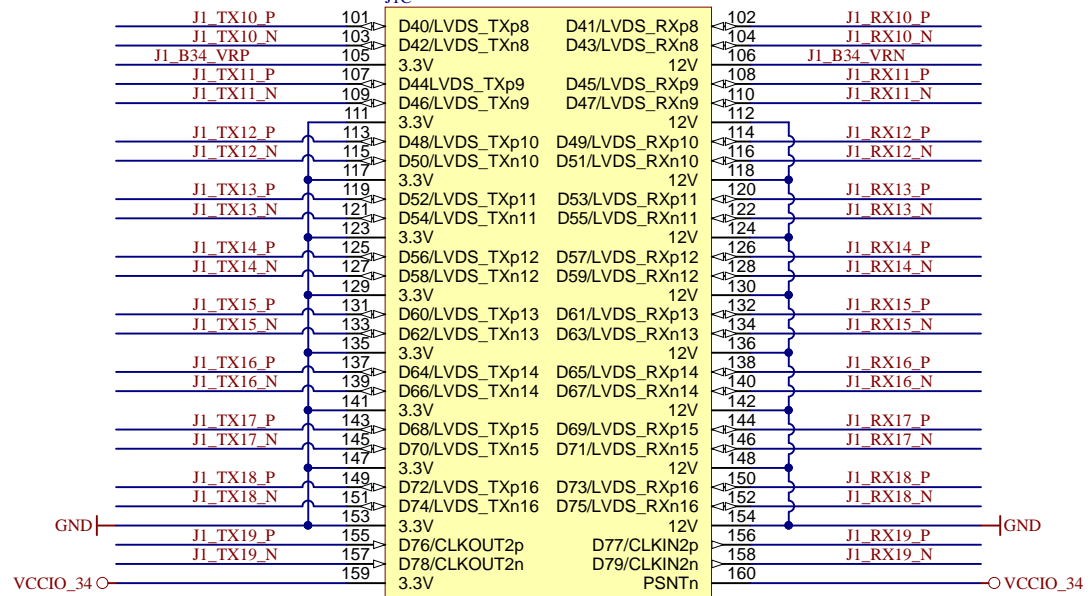
D

J1B



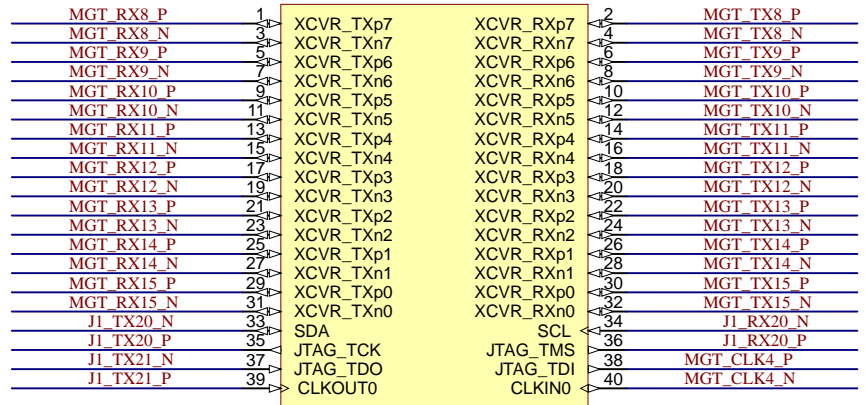
ASP-122952-01

J1C



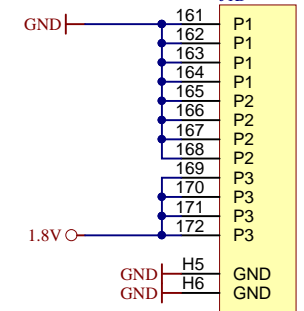
ASP-122952-01

J1A



ASP-122952-01

J1D



ASP-122952-01



Title: TE0782 - HSMC_Connector_J1		
A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page3 of 31
Filename: HSMC_CONN_J1.SchDoc		

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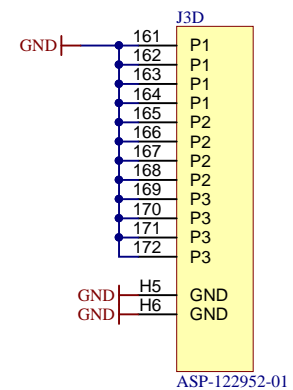
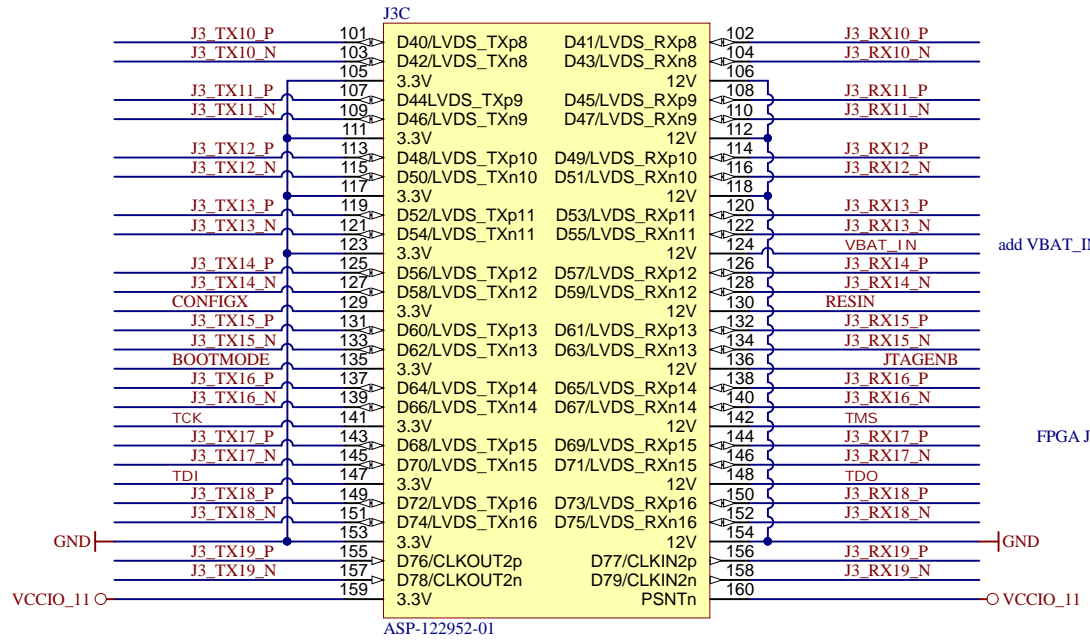
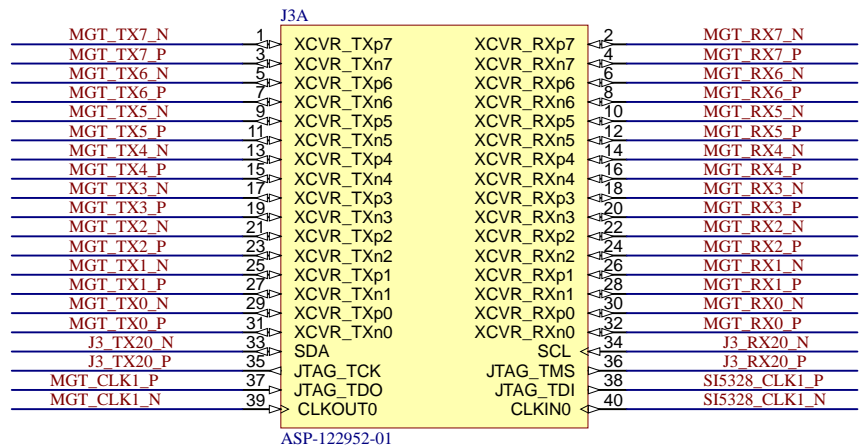
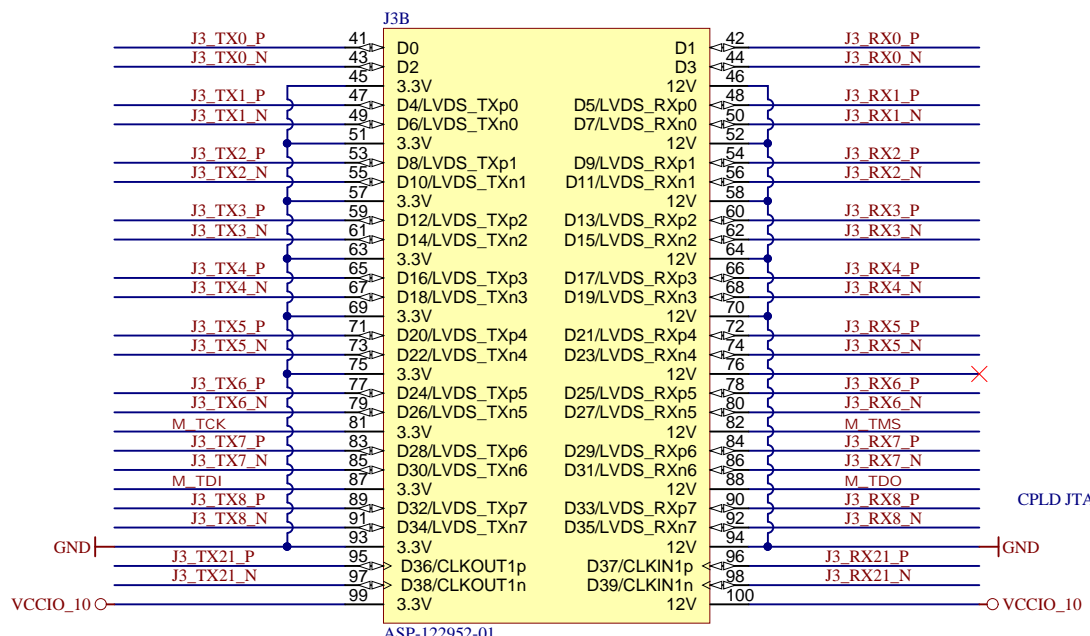
B

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Title: TE0782 - HSMC_Connector_J3		
A4	Number: TE0782 TE0782-02-045-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page4 of 31
Filename: HSMC_CONN_J3.SchDoc		

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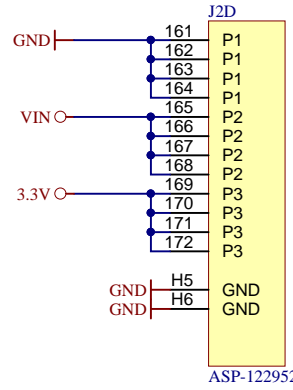
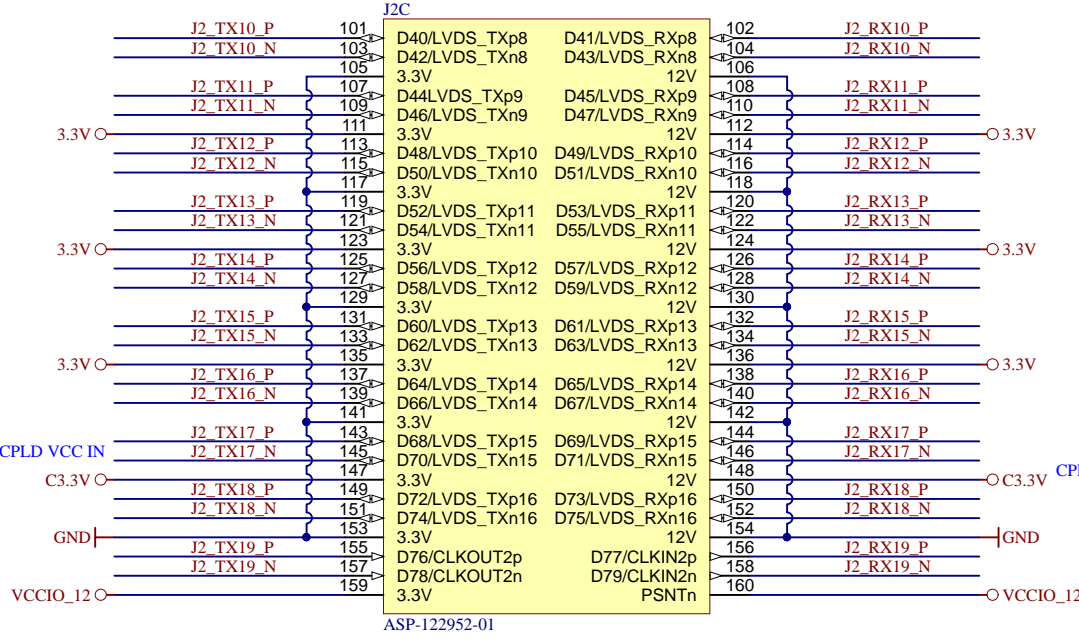
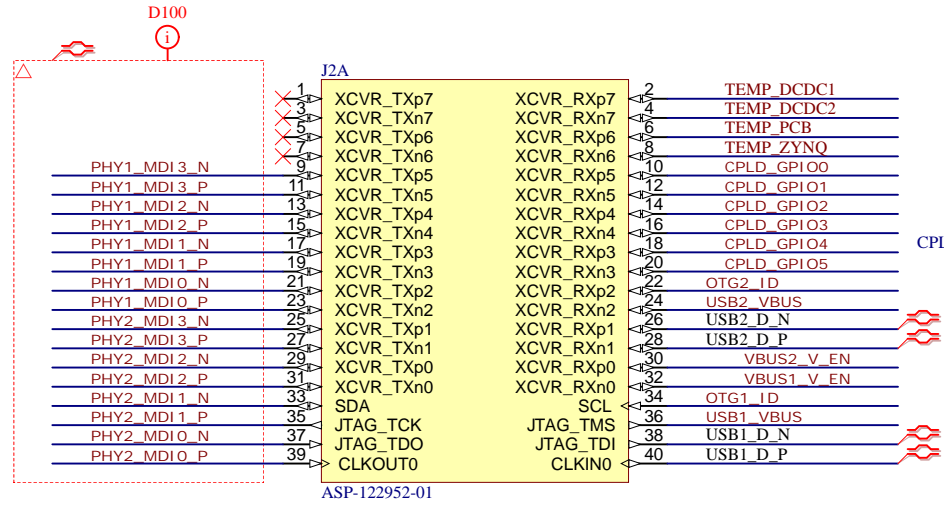
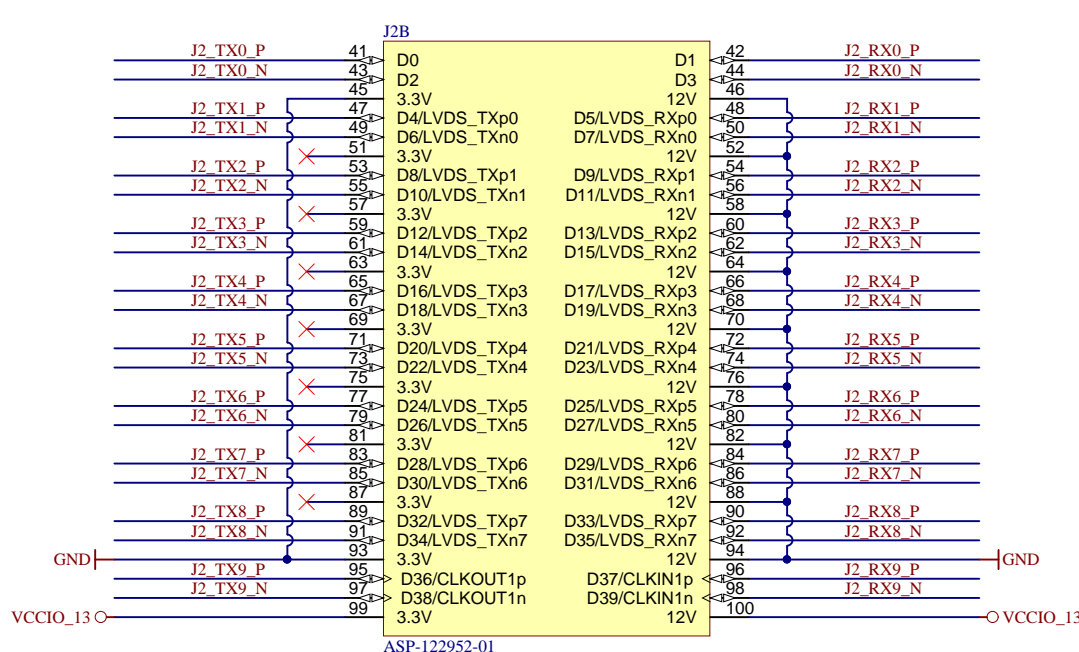
D

A

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D



Title: TE0782 - HSMC_Connector_J2		
A4	Number: TE0782 TE0782-02-045-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page5 of 31
Filename: HSMC_CONN_J2.SchDoc		

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A

A

U_PS-DDR
PS-DDR.SchDoc



U_B9
B9.SchDoc



U_MIO-BANKS
MIO-BANKS.SchDoc



U_B10
B10.SchDoc



U_HP-BANKS
HP-BANKS.SchDoc



U_B11
B11.SchDoc



B

B

U_FPGA-MGT
FPGA-MGT.SchDoc



U_B12
B12.SchDoc



U_FPGA-CFG
FPGA-CFG.SchDoc



U_B13
B13.SchDoc



C

C

U_FPGA-PWR
FPGA-PWR.SchDoc



D

D



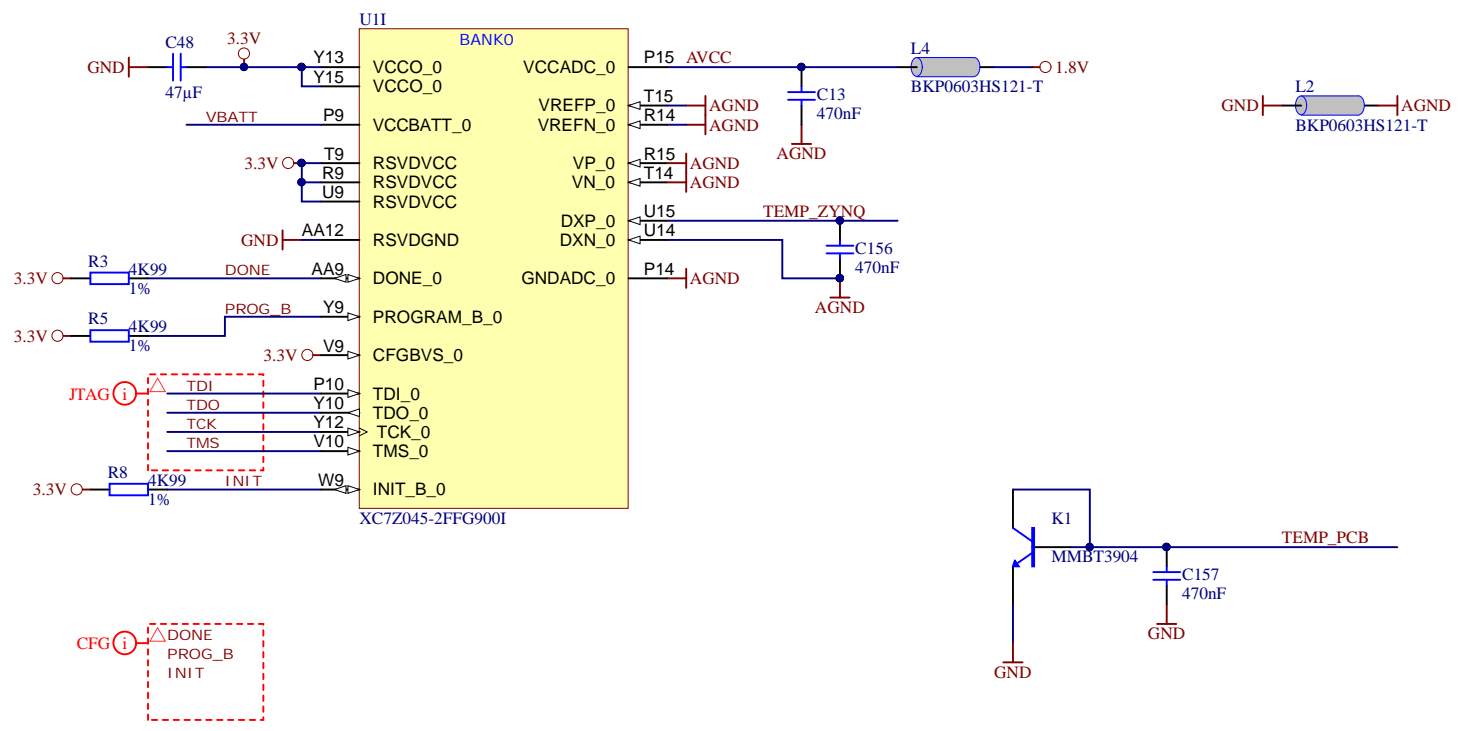
Title: TE0782 - SOC		
A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 6 of 31
Filename: SOC.SchDoc		

1

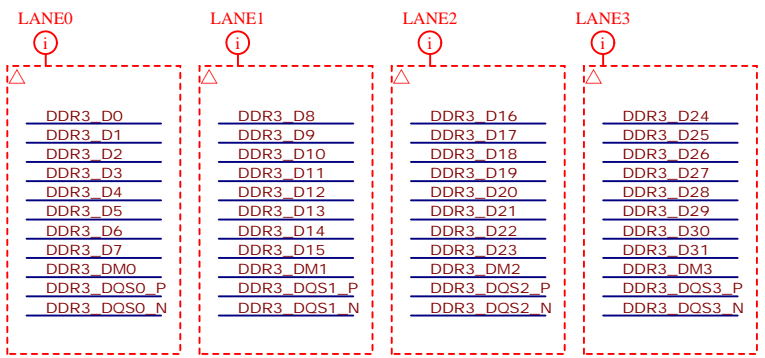
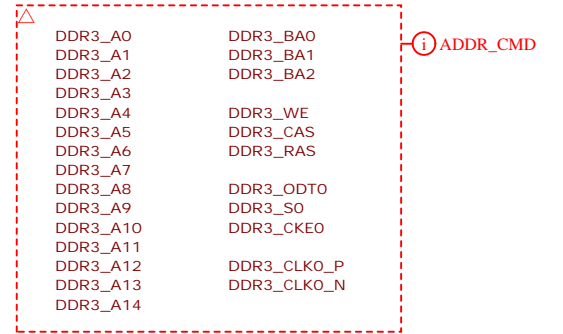
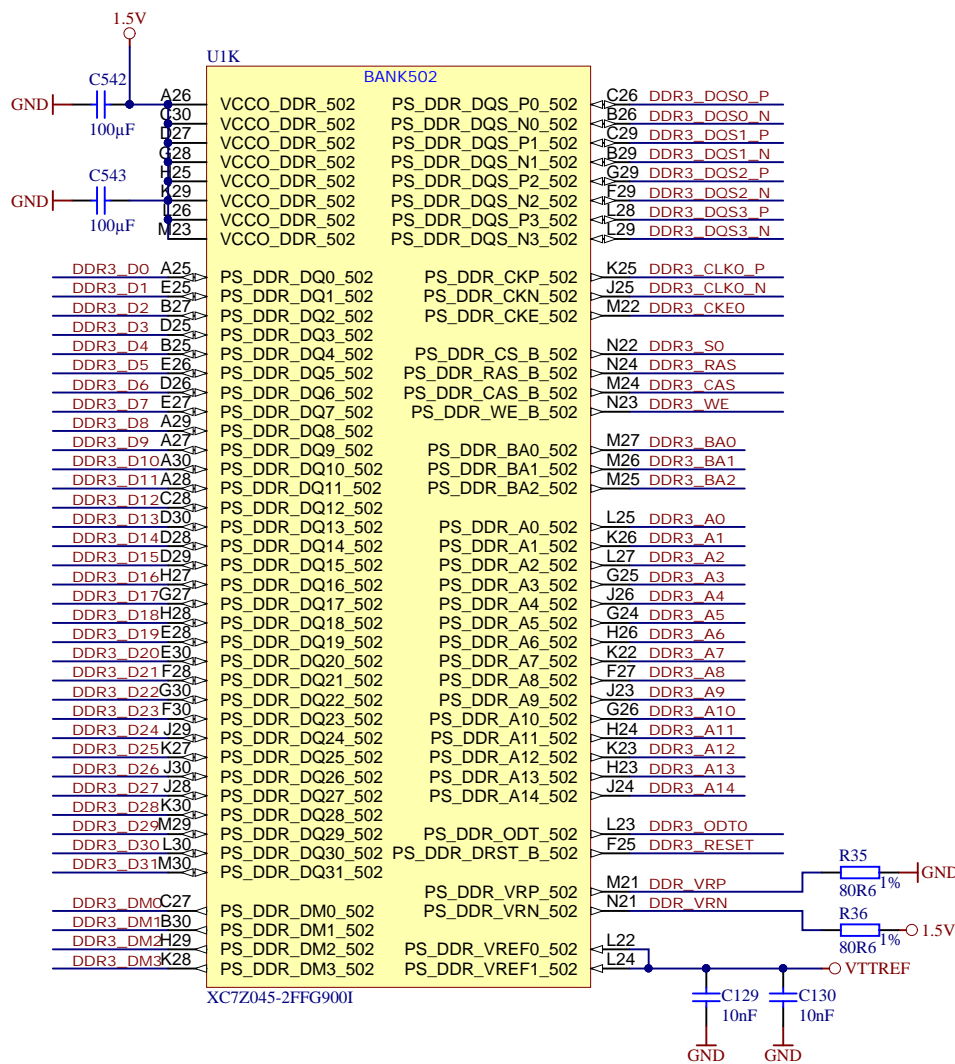
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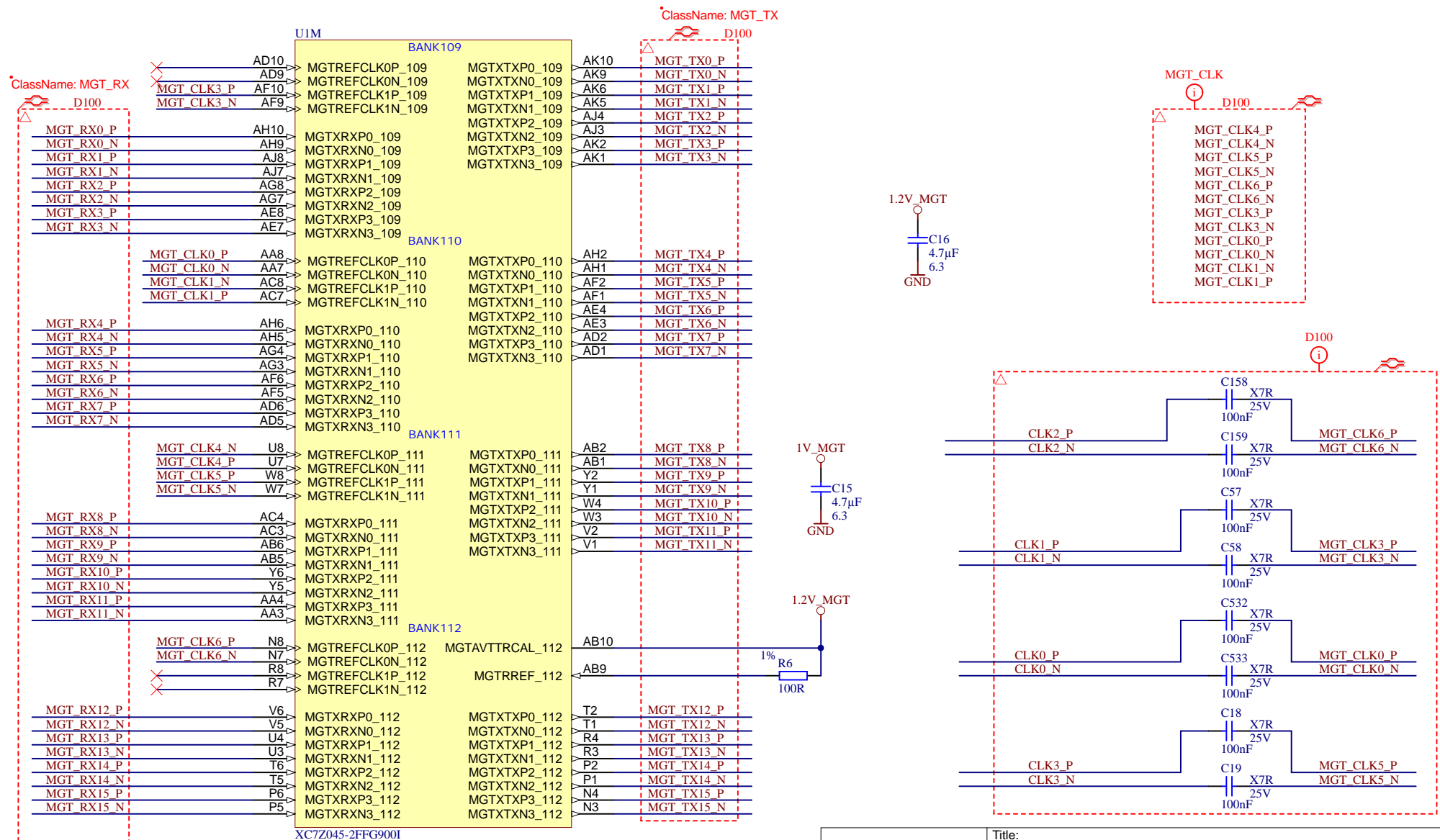
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Title: TE782 - FPGA Configuration		
A4	Nummer: TE0782 TE0782-02-045-2I	Rev. 02
Datum: 2015-05-27	Zeichner: Trenz Electronic GmbH	Blatt 7 von 31
Filename: FPGA-CFG.SchDoc		



			Title: TE0782 - FPGA DDR Banks	
			A4	Number: TE0782 TE0782-02-045-21
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 8 of 31
Filename: PS-DDR.SchDoc				



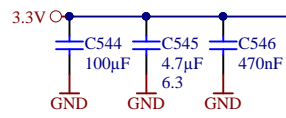
XC7Z045-2FFG900I



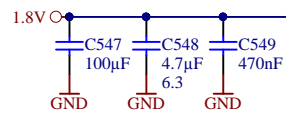
Title: TE0782 - FPGA MGT		
A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page9 of 31
Filename: FPGA-MGT.SchDoc		

U1J
BANK500 & 501

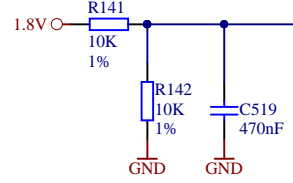
SPI and JTAG modes supported
Cascade and independent modes supported



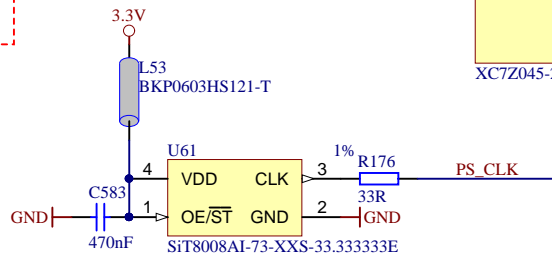
PS_CLK
PS_POR



PS_SRST



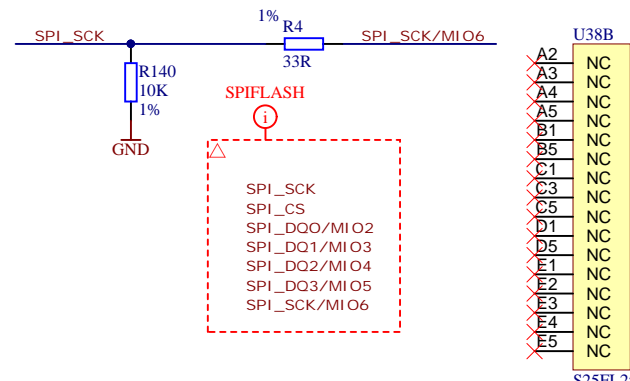
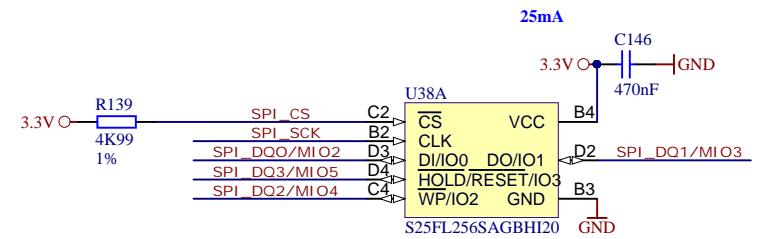
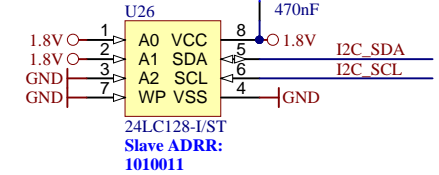
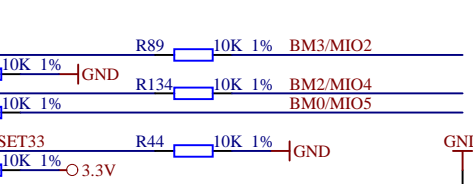
- B500
 ⓘ ClassName: PKG
 ⓘ ClassName: B500
- △ SPI_CS
 - △ SPI_DQ0/MIO2
 - △ SPI_DQ1/MIO3
 - △ SPI_DQ2/MIO4
 - △ SPI_DQ3/MIO5
 - △ SPI_SCK/MIO6
 - △ MMC-DO
 - △ MMC-CMD
 - △ MMC-CCLK
 - △ MMC-D1
 - △ MMC-D2
 - △ MMC-D3



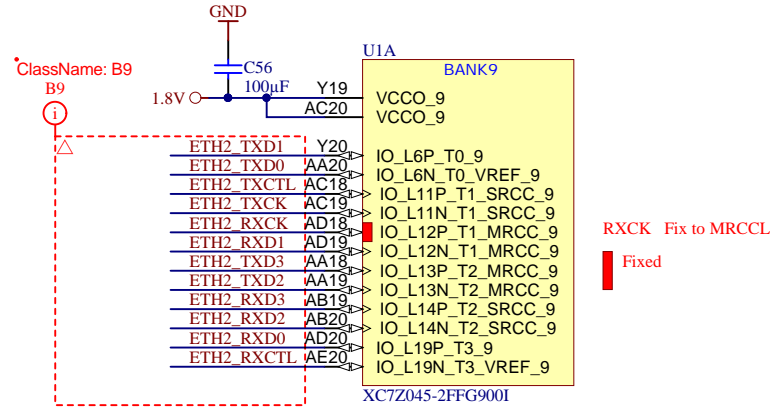
VCCO_MIO0_500	PS_MIO0_500	F24	OTG-RST33
VCCO_MIO0_500	PS_MIO1_500	D23	SPI_CS
VCCO_MIO0_500	PS_MIO2_500	F23	SPI_DQ0/MIO2
	PS_MIO3_500	C23	SPI_DQ1/MIO3 R133
	PS_MIO4_500	E23	SPI_DQ2/MIO4
	PS_MIO5_500	C24	SPI_DQ3/MIO5 R135
	PS_MIO6_500	D24	SPI_SCK/MIO6
	PS_MIO7_500	B24	ETH1_RESET33
	PS_MIO8_500	C21	MIO8
	PS_MIO9_500	A24	MIO9
	PS_MIO10_500	E22	MMC-DO
	PS_MIO11_500	A23	MMC-CMD
	PS_MIO12_500	E21	MMC-CCLK
	PS_MIO13_500	F22	MMC-D1
	PS_MIO14_500	B22	MMC-D2
	PS_MIO15_500	C22	MMC-D3
	PS_MIO16_501	L19	ETH1_TXCK
	PS_MIO17_501	K21	ETH1_TXD0
	PS_MIO18_501	K20	ETH1_TXD1
	PS_MIO19_501	J20	ETH1_TXD2
	PS_MIO20_501	M20	ETH1_TXD3
	PS_MIO21_501	J19	ETH1_TXCTL
	PS_MIO22_501	L20	ETH1_RXCK
	PS_MIO23_501	J21	ETH1_RXD0
	PS_MIO24_501	M19	ETH1_RXD1
	PS_MIO25_501	G19	ETH1_RXD2
	PS_MIO26_501	M17	ETH1_RXD3
	PS_MIO27_501	G20	ETH1_RXCTL
	PS_MIO28_501	L17	OTG-DATA4
	PS_MIO29_501	H22	OTG-DIR
	PS_MIO30_501	L18	OTG-STP
	PS_MIO31_501	H21	OTG-NXT
	PS_MIO32_501	K17	OTG-DATA0
	PS_MIO33_501	G22	OTG-DATA1
	PS_MIO34_501	K18	OTG-DATA2
	PS_MIO35_501	G21	OTG-DATA3
	PS_MIO36_501	H17	OTG-CLK
	PS_MIO37_501	B21	OTG-DATA5
	PS_MIO38_501	A20	OTG-DATA6
	PS_MIO39_501	F18	OTG-DATA7
	PS_MIO40_501	B20	OTG2-DATA4
	PS_MIO41_501	J18	OTG2-DIR
	PS_MIO42_501	D20	OTG2-STP
	PS_MIO43_501	E18	OTG2-NXT
	PS_MIO44_501	E20	OTG2-DATA0
	PS_MIO45_501	H18	OTG2-DATA1
	PS_MIO46_501	F20	OTG2-DATA2
	PS_MIO47_501	A18	OTG2-DATA3
	PS_MIO48_501	C19	OTG2-CLK
	PS_MIO49_501	D18	OTG2-DATA5
	PS_MIO50_501	A19	OTG2-DATA6
	PS_MIO51_501	F19	OTG2-DATA7
	PS_MIO52_501	D19	ETH1_MDC
	PS_MIO53_501	C18	ETH1_MDIO


XC7Z045-2FFG9001

B501
 ⓘ ClassName: B501
 ⓘ ClassName: PKG

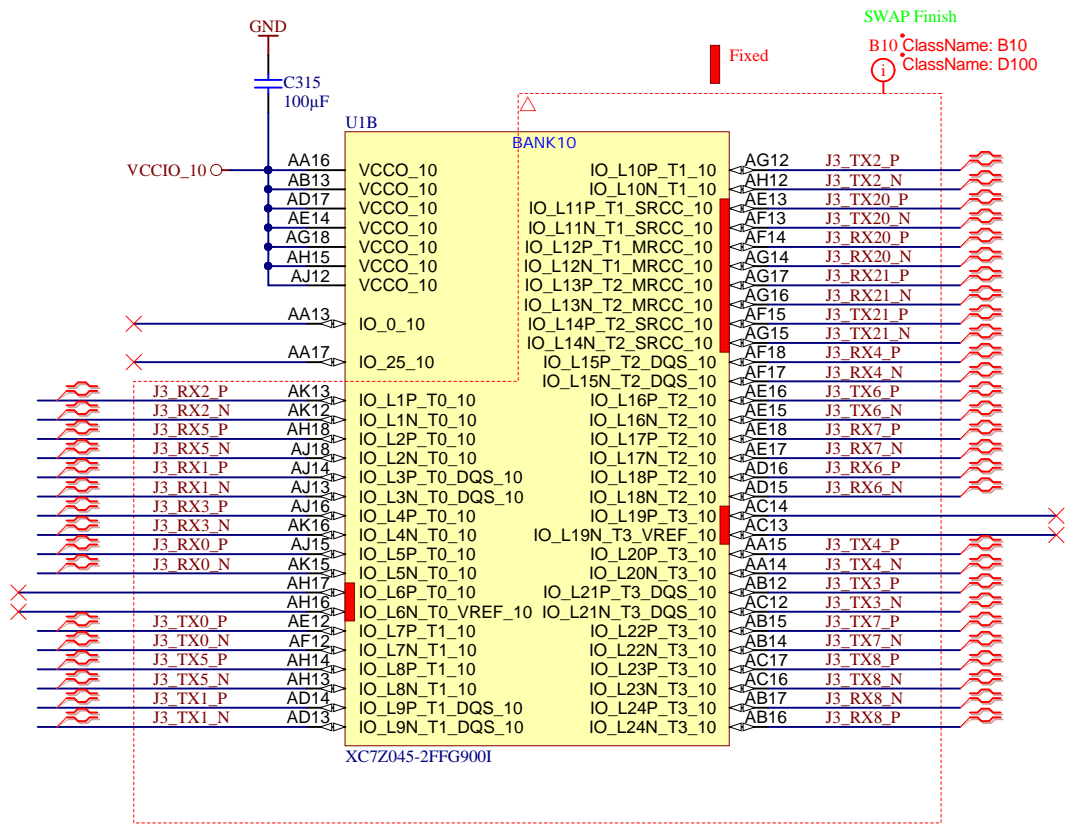


Title: TE0782 - FPGA MIO Banks		
A4	Number: TE0782 TE0782-02-045-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page10 of 31
Filename: MIO-BANKS.SchDoc		



			Title: TE0782 - FPGA B9	
			A4	Number: TE0782 TE0782-02-045-2I
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 11 of 31
Filename: B9.SchDoc				

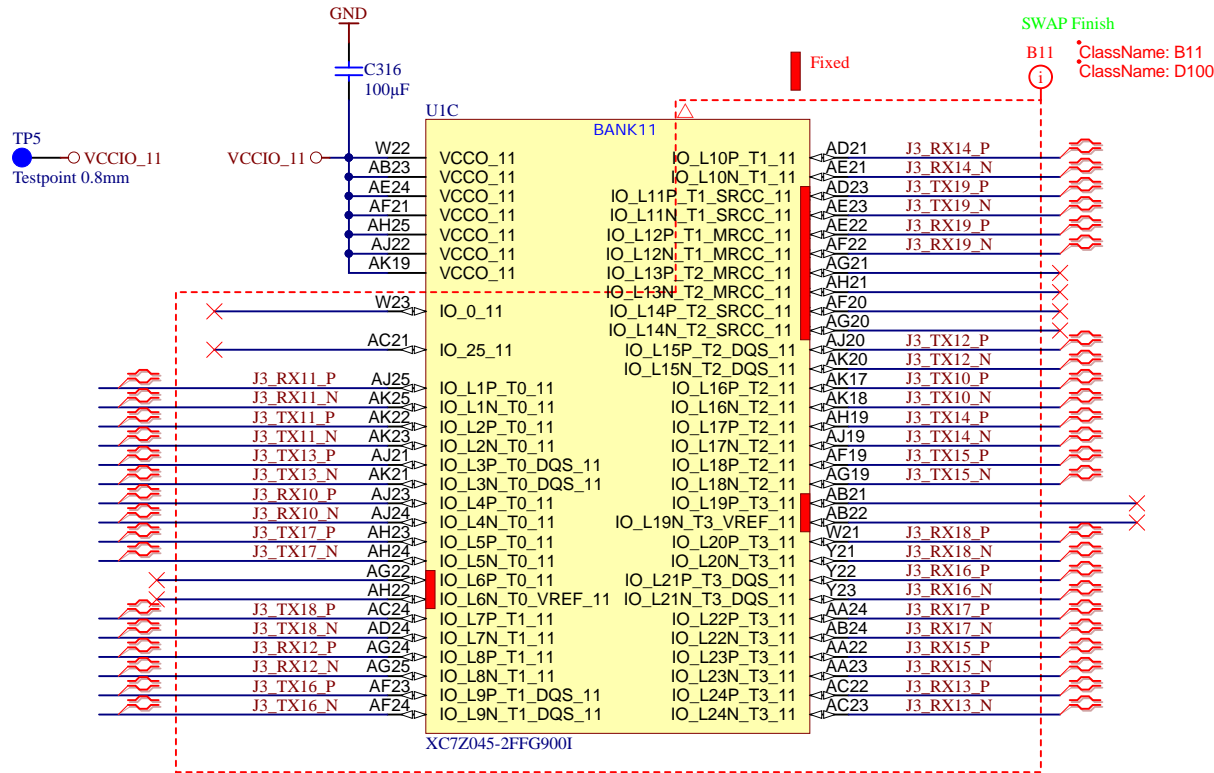
TP4
 ●—○ VCCIO_10
 Testpoint 0.8mm





SWAP Finish
 Fixed
 B10:ClassName: B10
 D100:ClassName: D100

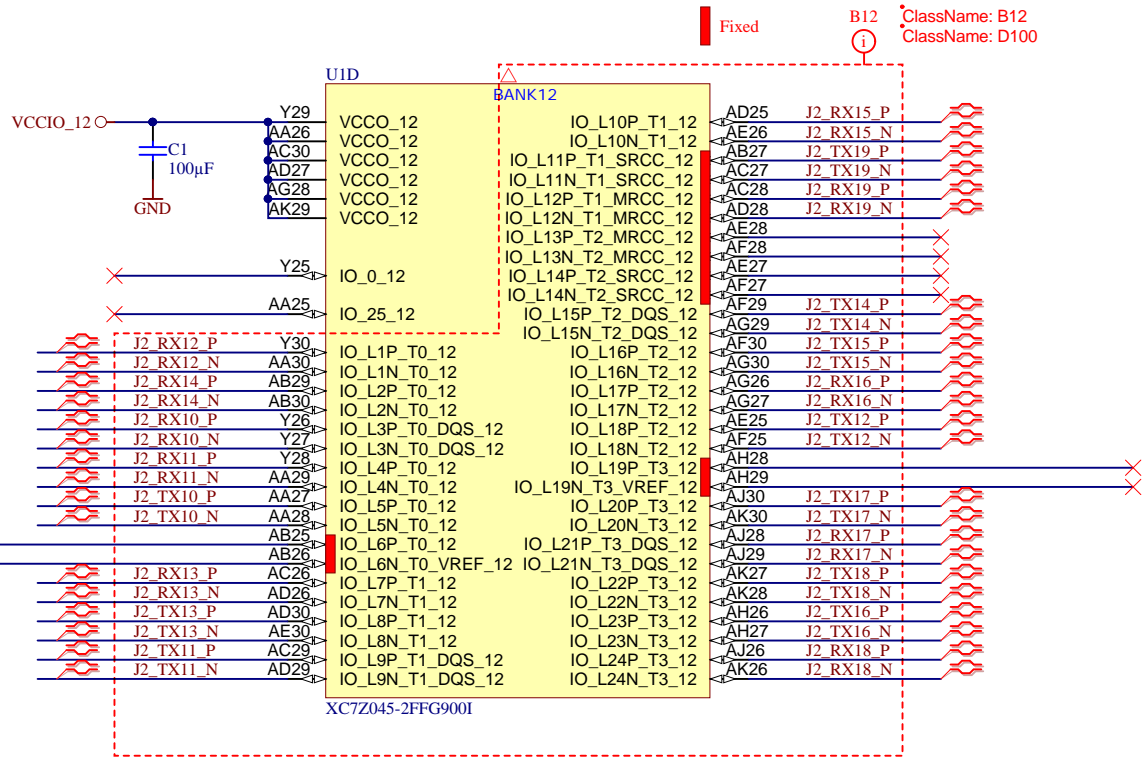


Title: TE0782 - FPGA B10		
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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 12 of 31
Filename: B10.SchDoc		




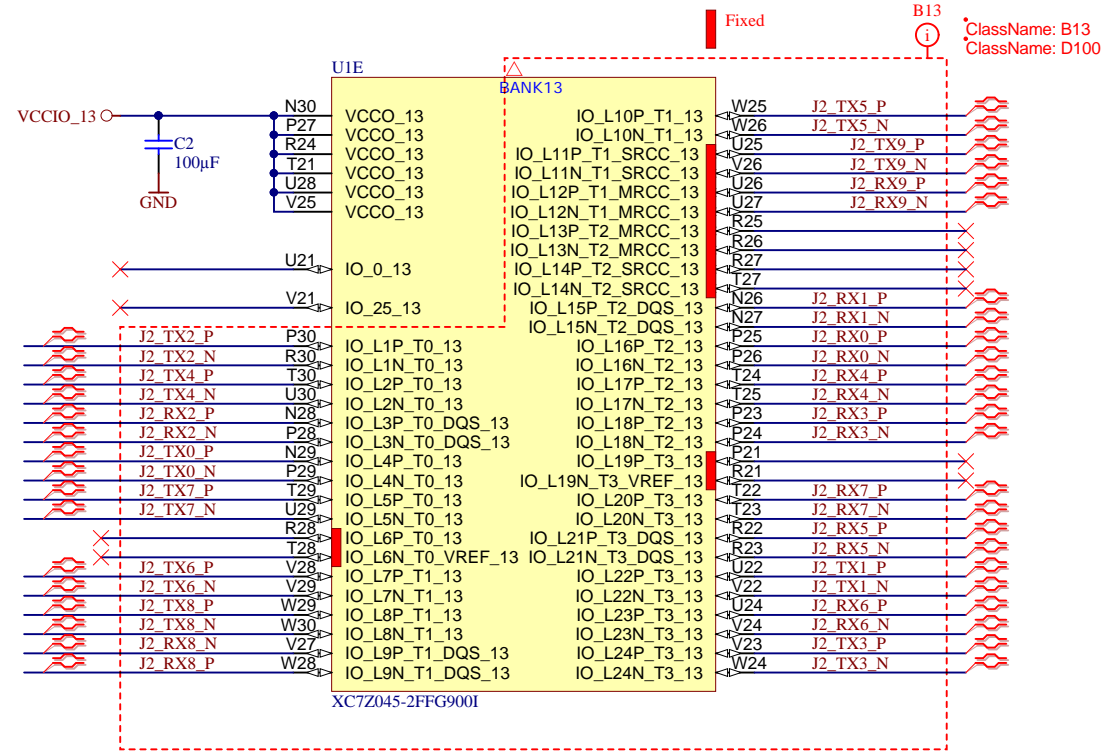
		Title: TE0782 - FPGA B11	
		A4	Number: TE0782 TE0782-02-045-2I
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Page 13 of 31		Page 13 of 31	
Filename: B11.SchDoc		Page 13 of 31	

TP1
 VCCIO_12
 Testpoint 0.8mm



Title: TE0782 - FPGA B12		
A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 14 of 31
Filename: B12.SchDoc		

TP2
 VCCIO_13
 Testpoint 0.8mm



Title: TE0782 - FPGA B13		
A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page15 of 31
Filename: B13.SchDoc		

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U_B33
B33.SchDoc



U_B34
B34.SchDoc



U_B35
B35.SchDoc



A

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D

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Title: TES0782 - FPGA HP Banks		
A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 16 of 31
Filename: HP-BANKS.SchDoc		

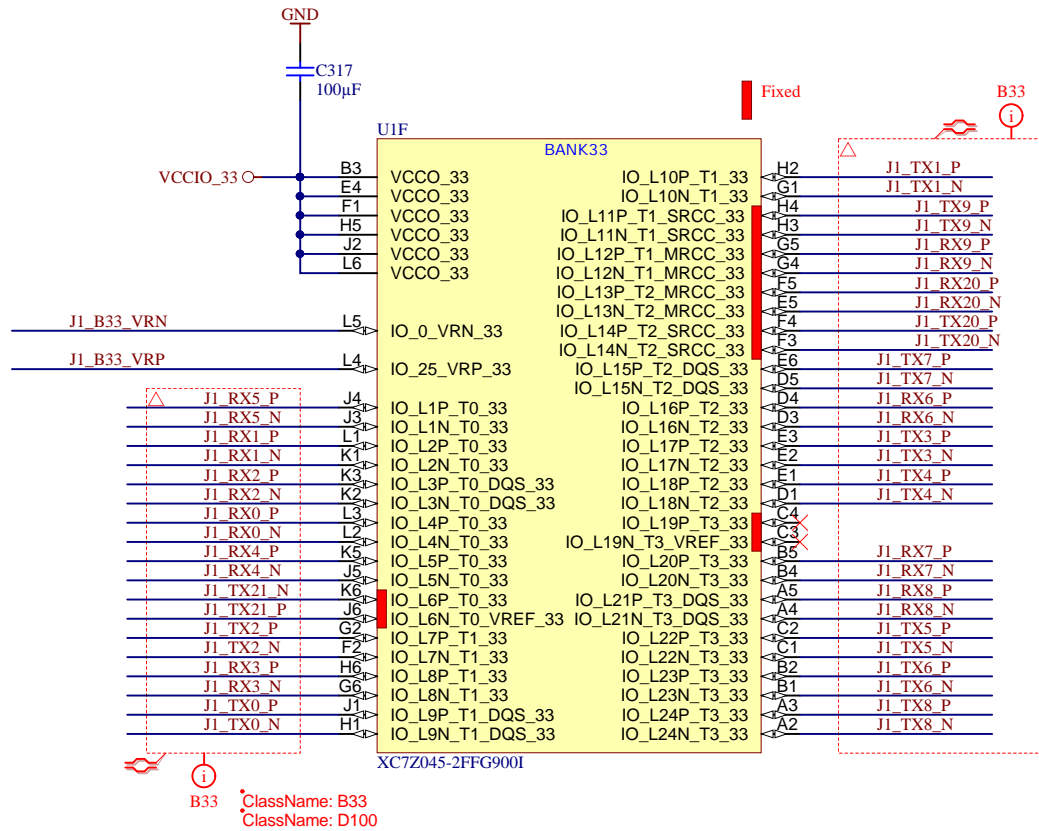
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TP6
 VCCIO_33
 Testpoint 0.8mm

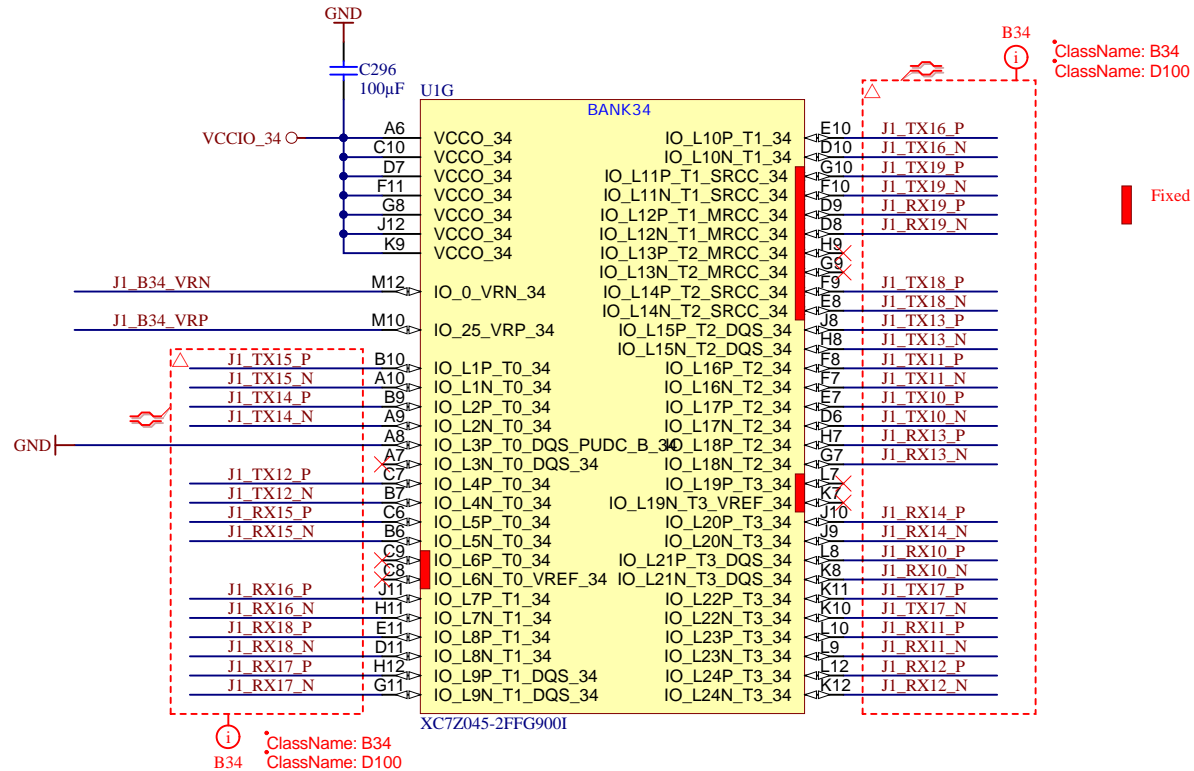


ClassName: B33
 ClassName: D100

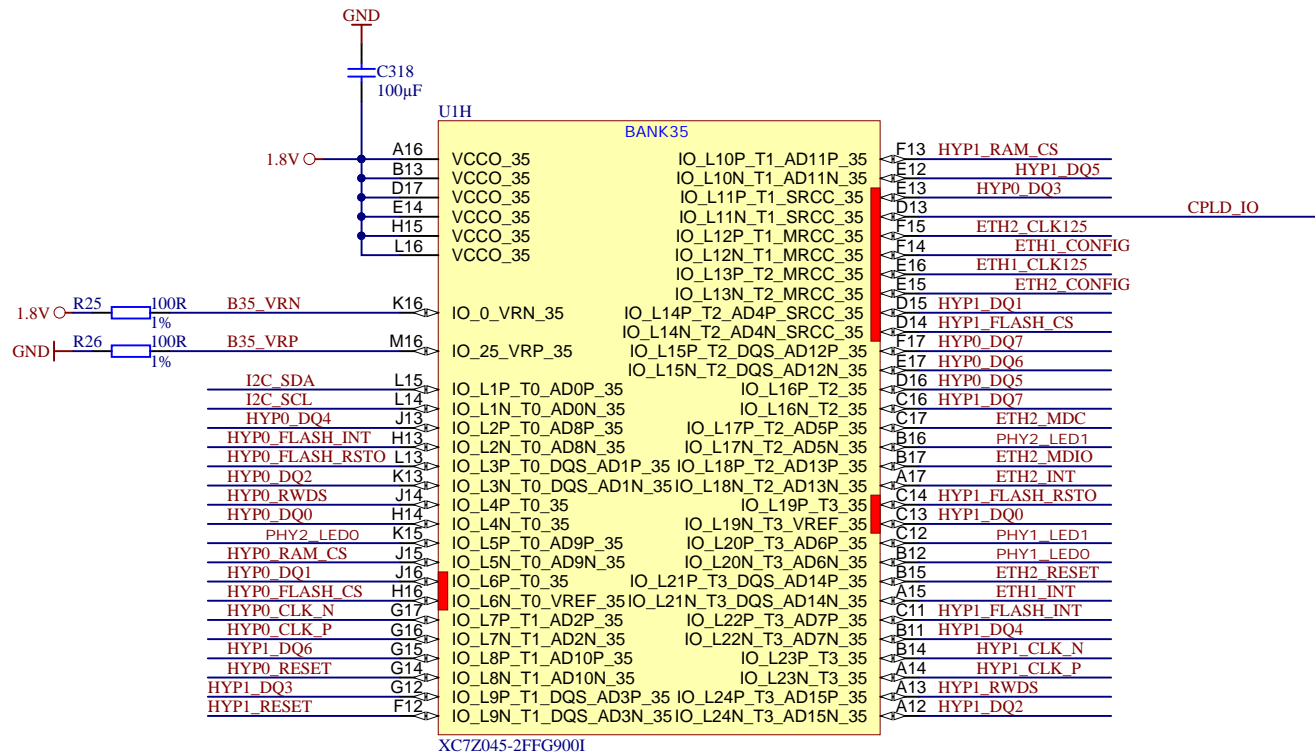
B33
 ClassName: B33
 ClassName: D100

	Title: TE0782 - FPGA B33		
	A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
	Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 17 of 31
	Filename: B33.SchDoc		

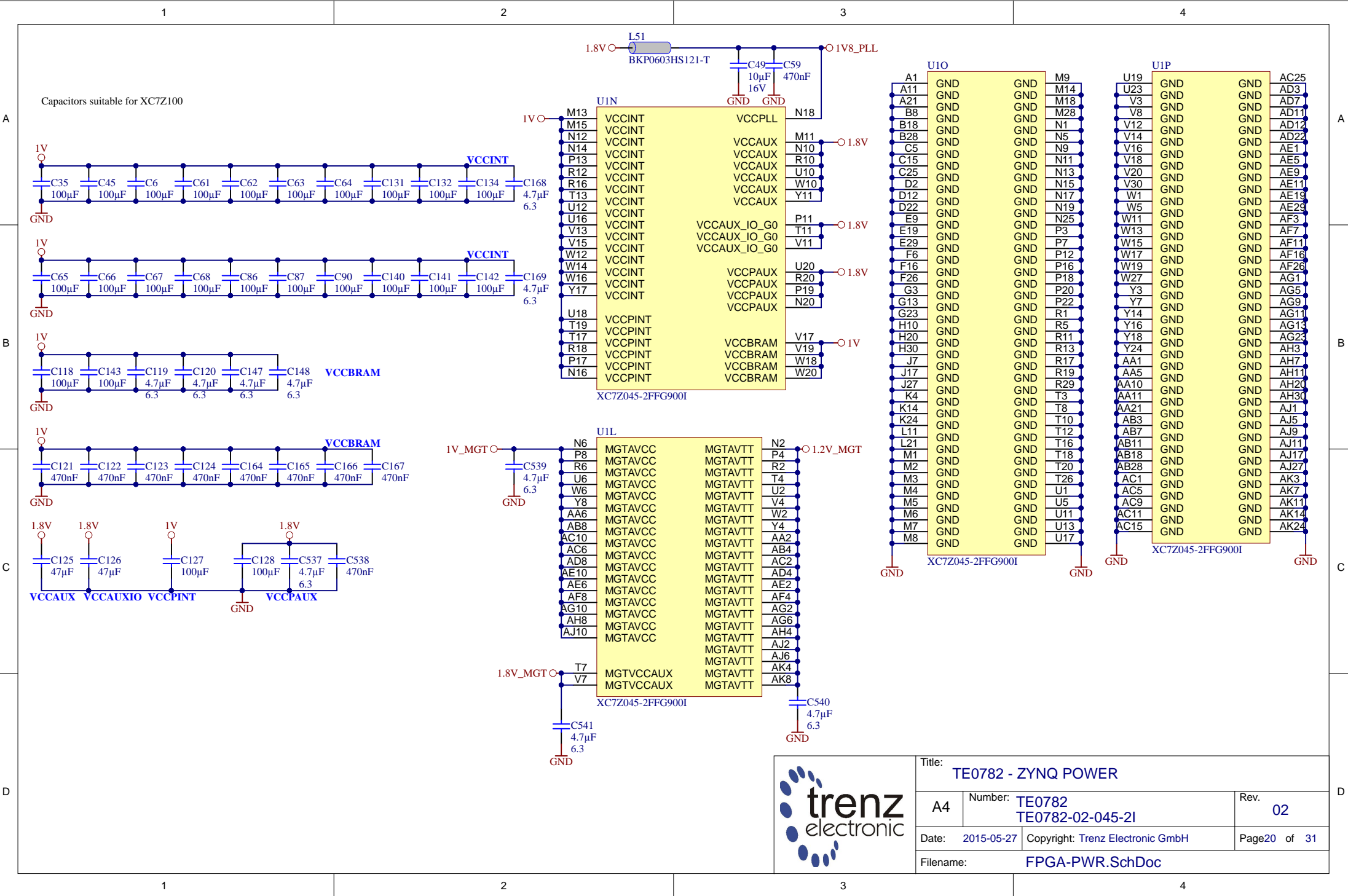
TP3
 VCCIO_34
 Testpoint 0.8mm



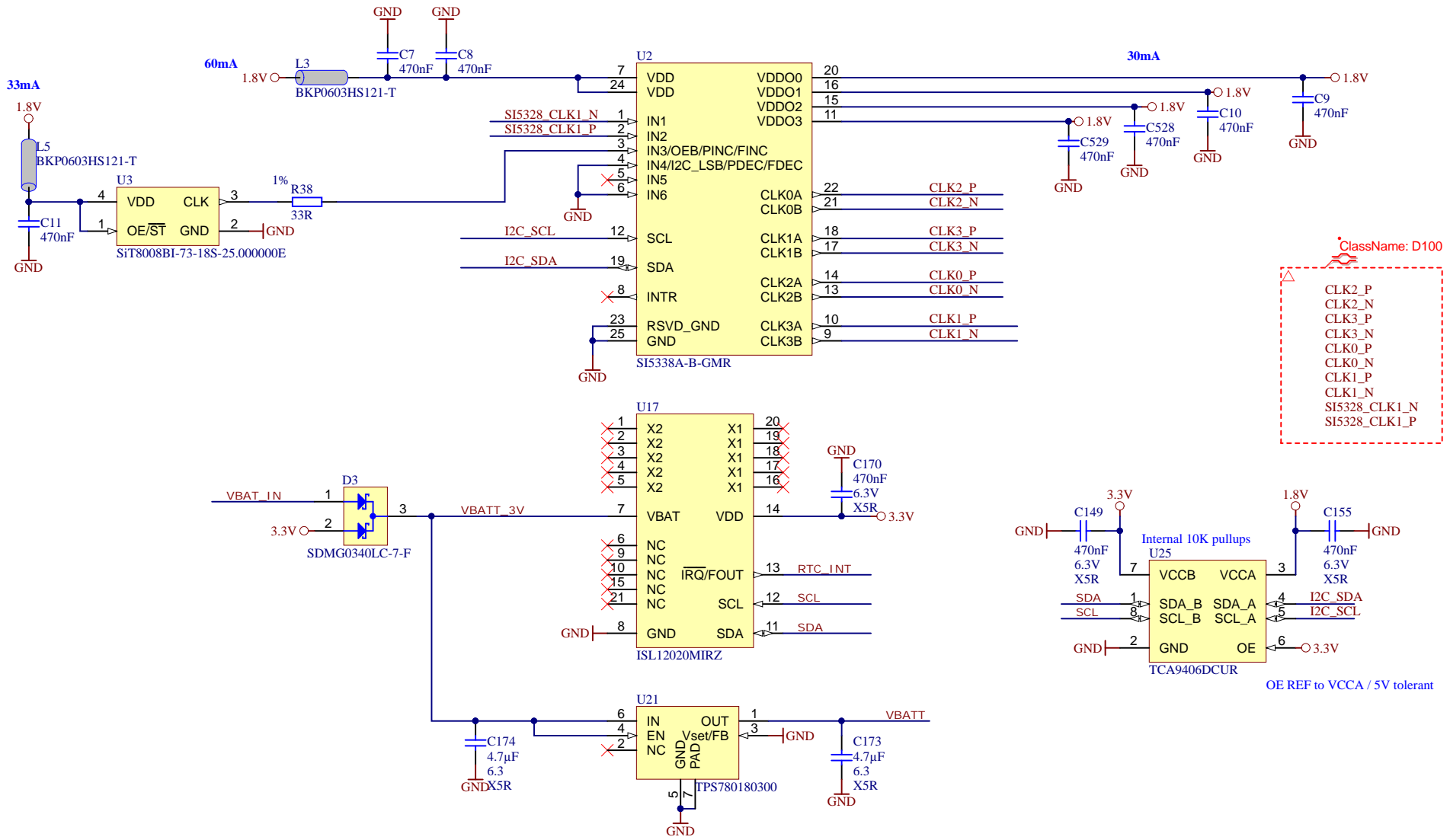
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A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 18 of 31
Filename: B34.SchDoc		



Title: TE0782 - FPGA B35		
A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 19 of 31
Filename: B35.SchDoc		



Title: TE0782 - ZYNQ POWER		
A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 20 of 31
Filename: FPGA-PWR.SchDoc		



Title: TE0782 - Clock		
A4	Number: TE0782 TE0782-02-045-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page21 of 31
Filename: Clock.SchDoc		

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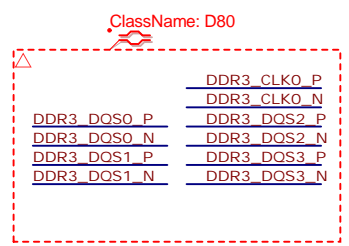
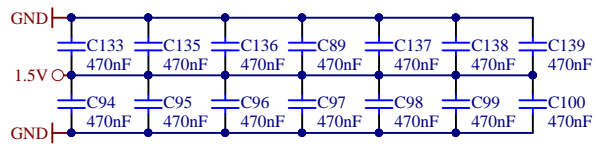
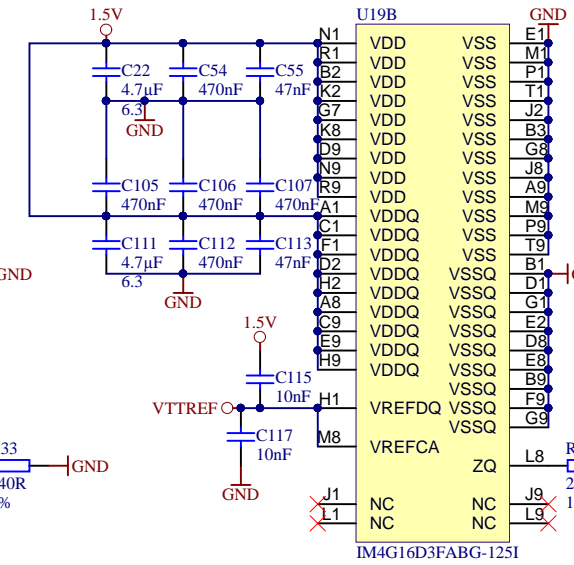
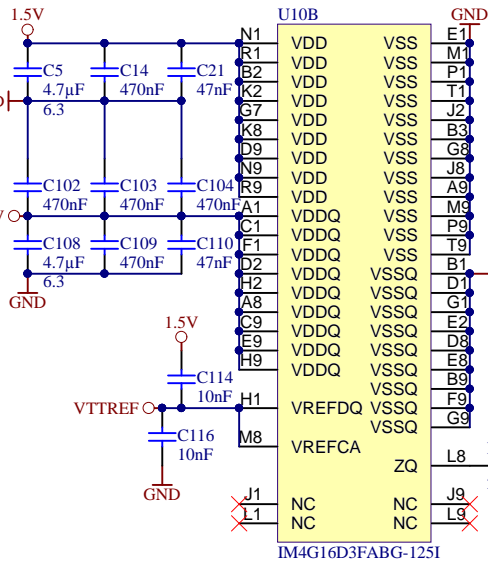
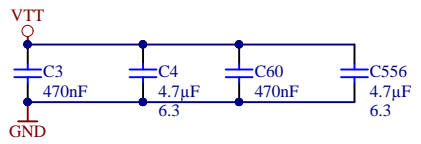
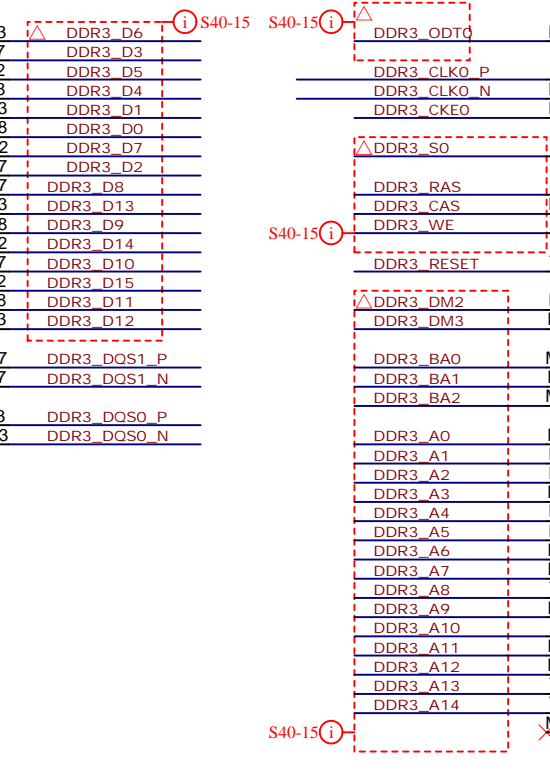
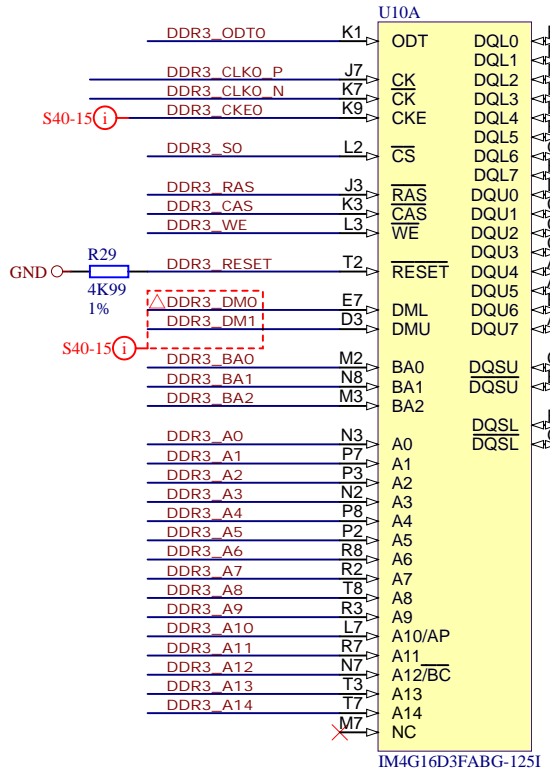
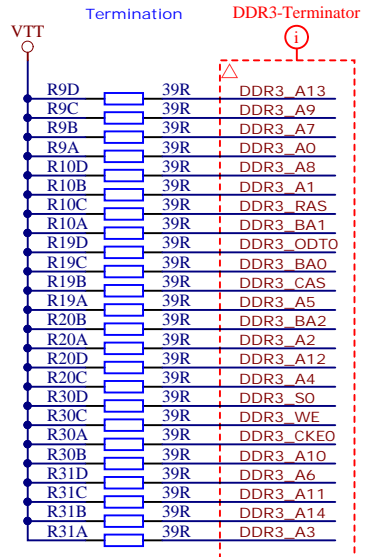
D

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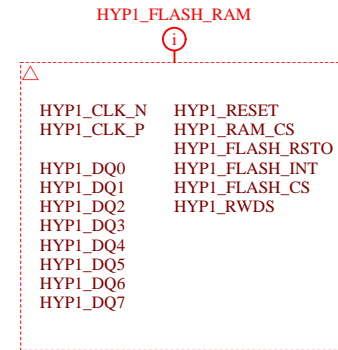
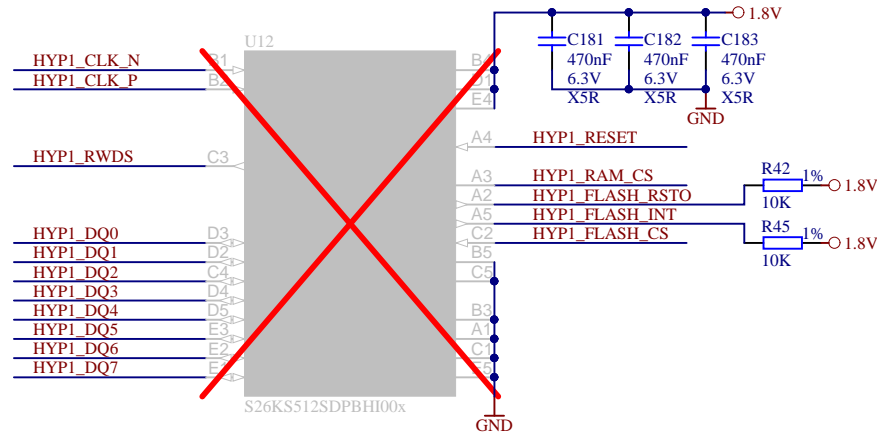
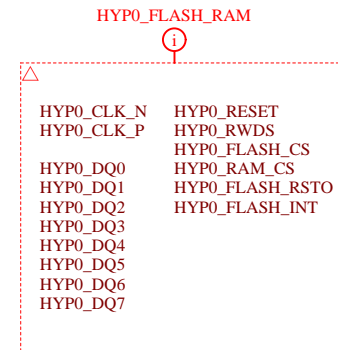
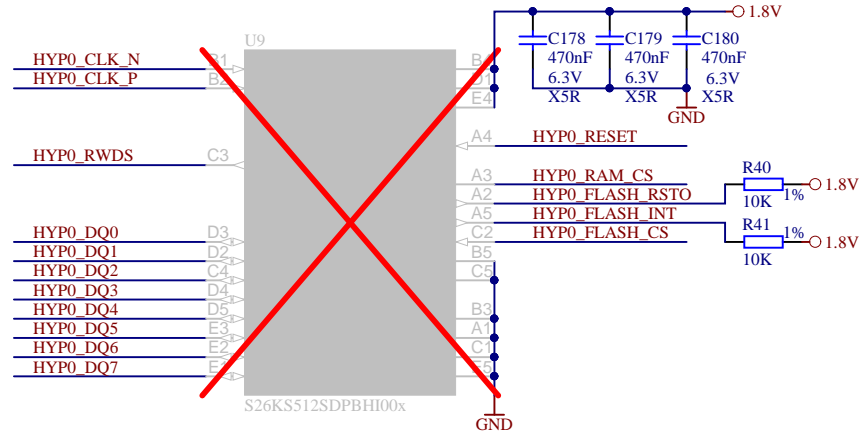
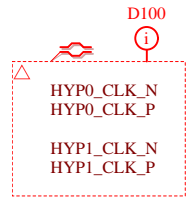
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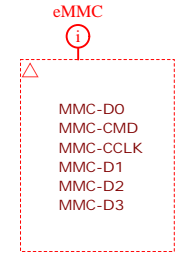
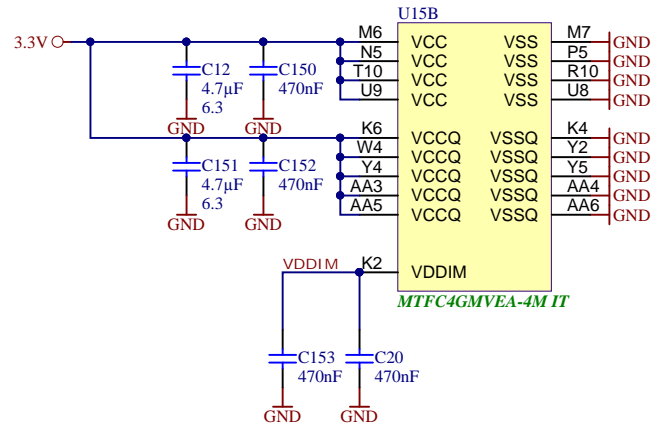
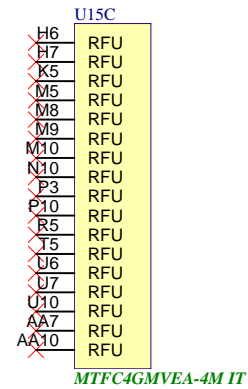
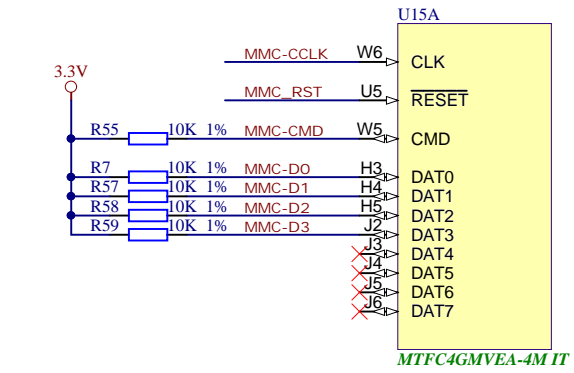
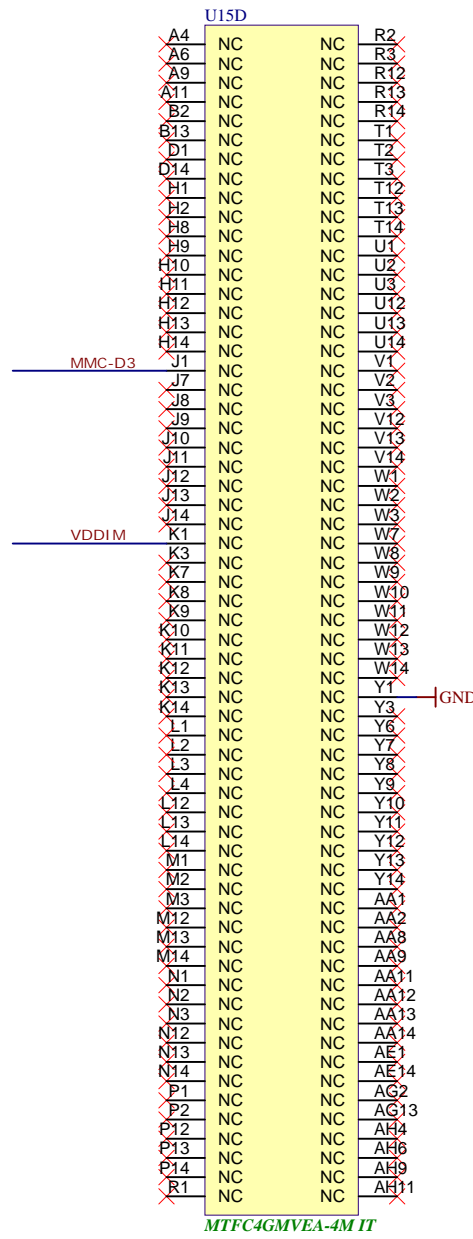
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Title: TE0782 - DDR3 RAM		
A4	Number: TE0782 TE0782-02-045-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 22 of 31
Filename: DDR3-RAM.SchDoc		

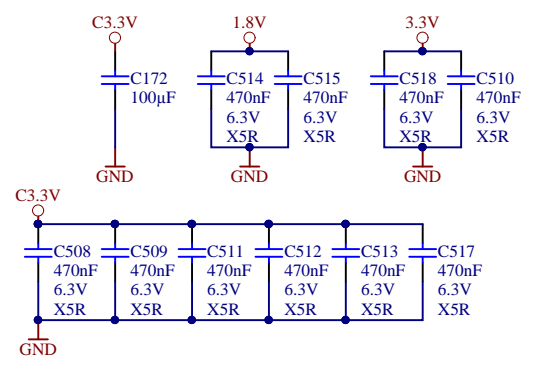
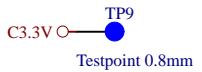
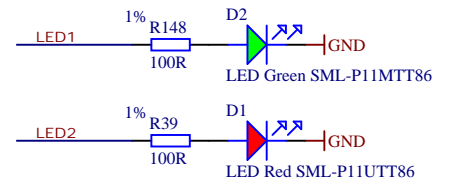
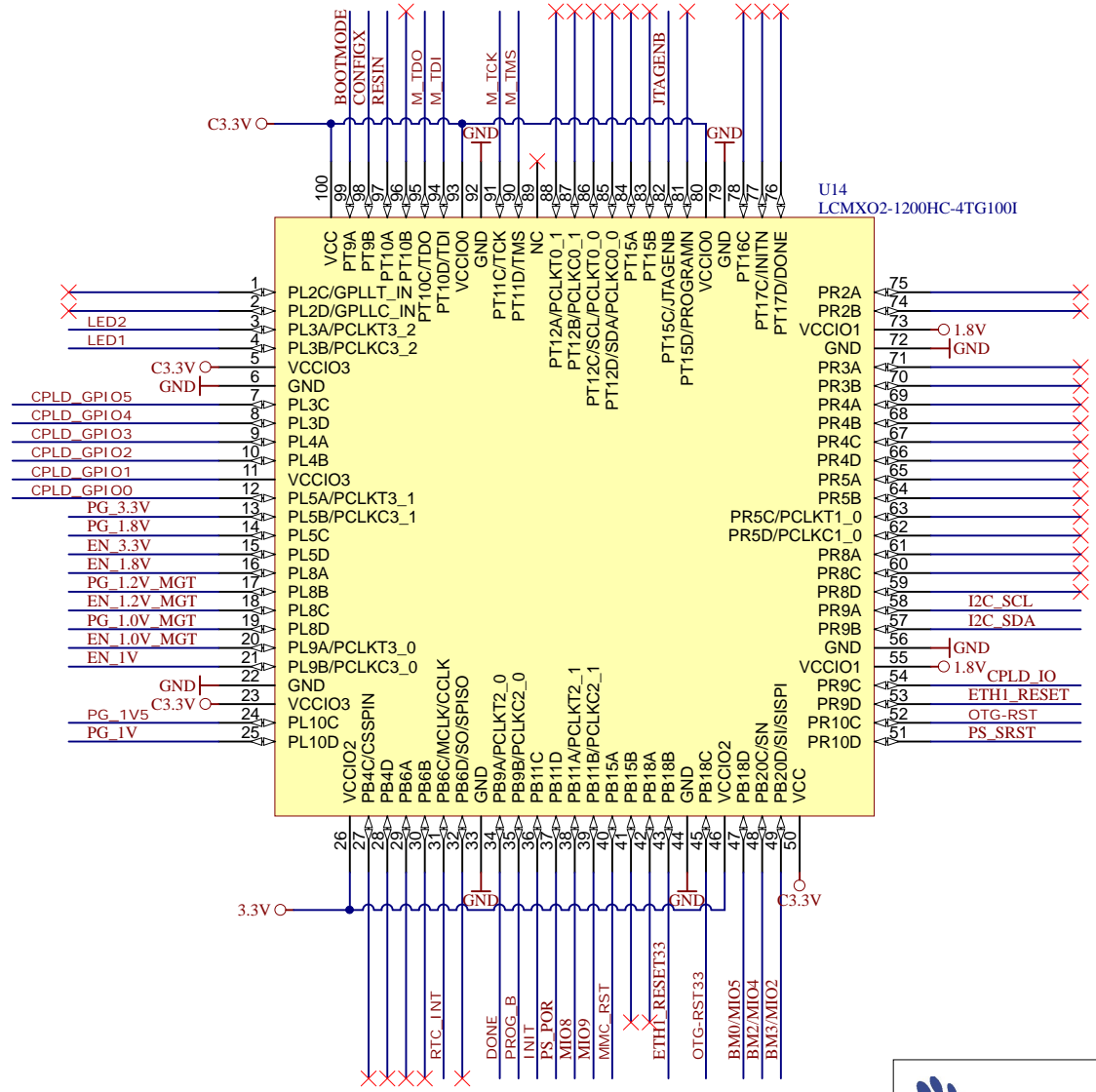


	Title: TE0782 - HyperFlash_RAM		
	A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
	Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page23 of 31
	Filename: HyperFlash_RAM.SchDoc		



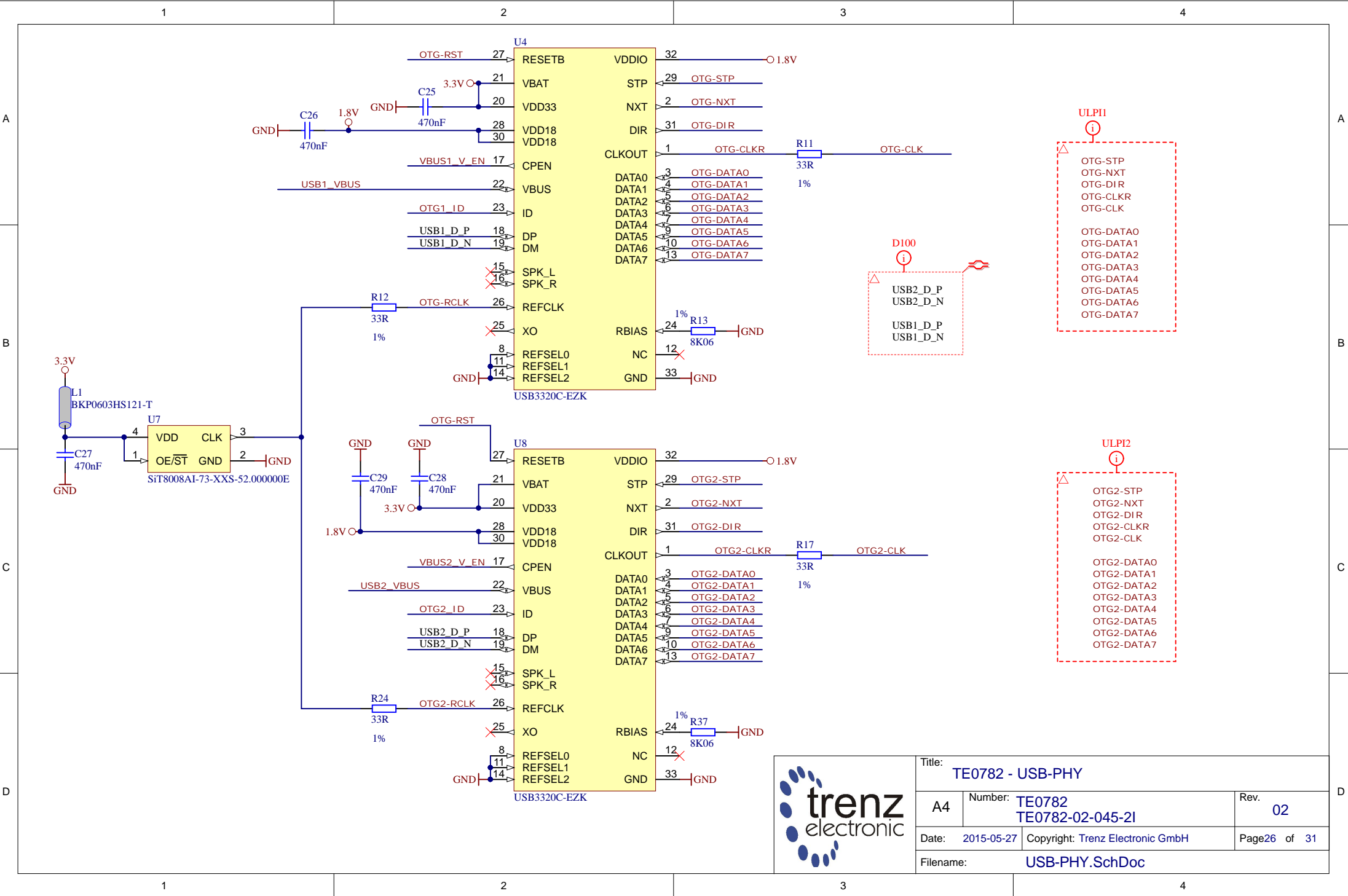
trenz electronic


Title: TE0782 - eMMC		
A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page24 of 31
Filename: eMMC.SchDoc		



Title: TE0782 - CPLD		
A4	Number: TE0782 TE0782-02-045-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 25 of 31
Filename: CPLD.SchDoc		





			Title: TE0782 - USB-PHY	
			A4	Number: TE0782 TE0782-02-045-21
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 26 of 31
Filename: USB-PHY.SchDoc				

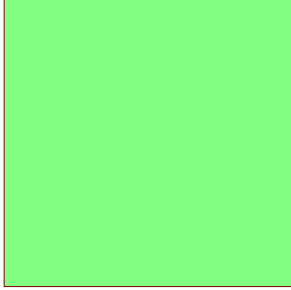
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2

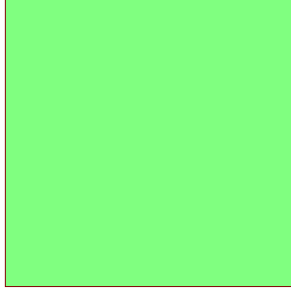
3

4

U_ETH1
ETH1.SchDoc



U_ETH2
ETH2.SchDoc



A

A

B

B

C

C

D

D



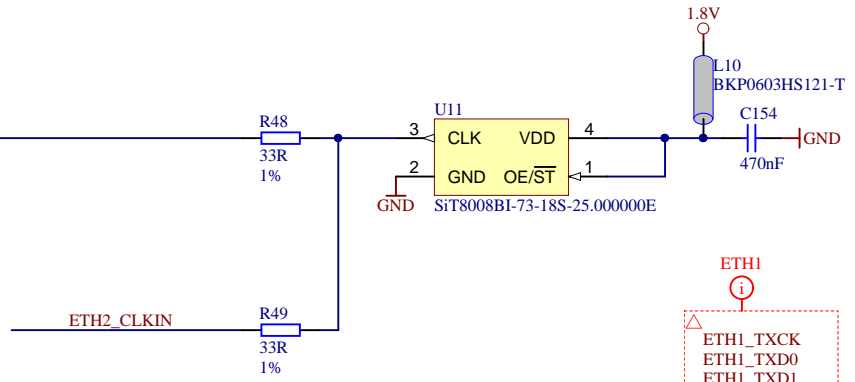
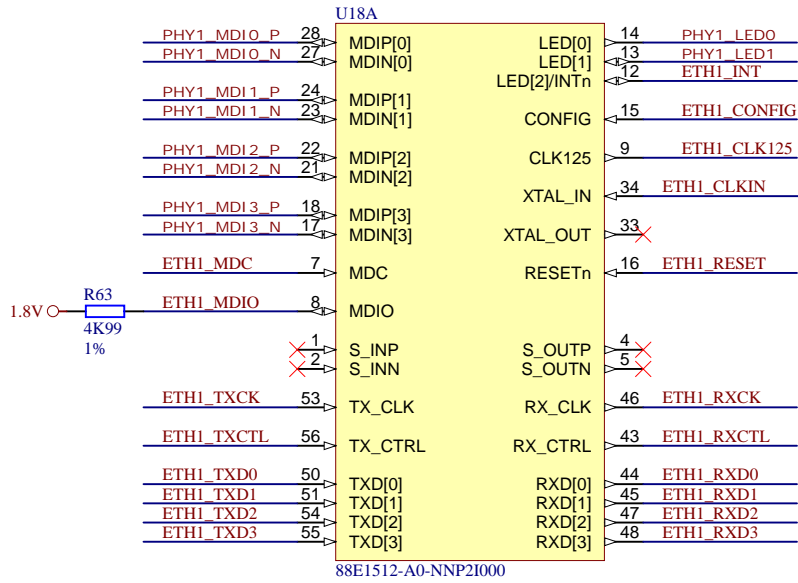
Title: TE0782 - Ethernet		
A4	Number: TE0782 TE0782-02-045-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 27 of 31
Filename: Ethernet.SchDoc		

1

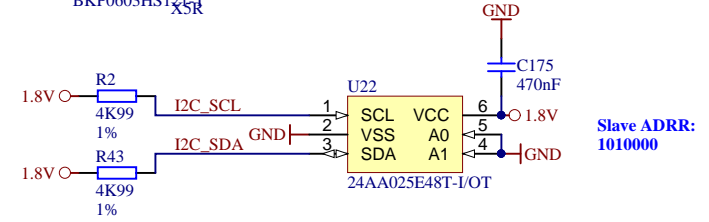
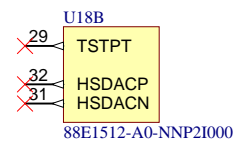
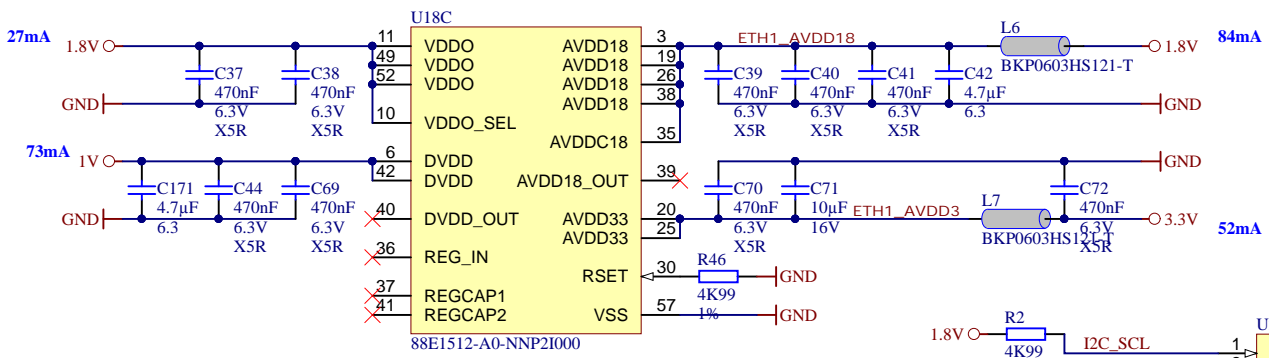
2

3

4



- ETH1**
- ETH1_TXCK
 - ETH1_TXD0
 - ETH1_TXD1
 - ETH1_TXD2
 - ETH1_TXD3
 - ETH1_TXCTL
 - ETH1_RXCK
 - ETH1_RXD0
 - ETH1_RXD1
 - ETH1_RXD2
 - ETH1_RXD3
 - ETH1_RXCTL
 - ETH1_MDC
 - ETH1_MDIO
- PHY1_LED0
PHY1_LED1
ETH1_INT
ETH1_CONFIG
ETH1_CLK125
ETH1_RESET



			Title: TE0782 - ETH_PHY1	
			A4	Number: TE0782 TE0782-02-045-21
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Filename: ETH1.SchDoc				

1

2

3

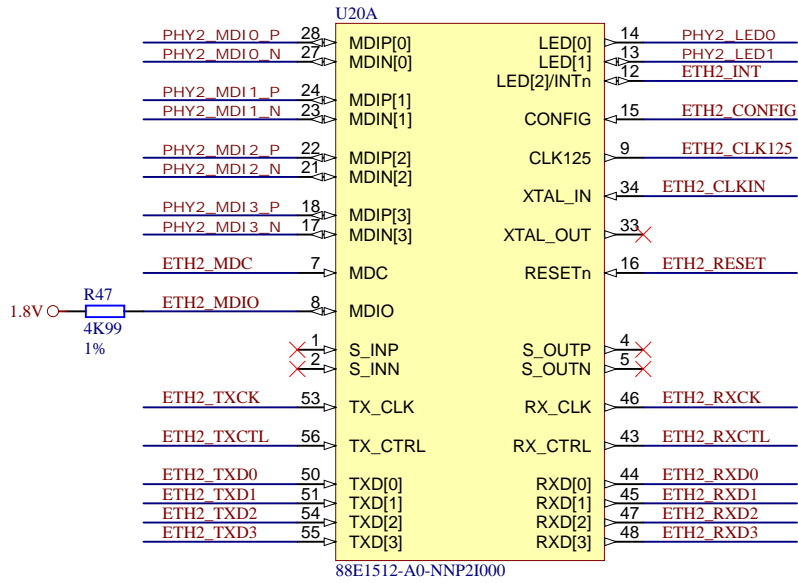
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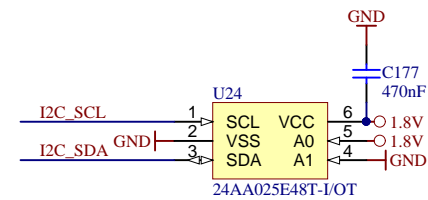
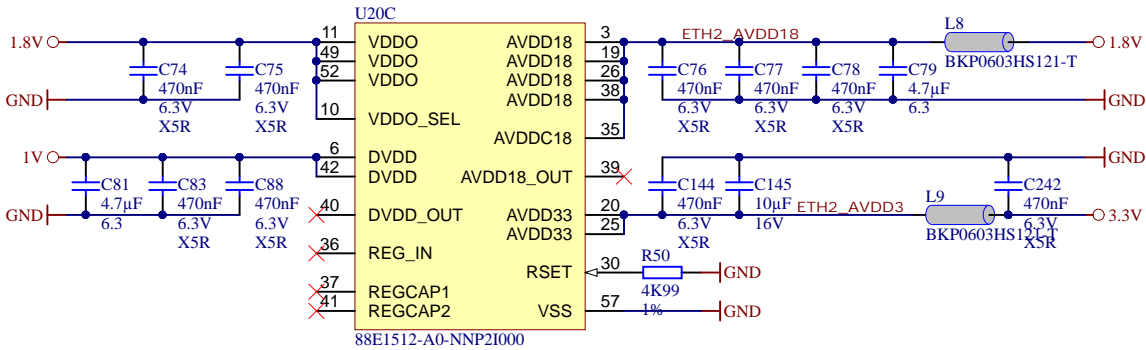
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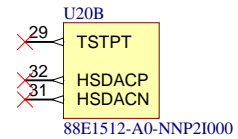
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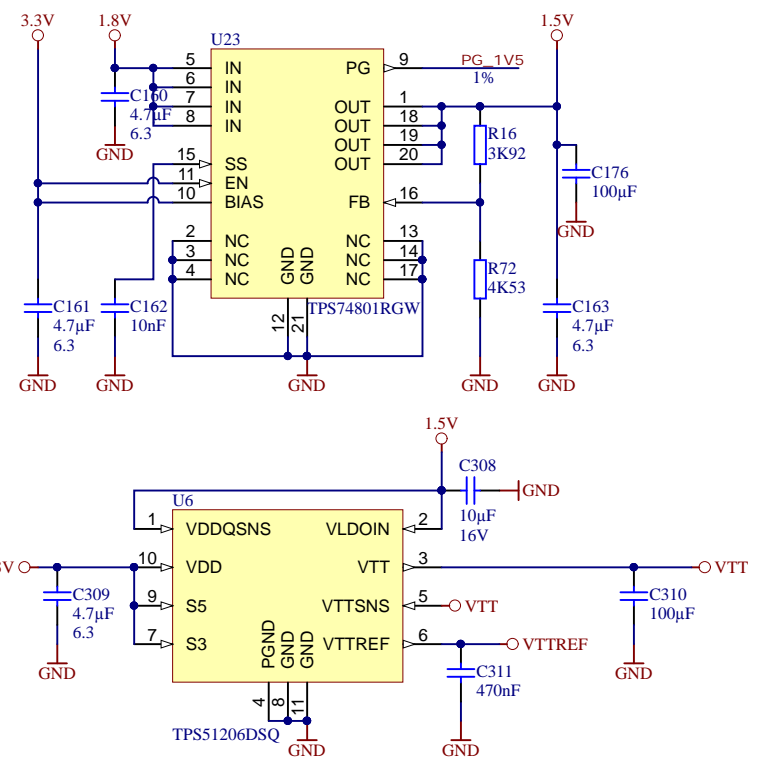
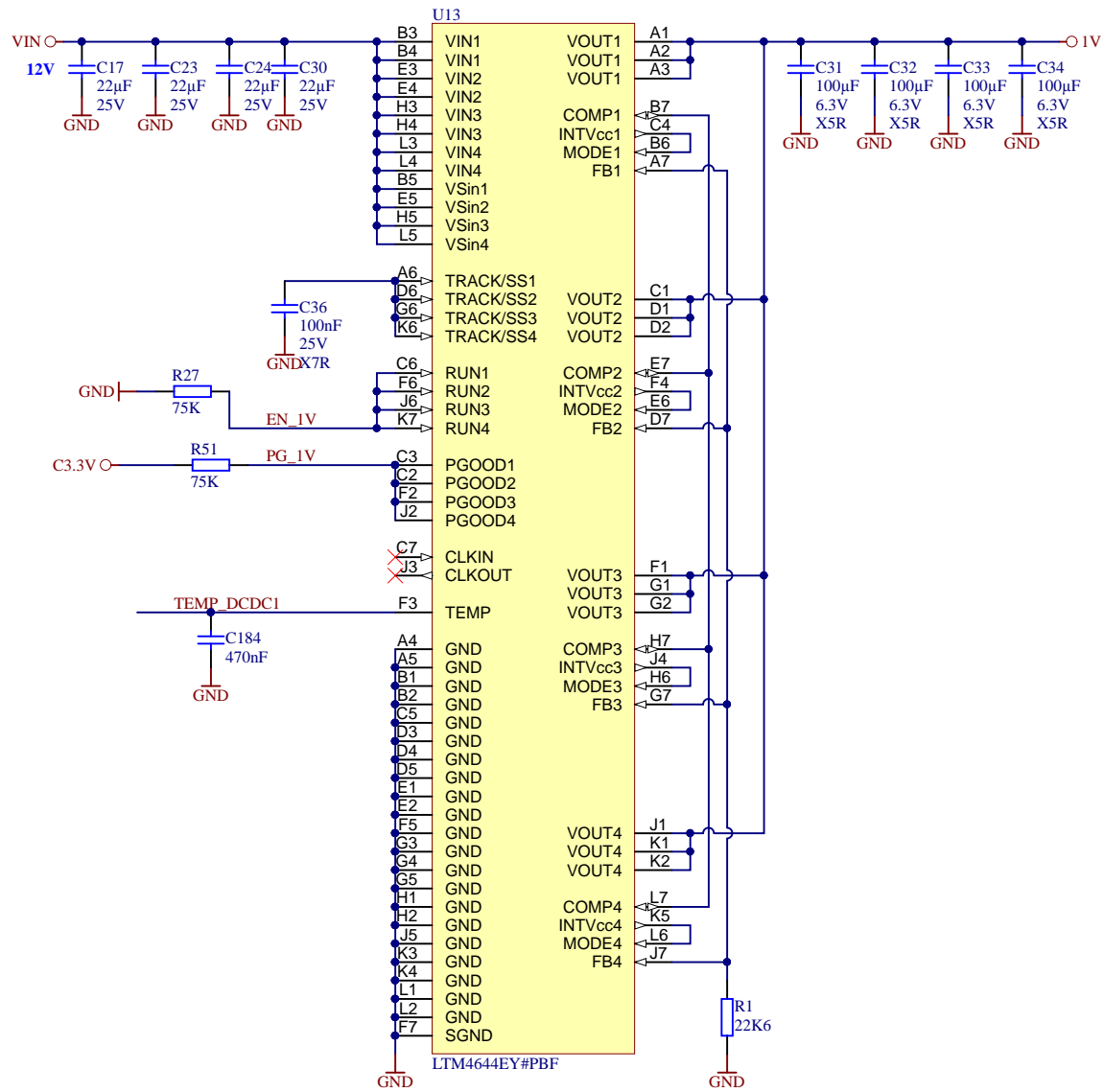
- ETH2**
- ETH2_TXD1
 - ETH2_TXD0
 - ETH2_TXCTL
 - ETH2_TXCK
 - ETH2_RXCK
 - ETH2_RXD1
 - ETH2_RXD3
 - ETH2_TXD2
 - ETH2_RXD3
 - ETH2_RXD2
 - ETH2_RXD0
 - ETH2_RXCTL
 - ETH2_MDC
 - ETH2_MDIO
- PHY2_LED0
PHY2_LED1
ETH2_INT
ETH2_CONFIG
ETH2_CLK125
ETH2_RESET



Slave ADDR:
1010001



	Title: TE0782 - ETH_PHY2		
	A4	Number: TE0782 TE0782-02-045-21	Rev. 02
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	Filename: ETH2.SchDoc		



- TP7 1V ○ ● Testpoint 0.8mm
- TP8 GND ○ ● Testpoint 0.8mm
- TP10 1.5V ○ ● Testpoint 0.8mm
- TP11 VTT ○ ● Testpoint 0.8mm
- TP12 VTTREF ○ ● Testpoint 0.8mm

Title: TE0782 - POWER		
A4	Number: TE0782 TE0782-02-045-21	Rev. 02
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Filename: POWER.SchDoc		

1

2

3

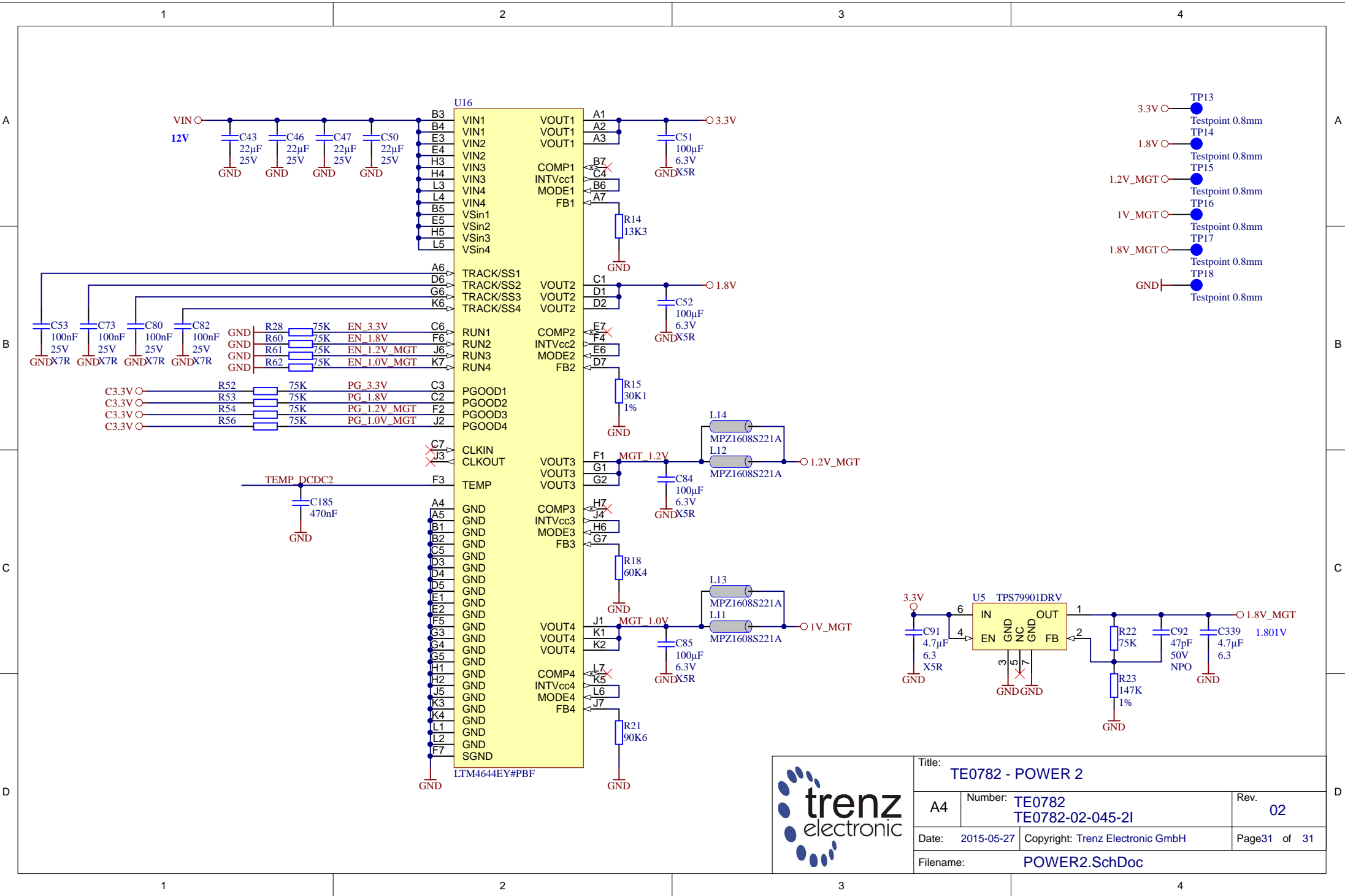
4

1

2

3

4



- 3.3V ○ TP13 Testpoint 0.8mm
- 1.8V ○ TP14 Testpoint 0.8mm
- 1.2V_MGT ○ TP15 Testpoint 0.8mm
- 1V_MGT ○ TP16 Testpoint 0.8mm
- 1.8V_MGT ○ TP17 Testpoint 0.8mm
- GND ○ TP18 Testpoint 0.8mm



Title: TE0782 - POWER 2		
A4	Number: TE0782 TE0782-02-045-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 31 of 31
Filename: POWER2.SchDoc		