Audio Application Kit

For AURIX™ lite Kit V2

Document Revision 1.0

Kit User's Manual

Revision 2021-12-15

Microcontroller

Edition 15. December, 2021

Published by

Infineon Technologies AG

81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History		
Page or Item	**Subjects (major changes since previous revision)**	**Author**
Revision V1.0 2021, December	Initial released Version is V1.0	Markus Noll

Table of Contents

1 Introduction

This document describes the features and hardware details of the **AURIX™ Audio Application Kit** consisting of two boards (**Audio Shield Board** and **Microphone Array Board**). Detailed information is provided on the board's content, layout and use.

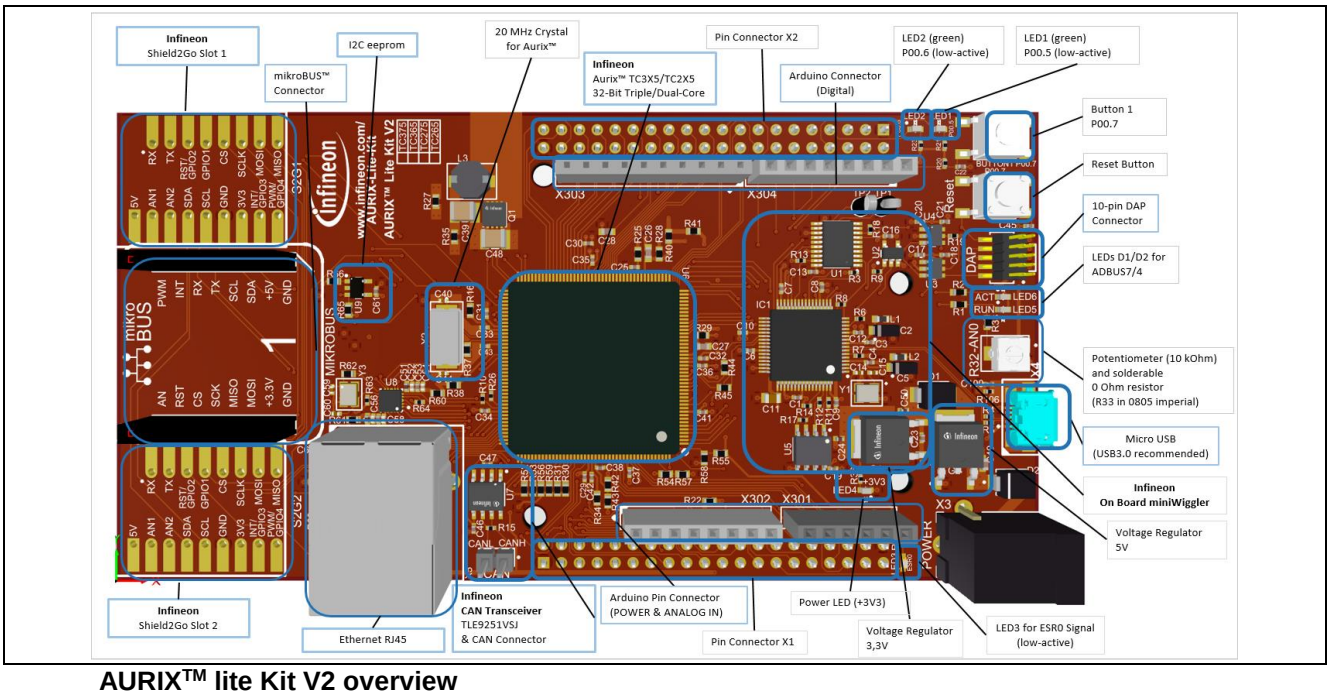
Due to the flexibility and the featureset of the **AURIX™ Audio Applikation Kit** in combination with the **AURIX™ lite Kit V2**, a lot of audio applications can be evaluated such as e.g.

- Generic I²S / TDM interfacing
- PDM microphone interfacing (software or hardware based PDM decimation)
- Audio DSP processing
- Sound Generation
- IP-Audiostreaming
- Realtime synchronized Audio over Ethernet (e.g. AVB, AES67)
- Microphone Beamforming
- Audio Playback / Recording from / to external SD card using mikroBUS™ extension shield
- Voice recognition / Hot-Word detection
- Smart Speaker
- Siren detection

The **AURIX™ Audio Application Kit** must be used together with an **AURIX™ lite Kit V2** (with SAK-TC375TP-96F300W) and is not operational on its own or with other microcontroller-kits.

While the **Audio Shield Board** can be used stand-alone together with the **AURIX™ lite Kit V2**, the **Microphone Array Board** additionally needs the **Audio Shield Board** for operation.

The **AURIX™ lite Kit V2** is a low-cost evaluation-board for the SAK-TC375TP-96F300W microcontroller and features an integrated debugger as well as Ethernet-Connectivity which makes it interesting especially for networked applications.



AURIX™ lite Kit V2 overview

Specification overview - Audio Shield Board

Devices	Audio Amplifier	Infineon MERUS™ MA12070P
	Microphones	Infineon XENSIV™ IM67D120A (AEC-Q103 qualified)
	Power Supply	Infineon OPTIREG™ TLS4120D0EPV Infineon OPTIREG™ TLS205B0LDV50 Infineon OPTIREG™ TLS205B0LDV33 Infineon OPTIREG™ TLS202A1MBV
	Audio Codec	NXP SGTL5000
	Audio PLL	Cirrus Logic CS2000CP-CZZ
	Reference Oscillator	ECS 7050MV-245.7-BN-TR (24.576 MHz)
Board Dimensions	68.5 x 53.3 mm	

Power	• Selectable Power Supply
	  ○ 3.3V supply from **AURIX™ lite Kit V2** (all functions available except audio amplifier)
	  ○ 12V to 24V input (all functionalities available)	

Connectors	• Audio Input - 3.5 mm Stereo Jack • Headphones Output – 3.5 mm Stereo Jack • Power Supply Input – 5.0 mm Screw Terminal (26 ... 14 AWG) • Stereo Audio Amplifier Output - 5.0 mm Screw Terminal (26 ... 14 AWG)	
Others	• Reverse Polarity Protection for external power supply input • Reverse power supply of **AURIX™ lite Kit V2** (when external power supply is used) • Reference Clock Mux • Additional unassembled Audio Line Output	

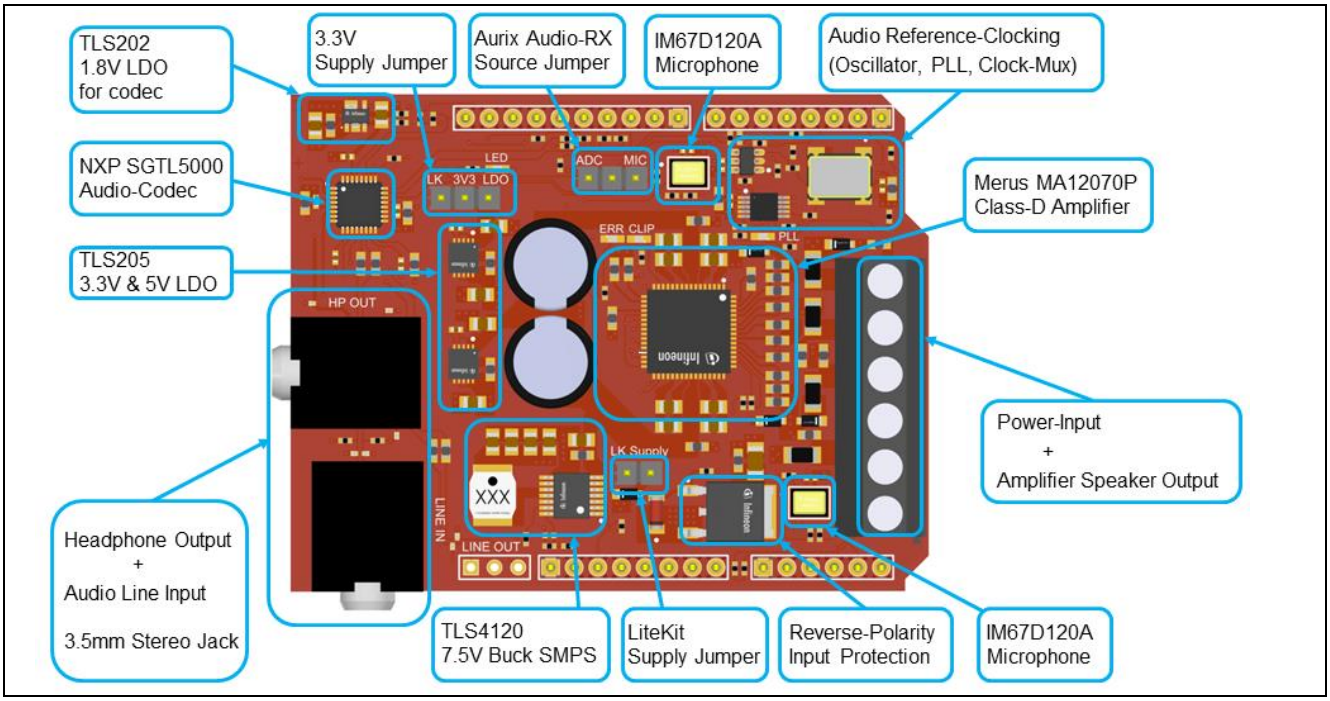
Specification overview - Microphone Array Board

Devices	Microphones	Infineon XENSIV™ IM67D120A (AEC-Q103 qualified)
	Clock Distribution	Texas Instruments LMK1C1108
Board Dimensions	131.0 x 66.04 mm	
Power	3.3V supply from **AURIX™ lite Kit V2**	
Others	• 12 LEDs in a 360° circle arrangement • 3 generic status LEDs	

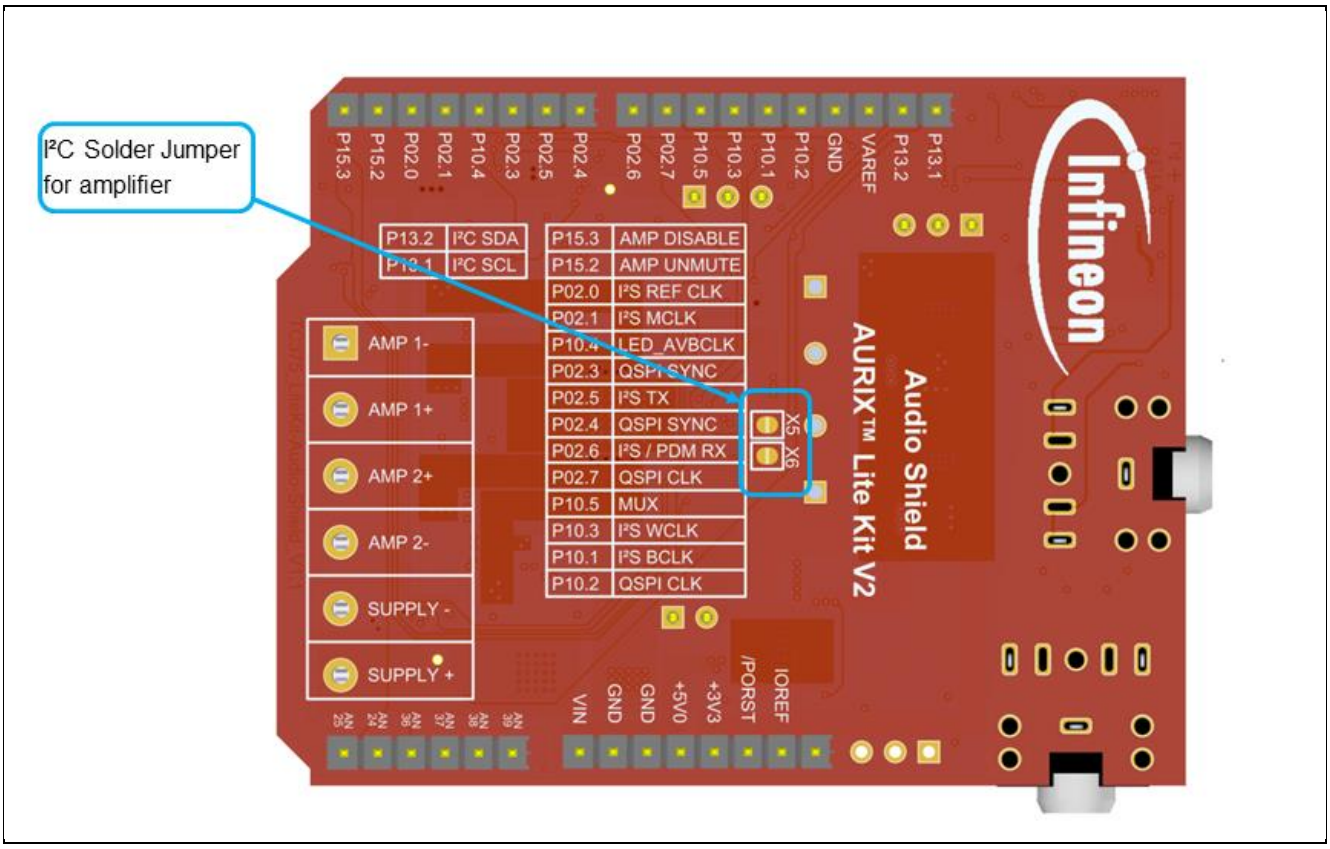
Info: These boards are neither cost nor size optimized and do not serve as a reference design.

2 Hardware Description

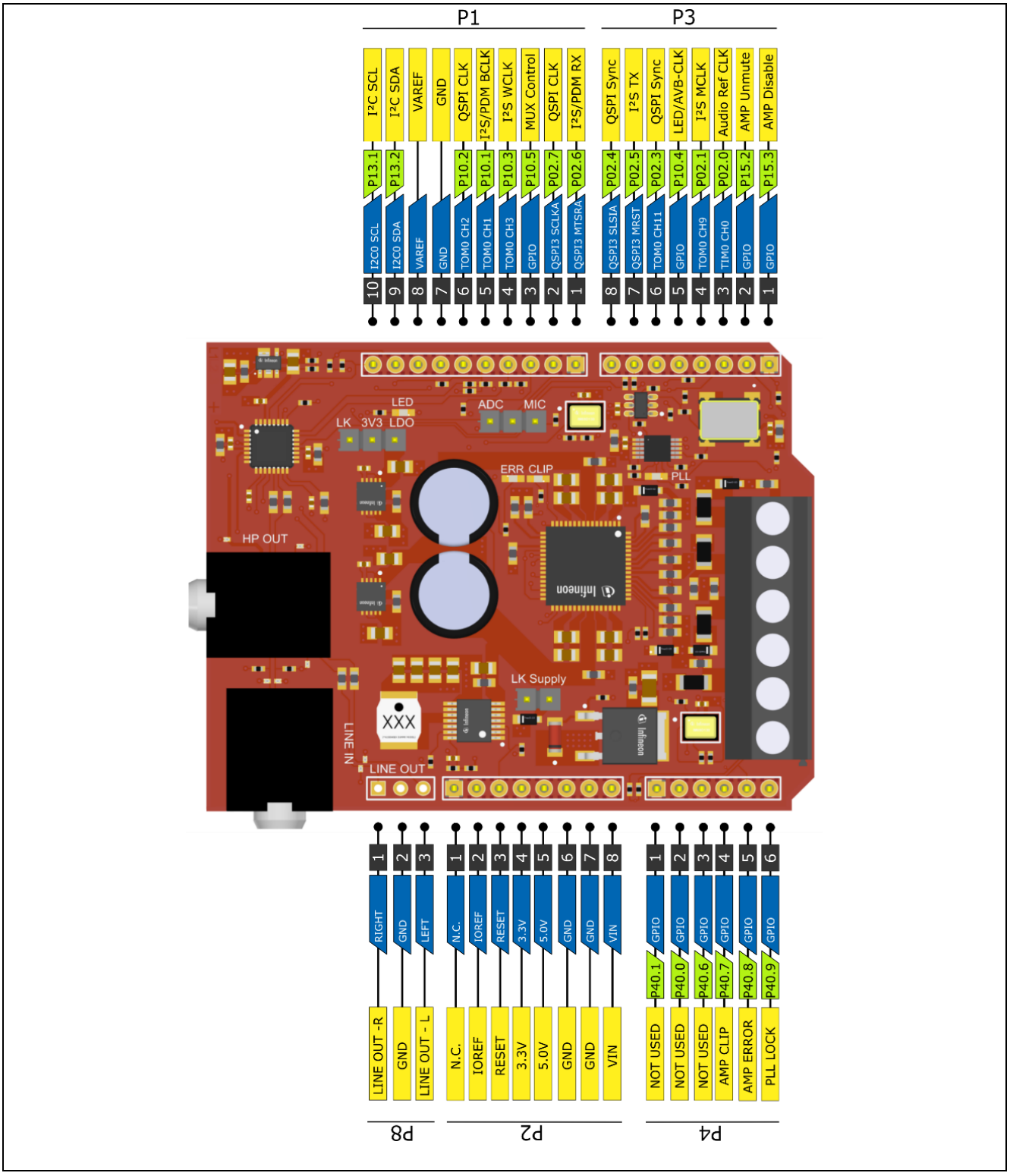
2.1 Audio Shield Board



Audio Shield Board - Top View



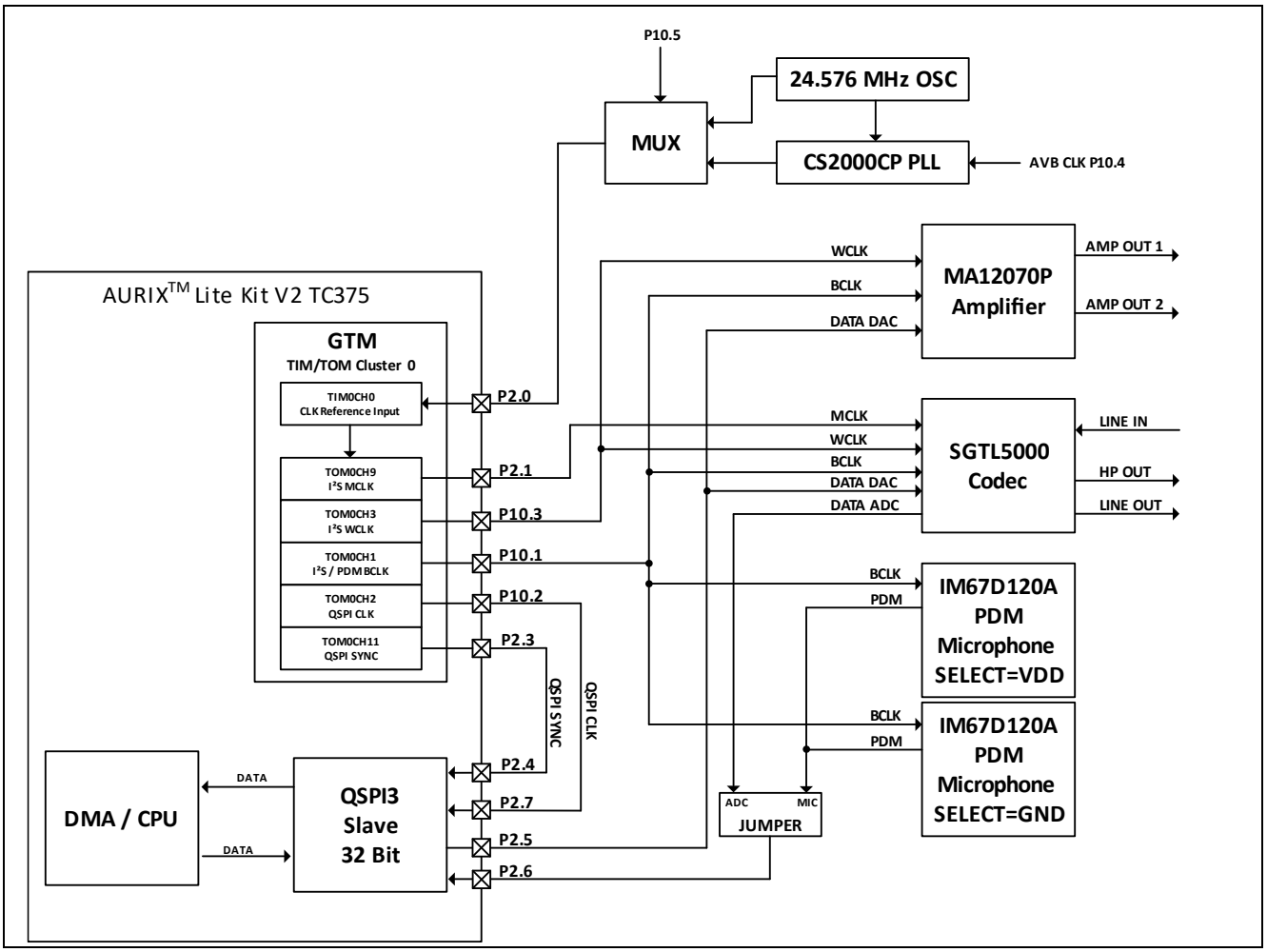
Audio Shield Board - Bottom View



Audio Shield Board - Pinout Overview

2.1.1 System Concept

2.1.1.1 I²S Emulation



Audio Shield Board concept with I²S emulation

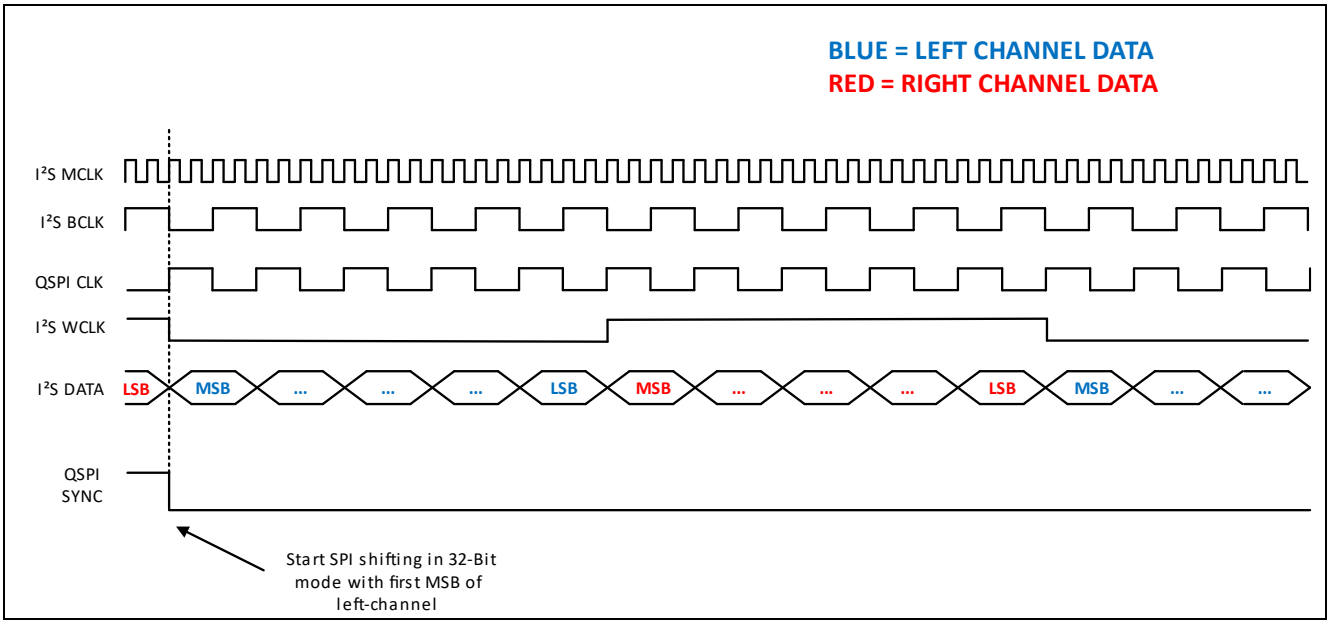
AURIX™ TC3xx family doesn't have a native I²S / TDM interface. However, the interface can be emulated by using the Q(ueued)-SPI module in slave-operation together with the GTM as clock generator. Overall, this emulates an I²S / TDM master interface on system level. An external Audio Reference Clock is used to drive the audio-clocking domain.

The reference clock is injected into a GTM cluster via a TIM (Timer Input Module) which is clocking an array of TOMs (Timer Output Module). Those are dividing the input clock in order to generate e.g. WCLK, BCLK, MCLK, etc.

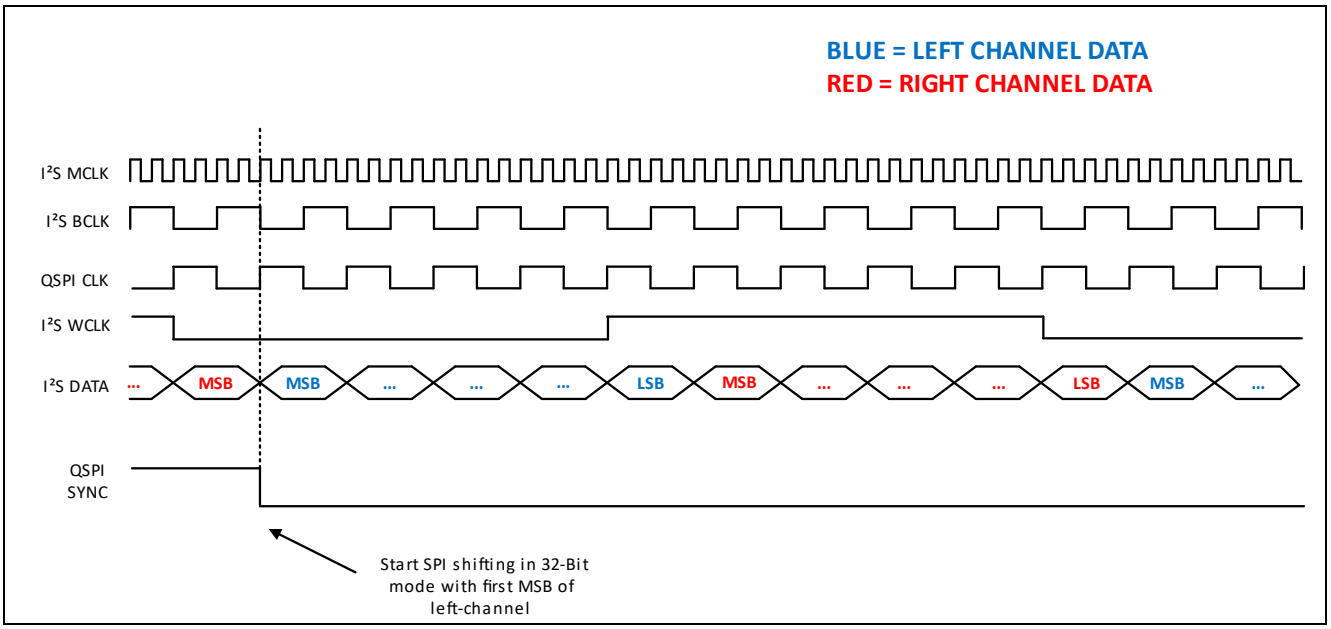
As the QSPI module supports slave-operation with CPOL=1 only, an inverted clock (in relation to BCLK) is needed to clock the QSPI module.
The QSPI's slave-select-input is connected to a TOM in one-shot timer mode. This TOM will generate a single high-to-low transition synchronized with the first MSB of the I²S data word.

Depending if a Standard-I²S or LeftJustified-I²S protocol is desired, this pulse can be shifted back and forth to synchronize to the MSB at various positions.

As the period-times but also the duty-cycles of all TOMs are freely configurable, almost any audio-interface configuration (I²S, TDM, AC'97) is possible.



LeftJustified-I²S Emulation Timing Diagram



Standard-I²S Emulation Timing Diagram

In most cases, MCLK=256*f_s and BCLK=64*f_s. Consequently, the various clock-frequencies could look like in following table (depending what sample-rate was configured and considering that a 2*32 Bit transmission is used).

	TOM divider	44.1 kHz	48 kHz	88.2 kHz	96 kHz
Reference-CLK	-	22.5792 MHz	24.587 MHz	45.1584 MHz	49.152 MHz
I²S – MCLK	2	11.2896 MHz	12.288 MHz	22.5792 MHz	24.576 MHz
I²S – BCLK	8	2.8224 MHz	3.072 MHz	5.6648 MHz	6.144 MHz
QSPI – CLK	8	2.8224 MHz	3.072 MHz	5.6648 MHz	6.144 MHz
I²S – WCLK	512	44.1 kHz	48 kHz	88.2 kHz	96 kHz

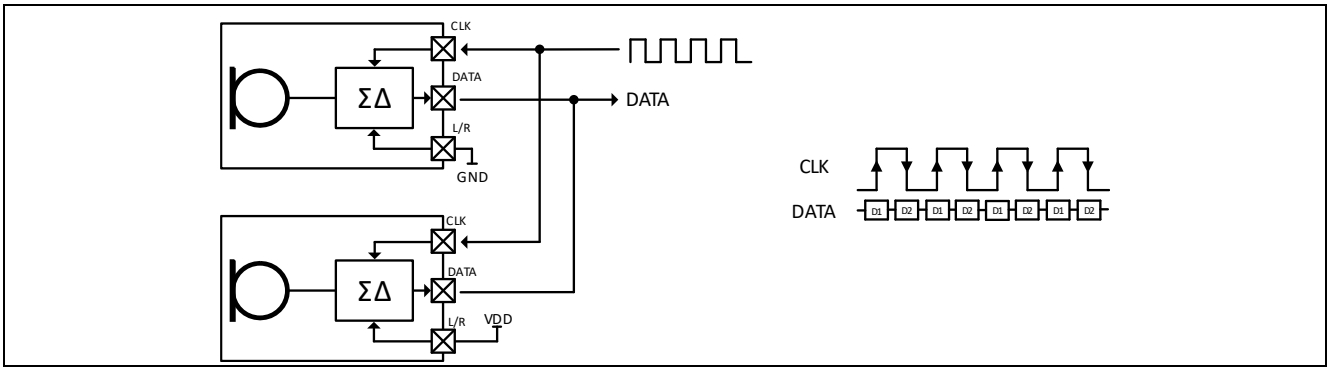
Example clock frequencies vs. Sample frequencies

The reference clock can be either generated by the CS2000CP-CZZ PLL in standalone clock-synthesizer mode or by the fixed 24.576 MHz oscillator and can be chosen by controlling the clock-multiplexer.

2.1.1.2 PDM microphone interfacing with software-based decimation

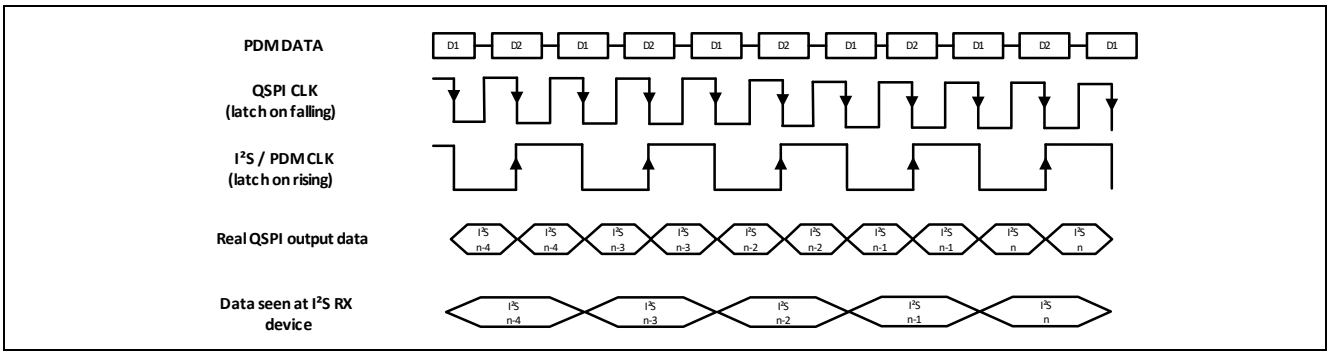
Due to the flexibility of this emulation concept, it is also possible to interface a Stereo-PDM (double-data-rate) stream and an I²S output simultaneously.

This is especially interesting for MEMS microphones in a stereo-setup configuration, where output data must be sampled on both rising- and falling edge of the global PDM-CLK.



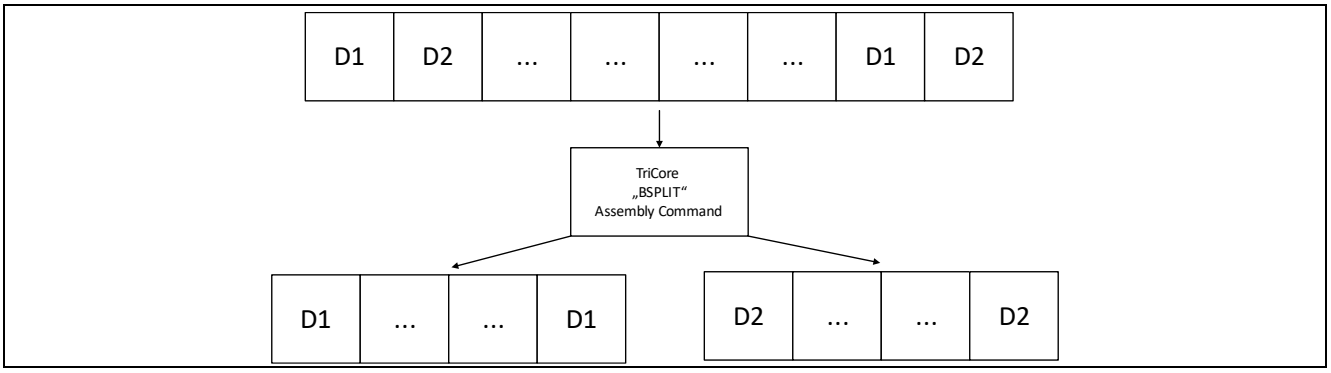
Stereo PDM Microphone Timing Diagram

In this case, the QSPI-CLK can be driven at double the frequency of the I²S-BCLK/PDM-CLK to latch both left- and right PDM bits.
On the same time, the QSPI can output a PCM-I²S data-stream related to the normal I²S-BCLK.

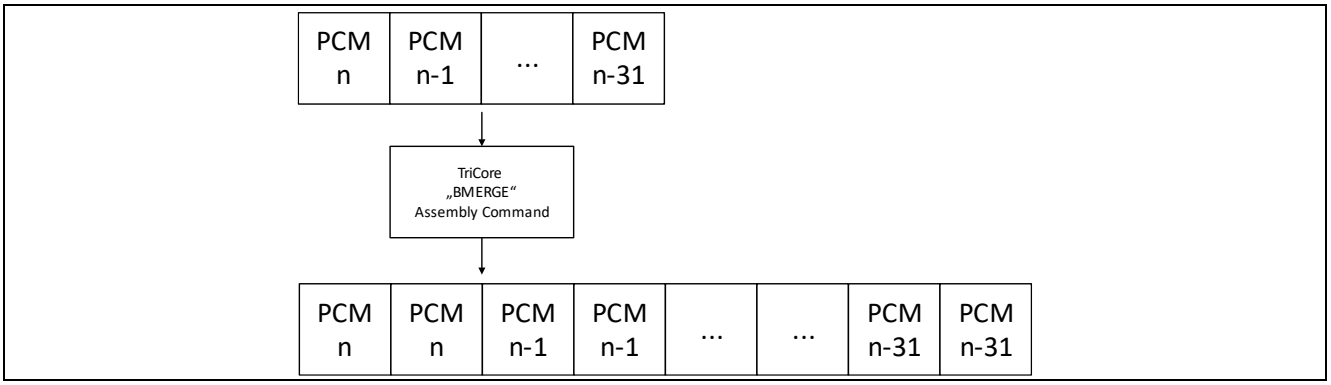


Stereo PDM Microphone Timing Diagram

Inside the TriCore, the interleaved PDM-stream can be efficiently restored into two separated PDM buffers using the “BSPLIT” assembly command. For the PCM output, where the single data-bits needs to be effectively doubled, the “BMERGE” command can be used.

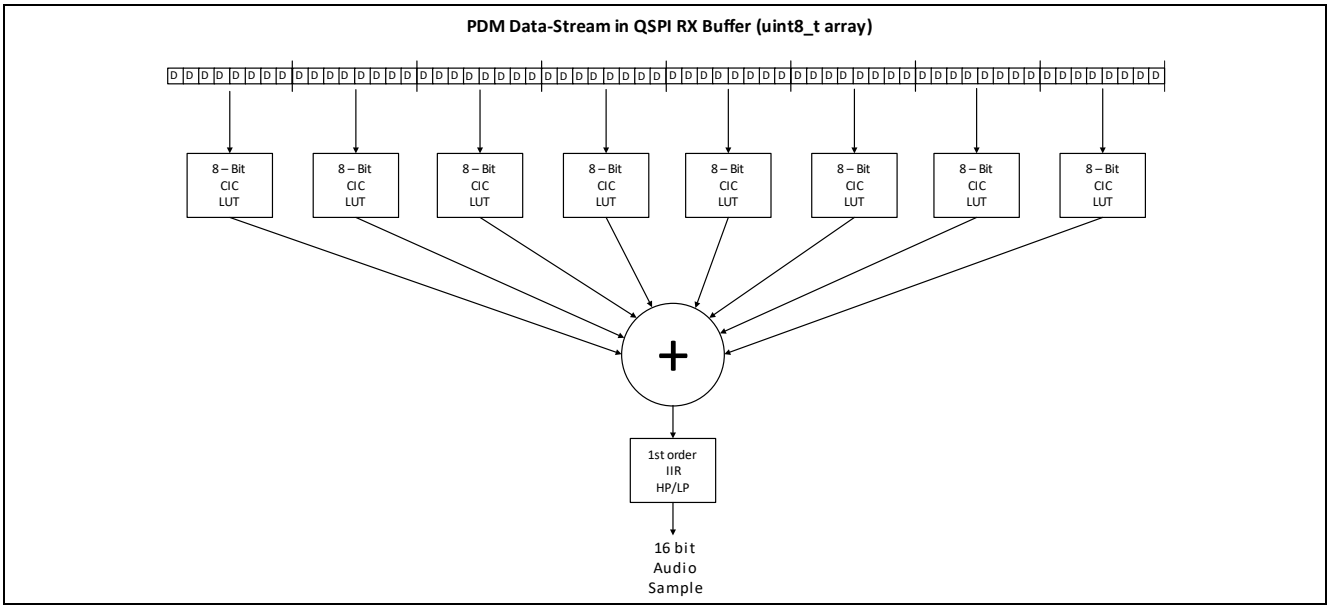


Recovering the interleaved PDM-stream into two separate buffers



Doubling up the PCM bits for double-data-rate QSPI output

After recovering the interleaved PDM stream, the PDM bits can be decimated/filtered into PCM samples. A decimation of e.g. 64 is quite common. There are various algorithms available to implement such a decimation. A possible software-based filter-structure could look like e.g. in following picture:



Possible PDM filter structure in software

For double-data-rate PDM interfacing, the CLK frequencies could look like following:

	TOM divider	24 kHz	48 kHz
Reference-CLK	-	12.288 MHz	24.576 MHz
I²S – MCLK	2	6.144 MHz	12.288 MHz
I²S – BCLK	8	1.536 MHz	3.072 MHz
QSPI – CLK	4	3.072 MHz	6.144 MHz
I²S – WCLK	512	44.1 kHz	48 kHz

Example clock frequencies vs. Sample frequencies for Stereo-PDM interfacing

2.1.2 Power Supply

The **Audio Shield Board** supports two different supply-modes.

2.1.2.1 Internal Supply

The board can be supplied from the 3.3V supply of the **AURIX™ lite Kit V2**. In this case, functionalities like microphones, clocking and audio codec are available. Only the audio-amplifier cannot be used in that case.

Needed jumper settings:

- 3V3 Supply Jumper: Set to “LK”
- LK Supply Jumper: Don’t care

2.1.2.2 External Supply

In case the audio-amplifier is needed, the board must be externally supplied with 12V to 24V through the supply-input on the screw-terminal.

Depending on the used loudspeaker-load and the needed amplifier-power, the power-supply should be able to deliver up to 6A peak-current at 24V.

Otherwise, the transient output power will be limited or worst-case leading to a system-reset due to detected undervoltage by the TLS4120 regulator.

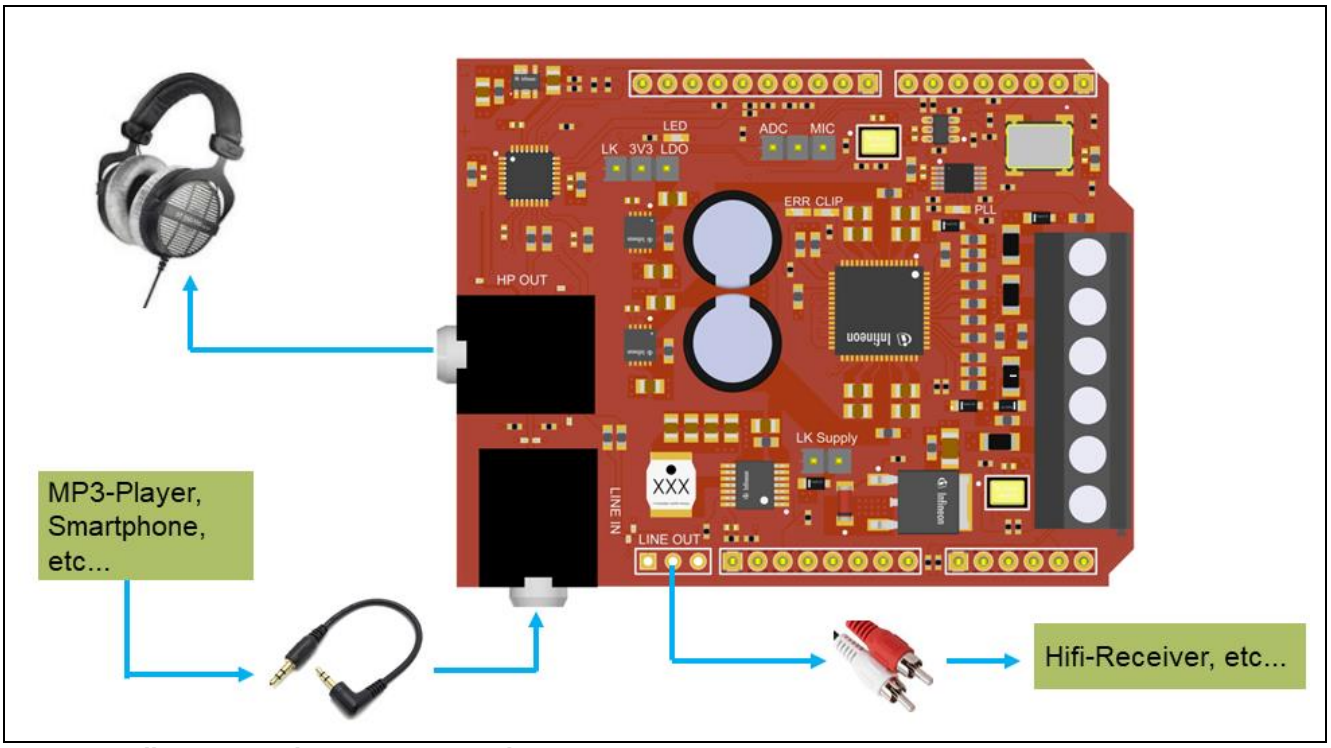
In this supply-mode, the **AURIX™ lite Kit V2** can also be supplied backwards through the **Audio Shield Board**.

Additionally, the 3.3V domain can also be powered from a local LDO.

Needed jumper settings:

- 3V3 Supply Jumper: Don’t care (but one of both options must be set)
- LK Supply Jumper: Set jumper, if **AURIX™ lite Kit V2** should be backwards supplied

2.1.3 Audio Inputs and Outputs



Audio Input and Output connections

By default, two 3.5mm Stereo Jacks are assembled for connecting to external audio-devices such as headphones or MP3-Players.

In case, the audio-output needs to be interfaced to an external audio-device like e.g. a Hifi-Receiver, please use the “LINE OUT”.

All three ports shown above are connected to the SGTL5000 audio-codec.

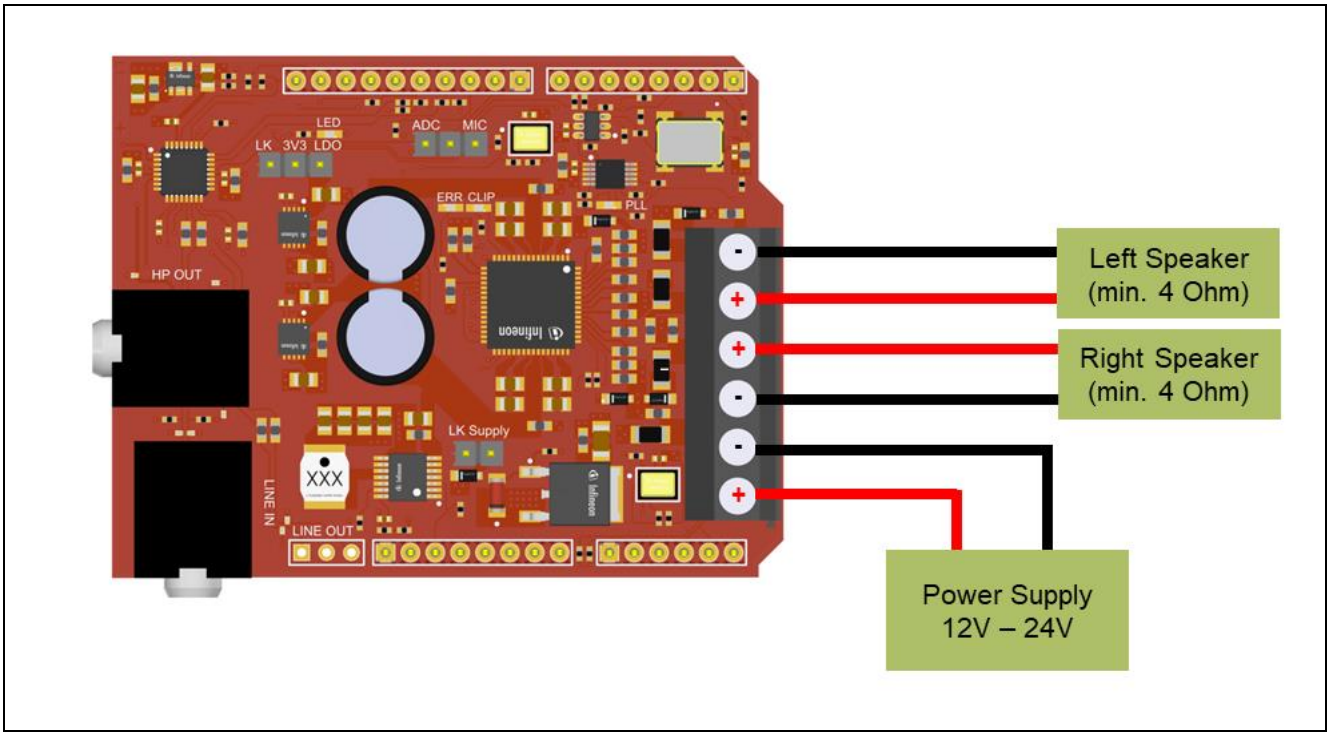
Note: *Please be aware, that the Headphone-GND is DC-biased. Therefore, do not make an external connection between Headphone-GND and global GND.*

This port is primarily considered for connecting headphones only or please use an audio isolation transformer.

2.1.4 Audio Amplifier

2.1.4.1 Stereo BTL operation

By default, the MA12070P audio amplifier is configured to be used in BTL (Bridged Tied Load) operation.
In this mode, a pair of Stereo-Speakers with a minimum impedance of 4 Ohms can be connected.



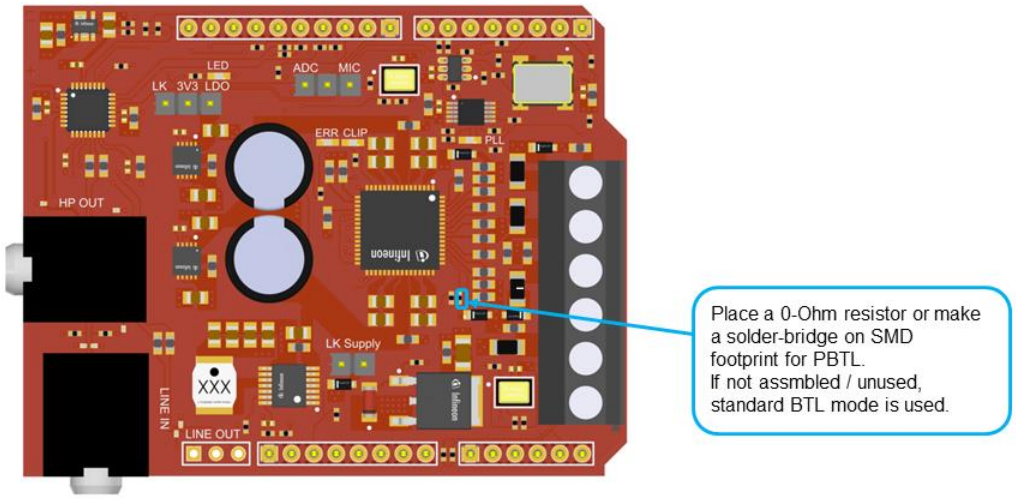
MA12070P amplifier in BTL mode (default configuration)

2.1.4.2 Mono PBTL operation

The **Audio Shield Board** can be modified, so that the MA12070P can be used in PBTL (Parallel Bridged Tied Load) mode. In this case, the amplifier works as mono-amplifier, but can drive loads down to 2 Ohms. Only the left-sample from the I²S bus is used while the right-sample on the I²S acts as dummy-sample.

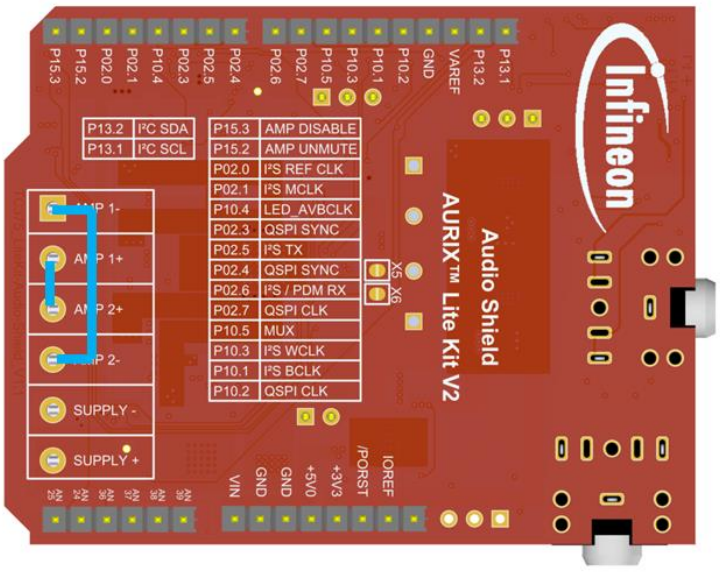
Please make following two modifications on the **Audio Shield Board** for using PBTL:

Place a 0402 0-Ohm resistor or make a solder-bridge on the shown PCB resistor footprint



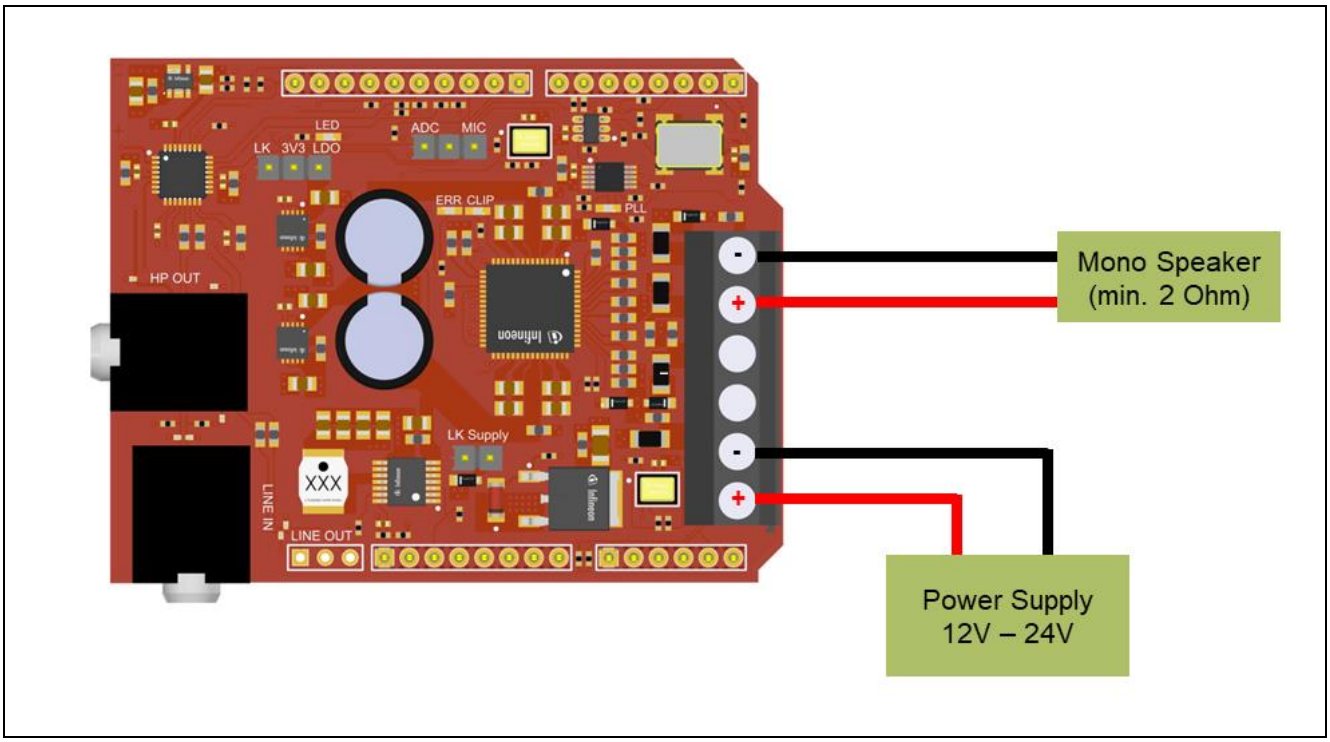
MA12070P amplifier PBTL modification (Step 1)

Make a wire-connection between the two positive outputs and the two negative outputs



MA12070P amplifier PBTL modification (Step 2)

After the modifications are done, a mono-speaker can be connected.



MA12070P amplifier PBTL mode

Note:

Depending on the assembled design-step of the MA12070P, the CLIP indicator will be constantly active during PBTL mode.

Please refer to following document:

Infineon-Errata_sheet_Integrated_audio_ICs_MERUS_MA12040_MA12040P_MA12070_MA12070P-ES-v01_00-EN.pdf

2.1.4.3 I²C operation and audio formats

As shown in "**Audio Shield Board - Bottom View"**, the I²C bus is disconnected by default from the MA12070P (as the I²C bus may be blocked in case MA12070P is unpowered and the 3.3V supply is taken from the **AURIX™ lite Kit V2** – see section 2.1.2.1).

However, the MA12070P doesn't need a certain configuration over I²C in advance to be usable.

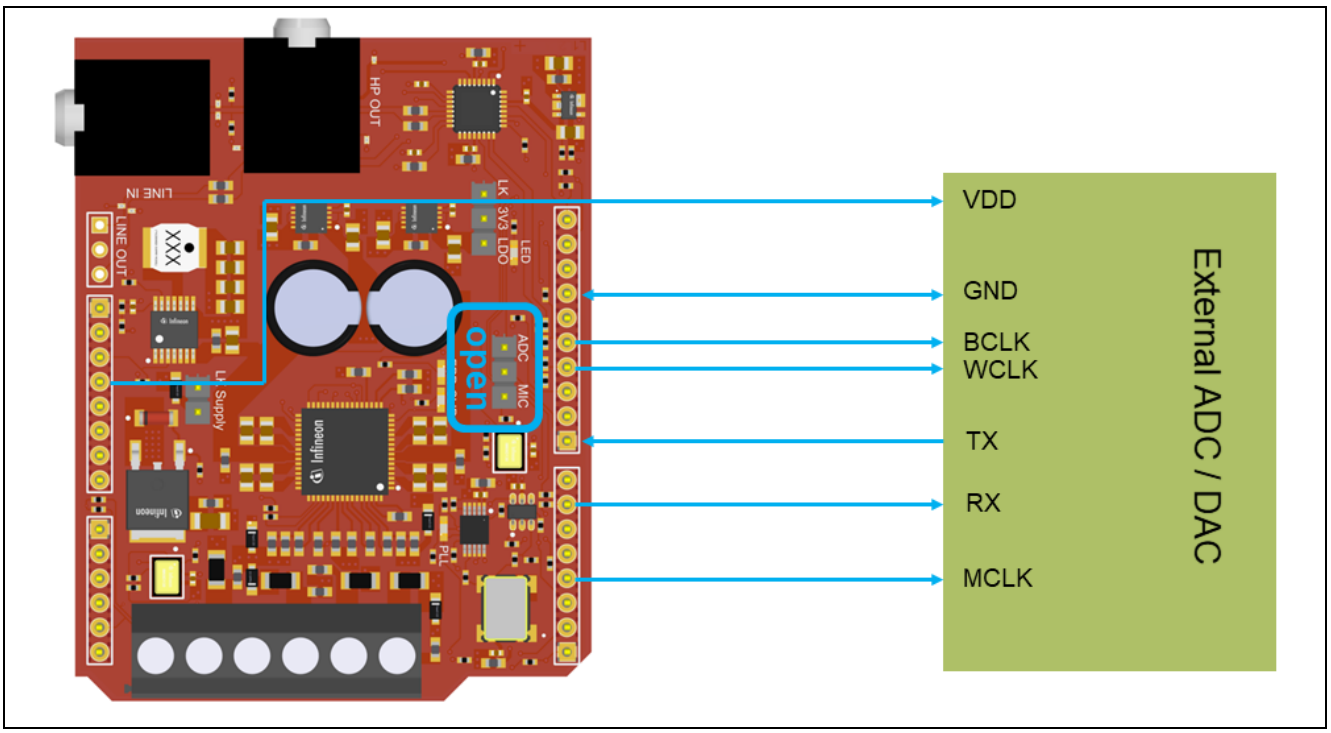
The MA12070P's default audio-format configuration after power-on-reset is following:

- 2* 32 Bit Data Framing
- BCLK = 64*f_s
- LeftJustified-I²S format

In case the audio-format needs to be changed or some further advanced configuration (like e.g. power-mode or limiter) should be configured inside MA12070P, the two solder jumpers on the bottom side must be bridged.

Please be aware, that the I²C bus might be not functional anymore, in case you try to use the **Audio Shield Board** without an external power supply (MA12070P being unpowered and I²C jumpers bridged).

2.1.5 External Audio ADC / DAC



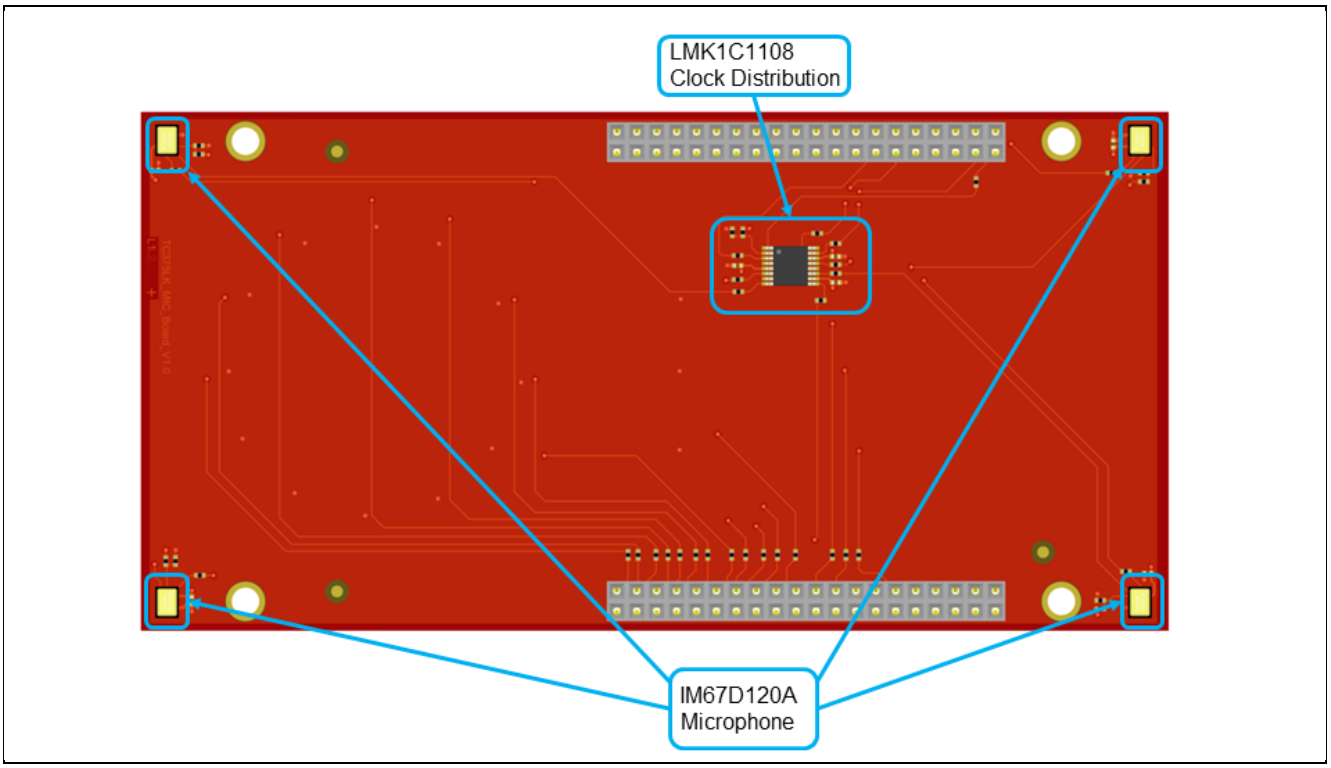
Connecting external audio ADC / DAC to the Audio Shield Board

For further performance evaluation (especially SNR measurements) of the XENSIV™ IM67D120A microphones or the MERUS™ MA12070P amplifier, the onboard codec might not have sufficient audio performance.

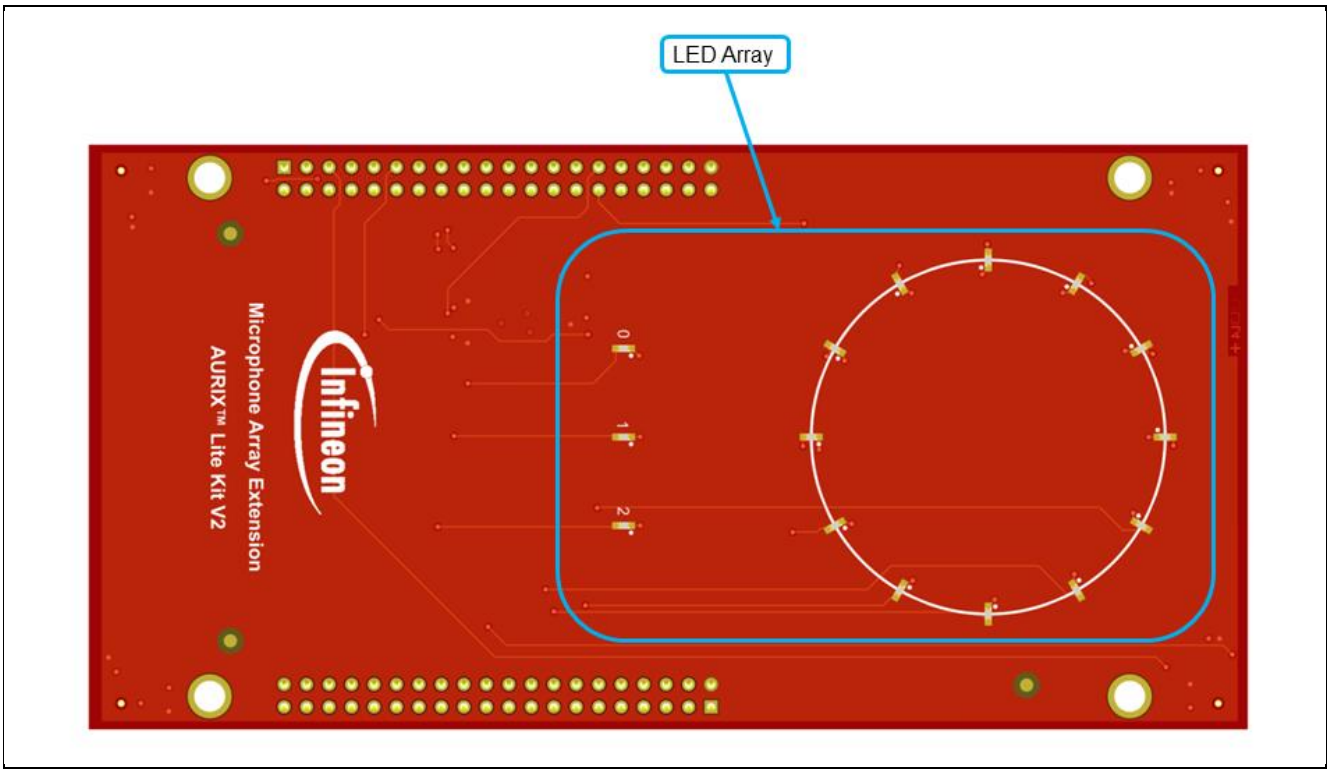
For this purpose, it is proposed to connect an external Audio ADC/DAC via header-wires as shown in the picture above.

Alternatively, audio can be also streamed uncompressed over the Ethernet connection.

2.2 Microphone Array Board

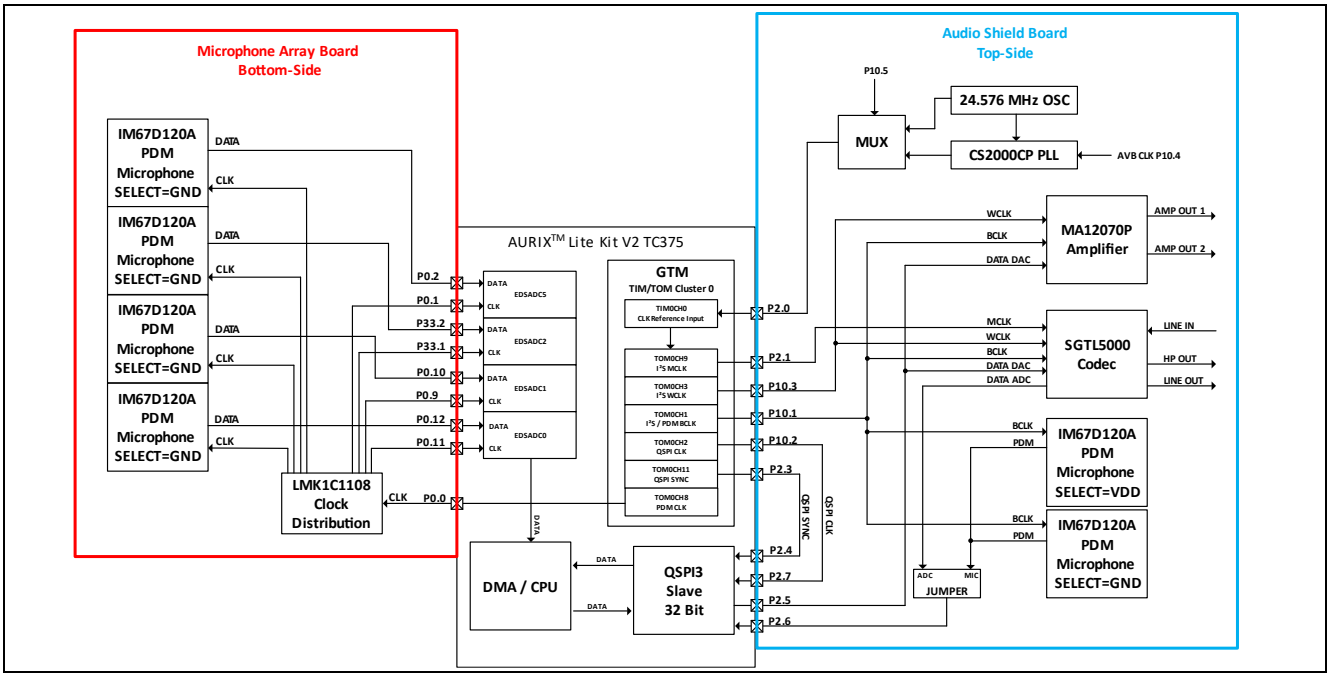


Microphone Array Board - Top View



Microphone Array Board - Bottom View

2.2.1 System Concept



System concept for Microphone Array Board

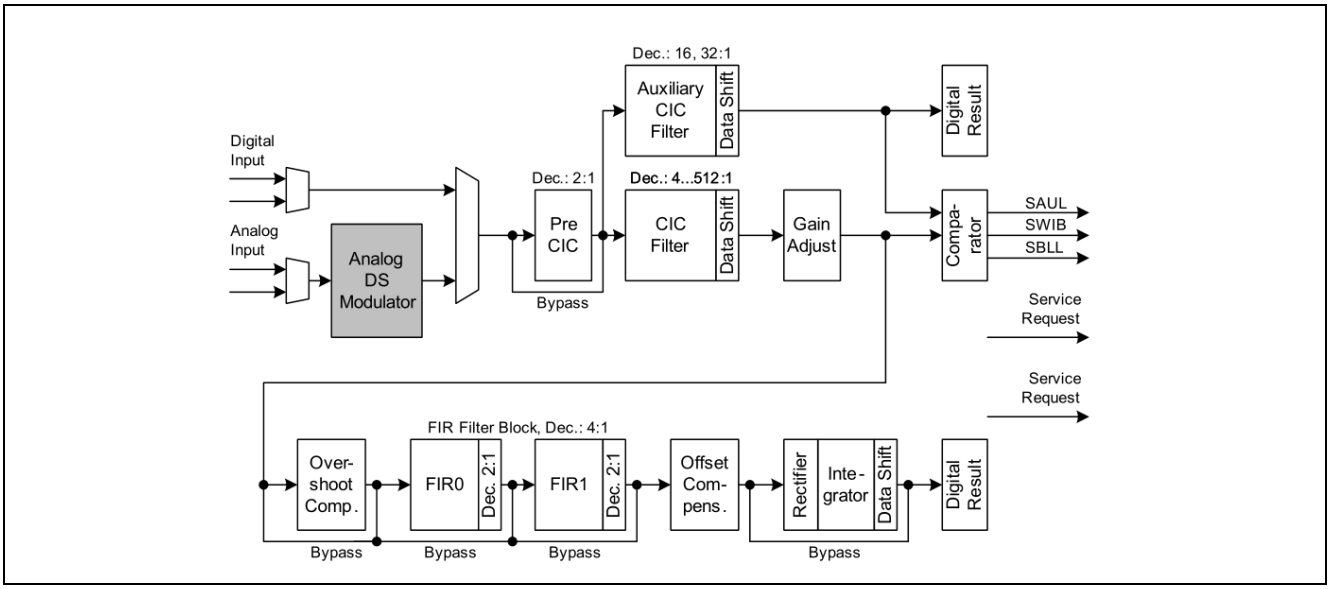
PDM microphones can also be interfaced by using the EDSADC module, where the internal analog DS-Modulator can be bypassed. Consequently, the filter-structure can directly get the PDM data from the microphone.

The EDSADC has a configurable decimation-rate of 4…512.

As it is usually desired to have the audio-stream synchronous to a dedicated audio-clock source (in this case to the other audio-devices on the top-side **Audio Shield Board**), an external PDM clock can be provided to the EDSADC.

In case of this AppKit, the PDM-Clock is generated by TOM0CH8 which is synchronous to all other audio-clocks like e.g. MCLK, BCLK, WCLK, etc.

As the clock signal must be distributed to 8 different clock-sinks, a clock-buffer device was integrated in the design.



EDSADC Structure Overview

3 Software Support

3.1 Toolchain

The **Aurix™ Audio Application Kit** and the **Aurix™ lite Kit V2** can be used with a range of development tools including Infineon's free of charge Eclipse based IDE **Aurix™ Development Studio** or the Eclipse based **FreeEntryToolchain** from HIGHTEC.

Aurix™ Development Studio is a comprehensive environment (including C-Compiler, Multi-core Debugger and Infineon's iLLD low-level driver), with no time and code-size limitations that enables editing, compiling and debugging application code.

Aurix™ Development Studio

The **FreeEntryToolchain** is a full C/C++ development environment which has a source-level UDE debugger from PLS-MC included and is also based on Infineon's low-level driver (iLLD).

FreeEntryToolchain

3.2 Code examples

There is a dedicated repository for the **AURIX™ Audio Application Kit** on Infineon's GitHub channel with further support material but also basic code-examples.

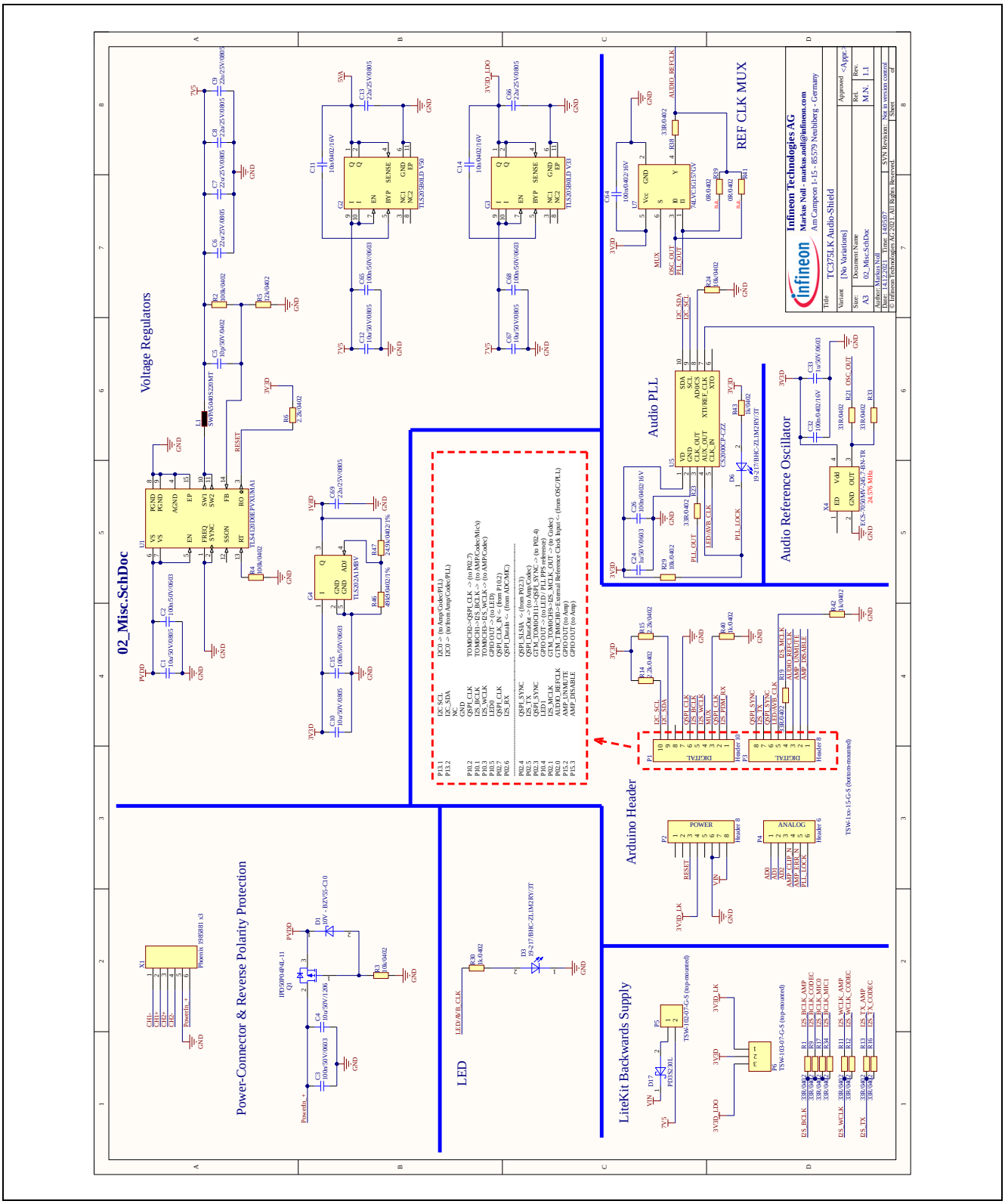
All those code-examples are developed with **AURIX™ Development Studio** and can be directly used without further modifications.

https://github.com/Infineon/Aurix_AudioAppKit

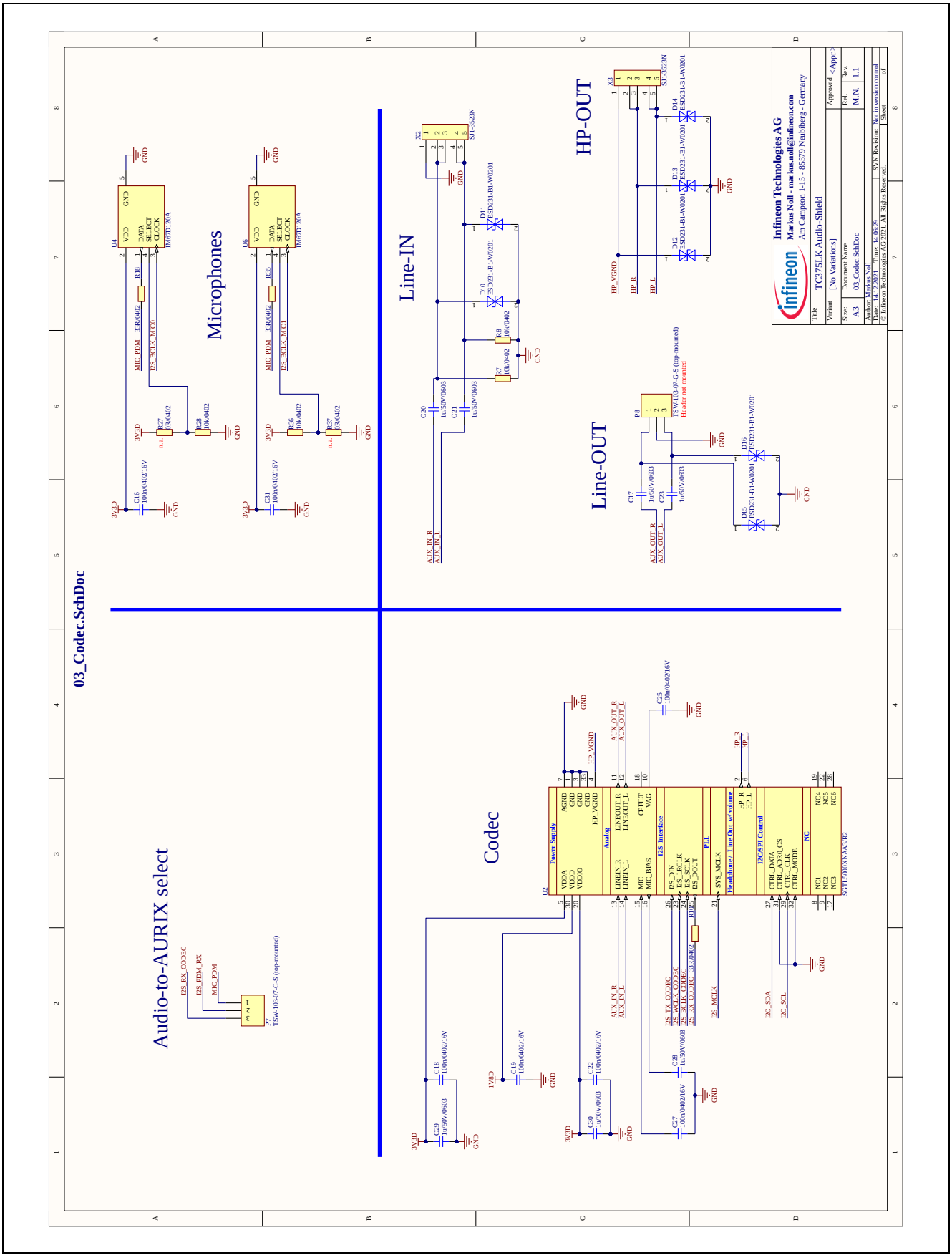
Note: *Please check this repository from time to time for new or updated code examples*

4 Schematics and Placement

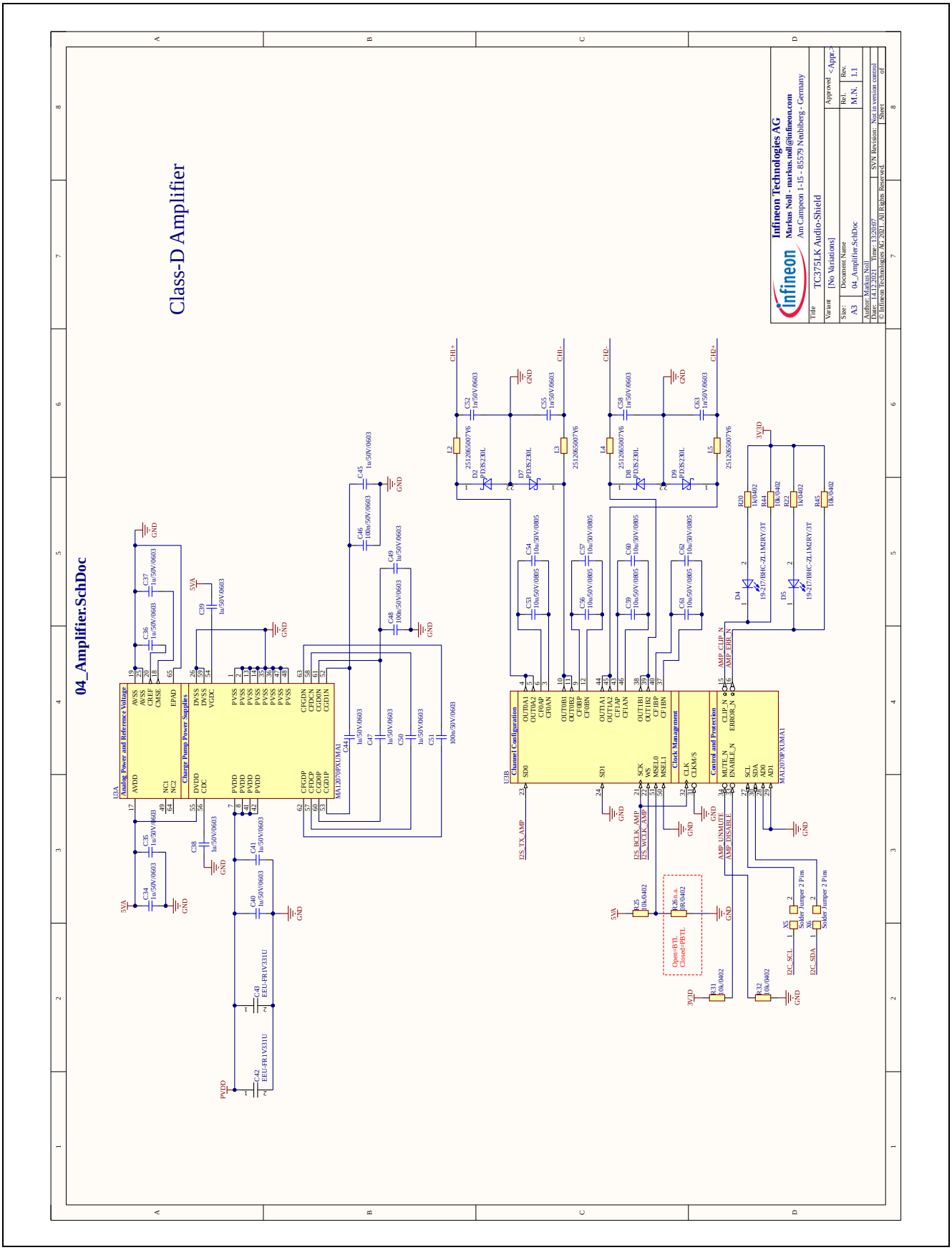
4.1 Audio Shield Board



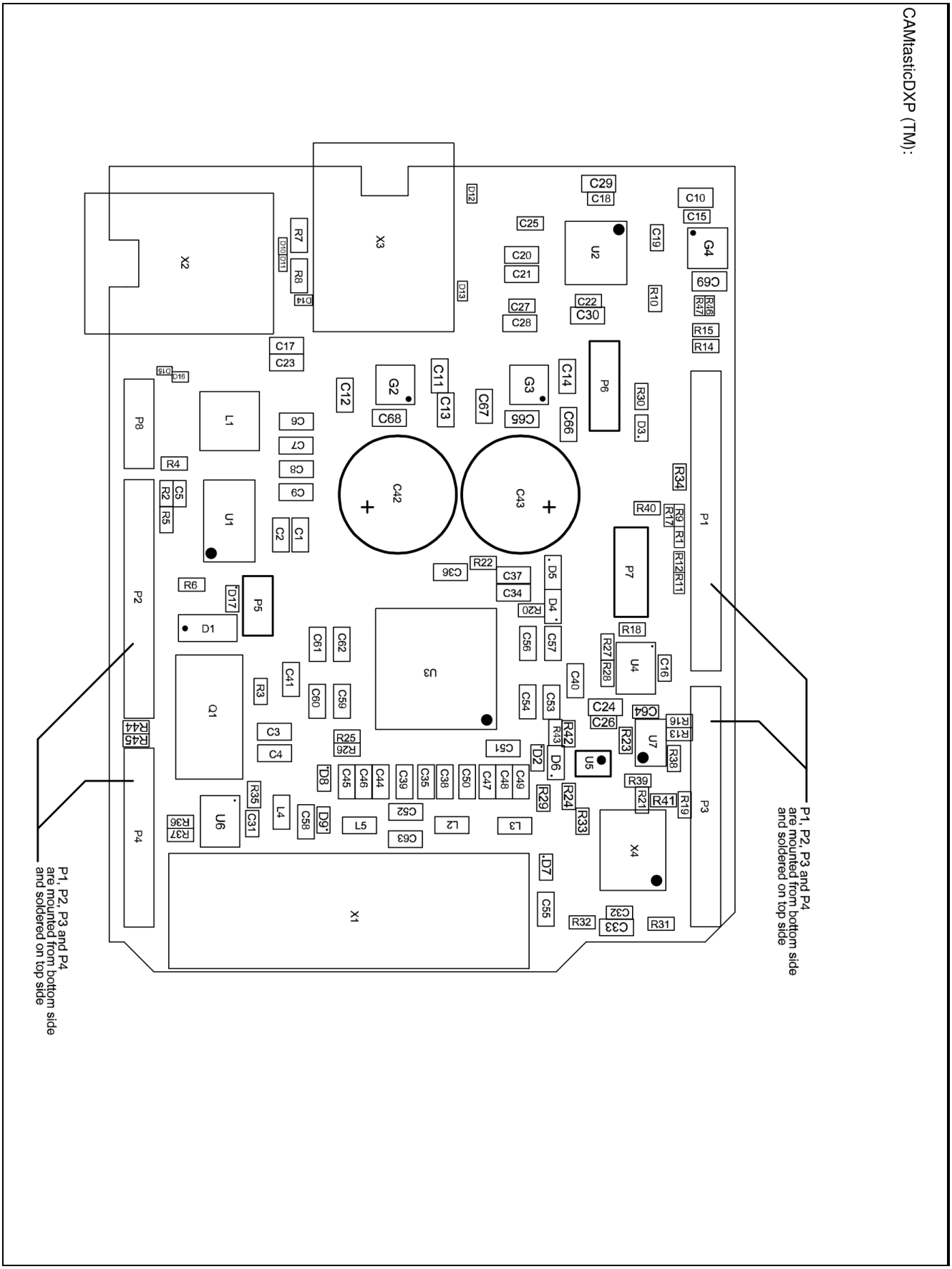
Audio Shield Board - Schematic Misc



Audio Shield Board - Schematic Codec

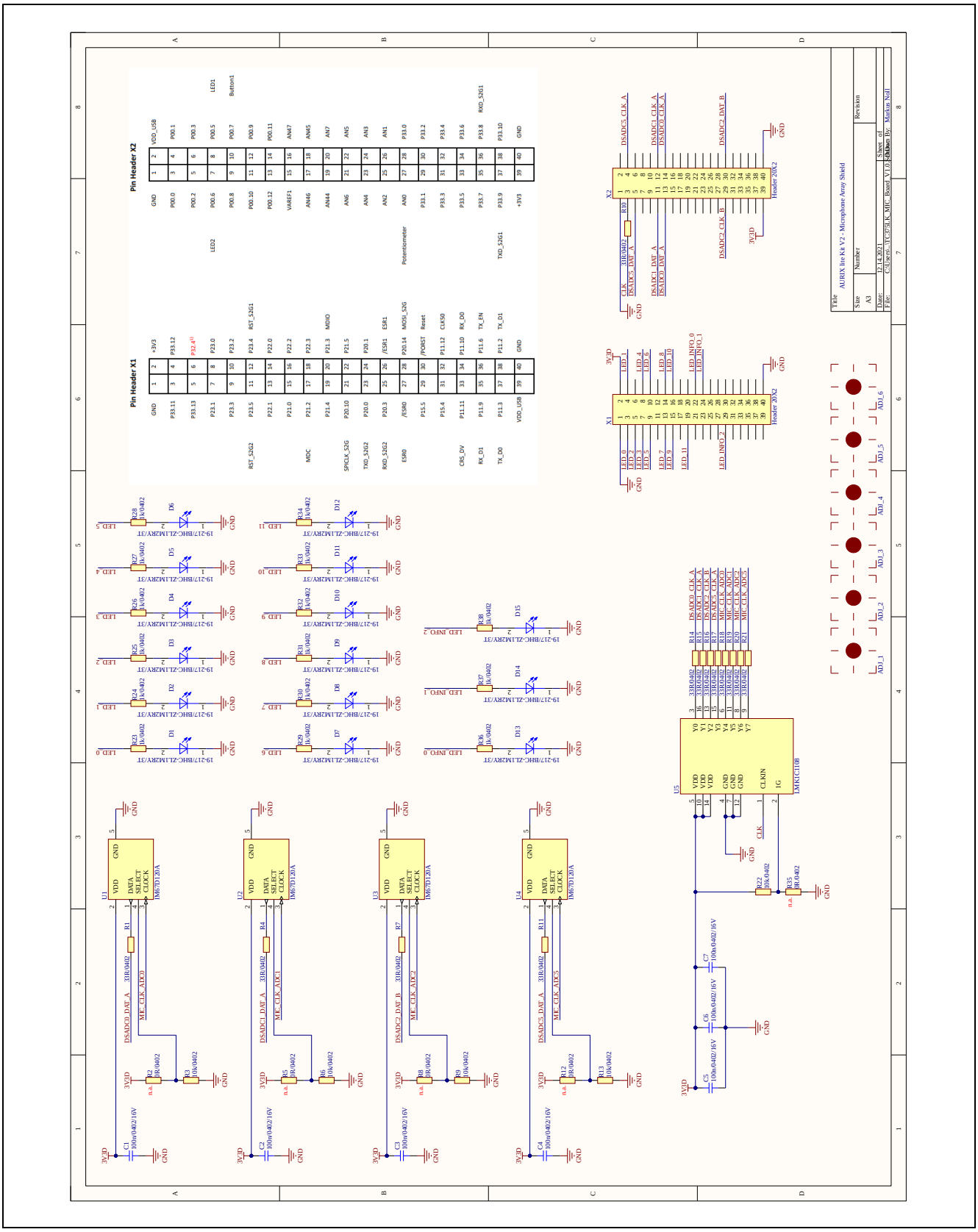


Audio Shield Board - Schematic Amplifier

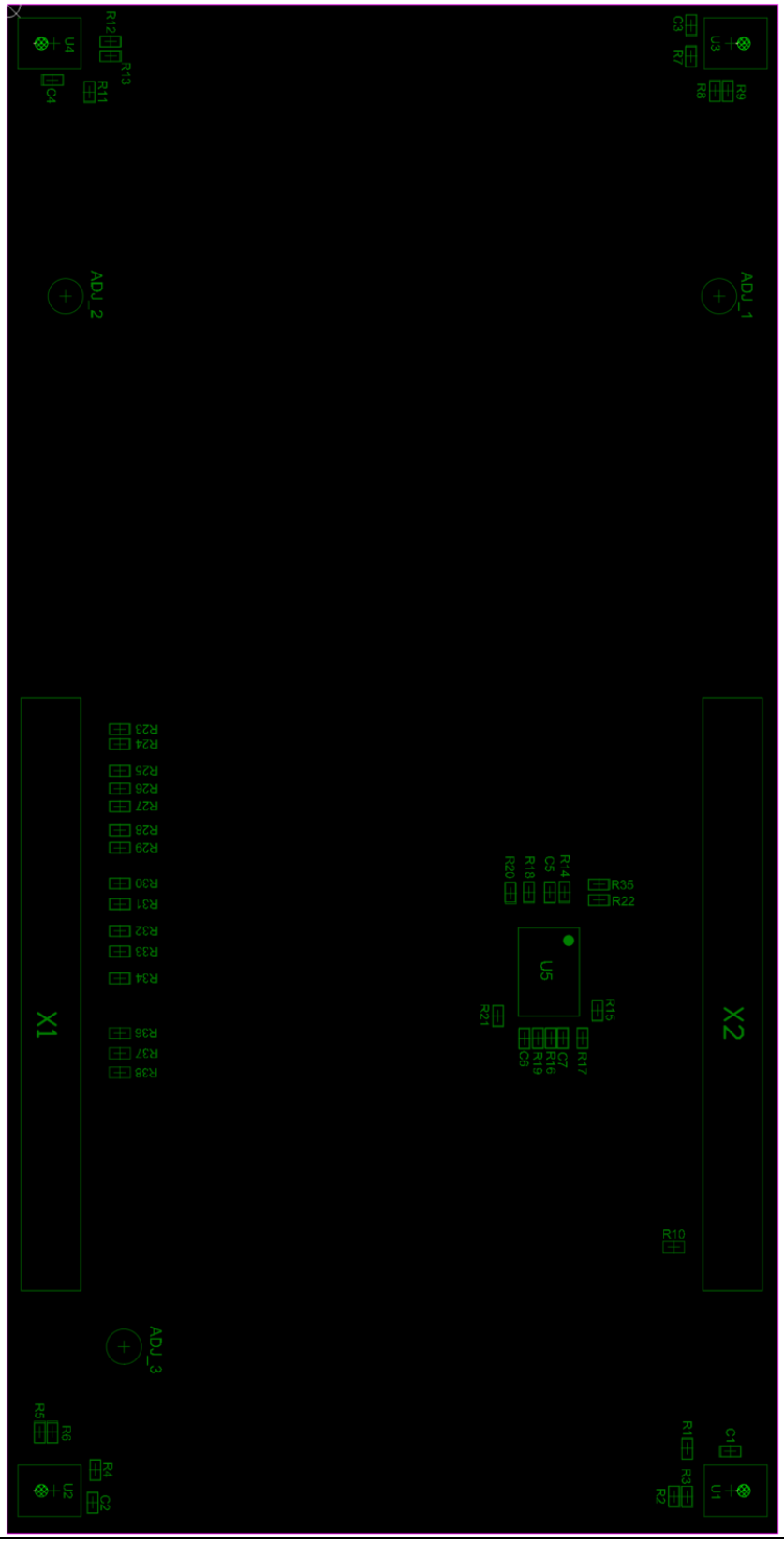


Audio Shield Board - Assembly Top View

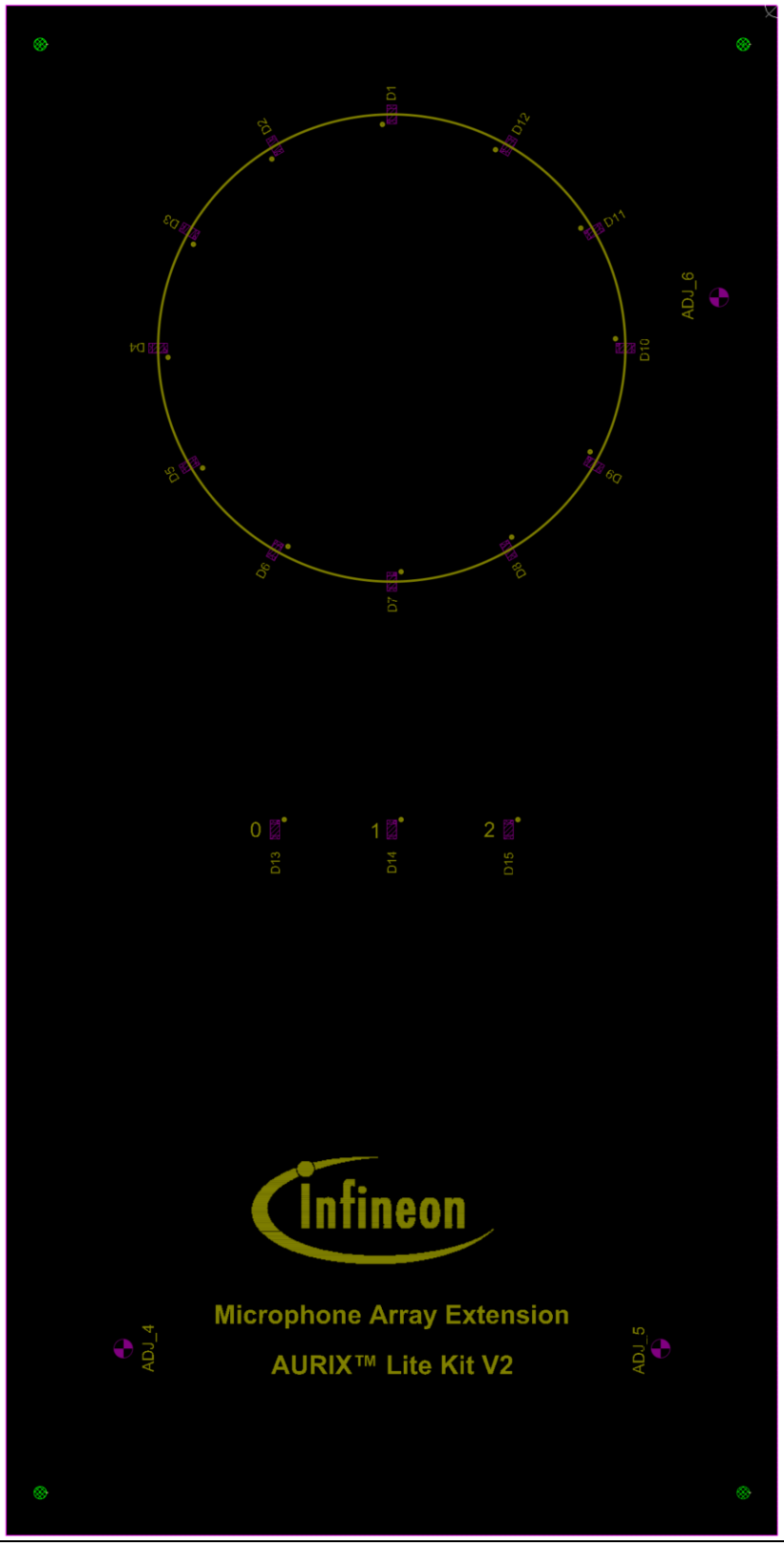
4.2 Microphone Array Board



Microphone Array Board - Schematic



Microphone Array Board - Assembly Top View



Microphone Array Board - Assembly Bottom View

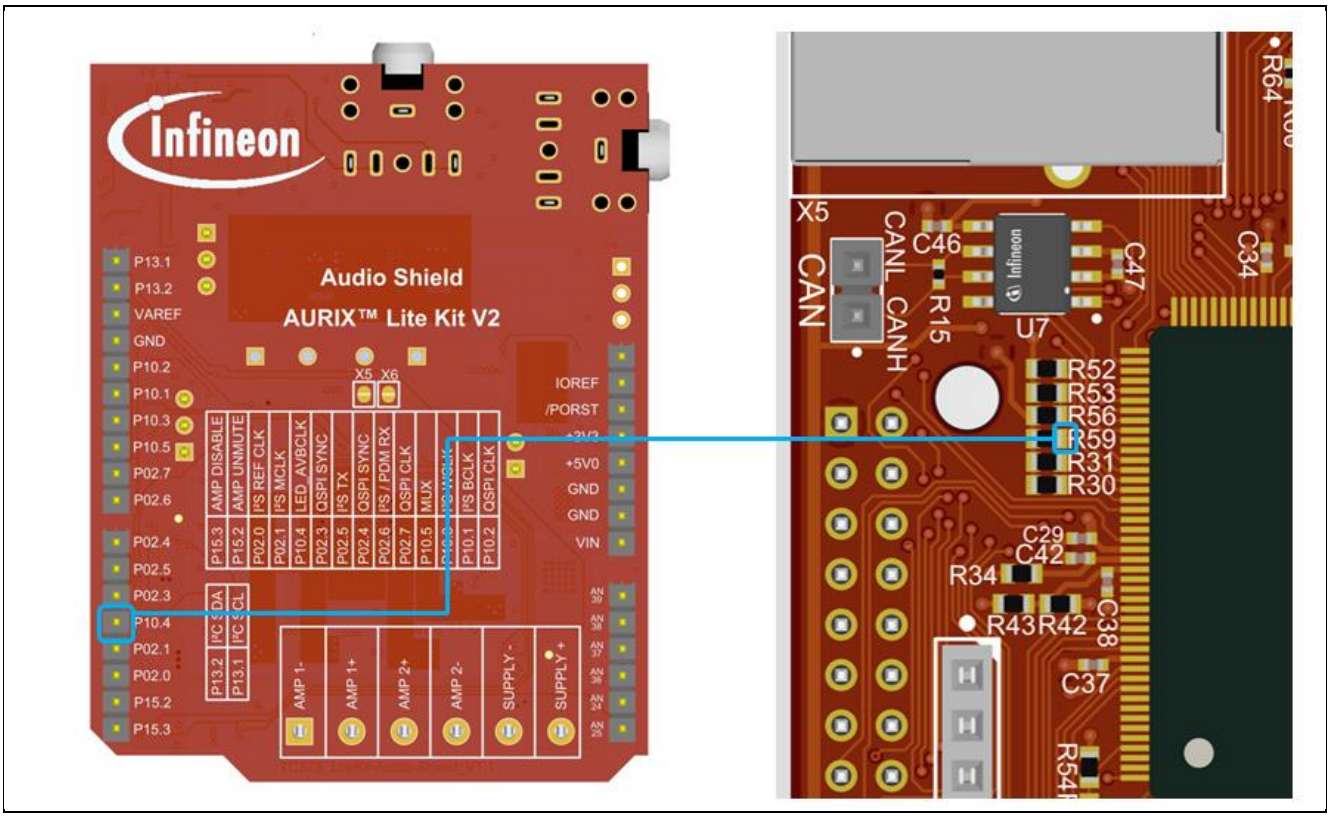
5 Application hints for networked audio

5.1 Using Ethernet PPS as audio reference clock

For high-performance audio-networks (like e.g. AVB), it might be necessary that the local audio-clock must be derived from a network distributed media-clock (e.g. AVB CRF-stream).

The media-clock can be locally recovered using the Ethernet-MAC's PPS output pin in flexible PPS-mode (generating pulses at dedicated timestamps in relation to the IEEE 802.1AS gPTP clock).
This clock signal can be recovered to e.g. a 24.576 MHz reference clock using the onboard CS2000CP-CZZ PLL.

5.1.1.1 Hardware-based



Manual ETH-MAC PPS connection to CS2000CP-CZZ PLL

The PPS signal is only available on P14.4. As this pin is not routed to the shield-header, a manual soldered wire connection must be made between **AURIX™ lite Kit V2** and the **Audio Shield Board** like shown in the picture above. Please ensure in software, that P10.4 stays in high-impedant state.

5.1.1.2 Software-based

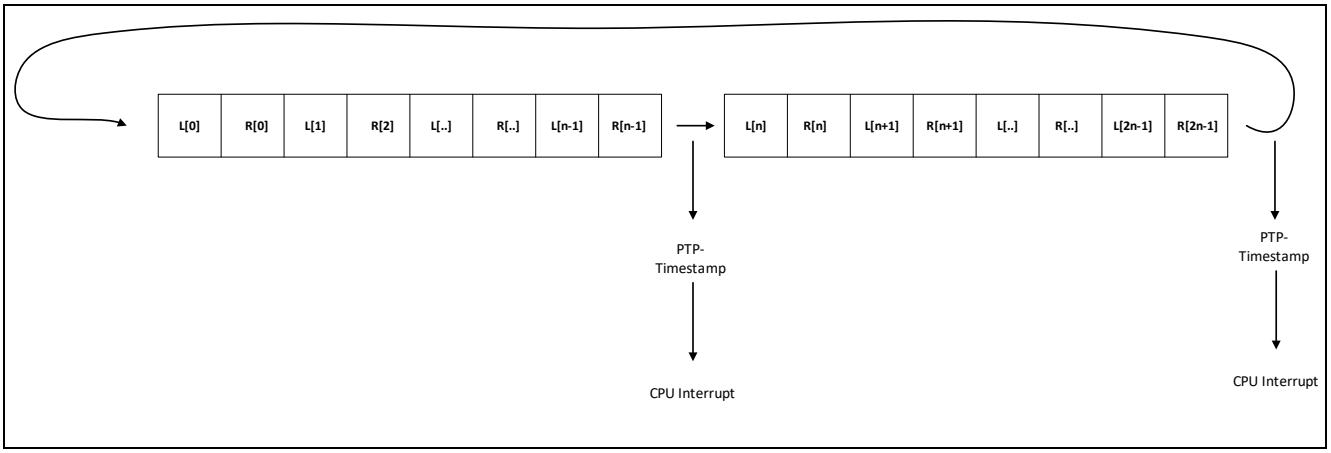
Alternatively, the PPS output can be software-emulated on P10.4.

Please use the Ethernet-MAC's PPS interrupt signal to trigger GTM TOM2CH6 (which is available on P10.4) to push out pulses using the single-shot mode.

5.2 Audio PTP cross-timestamping

Besides the clock-recovery, it is usually needed to implement a precise cross-timestamping between the audio-clock (usually WCLK) against the PTP time.

In Aurix™ it is proposed to operate the emulated audio-interface together with DMA in double-buffering operation. It is possible to generate a PTP cross-timestamp at every buffer-switchover directly in hardware without any CPU interaction. With this method, the audio-clock is indirectly timestamped with a precision in the range of below 50ns accuracy.



Audio cross-timestamping against PTP time

Please contact your local Infineon sales representative for further support and information regarding networked audio applications.

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG