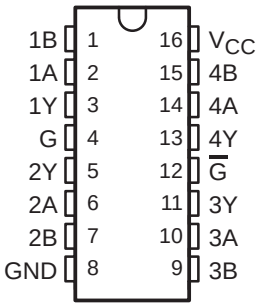
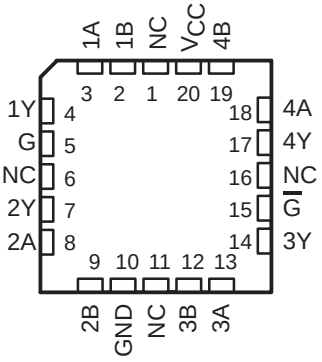
- **Meet or Exceed the Requirements of TIA/EIA-422-B, TIA/EIA-423-B, and TIA/EIA-485-A and ITU Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range of –12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operate From Single 5-V Supply**
- **Low Power Requirements**
- **Pin-to-Pin Replacement for AM26LS32**

**SN55173 . . . J PACKAGE**
**SN65173, SN75173 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN55173 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

**THE SN55173 IS NOT RECOMMENDED FOR NEW DESIGNS.**

## description

The SN55173, SN65173, and SN75173 are monolithic quadruple differential line receivers with 3-state outputs. They are designed to meet the requirements of TIA/EIA-422-B, TIA/EIA-423-B, TIA/EIA-485-A, and several ITU recommendations. The standards are for balanced multipoint bus transmission at rates up to 10 megabits per second. The four receivers share two OR enable inputs, one active when high, the other active when low. These devices feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of –12 V to 12 V. Fail-safe design specifies that if the inputs are open circuited, the outputs are always high. The SN65173 and SN75173 are designed for optimum performance when used with the SN75172 or SN75174 quad differential line drivers.

The SN55173 is characterized over the full military temperature range of –55°C to 125°C. The SN65173 is characterized for operation from –40°C to 85°C. The SN75173 is characterized for operation from 0°C to 70°C.

**AVAILABLE OPTIONS**

| $T_A$ | PACKAGED DEVICES | | | |
|---|---|---|---|---|
| | PLASTIC SMALL OUTLINE (D) | PLASTIC CHIP CARRIER (FK) | CERAMIC DIP (J) | PLASTIC DIP (N) |
| 0°C to 70°C | SN75173D | — | — | SN75173N |
| –40°C to 85°C | SN65173D | — | — | SN65173N |
| –55°C to 125°C | — | SN55173FK | SN55173J | — |

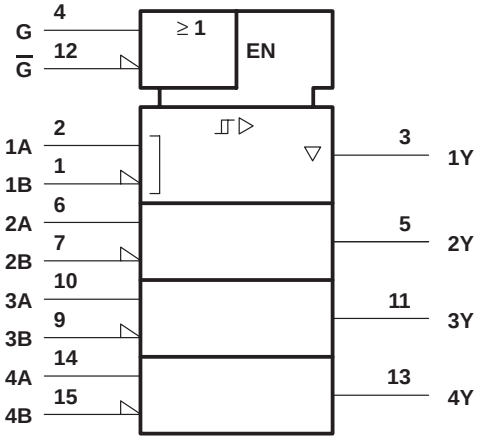
The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN75173DR).

**FUNCTION TABLE**
**(each receiver)**

| DIFFERENTIAL A–B | ENABLES | | OUTPUT Y |
|---|---|---|---|
| | G | $\overline{G}$ | |
| $V_{ID} \geq 0.2$ V | H | X | H |
| | X | L | H |
| –0.2 V < $V_{ID}$ < 0.2 V | H | X | ? |
| | X | L | ? |
| $V_{ID} \leq$ –0.2 V | H | X | L |
| | X | L | L |
| X | L | H | Z |
| Open circuit | X | L | H |
| | H | X | H |

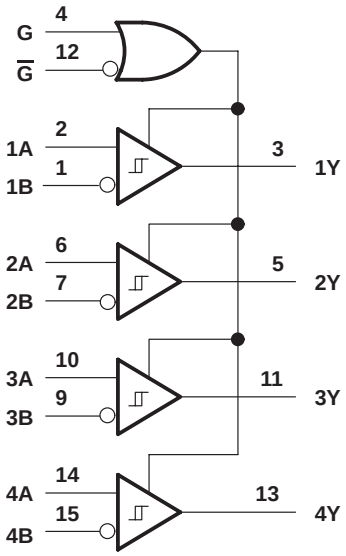
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

## logic symbol †



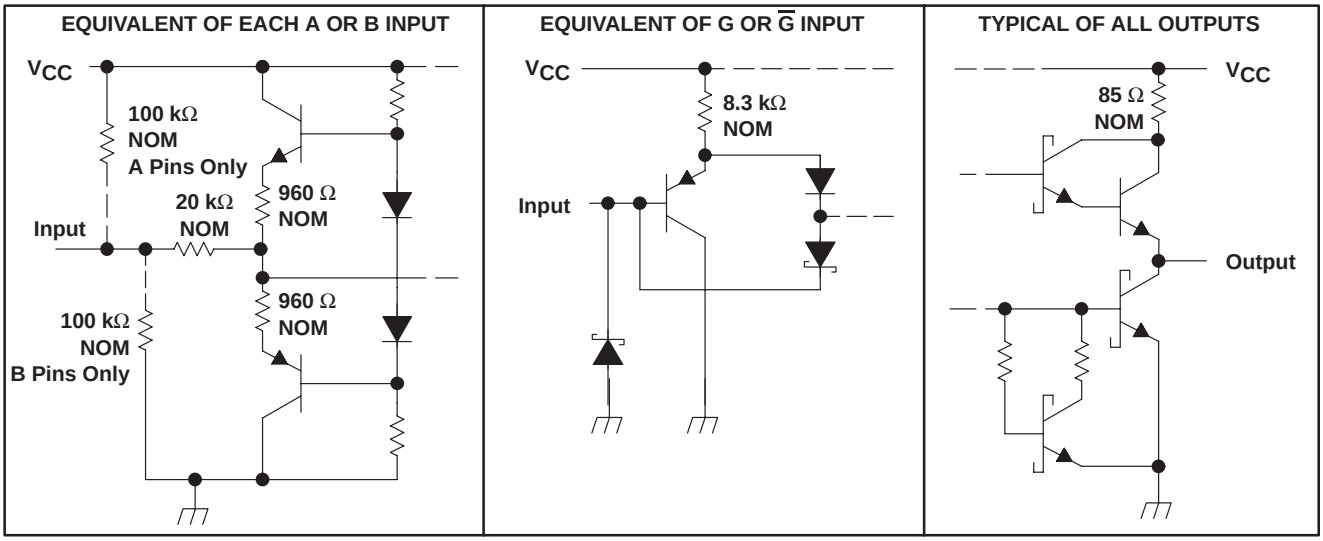

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)




Pin numbers shown are for the D, J, and N packages.

## schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage ($V_I$ or B inputs) . . . . . ±25 V
Differential input voltage, $V_{ID}$ (see Note 2) . . . . . ±25 V
Enable input voltage, $V_I$ . . . . . 7 V
Low-level output current, $I_{OL}$ . . . . . 50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package . . . . . 73°C/W
N package . . . . . 67°C/W
Continuous total dissipation . . . . . See Dissipation Rating Table
Case temperature for 60 seconds, $T_C$: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. The package thermal impedance is calculated in accordance with JESD 51.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR | $T_A = 70°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|
| FK | 1375 mW | 11 mW/°C | 880 mW | 275 mW |
| J | 1375 mW | 11 mW/°C | 880 mW | 275 mW |

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | SN55173 | 4.5 | 5 | 5.5 | V |
| | SN65173, SN75173 | 4.75 | 5 | 5.25 | V |
| Common-mode input voltage, $V_{IC}$ | | | | ±12 | V |
| Differential input voltage, $V_{ID}$ | | | | ±12 | V |
| High-level enable-input voltage, $V_{IH}$ | | 2 | | | V |
| Low-level enable-input voltage, $V_{IL}$ | | | | 0.8 | V |
| High-level output current, $I_{OH}$ | | | | –400 | μA |
| Low-level output current, $I_{OL}$ | | | | 16 | mA |
| Operating free-air temperature, $T_A$ | SN55173 | –55 | | 125 | °C |
| | SN65173 | –40 | | 85 | |
| | SN75173 | 0 | | 70 | |

## electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature

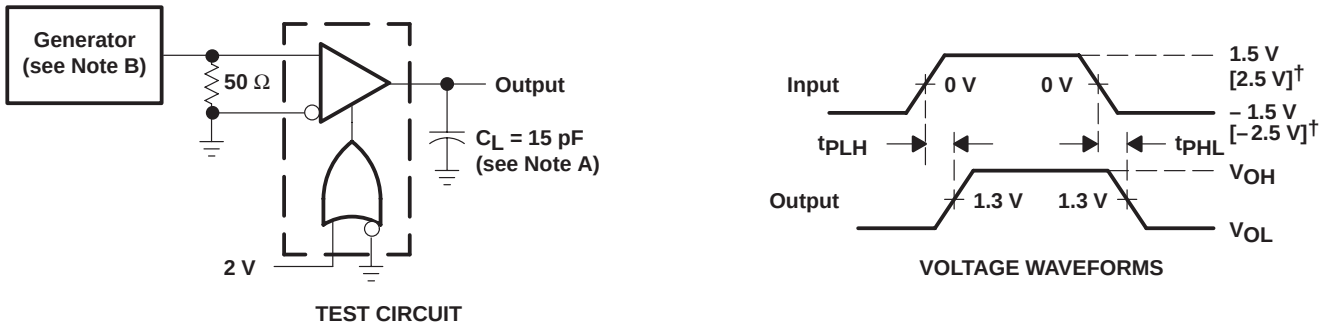
| PARAMETER | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | $V_O$ = 2.7 V, | $I_O$ = –0.4 mA | | | | 0.2 | V |
| $V_{IT–}$ | Negative-going input threshold voltage | $V_O$ = 0.5 V, | $I_O$ = 16 mA | | –0.2‡ | | | V |
| $V_{hys}$ | Hysteresis ($V_{IT+} – V_{IT–}$) | See Figure 4 | | | | 50 | | mV |
| $V_{IK}$ | Enable-input clamp voltage | $I_I$ = –18 mA | | | | | –1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 200 mV, | $I_{OH}$ = –400 μA | SN55173 | 2.5 | | | V |
| | | | | SN65173, SN75173 | 2.7 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = –200 mV, | See Figure 1 | $I_{OL}$ = 8 mA | | | 0.45 | V |
| | | | | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_{OZ}$ | High-impedance-state output current | $V_O$ = 0.4 V to 2.4 V | | | | | ±20 | μA |
| $I_I$ | Line input current | Other input at 0 V, | See Note 3 | $V_I$ = 12 V | | | 1 | mA |
| | | | | $V_I$ = –7 V | | | –0.8 | |
| $I_{IH}$ | High-level enable-input current | $V_{IH}$ = 2.7 V | | | | | 20 | μA |
| $I_{IL}$ | Low-level enable-input current | $V_{IL}$ = 0.4 V | | | | | –100 | μA |
| $r_i$ | Input resistance | | | | 12 | | | kΩ |
| $I_{OS}$ | Short-circuit output current | | | | –15 | | –85 | mA |
| $I_{CC}$ | Supply current | Outputs disabled | | | | | 70 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
NOTE 3: Refer to TIA/EIA-422-B and TIA/EIA-423-B for exact conditions.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $V_{ID}$ = –1.5 V to 1.5 V, $C_L$ = 15 pF, | See Figure 1 | | 20 | 35 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 22 | 35 | ns |
| $t_{PZH}$ | Output enable time to high level | $C_L$ = 15 pF, | See Figure 2 | | 17 | 22 | ns |
| $t_{PZL}$ | Output enable time to low level | $C_L$ = 15 pF, | See Figure 3 | | 20 | 25 | ns |
| $t_{PHZ}$ | Output disable time from high level | $C_L$ = 5 pF, | See Figure 2 | | 21 | 30 | ns |
| $t_{PLZ}$ | Output disable time from low level | $C_L$ = 5 pF, | See Figure 3 | | 30 | 40 | ns |

## PARAMETER MEASUREMENT INFORMATION

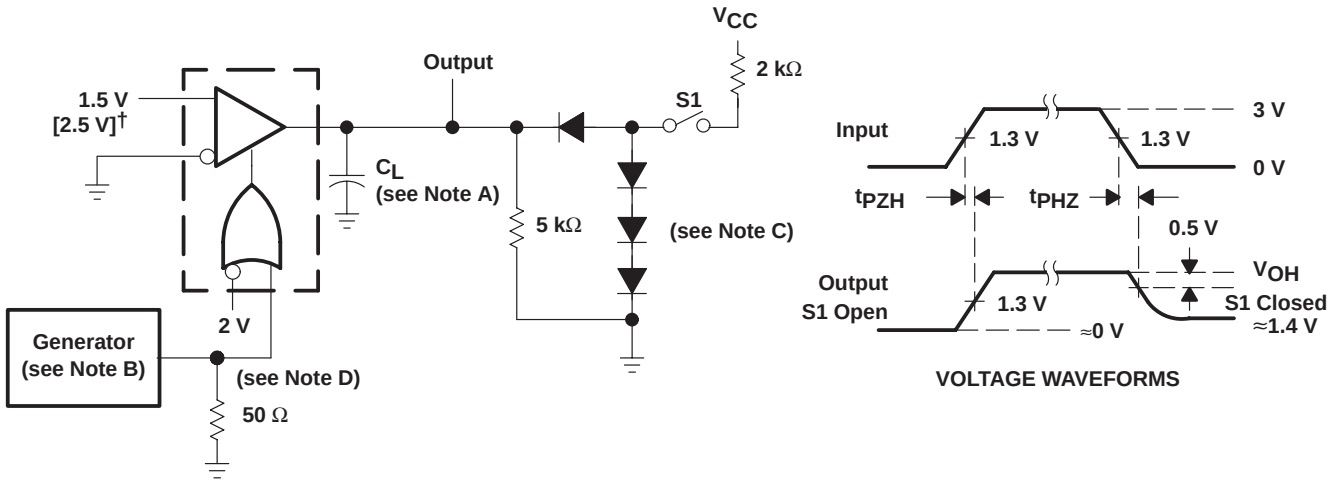



† Voltage for the SN55173 only.

NOTES: A. $C_L$ includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.

**Figure 1. $t_{PLH}$, $t_{PHL}$ Test Circuit and Voltage Waveforms**




† Voltage for the SN55173 only.

NOTES: A. $C_L$ includes probe and jig capacitance.

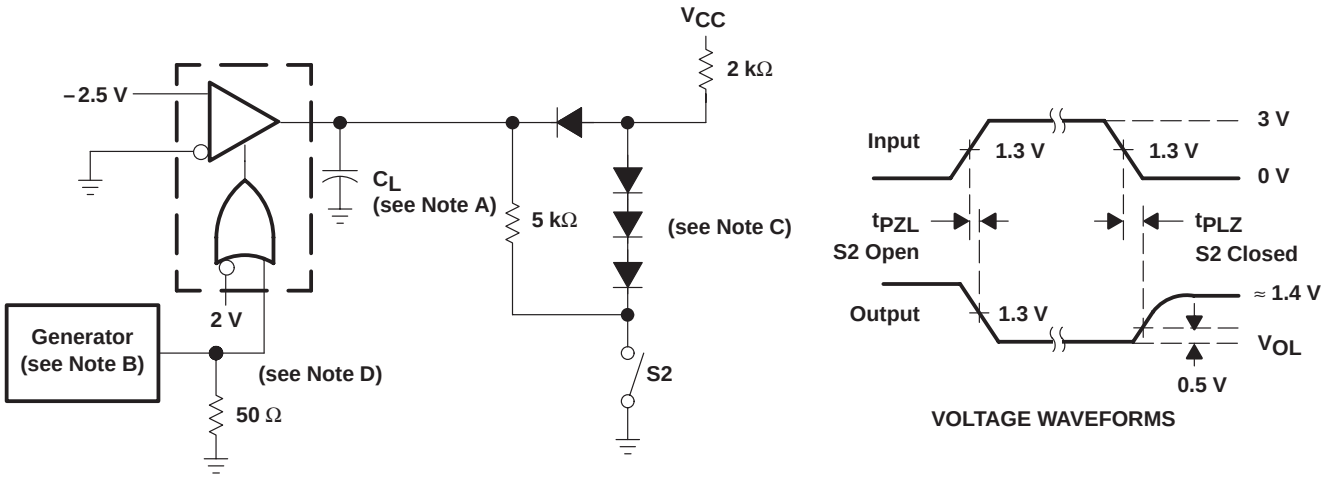
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.

C. All diodes are 1N916, or equivalent.

D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

**Figure 2. $t_{PHZ}$, $t_{PZH}$ Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
C. All diodes are 1N916, or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

**Figure 3. $t_{PZL}$, $t_{PLZ}$ Test Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS†

**OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE**

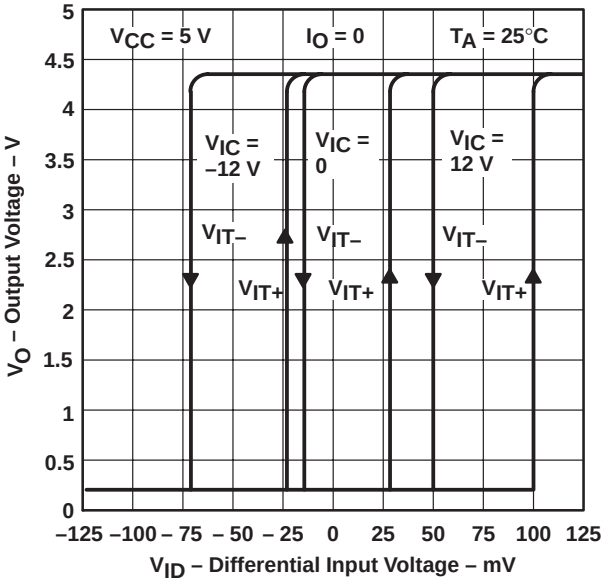



Figure 4

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

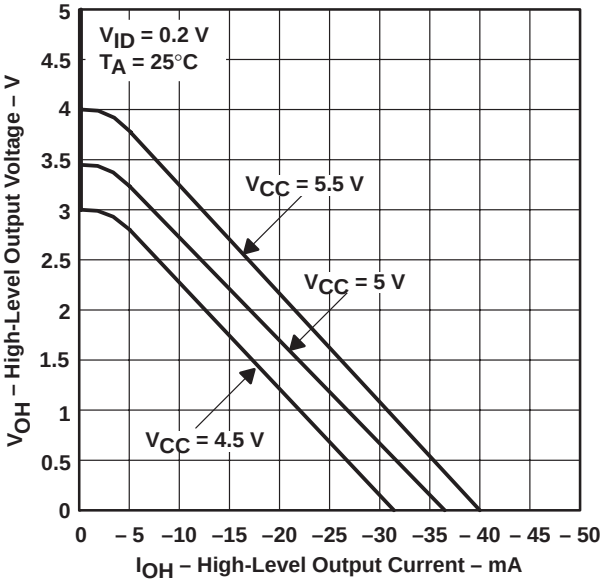



Figure 5

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

## TYPICAL CHARACTERISTICS†

**HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

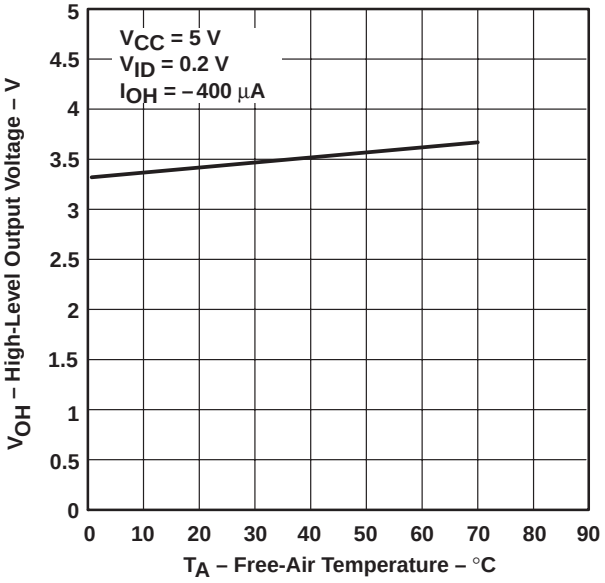



**Figure 6**

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

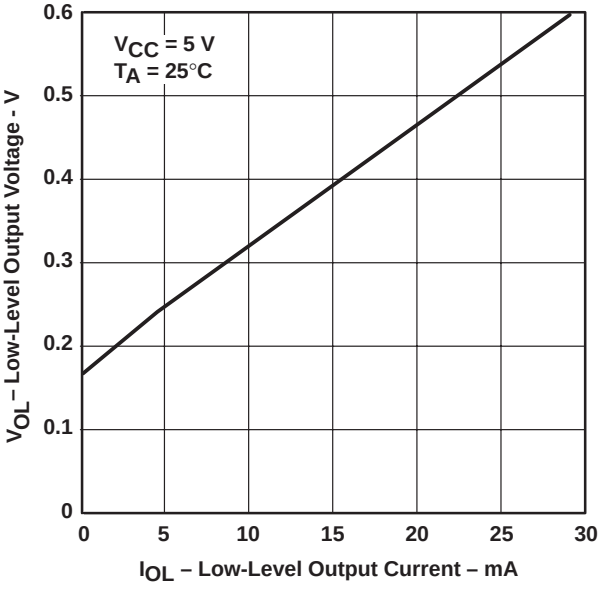



**Figure 7**

**LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

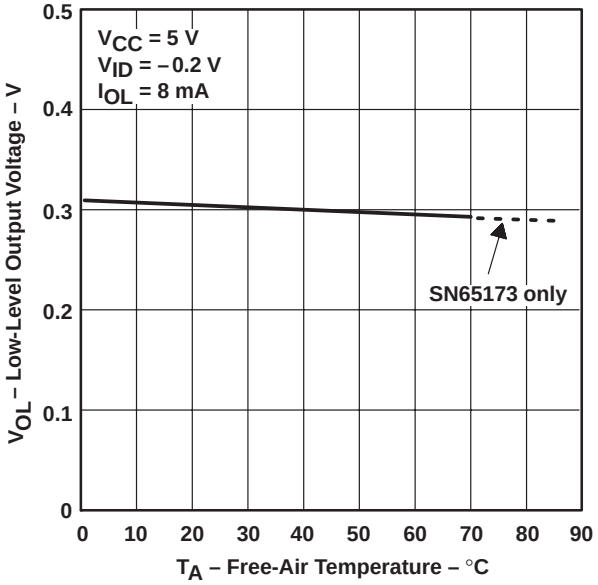



**Figure 8**

**OUTPUT VOLTAGE vs ENABLE G VOLTAGE**

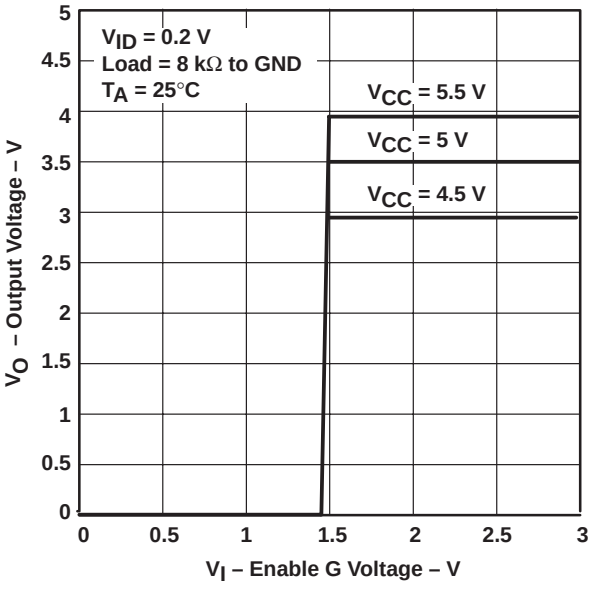



**Figure 9**

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

## TYPICAL CHARACTERISTICS

**OUTPUT VOLTAGE vs ENABLE G VOLTAGE**

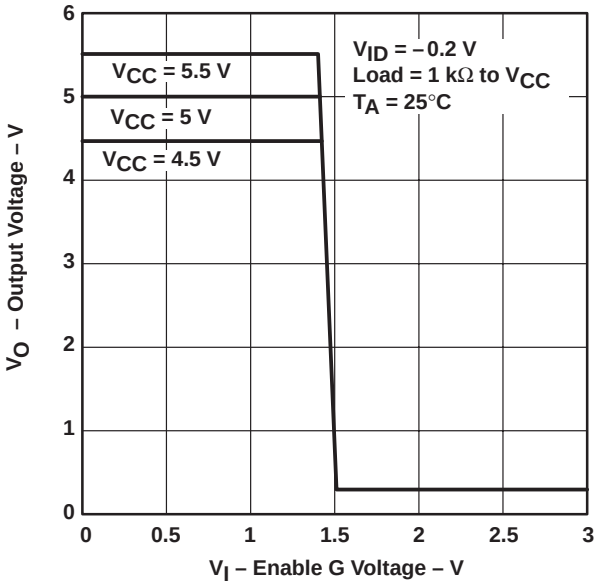



Figure 10

**INPUT CURRENT vs INPUT VOLTAGE**

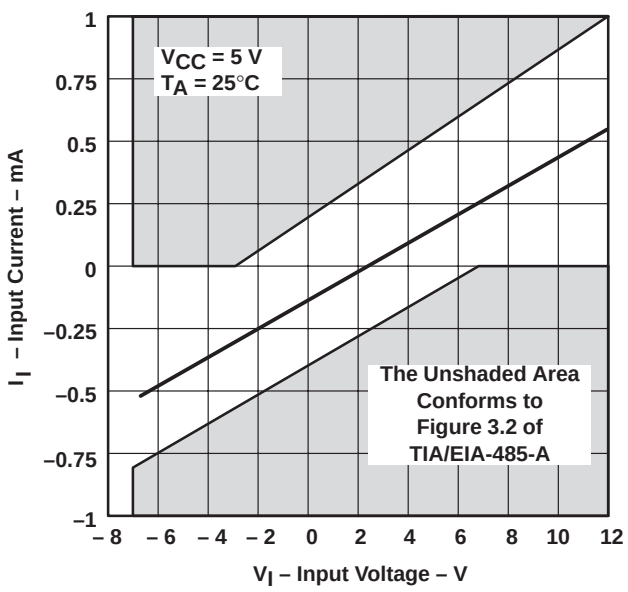
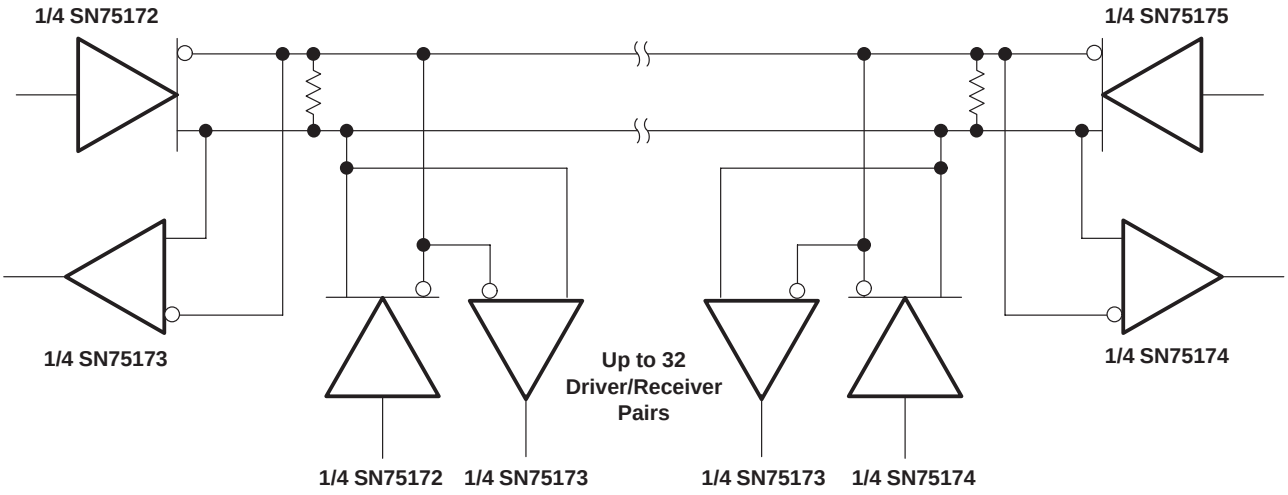



Figure 11

## APPLICATION INFORMATION




NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

**Figure 12. Typical Application Circuit**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN55173J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN55173J | Samples |
| SN75173D | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75173 | Samples |
| SN75173DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75173 | Samples |
| SN75173N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN75173N | Samples |
| SN75173NSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75173 | Samples |
| SNJ55173J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ55173J | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF SN55173, SN75173 :**

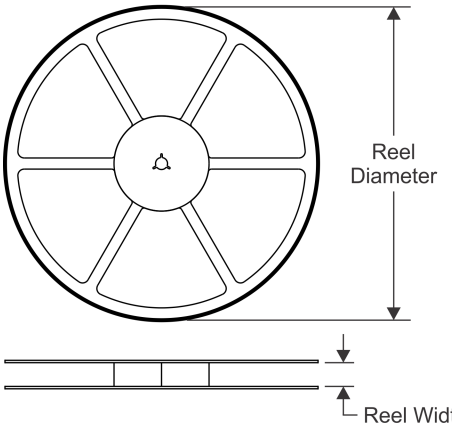
- Catalog : SN75173
- Military : SN55173

NOTE: Qualified Version Definitions:

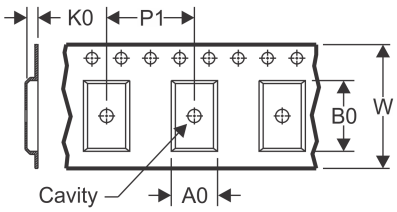
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

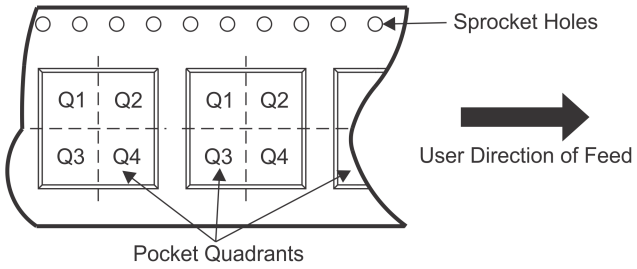



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

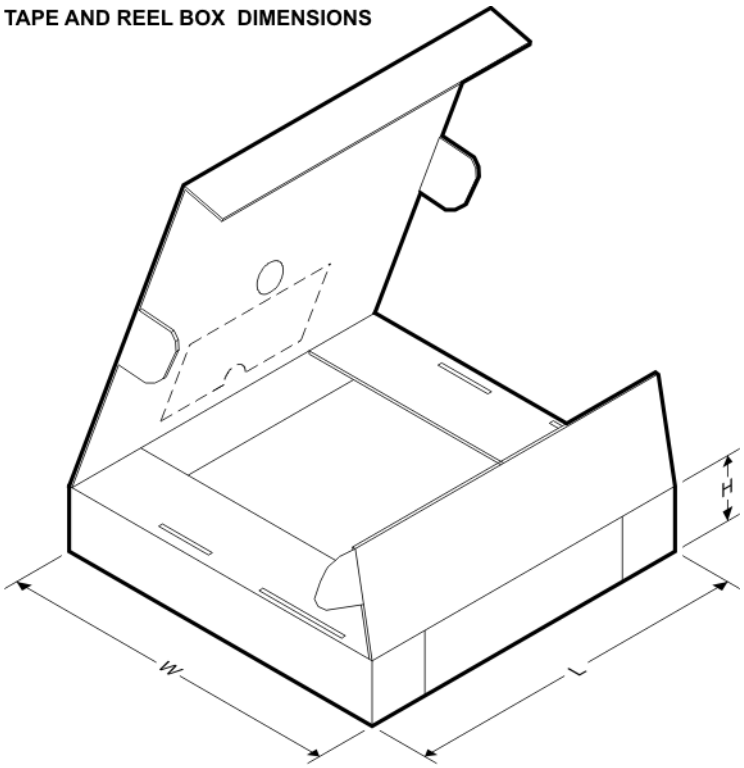
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75173DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN75173NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



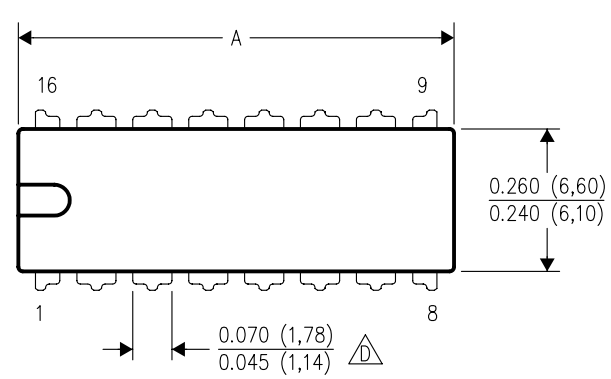

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN75173DR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN75173NSR | SO | NS | 16 | 2000 | 853.0 | 449.0 | 35.0 |

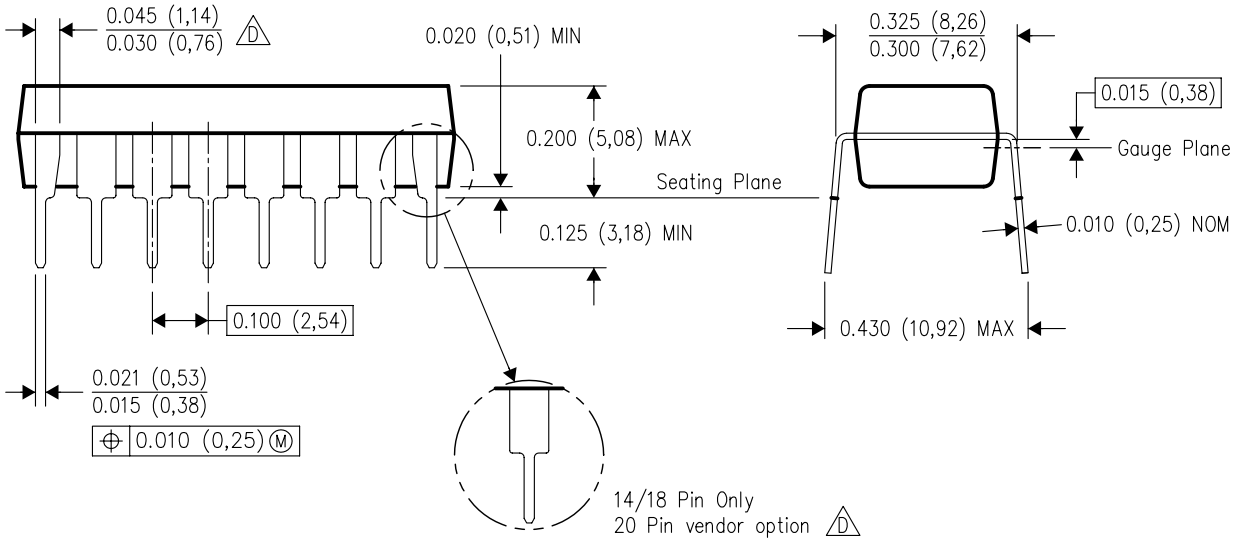
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



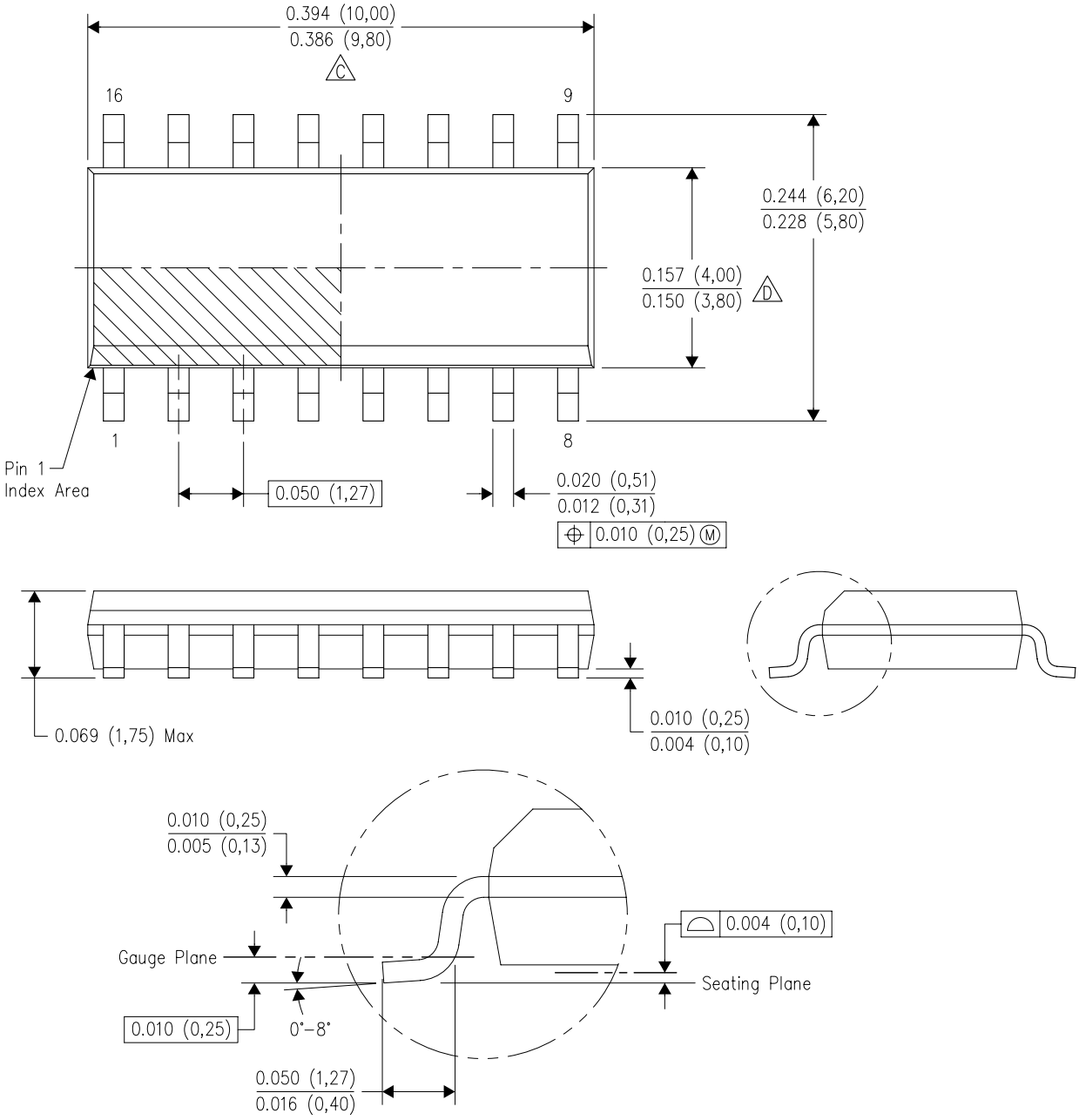

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

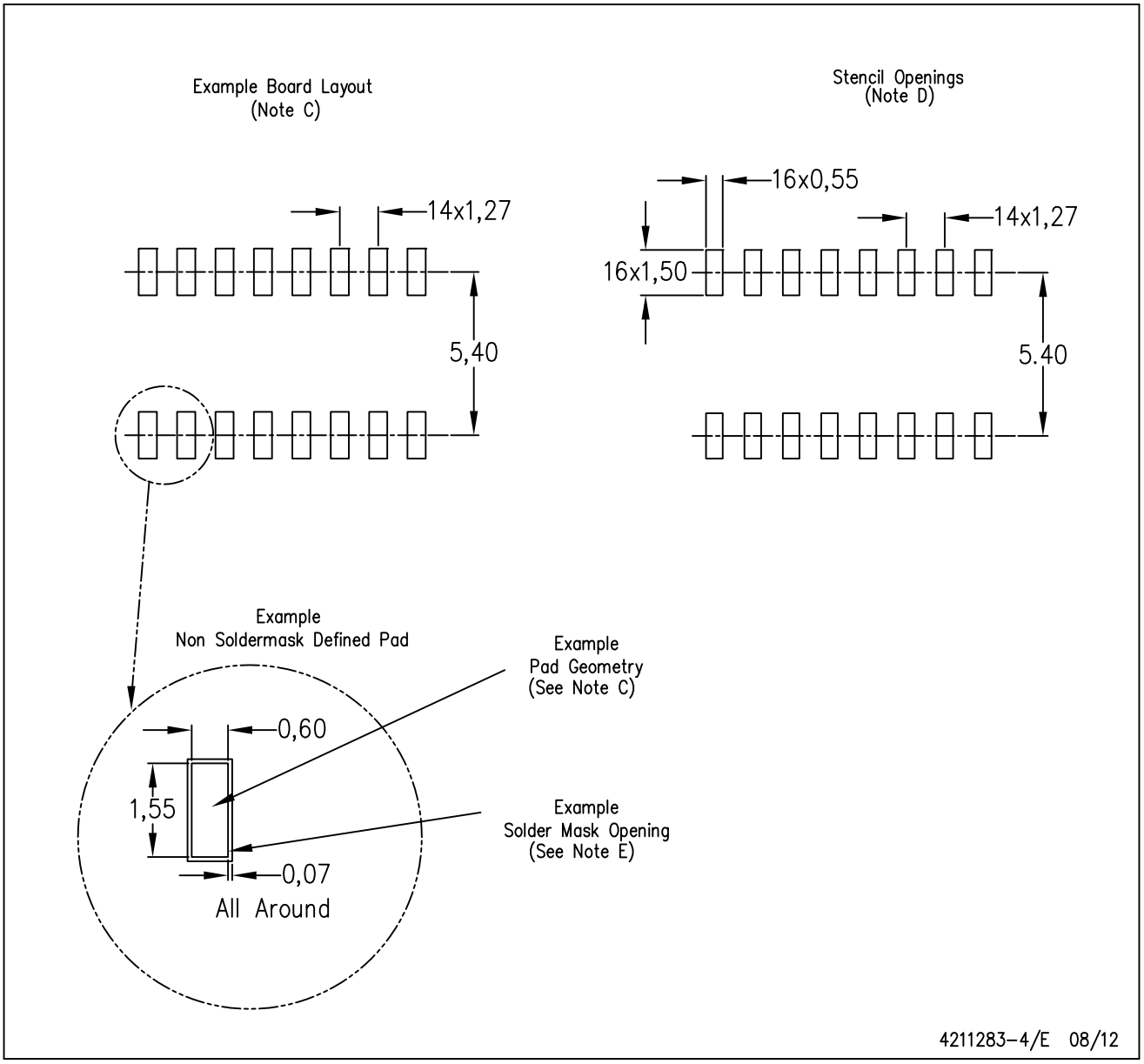
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

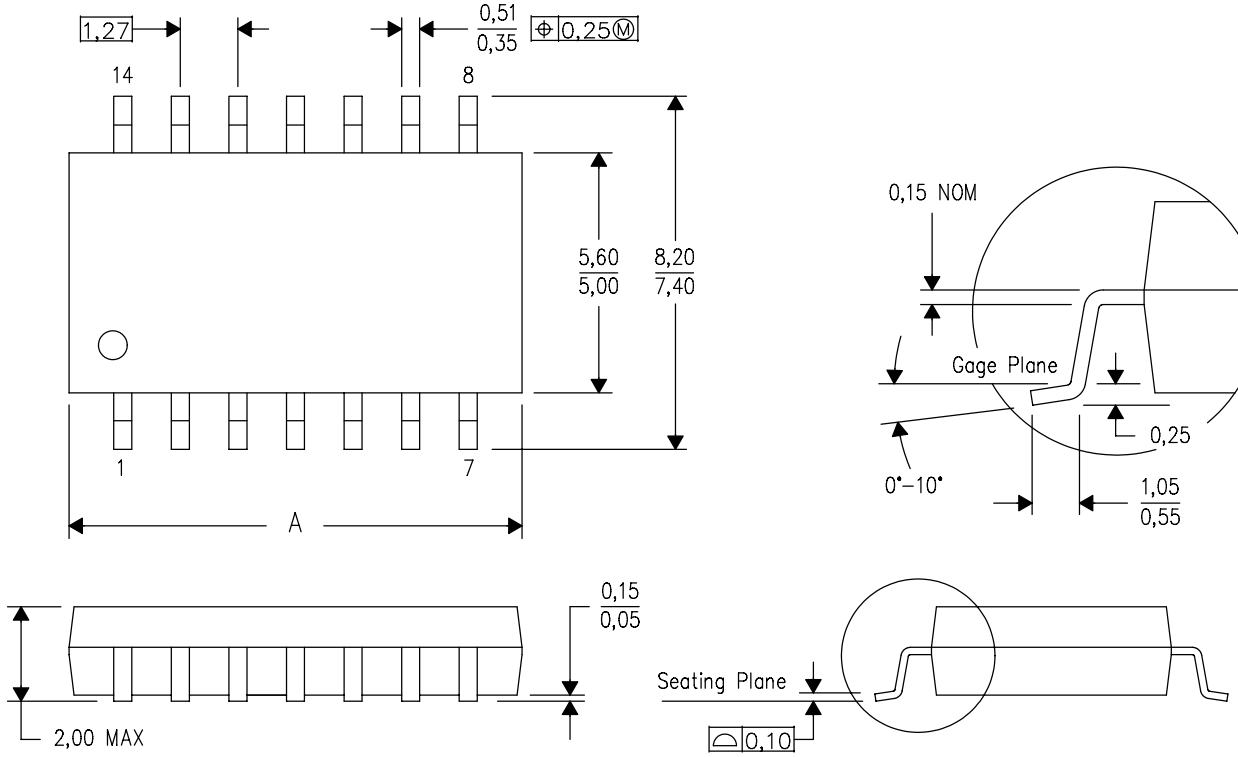



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

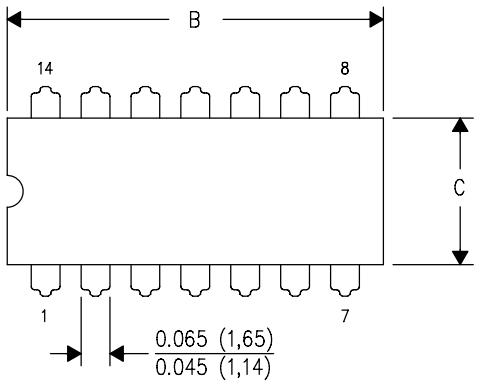
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

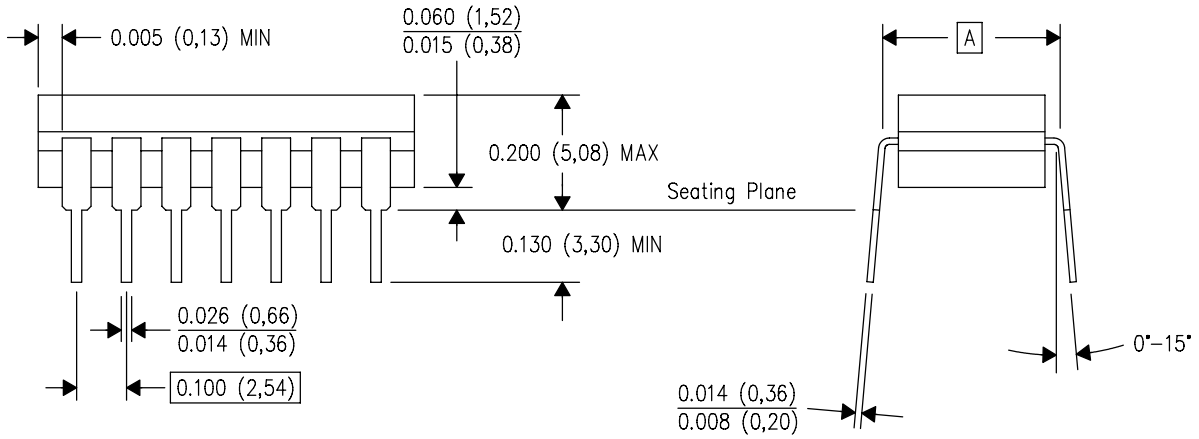
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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