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APPLICATION NOTE 394

HDLC Configuration of Framers and Transceivers

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Abstract: Application Note 394 contains guidelines showing how to use the necessary operation modes inside our framers, transceivers or single-chip transceivers (SCTs) to route HDLC data. This application note lists the register descriptions of different operation modes of our different framers and transceivers, enabling the user to select the proper configuration.

This application note applies to the following products:

FRAMERS		SCTs		
T1	**E1**	**T1**	**E1**	**T1/E1/J1**
DS21Q42	DS21Q44	DS21352	DS21354	DS2155
DS21FT42	DS21FT44	DS21552	DS21554	DS2156
DS21FF42	DS21FF44	DS21Q352	DS21Q354	DS21Q55
		DS21Q552	DS21Q554	DS21E55

1. DS21352, DS21552, and DS21Q42

The DS21352, DS21552, and DS21Q42 have the ability to route the HDLC data through the facilities data link (FDL) via a single DS0 or multiple DS0s. Table 1-1 shows the registers used for selecting HDLC operational mode. While the HDLC transmitter can be disabled, the HDLC receiver cannot. If operation of the HDLC receiver is not desired, it can be ignored without affecting the system.

Table 1-1. HDLC Control Registers

REGISTER	HDLC ADDRESS	FUNCTION
TDC1	0x92	Transmit HDLC control register #1
RDC1	0x90	Receive HDLC control register #1
TBOC	0x07	Transmit BOC control register
TCR1	0x35	Transmit control register #1
TCBR1 ... TCBR3	0x32 ... 0x34	Transmit channel blocking registers/Transmit HDLC channel selection registers
RCBR1 ... RCBR3	0x6C ... 0x6E	Receive channel blocking registers/Receive HDLC channel selection registers

The following tables list the different configurations that exist for the HDLC inside the DS21352, DS21552, and DS21Q42 devices. Throughout this section, the terms DS0, time slot, and channel refer to a single 64kbps data stream and can be used interchangeably.

HDLC Transmit Configuration

Table 1-2. Transmit control register mode selection

Mode	TDC1.7 TDS0E	TDC1.5 TDS0M	TBOC.6 HBEN	TCR1.2 TFDLS	FUNCTION
0	0	X	0	X	Disable transmit HDLC
1	0	X	1	1	HDLC routed through the FDL
2	1	0	0	X	HDLC routed through a single DS0
3	1	1	0	X	HDLC routed through multiple DS0s

X = don't care

Table 1-3. Transmit control register bit and channel selection

Mode	TDC1.4 TD4	TDC1.3 TD3	TDC1.2 TD2	TDC1.1 TD1	TDC1.0 TD0	FUNCTION
1	Sa4	Sa5	Sa6	Sa7	Sa8	Sa bit routing defined by TD4-TD0
2	Bit4	Bit3	Bit2	Bit1	Bit0	DS0 routing defined by TD4-TD0
3	X	X	X	X	X	DS0s routing defined by TCBR1-TCBR4

X = don't care

HDLC Receive Configuration

Table 1-4. Receive control register mode selection

Mode	RDC1.7 RDS0E	RDC1.5 RDS0M	FUNCTION
0	0	X	HDLC routed through the FDL
1	1	0	HDLC routed through a single DS0
2	1	1	HDLC routed through multiple DS0s

X = don't care

Table 1-5. Receive control register bit and channel selection

Mode	TDC1.4 RD4	TDC1.3 RD3	TDC1.2 RD2	TDC1.1 RD1	TDC1.0 RD0	FUNCTION
0	X	X	X	X	X	HDLC routed through the FDL
2	Bit4	Bit3	Bit2	Bit1	Bit0	DS0 routing defined by RD4-RD0
3	X	X	X	X	X	DS0s routing defined by RCBR1-RCBR4

X = don't care

Legacy FDL Configuration

When using the internal HDLC and BOC controller to route data through the FDL, the legacy FDL circuitry should be disabled. Table 1-6 shows a listing of the legacy FDL registers and how to program them to disable legacy FDL operation.

Table 1-6. Legacy FDL Control Registers

REGISTER	NAME	VALUE	FUNCTION
TCR1.2	TFDLS	1	Source FDL data from the HDLC and BOC controller
TBOC.6	HBEN	1	Enable HDLC and BOC controller
CCR2.5	TSLC96	0	Disable SLC-96 and D4 Fs-bit insertion
CCR2.4	TFDL	0	Disable legacy transmit FDL zero destuffer
CCR2.1	RSLC95	0	Disable SLC-96 reception
CCR2.0	RZSE	0	Disable legacy receive FDL zero destuffer
IMR2.4	RFDL	0	Disable legacy receive FDL buffer full interrupt
IMR2.3	TFDL	0	Disable legacy transmit FDL zero stuffer
IMR2.2	RMTCH	0	Disable legacy FDL match interrupt
IMR2.1	RAF	0	Disable legacy FDL abort interrupt

2. DS21354, DS21554, DS21Q44

The DS21354, DS21554, and DS21Q44 can route the HDLC data through the Sa bit positions (Sa4 to Sa8) via a single DS0 or multiple DS0s. Operational mode selection of the HDLC is accomplished using the registers described in Table 2-1. While the HDLC transmitter can be disabled, the HDLC receiver cannot. If operation of the HDLC receiver is not desired, it can be ignored without affecting the system.

Table 2-1. HDLC Control Registers

REGISTER	HDLC ADDRESS	FUNCTION
TDC1	0xBA	Transmit HDLC control register #1
RDC1	0xB8	Receive HDLC control register #1
RCR2	0x11	Receive control register #2
TCBR1 ... TCBR4	0x22 ... 0x25	Transmit channel blocking registers/Transmit HDLC channel selection registers
RCBR1 ... RCBR4	0x2B ... 0x2E	Receive channel blocking registers/Receive HDLC channel selection registers

The tables below list the different configurations that exist for the HDLC inside the DS21354, DS21554, and DS21Q44 devices. Throughout this section, the terms DS0, time slot, and channel refer to a single 64kbps data stream and can be used interchangeably.

HDLC Transmit Configuration

Table 2-2. Transmit control register mode selection

Mode	TDC1.7 THE	TDC1.6 TSaDS	TDC1.5 TDS0M	FUNCTION
0	0	X	X	Disable transmit HDLC
1	1	0	X	HDLC routed through the Sa bits
2	1	1	0	HDLC routed through a single DS0
3	1	1	1	HDLC routed through multiple DS0s

X = don't care

Table 2-3. Transmit control register bit and channel selection

Mode	TDC1.4 TD4	TDC1.3 TD3	TDC1.2 TD2	TDC1.1 TD1	TDC1.0 TD0	FUNCTION
1	Sa4	Sa5	Sa6	Sa7	Sa8	Sa bit routing defined by TD4-TD0
2	Bit4	Bit3	Bit2	Bit1	Bit0	DS0 routing defined by TD4-TD0
3	X	X	X	X	X	DS0s routing defined bt TCBR1-TCBR4

X = don't care

HDLC Receive Configuration

Table 2-4. Receive control register mode selection

Mode	RDC1.7 RHS	RDC1.6 RSaDS	RDC1.5 RDS0M	FUNCTION
0	0	X	X	HDLC routed through the Sa bits with RLCLK active
1	1	0	X	HDLC routed through the Sa bits
2	1	1	0	HDLC routed through a single DS0
3	1	1	1	HDLC routed through multiple DS0s

X = don't care

Table 2-5. Receive control register bit and channel selection

Mode	TDC1.4 RD4	TDC1.3 RD3	TDC1.2 RD2	TDC1.1 RD1	TDC1.0 RD0	FUNCTION
0	X	X	X	X	X	Sa bit routing defined by RCR2.3-RCR2.7
1	Sa4	Sa5	Sa6	Sa7	Sa8	Sa bit routing defined by RD4-RD0
2	Bit4	Bit3	Bit2	Bit1	Bit0	DS0 routing defined by RD4-RD0
3	X	X	X	X	X	DS0s routing defined by RCBR1-RCBR4

X = don't care

3. DS21354, DS21554, and DS21Q44; DS21352, DS21552, and DS21Q42

HDLC General Time Slot Configuration

When using the HDLC to route data through a single time slot or multiple time slots, there are two ways to assign which of the 32 time slots carry data. When only using a single time slot to route data, it can be defined by the TD4-TD0 and RD4-RD0 bits in the TDC1 and RDC1 registers, respectively. When using multiple time slots to route data, the channel blocking registers TCHBLK and RCHBLK are used for assigning which time slots are used for routing data.

In addition to controlling which time slots data is routed through, any combination of bits within the time slots can be blocked to limit data flow in the time slots. This is accomplished by configuring the transmit and receive HDLC control registers #2 (TDC2 at address 0x93 and RDC2 at address 0x91) to block the unused bits. See Tables 3-1 and 3-2 for details about blocking unused bits in each time slot.

Table 3-1. Transmit HDLC DS0 bit suppression

TDC2.7	TDC2.6	TDC2.5	TDC2.4	TDC2.3	TDC2.2	TDC2.1	TDC2.0	FUNCTION
TDB8	TDB7	TDB6	TDB4	TDB3	TDB2	TDB1	TDB0	
A	A	A	A	A	A	A	A	DS0 Block Bits

A = 0 (active), 1 (inactive)

Table 3-2. Receive HDLC DS0 bit suppression

RDC2.7	RDC2.6	RDC2.5	RDC2.4	RDC2.3	RDC2.2	RDC2.1	RDC2.0	FUNCTION
RDB8	RDB7	RDB6	RDB4	RDB3	RDB2	RDB1	RDB0	
A	A	A	A	A	A	A	A	DS0 Block Bits

A = 0 (active), 1 (inactive)

4. DS2155 and DS2156

The DS2155 and DS2156 have two HDLC controllers that have the ability to route the HDLC data through data via the FDL in T1 mode, the Sa bit positions (Sa4 to Sa8) in E1 mode, via a single DS0, or multiple DS0s. The two HDLC controllers, HDLC #1 and HDLC #2, are independently controlled by two sets of identical registers. Selection for the HDLC operation mode is accomp lished using the registers described in Table 4-1.

Table 4-1. HDLC control registers

REGISTER	HDLC #1 ADDRESS	HDLC #2 ADDRESS	FUNCTION
HxTC	0x90	0xA0	Transmit HDLC control register
HxRC	0x31	0x32	Receive HDLC control register
HxTTSBS	0x9B	0xAB	Transmit HDLC Sa/DS0 bit selection register
HxRTSBS	0x96	0xA6	Receive HDLC Sa/DS0 bit selection register
HxTCS1 ... HxTCS4	0x97 ... 0x9A	0xA7 ... 0xAA	Transmit HDLC channel selection registers
HxRCS1 ... HxRCS4	0x92 ... 0x95	0xA2 ... 0xA5	Receive HDLC channel selection registers

The tables below list the different configurations for the HDLC controllers inside the DS2155 and DS2156 devices. Throughout this section, the terms DS0, time slot, and channel refer to a single 64kbps data or voice stream and can be used interchangeably. It should also be noted that the two HDLC controllers should not be mapped simultaneously to the FDL in T1 mode, the same Sa bits in E1 mode, or the same time slots.

HDLC Transmit Configuration

Table 4-2. Transmit control register mode selection

MSTRREG.1	HxTC.4	HxTCS1/2/3/4	FUNCTION
T1/E1	THMS		
X	0	0x00	Disable transmit HDLC
0	1	NA	HDLC routed through the FDL
1	1	NA	HDLC routed through the Sa bits
X	0	CE	HDLC routed through single/multiple DS0

X = don't care, NA = not applicable, CE = channel enables

Table 4-3. Transmit HDLC Sa bit selection in E1 mode

HxTTSBS.7	HxTTSBS.6	HxTTSBS.5	HxTTSBS.4	HxTTSBS.3	HxTTSBS.2	HxTTSBS.1	HxTTSBS.0
TCB8SE	TCB7SE	TCB6SE	TCB5SE	TCB4SE	TCB3SE	TCB2SE	TCB1SE
X	X	X	Sa4	Sa5	Sa6	Sa7	Sa8

X = don't care; SaX = 0 (disable), 1 (enable)

Table 4-4. Transmit HDLC DS0 channel selection

MODE	HxTCS1	HxTCS2	HxTCS3	HxTCS4
	Channels 8-1	Channels 16-9	Channels 24-17	Channels 32-25
T1	CCCCCCCC	CCCCCCCC	CCCCCCCC	XXXXXXXX
E1	CCCCCCCC	CCCCCCCC	CCCCCCCC	CCCCCCCC

X = don't care; C = 0(deselect channel), 1 (select channel)

Table 4-5. Transmit HDLC DS0 bit suppression

HxTTSBS.7	HxTTSBS.6	HxTTSBS.5	HxTTSBS.4	HxTTSBS.3	HxTTSBS.2	HxTTSBS.1	HxTTSBS.0
TCB8SE	TCB7SE	TCB6SE	TCB5SE	TCB4SE	TCB3SE	TCB2SE	TCB1SE
A	A	A	A	A	A	A	A

A = 0 (active), 1 (inactive)

HDLC Receive Configuration

Table 4-6. Receive control register mode selection

MSTRREG.1	HxTC.4	HxTCS1/2/3/4	FUNCTION
T1/E1	THMS		
X	0	0x00	Disable transmit HDLC
0	1	NA	HDLC routed through the FDL
1	1	NA	HDLC routed through the Sa bits
X	0	CE	HDLC routed through single/multiple DS0

X = don't care, NA = not applicable, CE = channel enables

Table 4-7. Receive HDLC Sa bit selection in E1 mode

HxRTSBS.7	HxRTSBS.6	HxRTSBS.5	HxRTSBS.4	HxRTSBS.3	HxRTSBS.2	HxRTSBS.1	HxRTSBS.0
RCB8SE	RCB7SE	RCB6SE	RCB5SE	RCB4SE	RCB3SE	RCB2SE	RCB1SE
X	X	X	Sa4	Sa5	Sa6	Sa7	Sa8

X = don't care; SaX = 0 (disable), 1 (enable)

Table 4-8. Receive HDLC DS0 channel selection

MODE	HxRCS1	HxRCS2	HxRCS3	HxRCS4
	Channels 8-1	Channels 16-9	Channels 24-17	Channels 32-25
T1	CCCCCCCC	CCCCCCCC	CCCCCCCC	XXXXXXXX
E1	CCCCCCCC	CCCCCCCC	CCCCCCCC	CCCCCCCC

X = don't care; C = 0(deselect channel), 1 (select channel)

Table 4-9. Receive HDLC DS0 bit suppression

HxRTSBS.7	HxRTSBS.6	HxRTSBS.5	HxRTSBS.4	HxRTSBS.3	HxRTSBS.2	HxRTSBS.1	HxRTSBS.0
RCB8SE	RCB7SE	RCB6SE	RCB5SE	RCB4SE	RCB3SE	RCB2SE	RCB1SE
A	A	A	A	A	A	A	A

A = 0 (active), 1 (inactive)

Legacy FDL Configuration

When using the internal HDLC and BOC controller to route data through the FDL in T1 mode, the legacy FDL circuitry should be disabled. Table 22 shows a listing of the legacy FDL registers and how to program them to disable legacy FDL operation.

Table 4-10. Legacy FDL Control Registers

BITMAP	NAME	VALUE	FUNCTION
T1TCR1.2	TFDLS	1	Source FDL data from the HDLC controller
T1TCR2.6	TSCL96	0	Disable SLC-96 and D4 Fs-bit insertion
T1TCR2.5	TZSE	0	Disable legacy transmit FDL zero destuffer
T1RCR2.4	RSLC96	0	Disable SLC-96 reception
T1RCR2.3	RZSE	0	Disable legacy receive FDL zero destuffer
IMR8.3	RFDLF	0	Disable legacy receive FDL buffer full interrupt
IMR8.2	TFDLE	0	Disable legacy transmit FDL zero stuffer
IMR8.1	RMTCH	0	Disable legacy FDL match interrupt
IMR8.4	RFDLAD	0	Disable legacy FDL abort interrupt

DS21354	3.3V/5V E1 Single Chip Transceivers (SCT)	
DS2155	T1/E1/J1 Single-Chip Transceiver	Free Samples
DS21552	3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers	
DS21554	3.3V/5V E1 Single Chip Transceivers (SCT)	Free Samples
DS2156	T1/E1/J1 Single-Chip Transceiver TDM/UTOPIA II Interface	Free Samples
DS21FF42	4 x 4 16 Channel T1 Framer / 4 x 3 12 Channel T1 Framer	
DS21FF44	4x3 Twelve Channel E1 Framer / 4x4 Sixteen Channel E1 Framer	
DS21FT42	4 x 4 16 Channel T1 Framer / 4 x 3 12 Channel T1 Framer	
DS21FT44	4x3 Twelve Channel E1 Framer / 4x4 Sixteen Channel E1 Framer	Free Samples
DS21Q352	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q354	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q42	Enhanced Quad T1 Framer	
DS21Q44	Enhanced Quad E1 Framer	
DS21Q55	Quad T1/E1/J1 Transceiver	
DS21Q552	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q554	Quad T1/E1 Transceiver (3.3V, 5.0V)	

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