INVENTEK SYSTEMS

ISM4343-WBM-L151

System in Package

Module

802.11 b/g/n + 4.1 BT/BLE + Cortex M4

(BT/BLE 4.2 Secure Connection also supported)

Data Sheet

Table of Contents

1 PART NUMBER DETAIL DESCRIPTION 4
1.1 Ordering Information 4
2 OVERVIEW 4
3 FEATURES 5
3.1 Limitations 7
3.2 Regulatory Compliance 7
4 COMPLEMENTARY DOCUMENTATION 8
4.1 EVB 8
5 BLOCK DIAGRAM 8
6 HOST INTERFACES 9
6.1 UART Interface 9
7 ELECTRICAL SPECIFICATIONS 10
7.1 Absolute Maximum Ratings 10
7.2 Environmental Ratings 11
7.3 Recommended Operating Conditions and DC Characteristics 11
8 RF SPECIFICATIONS 12
8.1 Bluetooth RF Specifications 12
8.2 WLAN RF Specifications 13
8.3 Environmental Specifications 20
9 PIN OUT AND DESCRIPTIONS 21
9.1 Module Pin Number Sequence Definition 21
10 Additional Information 26
10.1 Communications Interfaces 26
10.1.1 I2C Interface Characteristics 26
10.1.2 SPI Interface Characteristics 28
10.1.3 TIM timer Interface Characteristics 29
10.1.4 I2S Timer Interface Characteristics 30
10.1.5 Controller Area Network (bxCAN) 30
11 Hardware Design Recommendations 31
11.1 Application Circuit – Single Antenna 31
11.2 Application Circuit –Antenna Diversity 32
11.3 Application Circuit –Power Supply 33
12 DC POWER CONDITIONING AND DISTRIBUTION 34
12.1 Power Conditioning 34
12.2 Power Distribution to Module 35
13 PCB LAYOUT GUIDELINES 36
13.1 DC Power 36
13.2 Antenna port RF signal 36
14 Mechanical Specification 38
14.1 Recommended PCB Footprint (Bottom View) 39
14.2 Recommended PCB Footprint (Top View) 40
14.3 Recommend Stencil: Unit: mm 45
15 Product Compliance Considerations 45
16 Reflow Profile 46

17 Packaging Information 47
17.1 MSL Level / Storage Condition 47
17.2 Device baking requirements prior to assembly 47
18 REVISION CONTROL 48
19 CONTACT INFORMATION 48

1 PART NUMBER DETAIL DESCRIPTION

1.1 Ordering Information

Device	Description	Ordering Number
ISM4343-WBM-L151	2.4 Wi-Fi + BT/BLE + Cortex M4 Module	ISM4343-WBM-L151
ISM4343-WBM-L151-EVB	2.4 Wi-Fi + BT/BLE Cortex M4 Module EVB (Evaluation Board)	ISM4343-WBM-L151-EVB

2 OVERVIEW

The Inventek ISM4343-WBM-L151 SoC (System on Chip), is a single-band IEEE 802.11 b,g,n-compliant MAC/PHY, and BT 4.1 radio. Channel bandwidth of 20MHz is supported for IEEE 802.11b,g,n traffic.

The ISM4343-WBM-L151 integrates clock, Wi-Fi/BT and front end into a small form factor 10x10 mm LGA Module. The ISM4343-WBM-L151 IEEE 802.11 b/g/n enables wireless connectivity to the simplest existing sensor products with minimal engineering effort. ISM4343-WBM-L151 reduces development time, lowers manufacturing costs, saves board space, simplifies certification compliance, and minimizes customer RF expertise required during development of target applications.

The ISM4343-WBM-L151 provides the highest level of integration for a wireless system, with integrated single band Wi-Fi and BT/BLE based on Cypress' WYW4343 IEEE802.11 b/g/n single-stream and BT/BLE 4.1 with support for antenna diversity and provisions for supporting future specifications. The ISM4343-WBM-L151 also supports BT 4.2LE Secure Connection via the Cypress stack. Integrated power amplifiers, LNAs and T/R switches for the 2.4 GHz WLAN band, are also included, greatly reducing the external part count, PCB footprint, and cost of the system solution.

The ISM4343-WBM-L151 module includes an ST Micro STM32F412 Cortex M4 MCU. SPI and UART interfaces enable easy connection to an embedded design. The ISM4343-WBM-L151 module requires no operating system. The ISM4343-WBM-L151 module also fully supports Cypress' WICED Platform SDK.

The ISM4343-WBM-L151 is compatible with the Bluetooth Low Energy operating mode, which provides a dramatic reduction in the power consumption of the Bluetooth radio and baseband. The primary application for this mode is to provide support for low data rate devices, such as sensors and remote controls.

The ISM4343-WBM-L151 implements the highly sophisticated Enhanced Collaborative Coexistence algorithms and hardware mechanisms, allowing for an extremely

collaborative Bluetooth coexistence scheme along with coexistence support for external radios such as cellular and LTE, GPS, and Ultra-Wideband. An independent, high-speed UART is provided for the Bluetooth host interface.

3 FEATURES

The ISM4343-WBM-L151 supports the following WLAN, Bluetooth & MCU functions:

- STM32 ARM 32-bit CortexTM-M4 with a frequency up to 100 MHz
  - 1 Mbyte of MCU internal Flash
  - 256KB of SRAM
  - SPI, Quad SPI (support Dual mode), USART, PCM
  - ADC, I2C, I2S, GPIO, Timers
  - JTAG
- Single-band 2.4 GHz b/g/n, 802.11b, 802.11g, 802.11n (single stream)
  - IEEE 802.11b 1 – 11 Mbps
  - IEEE 802.11g 6 – 54 Mbps
  - IEEE 802.11n (2.4 GHz) 7.2 – 150Mbps
- Support BT COEX
- WICED Fully compatible
- Host serial interface with UART, SPI, I2S, GPIO's
- On-chip WLAN driver execution capable of supporting IEEE 802.11 functionality
- Advanced 1x1 802.11n features:
  - Full/Half Guard Interval
  - Frame Aggregation
  - Space Time Block Coding (STBC)
  - Low Density Parity Check (LDPC) Encoding
- Hardware Encryption WEP, WPA/WPA2
- Modulation Modes include:
  - WiFi: CCK and OFDM with BPSK, QPSK, 16 QAM, 64QAM, 256QAM
  - BT: Dual-mode classic Bluetooth and Classic Low Energy operation
- Concurrent Bluetooth and WLAN operation
- Supports a single 2.4 GHz antenna shared between WLAN and Bluetooth
- BT host digital interface (can be used concurrently with above interface):
  - UART (up to 4 Mbps)
- Bluetooth v4.1 with integrated Class 1 PA
- Buletooth 2.1+EDR, Buletooth 3.0, Bluetooth 4.1 (Bluetooth Low Energy)
- Bluetooth v4.2LE Secure Connection via the Cypress BSA stack.
- ECI – enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- I²S/PCM for BT audio
- HCI high-speed UART (H4, H4 +, H5) transport support

- Bluetooth SmartAudio® technology improves voice and music quality to headsets
- Bluetooth low power inquiry and page scan
- Bluetooth Low Energy (BLE) support
- Bluetooth Packet Loss Concealment (PLC)
- Bluetooth Wide Band Speech (WBS)
- Operating Temperature: -40℃ to 85℃

The BBC supports all Bluetooth 4.0 features, with the following benefits:

- Dual-mode classic Bluetooth and classic Low Energy (BT and BLE) operation.
- Low Energy Physical Layer
- Low Energy Link Layer
- Enhancements to HCI for Low Energy
- Low Energy Direct Test mode
- AES encryption

3.1 Limitations

Inventek Systems products are not authorized for use in safety-critical applications (such as life support) where a failure of the Inventek Systems product would reasonably be expected to cause severe personal injury or death.

3.2 Regulatory Compliance

CE FCC

Regulator	Status
FCC	Pending
IC	Pending
RoHS	Compliant

Inventek is obtaining FCC, IC, and CE modular transmitter certifications for the ISM4343-WBM-L151 Module. These certifications can be used to the advantage of any manufacturer developing a product using these devices. In order to take full advantage of the certifications, developers must follow the antenna design/layout guidelines exactly as shown in the datasheet. For FCC compliance, products will still need to go through verification testing or have a declaration of conformance according to 47 CFR Chapter 1, part 15, subpart B.

The testing required for both verification and declaration of conformance is specified in sections 15.107 and 15.109. The official documents can be obtained from the U.S Government Printing Office online. U.S. Government Printing Office CFR 47. There are some changes allowed to the reference design which do not require any testing beyond the verification or declaration of conformance.

If it is desired to add a connector or U.FL connector in the RF path, or change the antenna to one of the same type (chip) with equal or less gain, they can do so without refiling. Other changes such as a different antenna, or adding an antenna diversity switch will require filing for a class 2 permissive change. Any class 2 permissive changes must be performed under Inventek's grant, and therefore must be done in cooperation with Inventek. In addition to this document, Inventek recommends verifying the schematic board design with Inventek Engineering once the schematic is complete for further review and validation.

4 COMPLEMENTARY DOCUMENTATION

4.1 EVB

- Evaluation Board
  - Evaluation Board Specification
  - EVB User's Guide
  - Design Guidelines

5 BLOCK DIAGRAM

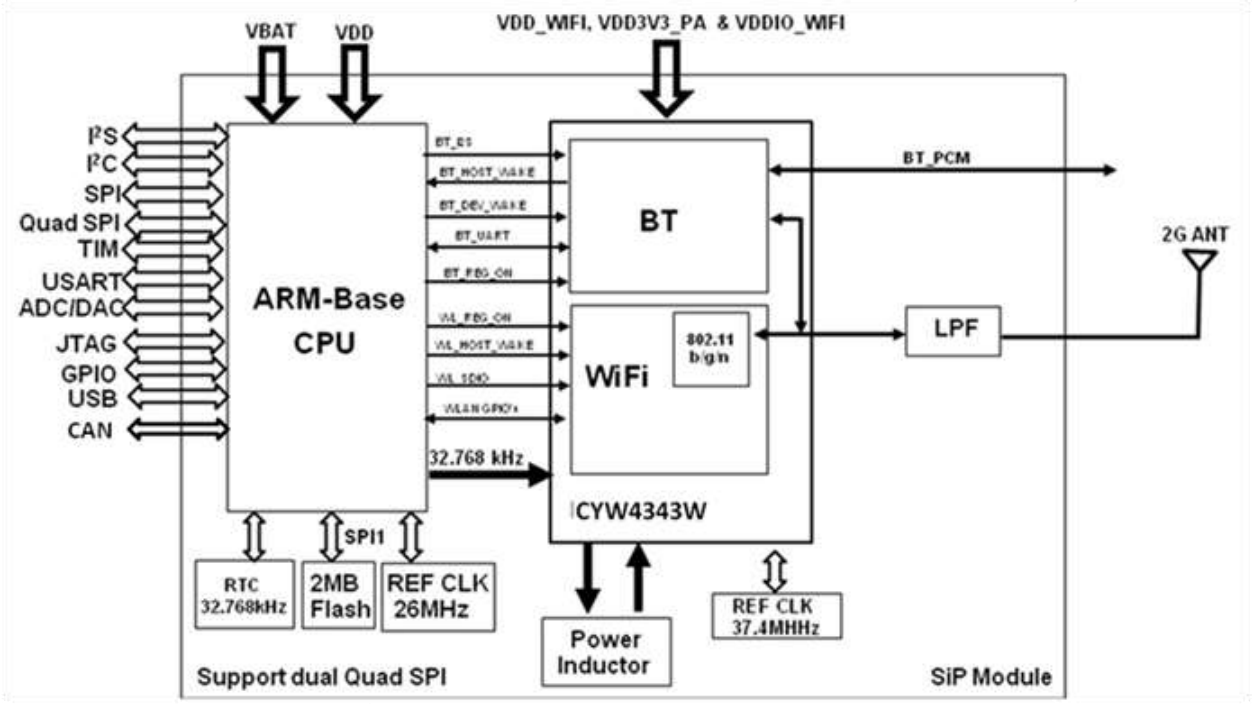


Figure 1 Inventek's ISM4343-WBM-L151 General Block Diagram

- **ADC**: Analog to Digital Converter
- **I2C**: Intelligent Interface Controller
- **SPI**: Serial Peripheral Interface
- **Quad SPI**: Quad Serial Peripheral Interface
- **USART**: Universal Synchronous/Asynchronous Receiver Transmitters
- **TIM**: Timers
- **I2S:** Inter-integrated Sound
- **CAN:** Controller Area Network

6 HOST INTERFACES

6.1 UART Interface

The ISM4343-WBM-L151 shares a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS and CTS) with adjustable baud rates from 9600 baud to 4.0 Megabaud. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

The UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFO is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.0 UART HCI specification: H4, a custom Extended H4 and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“Three-wire UART Transport Layer”). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The ISM4343-WBM-L151 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleet state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The ISM4343-WBM-L151 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2% (see Table 12).

Desired Rate	***Actual Rate***	***Error (%)***
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16

57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Table 1: Example of Common Baud Rates

7 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

⚠ **Caution!** The absolute maximum ratings in Table 28 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Rating	***Symbol***	***Value***	***Unit***
Power Supply	MAX	+4.0	V
Storage Temp	Celsius	-40 to +85	Degrees
Voltage Ripple	Ripple Voltage	+/- 2%	Max value not to exceed Operating Voltage
Power Supply Absolute Maximum Rating	VBAT	0 to 4	V
Power Supply Absolute Maximum Rating	VDD 3V3_1	0 to 4	V
Power Supply Absolute Maximum Rating	VDD 3V3_2	0 to 4	V
Power Supply Absolute Maximum Rating	VDD 3V3_3	0 to 4	V
Power Supply Absolute Maximum Rating	VDD 3V3_WiFi	0 to 6	V
Power Supply Absolute Maximum Rating	VDD 3V3_WiFi_PA	0 to 6	V
Power Supply Absolute Maximum Rating	VDDIO_WiFi	0 to 4	V

NOTE: Please place a 10-15uF Bulk CAP as close to the module as possible to VBAT.

Table 3: Absolute Maximum Ratings

7.2 Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (Ta)	-40 to +85	°C	* Functional operation
Storage Temperature	-40 to +125	°C	-
Relative Humidity (Non Condensing, relative humidity)	Less than 60	%	Storage
	Less than 85	%	Operation

Table 4: Environmental Ratings

7.3 Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 5 and operation outside these limits for extended periods can adversely affect long-term reliability of this devices.

Parameter	Symbol	Min	Typical	Max	Unit
MCU VBAT Voltage	VBAT	2.0	3.3	3.6	V
GPIO I/O Supply	VDD3V3_1	2.4	3.3	3.6	V
GPIO I/O Supply	VDD3V3_2	2.4	3.3	3.6	V
GPIO I/O Supply	VDD3V3_3	2.4	3.3	3.6	V
WiFi Voltage	VDD_3V3_WIFI	3.0	3.3	3.6	V
WiFi PA Voltage	VDD_3V3_WIFI_PA	3.0	3.3	3.6	V
MCU With WiFi	VDDIO_WIFI	3.0	3.3	3.6	V

Table 5: Recommended Operating Conditions and DC Characteristics

a. *The ISM4343-WBM-L151 power supply will be provided by the host via the power pins.*

8 RF SPECIFICATIONS

8.1 Bluetooth RF Specifications

Note: *Values in this datasheet are design goals and are subject to change based on the results of device characterization.*

Unless otherwise stated, limit values apply for the condition specified in Table 4: "Environmental Ratings", Section 7.2 and Table 5: "Recommended Operating Conditions, and DC Characteristics", Section 7.5.

Parameter	***Conditions***	***Min***	***Typical***	***Max***	***Unit***
Note: The specifications in this table are measured at the Chip port output unless otherwise specified:					
General					
Frequency Range	-	2402	-	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	-	-93.5	-	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	-	-95.5	-	dBm
	8-DPSK, 0.01% BER, 3 Mbps	-	-89.5	-	dBm
Input IP3	-	-16	-	-	dBm
Maximum input at antenna	-	-	-	-20	dBm

Table 6: Bluetooth Receiver RF Specifications

Parameter	***Conditions***	***Min***	***Typical***	***Max***	***Unit***
General					
Frequency Range		2402	-	2480	MHz
Basic rate (GFSK) Tx power at Bluetooth	-	10.0	12.0	-	dBm
QPSK Tx Power at Bluetooth		7.0	9.0	-	dBm
8PSK Tx Power at Bluetooth		7.0	9.0	-	dBm
Power control step		2	4	6	dB

Table 7: Bluetooth Transmitter RF Specifications

Parameter: Bluetooth	Condition	Min	Typical	Max	Unit
Condition: 25 Deg. C, includes Wi-Fi and BT					
Tx Mode	3DH5		35		mA
Rx Mode	3DH5		16		mA

Table 8: Bluetooth Current Consumption (M4 MCU not calculated)

Parameter: Bluetooth Low Energy	Condition	Min	Typical	Max	Unit
Condition: 25 Deg. C, includes both Wi-Fi and BT					
Tx Mode	Transmitter and baseband are both operating, 100%		35		mA
Rx Mode	Receiver and baseband are both operating, 100%		16		mA

Table 9: BLE Current Consumption (M4 MCU not calculated)

8.2 WLAN RF Specifications

The ISM4343-WBM-L151 includes an integrated single-band direct conversion radio that supports the 2.4 GHz band.

> ***Note:*** *Values in the data sheet are design goals and are subject to change based on the results of device characterization.*

Unless otherwise stated, limit values apply for the condition specified in Table 4: “Environmental Ratings”, Section 7.2 and Table 5: “Recommended Operating Conditions, and DC Characteristics”, Section 7.5.

2.4 GHz Band General RF Specifications

Features	Description
WLAN Standards	IEEE 802 Part 11b/g/n (802.11b/g/n single stream n)
Antenna Port	Support Single Antenna for WiFi
Frequency Band	2.400 – 2.484 GHz (2.4 GHz ISM Band)
Number of selectable Sub channels	14 channels
Modulation	OFDM, DSSS (Direct Sequence Spread Spectrum), DBPSK, DQPSK, CCK , 16QAM, 64QAM, 256QAM

Supported rates	1,2, 5.5,11,6,9,12,24,36,48,54 Mbps & HT20 MCS 0~7
Maximum receive input level	- 10dBm (with PER < 8%@11 Mbps) - 20dBm (with PER < 10%@54 Mbps) - 20dBm (with PER < 10%@MCS7)
Output Power	17dBm @ 802.11b 13dBm @ 802.11g 12dBm @ 802.11n 10dBm @ 802.11n (256QAM)
Carrier Frequency Accuracy	+/- 20ppm (crystal: 26MHz +/-10ppm in 250C)

Item	***Conditions***	***Min***	***Typical***	***Max***	***Unit***
Tx/Rx switch time	Including TX ramp down	-	-	5	µs
Rx/Tx switch time	Including TX ramp up	-	-	2	µs
Power-up and power-down ramp time	DSSS/CCK Modulations	-	-	<2	µs

Table 10: 2.4 GHz Band General RF Specifications (default voltage is 3.3V)

WLAN 2.4 GHz Receiver Performance Specification

Parameter	***Condition/Notes***	***Min***	***Typical***	***Max***	***Unit***
Frequency Range	-	2400	-	2500	MHz
RX sensitivity (8% PER for 1024 octet PSDU)[a]	1 Mbps DSSS	-	-97.9	-	dBm
	2 Mbps DSSS	-	-96.9	-	dBm
	5.5 Mbps DSSS	-	-92.5	-	dBm
	11 Mbps DSSS	-	-90.7	-	dBm
RX sensitivity (10% PER for 1024 octet PSDU)[a]	6 Mbps OFDM	-	-92.7	-	dBm
	9 Mbps OFDM	-	-91.4	-	dBm
	12 Mbps OFDM	-	-89	-	dBm
	18 Mbps OFDM	-	-87.4	-	dBm
	24 Mbps OFDM	-	-84.4	-	dBm
	36 Mbps OFDM	-	-81.7	-	dBm
	48 Mbps OFDM	-	-78.3	-	dBm
	54 Mbps OFDM	-	-77.1	-	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a],[b] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates (GF)				
	MCS0	-	-92.6	-	dBm
	MCS 1	-	-89.6	-	dBm
	MCS 2	-	-87.3	-	dBm
	MCS 3	-	-84.7	-	dBm
	MCS 4	-	-82	-	dBm

	MCS 5	-	-78.4	-	dBm
	MCS 6	-	-76.9	-	dBm
	MCS 7	-	-75	-	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a],[b] Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates (GF)				
	MCS0	-	-91	-	dBm
	MCS 1	-	-87.5	-	dBm
	MCS 2	-	-85.5	-	dBm
	MCS 3	-	-83	-	dBm
	MCS 4	-	-80	-	dBm
	MCS 5	-	-.75	-	dBm
	MCS 6	-	-73.5	-	dBm
	MCS 7	-	-72	-	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a],[c] Defined for default parameters: Mixed mode-800n ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates (Mixed mode)				
	MCS0	-	-91	-	dBm
	MCS 1	-	-87.9	-	dBm
	MCS 2	-	-85.5	-	dBm
	MCS 3	-	-82.8	-	dBm
	MCS 4	-	-79.9	-	dBm
	MCS 5	-	-76.2	-	dBm
	MCS 6	-	-74.6	-	dBm
	MCS 7	-	-72.6	-	dBm
RX sensitivity (10% PER for 4096 octet PSDU)[a],[b] Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates (Mixed mode)				
	MCS0	-	-89.0	-	dBm
	MCS 1	-	-85.4	-	dBm
	MCS 2	-	-83.2	-	dBm
	MCS 3	-	-80.6	-	dBm
	MCS 4	-	-77.4	-	dBm
	MCS 5	-	-72.3	-	dBm
	MCS 6	-	-70.6	-	dBm
	MCS 7	-	-69.0	-	dBm

Table 11: WLAN 2.4 GHz Receiver Performance Specifications

802.11 b Receiver					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Receiver minimum input level sensitivity (PER< 8 %)	1Mbps	-80*	-93		dBm
	2Mbps	-80*	-91		dBm
	5.5Mbps	-76*	-89		dBm
	11Mbps	-76*	-86		dBm
Receiver maximum input level sensitivity (PER< 8 %)	1/2/5.5/11 Mbps	-10*			dBm

Table 12: WLAN 2.4 GHz 802.11b Receiver Performance Specifications

802.11g Receiver					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Receiver minimum input level sensitivity (PER<10 %)	6Mbps	-82*	-88		dBm
	9Mbps	-81*	-87		dBm
	12Mbps	-79*	-85		dBm
	18Mbps	-77*	-83		dBm
	24Mbps	-74*	-80.5		dBm
	36Mbps	-70*	-78.5		dBm
	48Mbps	-66*	-74		dBm
	54Mbps	-65*	-72		dBm
Receiver maximum input level (PER<10%)	6/9/12/18/24/36/48/54	-20*			dBm

Table 13: WLAN 2.4 GHz 802.11g Receiver Performance Specifications

802.11n Receiver					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Receiver minimum input level sensitivity (PER<10 %)	HT20, MCS0	-82*	-87.5		dBm
	HT20, MCS1	-79*	-84		dBm
	HT20, MCS2	-77*	-82		dBm
	HT20, MCS3	-74*	-80.5		dBm
	HT20, MCS4	-70*	-77		dBm
	HT20, MCS5	-66*	-72		dBm
	HT20, MCS6	-65*	-71		dBm
	HT20, MCS7	-64*	-70		dBm
	256-QAM R=3/4		-68		dBm
	256-QAM R=5/6		-66		dBm
Receiver maximum input level (PER<10%)	MSC0~MSC7	-20*			dBm

Table 14: WLAN 2.4 GHz 802.11n Receiver Performance Specifications

WLAN 2.4 GHz Transmitter Performance Specification

802.11b Transmit					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Transmit output power level	1M/2M/5.5M/11M		17		dBm
Transmit center frequency tolerance		-20	0	20	ppm
Transmit spectrum mask	Fc-22MHz<F<Fc-11MHz & Fc+11MHz<F<Fc+22MHz(1/2/5.5/11Mbps; channel 1~13)			-30*	dBr
	F<Fc-22MHz & F>Fc+22MHz(1/2/5.5/11Mbps; channel 1~13)			-50*	dBr
Transmit power -on	10% ~ 90 %		0.3	2*	us
Transmit power -down	90% ~ 10 %		1.5	2*	us
Transmit modulation accuracy	1/2/5.5/11 Mbps		-17	-10	dB

Table 15: WLAN 2.4 GHz 802.11b Transmit Performance Specifications

802.11g Transmit					
Item	Condition	Min.	Typ.	Max.	Unit
Transmit output power level	6M/9M/12M/18M/24M/36M/48M/54M		13		dBm
					dBm
					dBm
Transmit center frequency tolerance		-20	0	20	ppm
Transmit modulation accuracy	6Mbps			-5*	dB
	9Mbps			-8*	dB
	12Mbps			-10*	dB
	18Mbps			-13*	dB
	24Mbps			-16*	dB
	36Mbps			-19*	dB
	48Mbps			-22*	dB
	54Mbps			-25*	dB
Transmit spectrum mask	@ 11MHz			-20*	dBr
	@ 20MHz			-28*	dBr
	@ 30MHz			-40*	dBr

Table 16: WLAN 2.4 GHz 802.11g Transmit Performance Specifications

802.11n Transmit					
Item	Condition	Min.	Typ.	Max.	Unit
Transmit output power level	HT20 MCS 0~7		12		dBm
	HT20 MCS 7 (Turboqam)		10		dBm
Transmit center frequency tolerance		-20	0	20	ppm
Transmit modulation accuracy	HT20, MCS0~7			-27*	dB
	HT20 MCS 7 (Turboqam)			-32*	dB
Transmit Spectrum mask	@ 11MHz			-20*	dBr
	@ 20MHz			-28*	dBr
	@ 30MHz			-40*	dBr

Table 17: WLAN 2.4 GHz 802.11m Transmit Performance Specifications

BT Transmitter Performance Specification

Parameter	Mode and Condition	Min.	Typ.	Max.	Unit
Transmitter Section					
Frequency Range		2402		2480	MHz
Output power	GFSK		10		dBm
	QPSK		6		dBm
	BPSK		6		dBm
Power control step		2	4	8	dB
Lo performance					
Initial carrier frequency tolerance			±25	±75	kHz
Lock Time			72		µs
Frequency Drift					
DH1 packet			± 8	± 25	kHz
DH3 packet			± 8	± 40	kHz
DH5 paclet			± 8	± 40	kHz
Drift rate			5	20	kHz/50µs
Frequency Deviation					
00001111 sequence in payload[a]		140	155	175	kHz
10101010 sequence in payload[b]		115	140		kHz
Channel spacing			1		MHz

- This pattern represents an average deviation in payload.
- Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Table 18: BT Transmit Performance Specifications

Parameter	Mode and Condition	Min.	Typ.	Max.	Unit
Receiver Section					
Frequency Range		2402		2480	MHz
Output power	GFSK,0.1% BER, 1Mbps		-91		dBm
	π/4-DQPSK,0.01% BER, 2Mbps		-93		dBm
	8-DPSK, 0.01% BER, 3Mbps		-87		dBm
Input IP3		-16			dBm
Maximum input				-20	dBm

Table 19: BT Receiver Performance Specifications

Parameter	Mode and Condition	Min.	Typ.	Max.	Unit
Frequency Range		2402		2480	MHz
RX Sense[a]	GFSK,0.1% BER, 1Mbps		-94		dBm
TX Power			8		dBm
Mod char: delta f1 average		225	225	275	kHz
Mod char: delta f2 max[b]		99.9			%
Mod char: ratio		0.8	0.95		%

- The Bluetooth tester is set so that Dirty TX is on.
- At least 99.9% of all delta F2 max. Frequency values recorded over 10 packets must be greater than 185kHz.

Table 20: BLE RF Performance Specifications

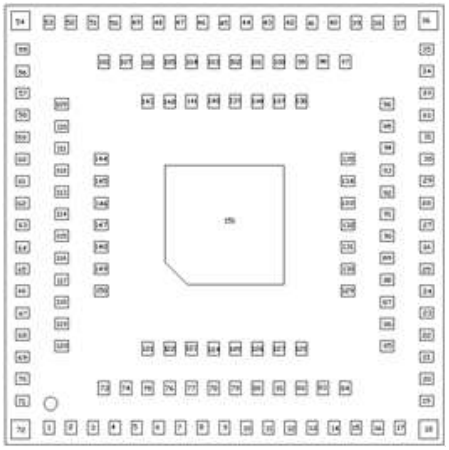
8.3 Environmental Specifications

Item	Description
Operating temperature range	-40 deg. C to +85 deg. C
Storage temperature range	-40 deg. C to +125 deg. C
Humidity (Non Condensing, relative humidity)	Less than 60% max for Storage Less than 85% max for Operation

Note 1: The ISM4343-WBM-L151 supports a functional operating range of -40°C to +85°C. However, the optimal RF performance specified in this data sheet is only guaranteed for temperatures from -10°C to +65°C

9 PIN OUT AND DESCRIPTIONS

9.1 Module Pin Number Sequence Definition



Top View

Pin Number	Pin Name	type	Description	Mapping for STM32F412 Packaged Datasheet
1	ANT	I/O	RF transmitter output and RF receiver input	
2	GND	-	Ground	
3	VDD_3V3_Wifi_PA	PI	Wi-Fi PA power supply	
4	VDD_3V3_Wifi_PA	PI	Wi-Fi PA power supply	
5	GND	-	Ground	
6	VDD_3V3_5	PI	DC supply for MCU and I/O	
7	GND	-	Ground	
8	MICRO_SPI1_MOSI	I/O	MCU_SPI_MOSI	PA7
9	QUADSPI_CLK	I/O	QUADSPI_CLK	PB1
10	GND	-	Ground	
11	MICRO_SPI4_NSS	I/O	MCU_SPI4_NSS	PE11
12	MICRO_SPI4_SCK	I/O	MCU_SPI4_SCK form MCU	PE12
13	MICRO_SPI4_MISO	I/O	MCU_SPI4_MISO	PE13
14	MICRO_SPI4_MOSI	I/O	MCU_SPI4_MOSI	PE14
15	GND	-	Ground	
16	NC	-	Floating	
17	NC	-	Floating	
18	GND	-	Ground	
19	NC	-	Floating	

Pin Number	Pin Name	type	Description	Mapping for STM32F412 Packaged Datasheet
20	BT_GPIO_3	I/O	WPT_INTb to wireless charging PMU	
21	MICRO_SPI2_MISO	I/O	MICRO_SPI2_MISO	PB14
22	MICRO_SPI2_MOSI	I/O	MICRO_SPI2_MOSI	PB15
23	GND	-	Ground	
24	VDD_3V3_3	PI	DC supply for MCU and I/O	
25	GND	-	Ground	
26	NC	-	Floating	
27	GND	-	Ground	
28	VDD3V3_WiFi_IO	PI	DC supply for WIFI and I/O	
29	GND	-	Ground	
30	MICRO_USART1_TX	I/O	MCU_USART1_TX	PA9
31	MICRO_USART1_RX	I/O	MCU_USART1_RX	PA10
32	MICRO_USART1_CTS	I/O	MCU_USART1_ CTS	PA11
33	MICRO_USART1_RTS	I/O	MCU_USART1_ RTS	PA12
34	GND	-	Ground	
35	MICRO_JTAG_TMS	I/O	MCU_JATG_TMS	PA13
36	GND	-	Ground	
37	MICRO_JTAG_TCK	I/O	MCU_JATG_TCK	PA14
38	MICRO_JTAG_TDI	I/O	MCU_JATG_TDI	PA15
39	GND	-	Ground	
40	NC	-	Floating	
41	GND	-	Ground	
42	VDD3V3_WiFi	PI	Wi-Fi power supply	
43	VDD3V3_WiFi	PI	Wi-Fi power supply	
44	GND	-	Ground	
45	MICRO_JTAG_TDO	I/O	MCU_JATG_TDO	PB3
46	MICRO_JTAG_TRSTN	I/O	MCU_JATG_RSTN	PB4
47	GND	-	Ground	
48	VDD_3V3_2	PI	DC supply for MCU and I/O	
49	GND	-	Ground	
50	QUADSPI_BK1_IO3	I/O	QUADSPI_BK1_IO3	PF6
51	GND	-	Ground	
52	NC	-	NC	
53	NC	-	NC	
54	GND	-	Ground	
55	BT_PCM_CLK	I/O	PCM clock; can be master	

			(output) or slave (input)	
56	NC	-	Floating	
57	BT_HOST_WAKE	O	BT_HOST_WAKE	
58	GND	-	Ground	
59	VBAT	PI	Power supply for backup circuitry when VDD is not present	
60	GND	-	Ground	
61	GND	-	Ground	
62	NC	-	Floating	
63	NC	-	Floating	
64	GND	-	Ground	
65	VDD_3V3	PI	DC supply for MCU and I/O	
66	GND	-	Ground	
67	QUADSPI_BK1_IO1	I/O	QUADSPI_BK1_IO1	PF9
68	QUADSPI_BK1_IO2	I/O	QUADSPI_BK1_IO2	PF7
69	MICRO_I2S2_SD	I/O	MICRO_I2S2_SD	PC3
70	GND	-	Ground	
71	GND	-	Ground	
72	GND	-	Ground	
73	GND	-	Ground	
74	MICRO_SPI1_NSS	I/O	MCU_SPI_NSS	PA4
75	MICRO_SPI1_SCK	I/O	MCU_SPI_SCK form MCU	PA5
76	MICRO_SPI1_MISO	I/O	MCU_SPI_MISO	PA6
77	GND	-	Ground	
78	QUADSPI_BK2_IO3	I/O	QUADSPI_BK2_IO3	PC5
79	BOOT1/ QUADSPI_CLK	I/O	BOOT1/ QUADSPI_CLK	PB2
80	QUADSPI_BK2_IO0	I/O	QUADSPI_BK2_IO0	PE7
81	QUADSPI_BK2_IO1	I/O	QUADSPI_BK2_IO1	PE8
82	MICRO_I2C2_SCL	I/O	MICRO_I2C2_SCL	PB10
83	MICRO_I2C2_SDA	I/O	MICRO_I2C2_SDA	PB11
84	MCIRO_SPI2_NSS	I/O	MCIRO_SPI2_NSS	PB12
85	MCIRO_SPI2_SCK	I/O	MCIRO_SPI2_SCK	PB13
86	MICRO_GPIO_27	I/O	MCU_GPIO	PD8
87	MICRO_GPIO_25	I/O	MCU_GPIO	PD10
88	NC	-	Floating	
89	NC	-	Floating	
90	VDD_USB	PI	VDD for USB	
91	GND	-	Ground	
92	MICRO_I2S2_MCK/ MICRO_USART6_TX	I/O	MICRO_I2S2_MCK/ MICRO_USART6_TX	PC6
93	MICRO_I2S2_CK/ MICRO_USART6_RX	I/O	MICRO_I2S2_CK/ MICRO_USART6_RX	PC7

94	GND	-	Ground	
95	NC	-	Floating	
96	NC	-	Floating	
97	NC	-	Floating	
98	NC	-	Floating	
99	GND	-	Ground	
100	NC	-	Floating	
101	GND	-	Ground	
102	MICRO_I2C1_SCL	I/O	MICRO_I2C1_SCL	PB6
103	MICRO_I2C1_SDA	I/O	MICRO_I2C1_SDA	PB7
104	BOOT0	O	Normal operation if connected to ground at power up.	BOOT0
105	NC	-	Floating	
106	MICRO_GPIO_0	I/O	MCU_GPIO	PE3
107	QUADSPI_BK2_NCS	I/O	QUADSPI_BK2_NCS	PC11
108	MICRO_GPIO_30	I/O	MCU_GPIO	PE0
109	NC	-	Floating	
110	NC	-	Floating	
111	MICRO_I2S_DI	I/O	MICRO_I2S_DI	PE5
112	GND	-	Ground	
113	GND	-	Ground	
114	GND	-	Ground	
115	GND	-	Ground	
116	GND	-	Ground	
117	MICRO_RST_N	I/O	MCU_RST_N	NRST
118	QUADSPI_BK1_IO0	I/O	QUADSPI_BK1_IO0	PF8
119	MICRO_WKUP	I/O	MCU_WKUP	PA0
120	GND	-	Ground	
121	MICRO_ADC_IN2	I/O	MCU_ADC_IN_2	PA2
122	MICRO_ADC_IN3	I/O	MCU_ADC_IN_3	PA3
123	GND	-	Ground	
124	QUADSPI_BK2_IO2	I/O	QUADSPI_BK2_IO2	PC4
125	MICRO_GPIO_5	I/O	MCU_GPIO	PB0
126	RF_SW_CTRL	I/O	Antenna diversity control signal	
127	NC	-	Floating	
128	MICRO_GPIO_16	I/O	MCU_GPIO	PE15
129	BT_GPIO_4	I/O	BSC_SDA to/from wireless charging PMU.	
130	BT_GPIO_5	I/O	BSC_SCL from wireless charging PMU.	
131	NC	-	Floating	
132	GND	-	Ground	
133	QUADSPI_BK1_NCS	I/O	QUADSPI_BK1_NCS	PG6

134	GND	-	Ground	
135	GND	-	Ground	
136	NC	-	Floating	
137	MICRO_GPIO_26	I/O	MCU_GPIO	PD1
138	NC	-	Floating	
139	NC	-	Floating	
140	NC	-	Floating	
141	NC	-	Floating	
142	MICRO_GPIO_28	I/O	MCU_GPIO	PB8
143	MICRO_I2S2_WS	I/O	MICRO_I2S2_WS	PB9
144	BT_PCM_SYNC	I/O	PCM Sync; can be master(output) or slave (input)	
145	BT_PCM_OUT	O	PCM data output	
146	BT_PCM_IN	I	PCM data input sensing	
147	PC13	I/O		PC13
148	GND	-	Ground	
149	GND	-	Ground	
150	MICRO_ADC_IN1	I/O	MCU_ADC_IN_1	PA1
151	GND	-	Ground	

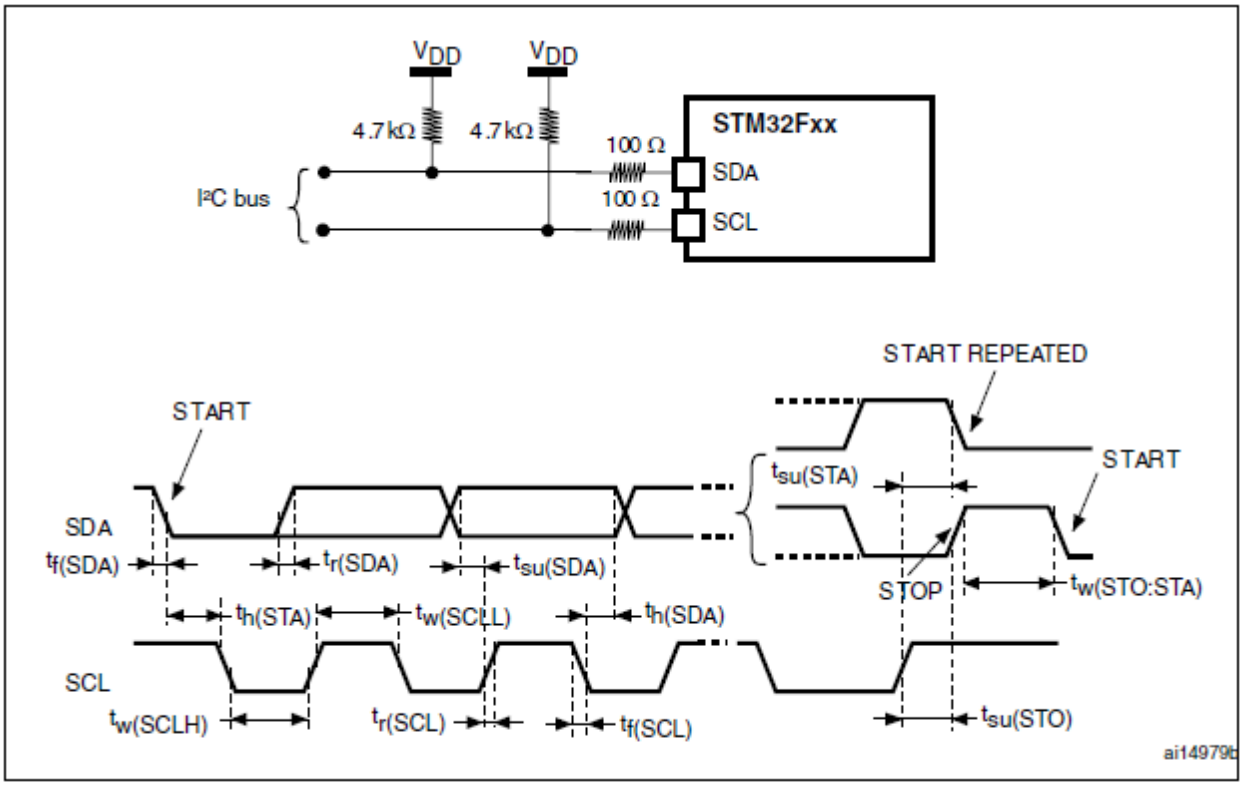
10 Additional Information

10.1 Communications Interfaces

10.1.1 I2C Interface Characteristics

Symbol	Parameter	Standard mode I²C(1)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	3450(3)	0	900(4)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard fast mode	0	50(5)	0	50(5)	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. fPCLK1 must be at least 2 MHz to achieve standard mode I2C frequencies. It must be at least 4MHz to achieve fast mode I2C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

10.1.2 SPI Interface Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master full duplex/receiver mode, 2.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	42	MHz
		Master full duplex/receiver mode, 3.0 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Master transmitter mode 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Master mode 1.7 V < V_{DD} < 3.6 V SPI1/2/3/4/5	-	-	25	
		Slave transmitter/full duplex mode 2.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	38(2)	
		Slave receiver mode, 1.8 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Slave mode, 1.8 V < V_{DD} < 3.6 V SPI1/2/3/4/5	-	-	25	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, SPI presc = 2	T_{PCLK}–1.5	T_{PCLK}	T_{PCLK} +1.5	ns
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$3T_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2T_{PCLK}$	-	-	ns
$t_{su(MI)}$	Data input setup time	Master mode	4	-	-	ns
$t_{su(SI)}$		Slave mode	2.5	-	-	ns
$t_{h(MI)}$	Data input hold time	Master mode	7.5	-	-	ns
$t_{h(SI)}$		Slave mode	3.5	-	-	ns

1. Guaranteed by characterization, not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(so)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sample edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ =0 while Duty(SCK)=50%

10.1.3 TIM timer Interface Characteristics

Symbol	Parameter	Conditions[3]	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 100 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 100 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 100 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	50	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	$f_{TIMxCLK}$ = 100 MHz	0.0119	780	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter		-	65536 x 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 100 MHz	-	51.1	S

1. TIMx is used as a general term to refer to the TIM1 to TIM11 timers.
2. Guaranteed by design, not tested in production.
3. The maximum timer frequency on APB1 is 50MHz and on APB2 is up to 100MHz by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4,then TIMxCLK = HCKL, otherwise TIMxCLK >= 4x PCLKx.

10.1.4 I2S Timer Interface Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	0	7	ns
$t_{h(WS)}$	WS hold time	Master mode	1.5	-	
$t_{su(WS)}$	WS setup time	Slave mode	1.5	-	
$t_{h(WS)}$	WS hold time	Slave mode	3	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_SR)}$		Slave receiver	2.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	7	-	
$t_{h(SD\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	6	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	2	-	

1. Guaranteed by characterization, not tested in production.
2. The maximum value of 256 x Fs is 50 MHz (APB1 maximum frequency).

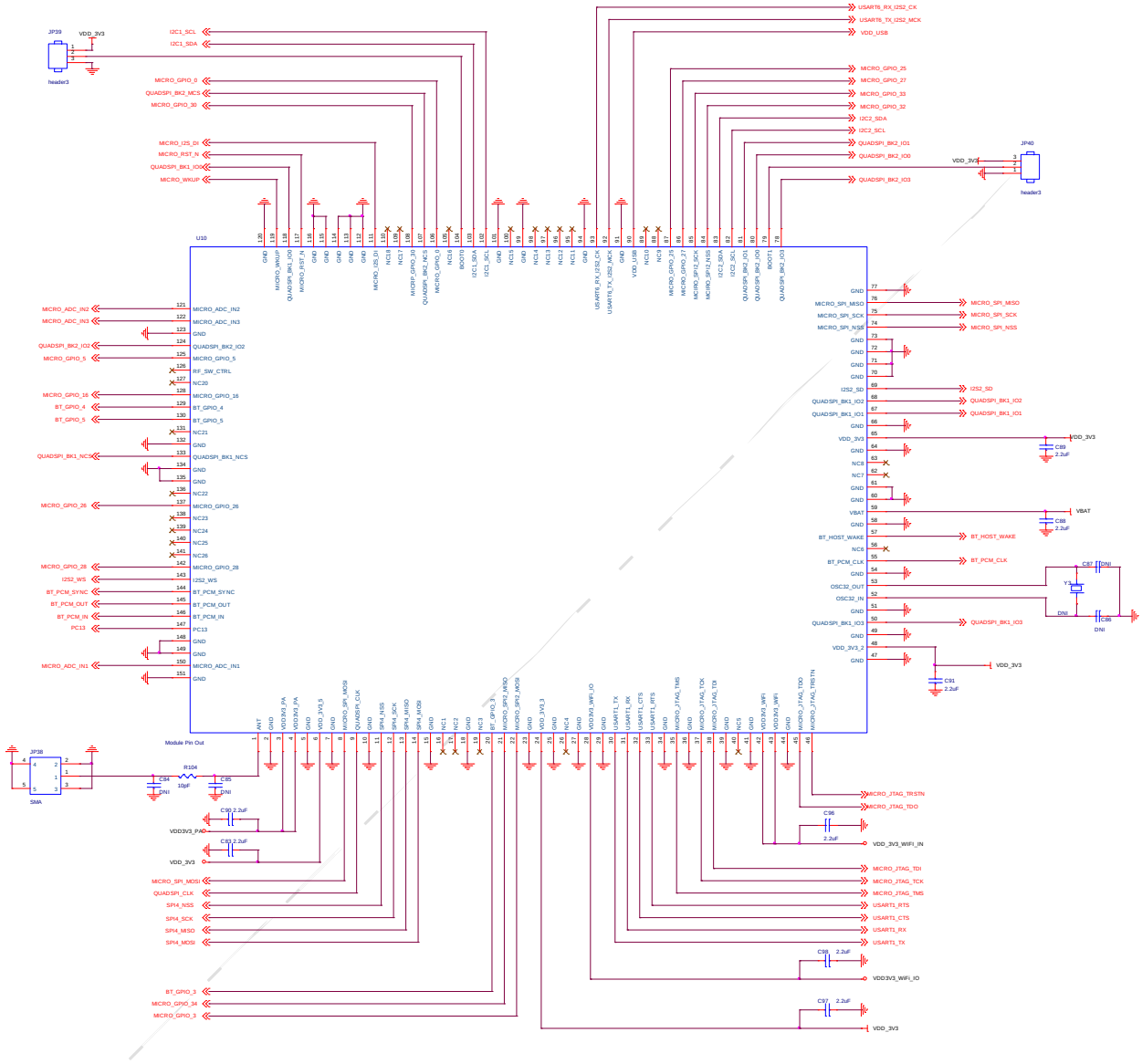
Note: Refer to the I2S section of RM0383 reference manual for more details on the sampling frequency (Fs). f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The value of these parameters might be slightly impacted by the source clock accuracy. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV / (2 x I2SDIV + ODD) and a maximum value of (I2SDIV + ODD) / (2 x I2SDIV + ODD). F_S maximum value is supported for each mode/condition.

10.1.5 Controller Area Network (bxCAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 byte of SRAM are allocated for each CAN.

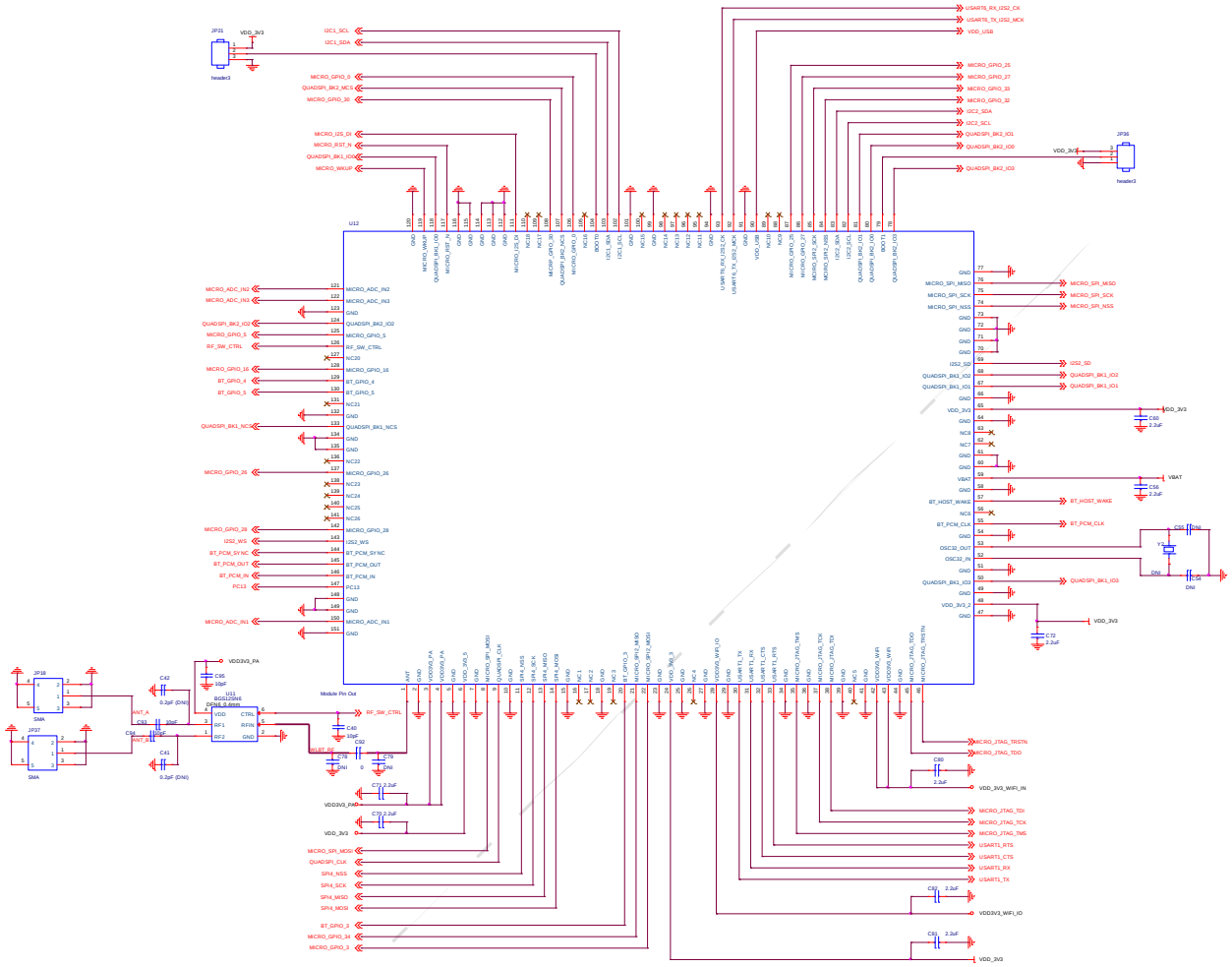
11 Hardware Design Recommendations

11.1 Application Circuit – Single Antenna



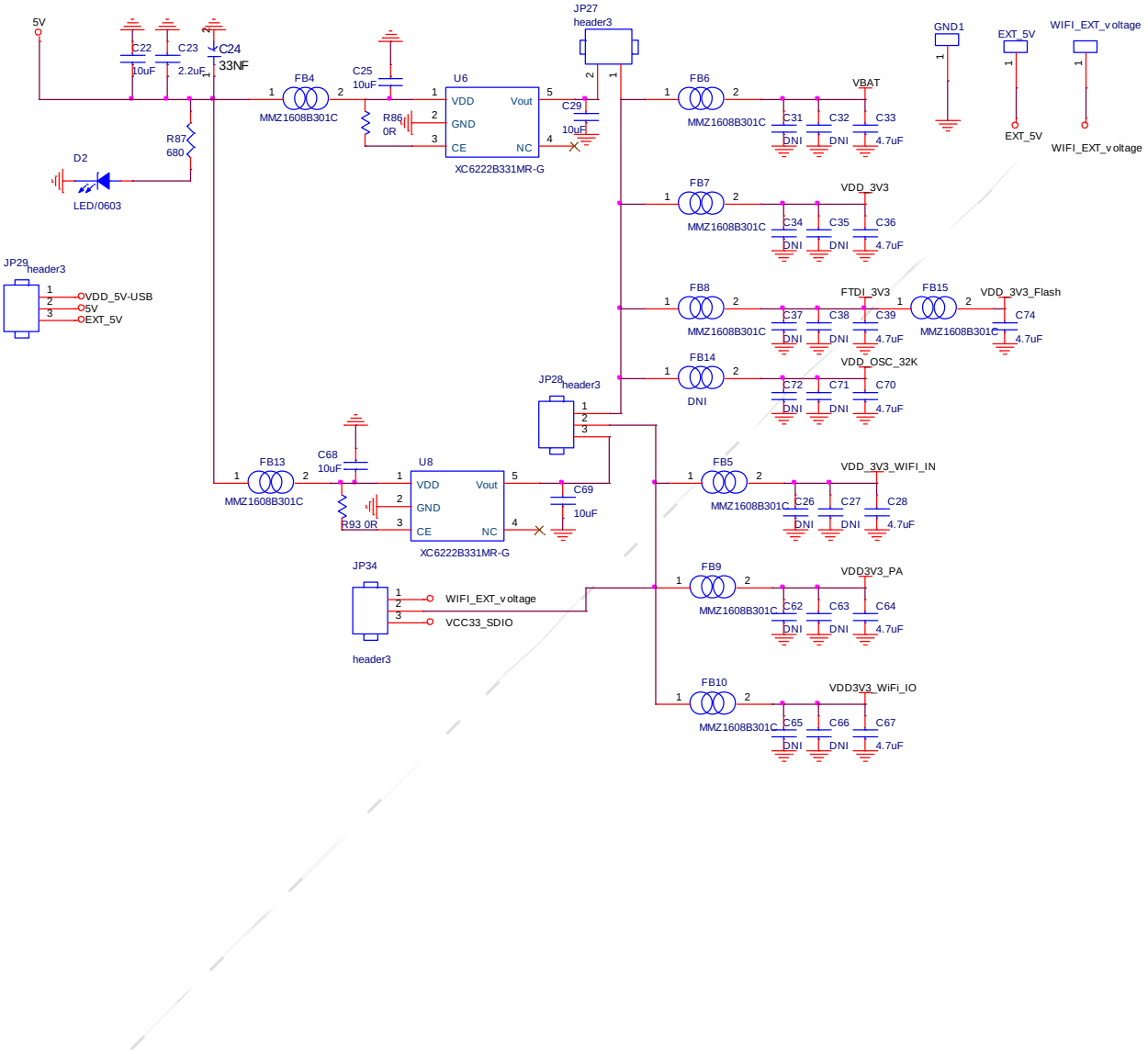
Reference Matching circuit:
1. RF trace impedance control: 50ohm.
2. Reference RF matching value (will be changed on customer's board)

11.2 Application Circuit –Antenna Diversity



Reference Matching circuit:
1. RF trace impedance control: 50ohm.
2. Reference RF matching value (will be changed on customer's board)

11.3 Application Circuit –Power Supply



12 DC POWER CONDITIONING AND DISTRIBUTION

Appropriate DC voltages are conditioned using the external power IC. Detailed performance specifications for the combo module and external power ICs are available in their respective device specifications as below.

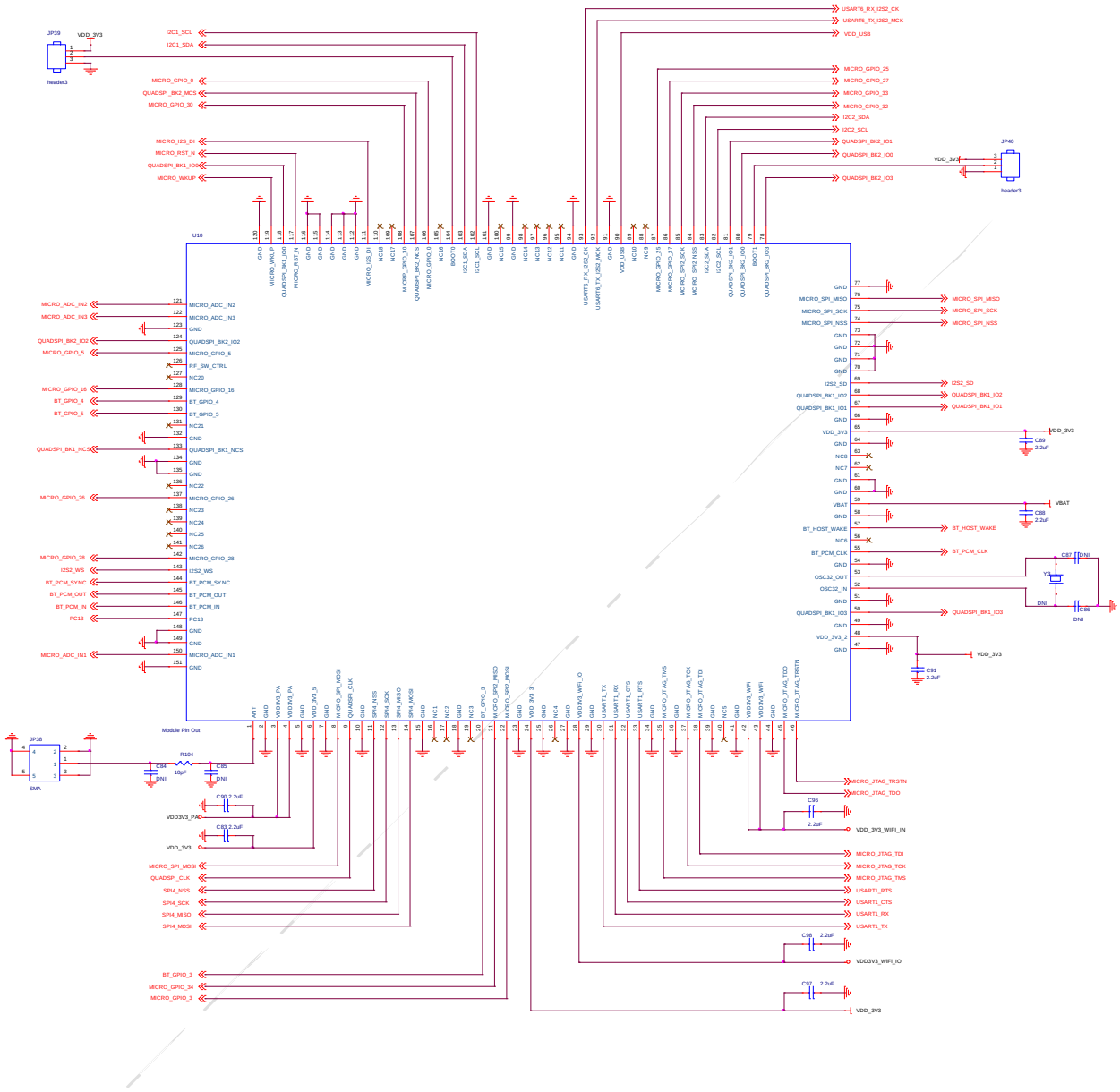
12.1 Power Conditioning

Symbol	Parameter	Min	Typ	Max	Unit
VBAT	MCU VBAT Voltage	2.0	3.3	3.6	V
VDD3V3_1	GPIO I/O Supply	2.4	3.3	3.6	V
VDD3V3_2	GPIO I/O Supply	2.4	3.3	3.6	V
VDD3V3_3	GPIO I/O Supply	2.4	3.3	3.6	V
VDD_3V3_WIFI	WiFi Voltage	3.0	3.3	3.6	V
VDD_3V3_WIFI_PA	WiFi PA Voltage	3.0	3.3	3.6	V
VDDIO_WIFI	MCU With WiFi	3.0	3.3	3.6	V

Each regulator output must be connected directly to its recommended output capacitor per the Power source. Additional filtering and bypassing of the RF supply voltages are described in the following sections

12.2 Power Distribution to Module

All the power supply pins should be decoupled as below.



13 PCB LAYOUT GUIDELINES

13.1 DC Power

Use wide traces for power supply lines. Know the maximum currents being carried on each power supply trace, and make the trace widths proportionate to the current (especially for long trace lengths). Where possible, fill large areas with copper to distribute the highest currents. These measures minimize IR drops, line inductance, and switching transients.

• Use several plated via holes to connect power supply traces between layers. The number of vias used should be proportional to the current being routed.

• Avoid loops in the supply distribution traces. Current-carrying loops are essentially antennas radiating electromagnetic fields that may corrupt transceiver performance or cause regulatory electromagnetic interference (EMI) test failures.

• High current traces should be kept as short as possible and devices on the same supply should be fed from a ‘star point’ rather than ‘daisy-chained’.

• Avoid loop in the VDD supply and clock supply traces, VDD supply traces and clock supply traces to be independent where possible.

13.2 Antenna port RF signal

General guidelines for routing RF signals of WLAN/BT antenna port. RF signals require controlled-impedance lines to minimize mismatch losses and efficiently transfer energy from source to load. The line impedance depends upon several variables — trace width and thickness, co-planar ground spacing, height of dielectric material between the trace and ground plane(s), and dielectric constant of the PCB material. Given the PCB material selected, the geometry of the micro-strip, strip-line, or co-planar grounded waveguide (CGW) elements must be designed properly to provide the desired 50-Ω impedance. Design of micro-strip, strip-line, and CGW elements is well documented and supported in many microwave software applications.

Additional RF-specific PCB design guidelines include:

• Keep the RF traces on the component sides (top or bottom layer) using micro-strip or CGW techniques where possible.

• Screen these traces to avoid electromagnetic interference.

• Use internal layers with strip-line techniques if necessary.

• Maintain continuous ground below micro-strip traces, beside CGW traces, and above and below strip-line traces.

• Keep traces short and direct, to minimize loss and undesired coupling.

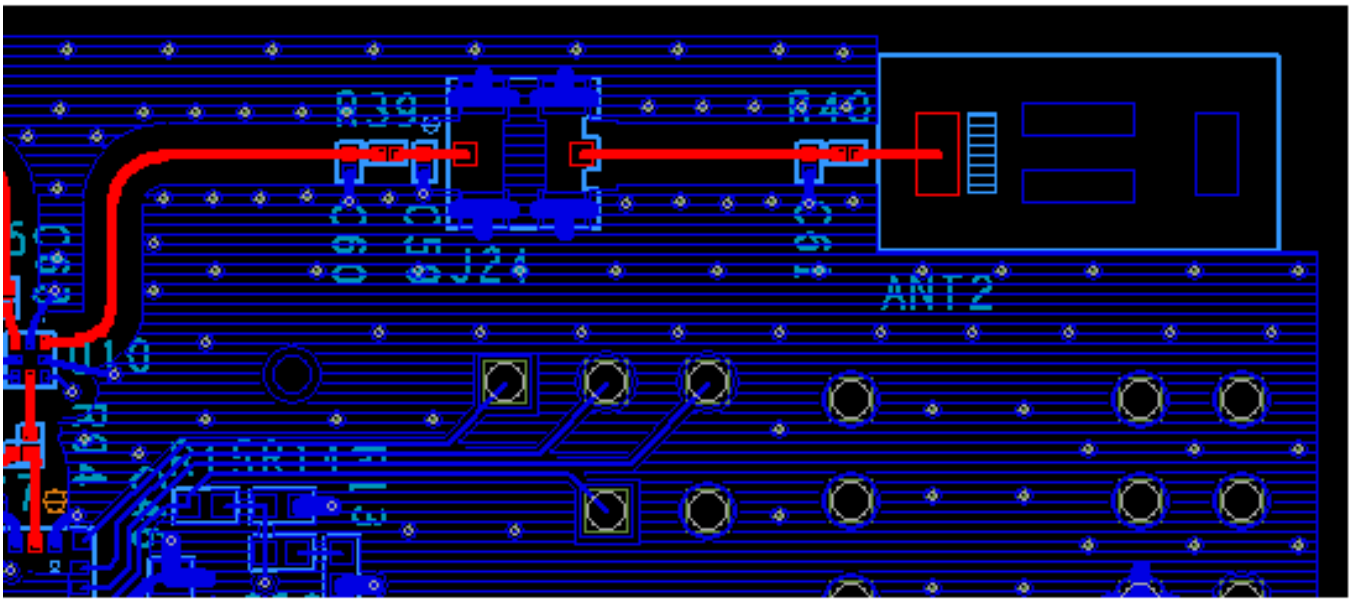
• Front-end losses increase the system noise figure — keep traces before the first gain stage as short as possible and use low-loss capacitors and inductors.

• Clear internal layer (or layers) of metal. This improves micro-strip, CGW, and strip-line geometries, allowing wider traces.

• Fill the areas along both sides of traces with ground to improve isolation, but provide adequate clearance to minimize co-planar capacitance and leakage. These ground-filled areas are integral to CGW designs.

• Use several ground vias along both sides of the signal traces to connect RF ground-fill areas to the internal RF ground plane.
• Avoid crossing RF traces if possible.

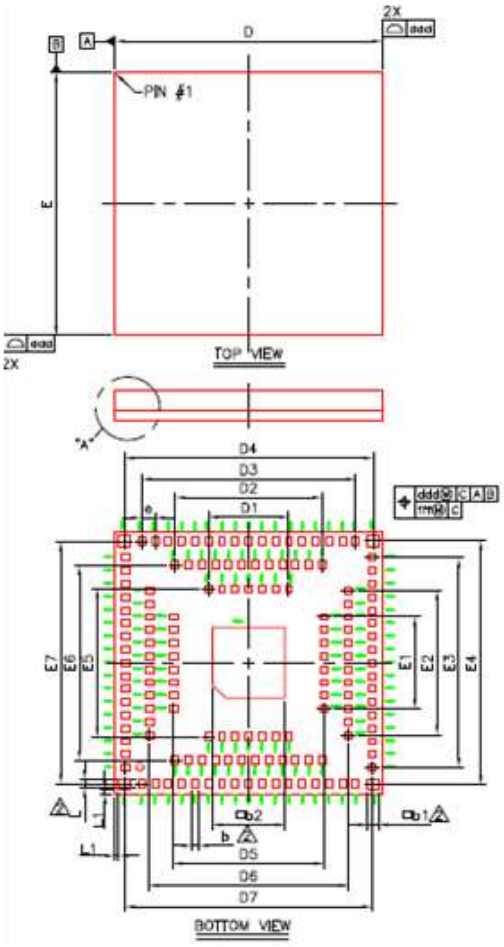
Example:



14 Mechanical Specification

The following paragraphs provide the requirements for the size, weight.
The size and thickness of the ISM4343-WBM-L151 Module is 10mm (W) x 10mm (L) x 1.2mm (H):
(Tolerance: +/- 0.1mm)

Mechanical Dimension
Dimension: 10 x 10 x 1.2 mm3

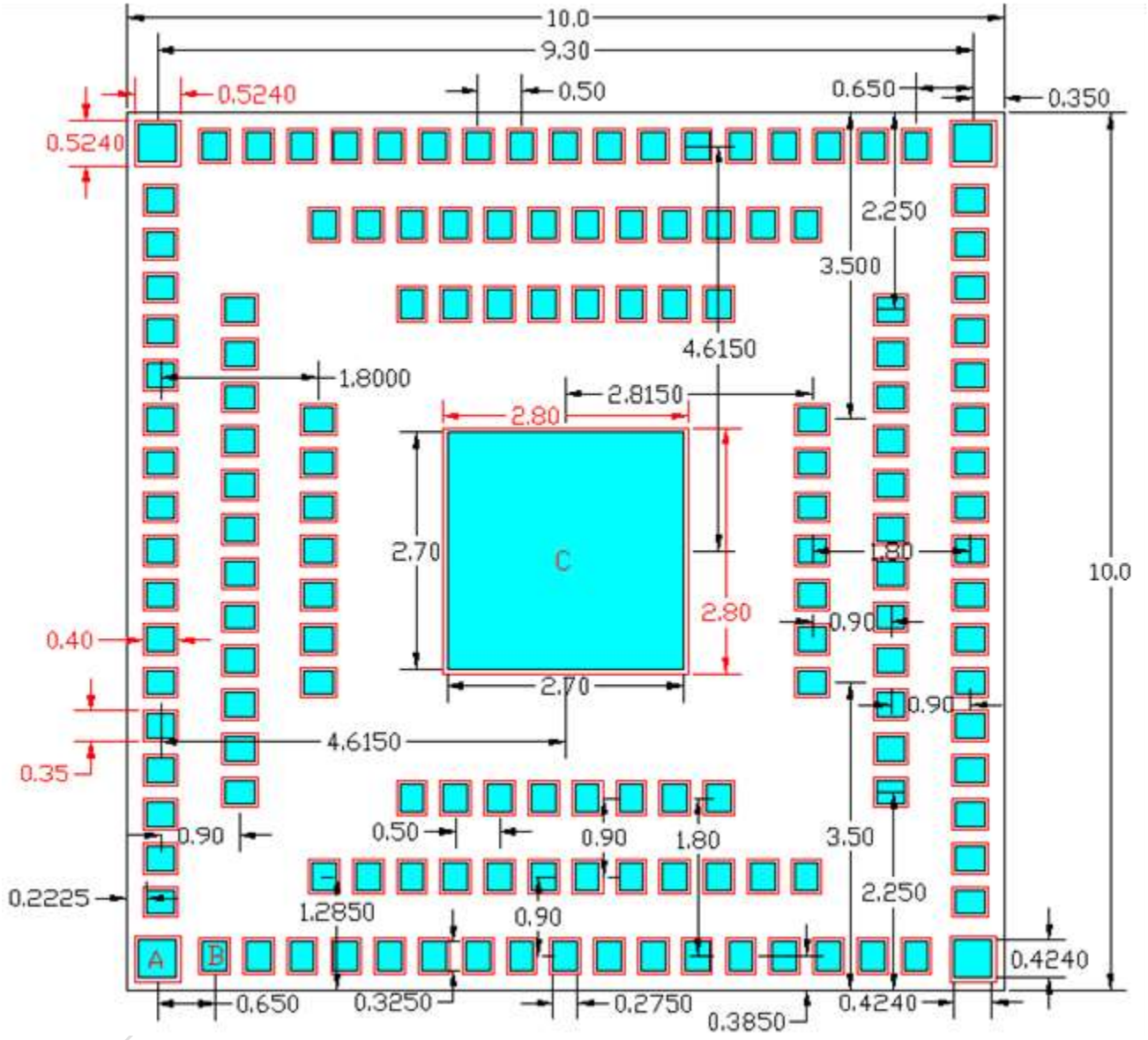


Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.14	1.20	1.26	0.045	0.047	0.050
c	0.36	0.40	0.44	0.014	0.016	0.017
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D1	---	3.00	---	---	0.118	---
E1	---	3.50	---	---	0.138	---
D2/E2	---	5.50	---	---	0.217	---
D3/E3	---	8.00	---	---	0.315	---
D4/E4	---	9.30	---	---	0.366	---
D5/E5	---	5.63	---	---	0.222	---
D6/E6	---	7.43	---	---	0.293	---
D7/E7	---	9.23	---	---	0.363	---
e	---	0.50	---	---	0.020	---
b	0.20	0.25	0.30	0.008	0.010	0.012
L	0.25	0.30	0.35	0.010	0.012	0.014
b1	0.37	0.42	0.47	0.015	0.017	0.019
L1	---	0.14	---	---	0.006	---
b2	2.65	2.70	2.75	0.104	0.106	0.108
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.15			0.006	
fff		0.05			0.002	

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. DIMENSION b,b1,b2,L IS MEASURED AT THE MAXIMUM OPENING DIAMETER, PARALLEL TO PRIMARY DATUM C.

14.1 Recommended PCB Footprint (Bottom View)

Dimension Measurement
Unit: mm



Note:

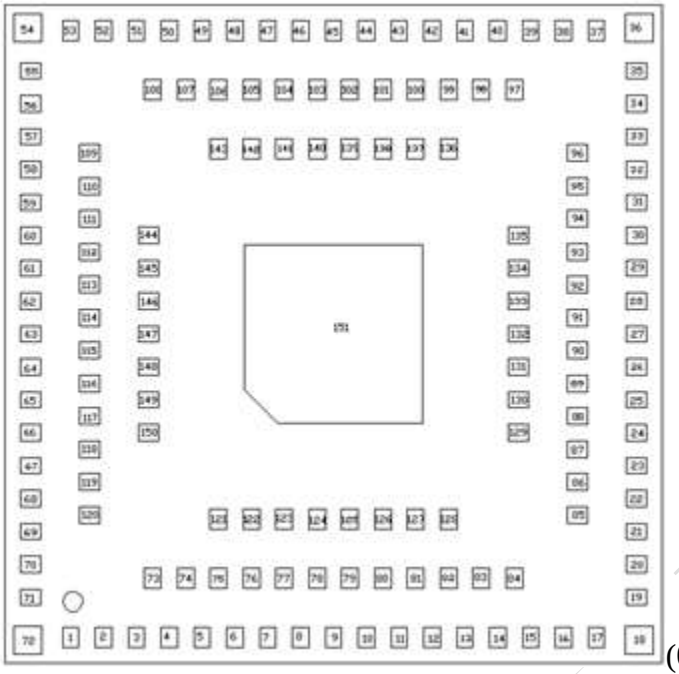
1. Please use Un-Solder Mask to design the Module Footprint.
2. There are three types pad size in the Module.

- Type A: Pad size: 0.424 x 0.424mm2 & Solder Mask size: 0.524 x 0.524 mm2
- Type B: Pad size: 0.275 x 0.325mm2 & Solder Mask size: 0.35 x 0.4 mm2
- Type C: Pad size: 2.7 x 2.7mm2 & Solder Mask size: 2.8 x 2.8 mm2

14.2 Recommended PCB Footprint (Top View)

The X-Y Central Location Coordinates
Unit: mm (Drawn dimensions with chip 0,0 at bottom right corner)

Top View



PIN_NUMBER	PAD_Size (mm)	Solder Mask_Size (mm)	PIN_X(mm)	PIN_Y(mm)
1	0.275 x 0.325	0.35 x 0.4	-9	0.385
2	0.275 x 0.325	0.35 x 0.4	-8.5	0.385
3	0.275 x 0.325	0.35 x 0.4	-8	0.385
4	0.275 x 0.325	0.35 x 0.4	-7.5	0.385
5	0.275 x 0.325	0.35 x 0.4	-7	0.385
6	0.275 x 0.325	0.35 x 0.4	-6.5	0.385
7	0.275 x 0.325	0.35 x 0.4	-6	0.385
8	0.275 x 0.325	0.35 x 0.4	-5.5	0.385
9	0.275 x 0.325	0.35 x 0.4	-5	0.385
10	0.275 x 0.325	0.35 x 0.4	-4.5	0.385
11	0.275 x 0.325	0.35 x 0.4	-4	0.385
12	0.275 x 0.325	0.35 x 0.4	-3.5	0.385
13	0.275 x 0.325	0.35 x 0.4	-3	0.385
14	0.275 x 0.325	0.35 x 0.4	-2.5	0.385

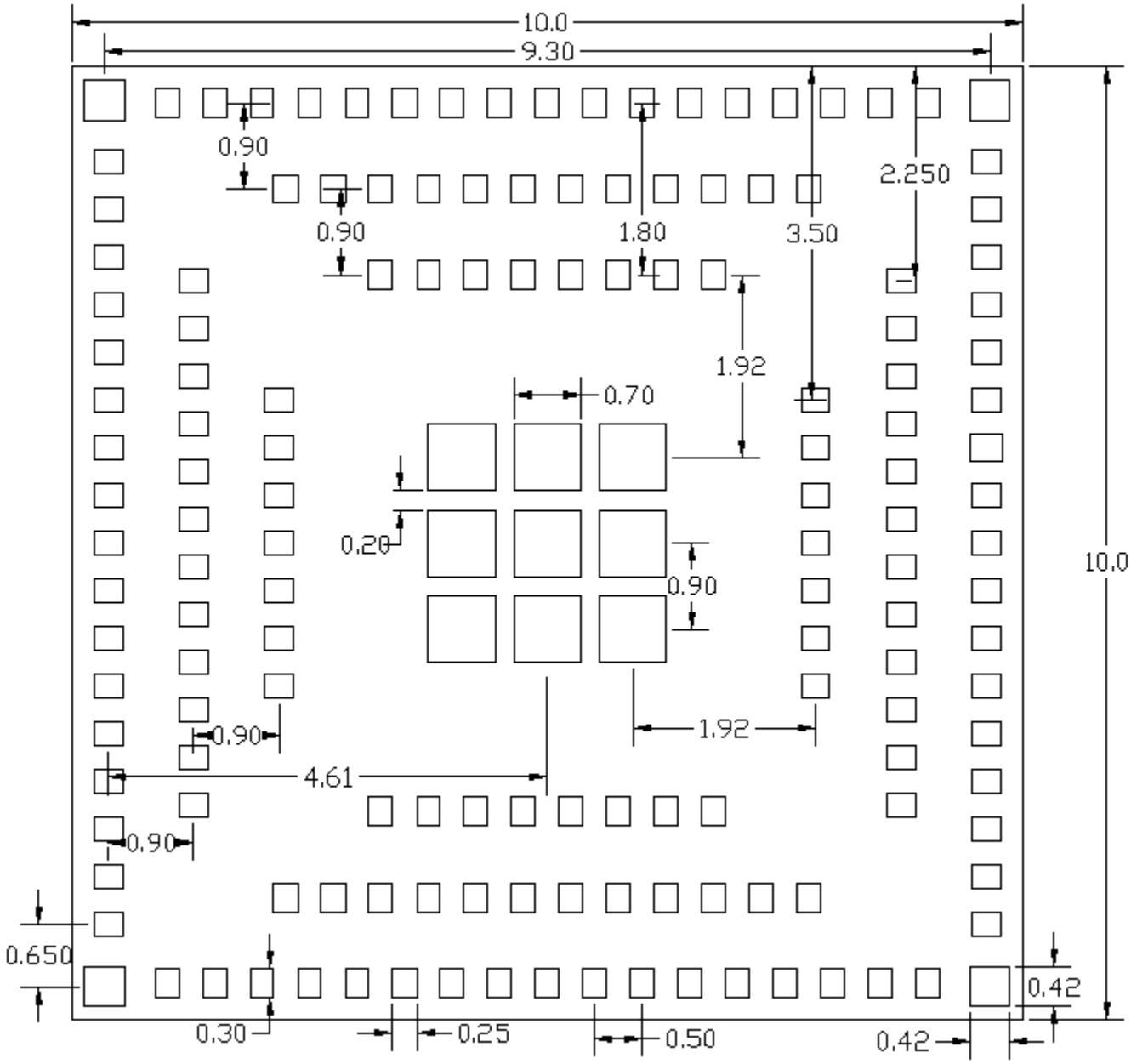
15	0.275 x 0.325	0.35 x 0.4	-2	0.385
16	0.275 x 0.325	0.35 x 0.4	-1.5	0.385
17	0.275 x 0.325	0.35 x 0.4	-1	0.385
18	0.424 x 0.424	0.524 x 0.524	-0.35	0.35
19	0.325 x 0.275	0.4 x 0.35	-0.385	1
20	0.325 x 0.275	0.4 x 0.35	-0.385	1.5
21	0.325 x 0.275	0.4 x 0.35	-0.385	2
22	0.325 x 0.275	0.4 x 0.35	-0.385	2.5
23	0.325 x 0.275	0.4 x 0.35	-0.385	3
24	0.325 x 0.275	0.4 x 0.35	-0.385	3.5
25	0.325 x 0.275	0.4 x 0.35	-0.385	4
26	0.325 x 0.275	0.4 x 0.35	-0.385	4.5
27	0.325 x 0.275	0.4 x 0.35	-0.385	5
28	0.325 x 0.275	0.4 x 0.35	-0.385	5.5
29	0.325 x 0.275	0.4 x 0.35	-0.385	6
30	0.325 x 0.275	0.4 x 0.35	-0.385	6.5
31	0.325 x 0.275	0.4 x 0.35	-0.385	7
32	0.325 x 0.275	0.4 x 0.35	-0.385	7.5
33	0.325 x 0.275	0.4 x 0.35	-0.385	8
34	0.325 x 0.275	0.4 x 0.35	-0.385	8.5
35	0.325 x 0.275	0.4 x 0.35	-0.385	9
36	0.424 x 0.424	0.524 x 0.524	-0.35	9.65
37	0.275 x 0.325	0.35 x 0.4	-1	9.615
38	0.275 x 0.325	0.35 x 0.4	-1.5	9.615
39	0.275 x 0.325	0.35 x 0.4	-2	9.615
40	0.275 x 0.325	0.35 x 0.4	-2.5	9.615
41	0.275 x 0.325	0.35 x 0.4	-3	9.615
42	0.275 x 0.325	0.35 x 0.4	-3.5	9.615
43	0.275 x 0.325	0.35 x 0.4	-4	9.615
44	0.275 x 0.325	0.35 x 0.4	-4.5	9.615
45	0.275 x 0.325	0.35 x 0.4	-5	9.615
46	0.275 x 0.325	0.35 x 0.4	-5.5	9.615
47	0.275 x 0.325	0.35 x 0.4	-6	9.615
48	0.275 x 0.325	0.35 x 0.4	-6.5	9.615
49	0.275 x 0.325	0.35 x 0.4	-7	9.615

50	0.275 x 0.325	0.35 x 0.4	-7.5	9.615
51	0.275 x 0.325	0.35 x 0.4	-8	9.615
52	0.275 x 0.325	0.35 x 0.4	-8.5	9.615
53	0.275 x 0.325	0.35 x 0.4	-9	9.615
54	0.424 x 0.424	0.524 x 0.524	-9.65	9.65
55	0.325 x 0.275	0.4 x 0.35	-9.615	9
56	0.325 x 0.275	0.4 x 0.35	-9.615	8.5
57	0.325 x 0.275	0.4 x 0.35	-9.615	8
58	0.325 x 0.275	0.4 x 0.35	-9.615	7.5
59	0.325 x 0.275	0.4 x 0.35	-9.615	7
60	0.325 x 0.275	0.4 x 0.35	-9.615	6.5
61	0.325 x 0.275	0.4 x 0.35	-9.615	6
62	0.325 x 0.275	0.4 x 0.35	-9.615	5.5
63	0.325 x 0.275	0.4 x 0.35	-9.615	5
64	0.325 x 0.275	0.4 x 0.35	-9.615	4.5
65	0.325 x 0.275	0.4 x 0.35	-9.615	4
66	0.325 x 0.275	0.4 x 0.35	-9.615	3.5
67	0.325 x 0.275	0.4 x 0.35	-9.615	3
68	0.325 x 0.275	0.4 x 0.35	-9.615	2.5
69	0.325 x 0.275	0.4 x 0.35	-9.615	2
70	0.325 x 0.275	0.4 x 0.35	-9.615	1.5
71	0.325 x 0.275	0.4 x 0.35	-9.615	1
72	0.424 x 0.424	0.524 x 0.524	-9.65	0.35
73	0.275 x 0.325	0.35 x 0.4	-7.75	1.285
74	0.275 x 0.325	0.35 x 0.4	-7.25	1.285
75	0.275 x 0.325	0.35 x 0.4	-6.75	1.285
76	0.275 x 0.325	0.35 x 0.4	-6.25	1.285
77	0.275 x 0.325	0.35 x 0.4	-5.75	1.285
78	0.275 x 0.325	0.35 x 0.4	-5.25	1.285
79	0.275 x 0.325	0.35 x 0.4	-4.75	1.285
80	0.275 x 0.325	0.35 x 0.4	-4.25	1.285
81	0.275 x 0.325	0.35 x 0.4	-3.75	1.285
82	0.275 x 0.325	0.35 x 0.4	-3.25	1.285
83	0.275 x 0.325	0.35 x 0.4	-2.75	1.285
84	0.275 x 0.325	0.35 x 0.4	-2.25	1.285
85	0.325 x 0.275	0.4 x 0.35	-1.285	2.25

86	0.325 x 0.275	0.4 x 0.35	-1.285	2.75
87	0.325 x 0.275	0.4 x 0.35	-1.285	3.25
88	0.325 x 0.275	0.4 x 0.35	-1.285	3.75
89	0.325 x 0.275	0.4 x 0.35	-1.285	4.25
90	0.325 x 0.275	0.4 x 0.35	-1.285	4.75
91	0.325 x 0.275	0.4 x 0.35	-1.285	5.25
92	0.325 x 0.275	0.4 x 0.35	-1.285	5.75
93	0.325 x 0.275	0.4 x 0.35	-1.285	6.25
94	0.325 x 0.275	0.4 x 0.35	-1.285	6.75
95	0.325 x 0.275	0.4 x 0.35	-1.285	7.25
96	0.325 x 0.275	0.4 x 0.35	-1.285	7.75
97	0.275 x 0.325	0.35 x 0.4	-2.25	8.715
98	0.275 x 0.325	0.35 x 0.4	-2.75	8.715
99	0.275 x 0.325	0.35 x 0.4	-3.25	8.715
100	0.275 x 0.325	0.35 x 0.4	-3.75	8.715
101	0.275 x 0.325	0.35 x 0.4	-4.25	8.715
102	0.275 x 0.325	0.35 x 0.4	-4.75	8.715
103	0.275 x 0.325	0.35 x 0.4	-5.25	8.715
104	0.275 x 0.325	0.35 x 0.4	-5.75	8.715
105	0.275 x 0.325	0.35 x 0.4	-6.25	8.715
106	0.275 x 0.325	0.35 x 0.4	-6.75	8.715
107	0.275 x 0.325	0.35 x 0.4	-7.25	8.715
108	0.275 x 0.325	0.35 x 0.4	-7.75	8.715
109	0.325 x 0.275	0.4 x 0.35	-8.715	7.75
110	0.325 x 0.275	0.4 x 0.35	-8.715	7.25
111	0.325 x 0.275	0.4 x 0.35	-8.715	6.75
112	0.325 x 0.275	0.4 x 0.35	-8.715	6.25
113	0.325 x 0.275	0.4 x 0.35	-8.715	5.75
114	0.325 x 0.275	0.4 x 0.35	-8.715	5.25
115	0.325 x 0.275	0.4 x 0.35	-8.715	4.75
116	0.325 x 0.275	0.4 x 0.35	-8.715	4.25
117	0.325 x 0.275	0.4 x 0.35	-8.715	3.75
118	0.325 x 0.275	0.4 x 0.35	-8.715	3.25
119	0.325 x 0.275	0.4 x 0.35	-8.715	2.75
120	0.325 x 0.275	0.4 x 0.35	-8.715	2.25
121	0.275 x 0.325	0.35 x 0.4	-6.75	2.185

122	0.275 x 0.325	0.35 x 0.4	-6.25	2.185
123	0.275 x 0.325	0.35 x 0.4	-5.75	2.185
124	0.275 x 0.325	0.35 x 0.4	-5.25	2.185
125	0.275 x 0.325	0.35 x 0.4	-4.75	2.185
126	0.275 x 0.325	0.35 x 0.4	-4.25	2.185
127	0.275 x 0.325	0.35 x 0.4	-3.75	2.185
128	0.275 x 0.325	0.35 x 0.4	-3.25	2.185
129	0.325 x 0.275	0.4 x 0.35	-2.185	3.5
130	0.325 x 0.275	0.4 x 0.35	-2.185	4
131	0.325 x 0.275	0.4 x 0.35	-2.185	4.5
132	0.325 x 0.275	0.4 x 0.35	-2.185	5
133	0.325 x 0.275	0.4 x 0.35	-2.185	5.5
134	0.325 x 0.275	0.4 x 0.35	-2.185	6
135	0.325 x 0.275	0.4 x 0.35	-2.185	6.5
136	0.275 x 0.325	0.35 x 0.4	-3.25	7.815
137	0.275 x 0.325	0.35 x 0.4	-3.75	7.815
138	0.275 x 0.325	0.35 x 0.4	-4.25	7.815
139	0.275 x 0.325	0.35 x 0.4	-4.75	7.815
140	0.275 x 0.325	0.35 x 0.4	-5.25	7.815
141	0.275 x 0.325	0.35 x 0.4	-5.75	7.815
142	0.275 x 0.325	0.35 x 0.4	-6.25	7.815
143	0.275 x 0.325	0.35 x 0.4	-6.75	7.815
144	0.325 x 0.275	0.4 x 0.35	-7.815	6.5
145	0.325 x 0.275	0.4 x 0.35	-7.815	6
146	0.325 x 0.275	0.4 x 0.35	-7.815	5.5
147	0.325 x 0.275	0.4 x 0.35	-7.815	5
148	0.325 x 0.275	0.4 x 0.35	-7.815	4.5
149	0.325 x 0.275	0.4 x 0.35	-7.815	4
150	0.325 x 0.275	0.4 x 0.35	-7.815	3.5
151	2.7 x 2.7	2.8 x 2.8	-5	5

14.3 Recommend Stencil: Unit: mm



15 Product Compliance Considerations

RoHS: Restriction of Hazardous Substances (RoHS) directive has come into force since 1st July 2006 all electronic products sold in the EU must be free of hazardous materials, such as lead. Inventek is fully committed to being one of the first to introduce lead-free products while maintaining backwards compatibility and focusing on a continuously high level of product and manufacturing quality.

EMI/EMC: The Inventek module design embeds EMI/EMC suppression features and accommodations to allow for higher operational reliability in noisier (RF) environments and easier integration compliance in host (OEM) applications.

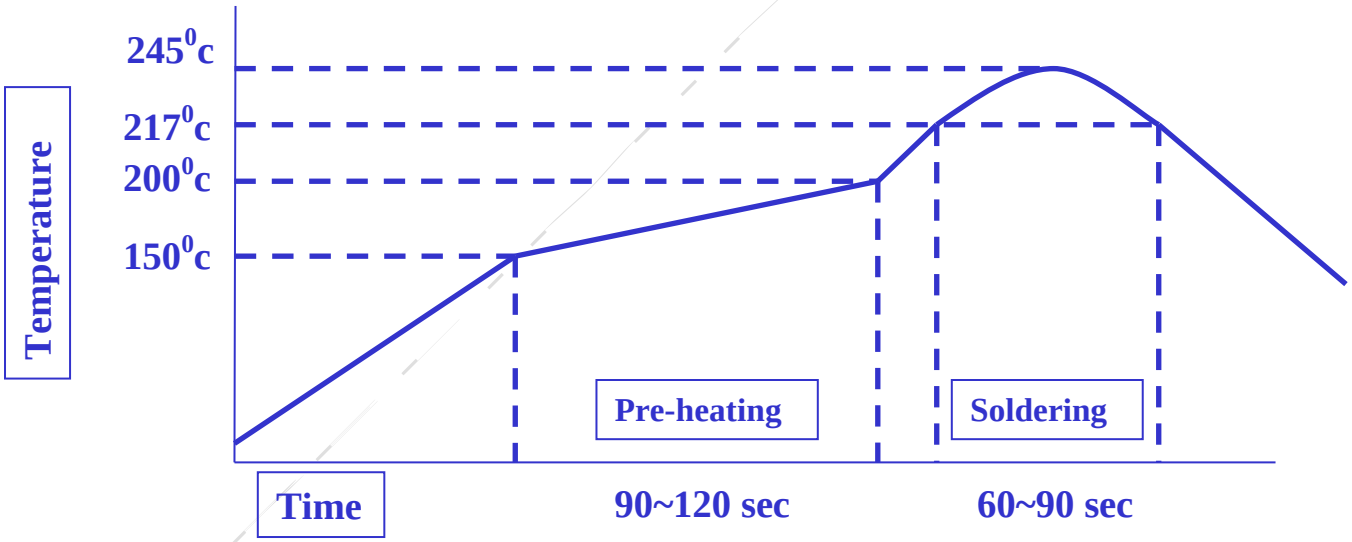
FCC/CE: THIS DEVICE IS PENDING CERTIFICATION. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS.

(1) THIS DEVICE MAY NOT CASUE HARMFUL INTERFERENCE, AND

(2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED, INCLUDING INTERFERENCE THAT MAY CASUE UNDESIRED OPERTATION.

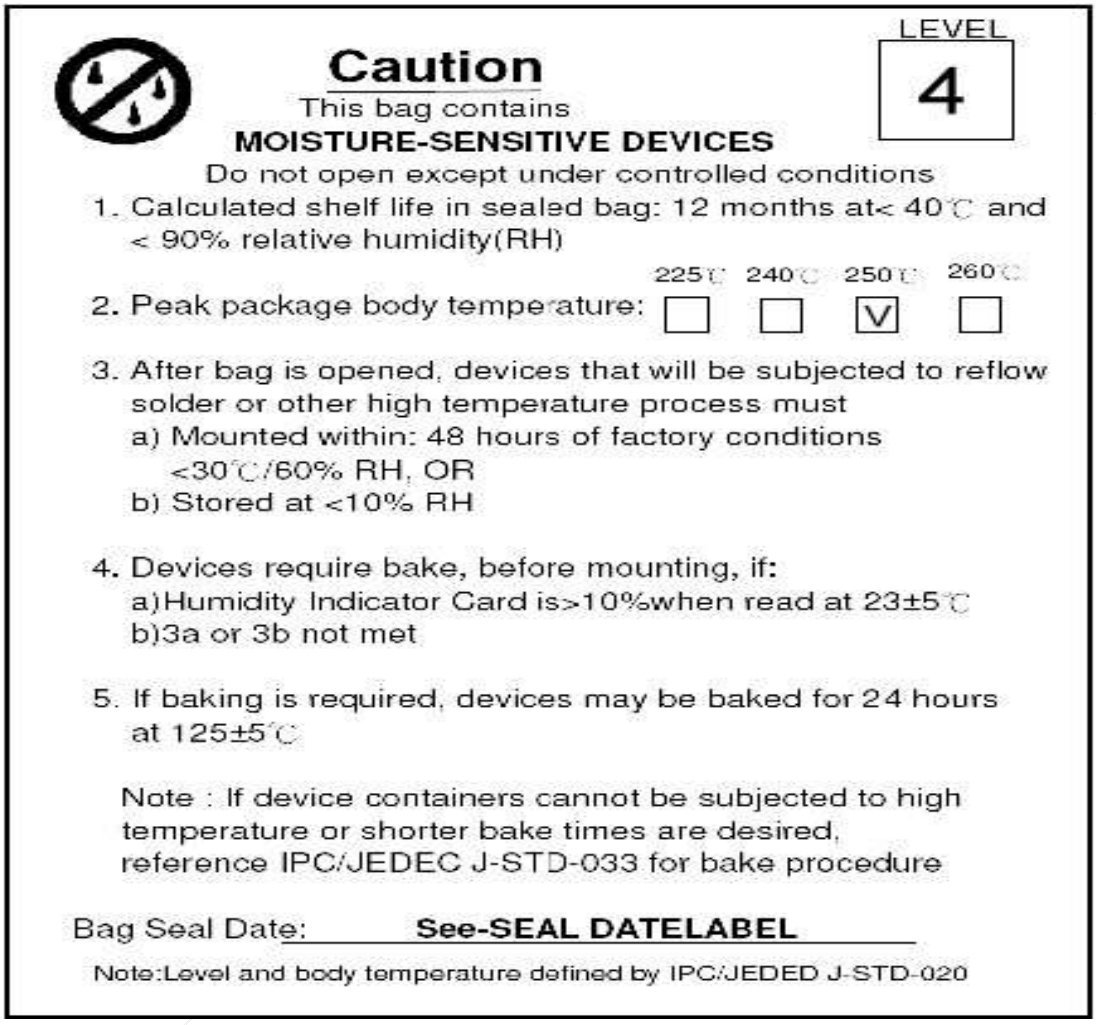
16 Reflow Profile

- Reference the IPC/JEDEC standard.
- Peak Temperature: <250°C
- Number of Times: ≤2 times



17 Packaging Information

17.1 MSL Level / Storage Condition



17.2 Device baking requirements prior to assembly

Boards must be baked prior to rework or assembly to avoid damaging moisture sensitive components during localized reflow. The default bake cycles is 24 hours at 125C.
Maintaining proper control of moisture uptake in components is critical.
Before opening the shipping bag and attempting solder reflow, you should maintain a minimal out-of-bag time and ensure the highest possible package reliability for the final product.

18 REVISION CONTROL

Document: ISM4343-WBM-L151	Wi-Fi + BT/BLE + Cortex M4 Module
External Release	DOC-DS-20074-2.1

Date	Author	Revision	Comment
1/15/2015	AS	1.0	Preliminary
12/17/2015	AS	1.1	Released
5/30/2017	AS	1.2	Diagram Updates
8/22/2017	KT	2.0	Part Number change / Formatting updates
4/12/2017	AS	2.1	Removed External Clock Option

19 CONTACT INFORMATION

Inventek Systems
2 Republic Road
Billerica Ma, 01862
Tel: 978-667-1962
Sales@inventeksys.com

www.inventeksys.com